DATA SHEET

PTN1111
1:10 PECL clock distribution device

Product data

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Philips
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1:10 PECL clock distribution device PTN1111

FEATURES

- 80 ps part-to-part skew
- 20 ps output-to-output skew
- Differential design
- PECL inputs and outputs
- V_{BB} reference output voltage available
- 75 kΩ input pulldown resistors
- Low voltage V_{CC} range of 2.375 V to +3.8 V
- High signaling rate capability (above 1 GHz)
- Pin and function compatible to MC100EP111, MC100LVEP111
- Available in LQFP32 package

DESCRIPTION

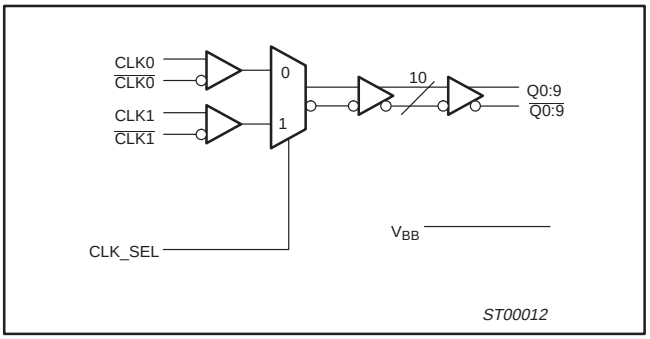
The PTN1111 is a low-skew, 1:10 PECL clock distribution device. One selected clock signal out of two selectable inputs is fanned out to 10 identical, precision time-aligned differential outputs.

The PTN1111 is provided with a V_{BB} reference voltage to allow for single-ended PECL input and with complementary clock inputs to allow for differential PECL input.

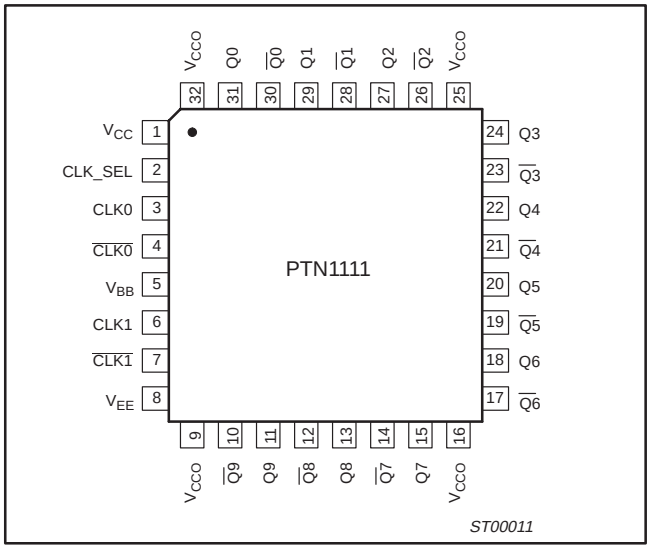
The main purpose and benefit of the PTN1111 is low skew: between individual outputs of a single PTN1111 (within-part skew or output-to-output skew) as well as measured from part-to-part. Within-part skew is realized by careful attention to internal layout and design of the PTN1111, whereas part-to-part skew is achieved by control and monitoring of relevant process parameters.

The PTN1111 can be used for high-performance, high-speed clock distribution in systems which utilize PECL as the primary signaling standard. Designers can take advantage of the device's performance to distribute clocks across a board or backplane, at an extremely high degree of time alignment, thereby affording system processors to achieve maximum utilization of the clock cycle.

LOGIC DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{CC}	Power supply voltage
2	CLK_SEL	Clock select input
3, 4	CLK0, $\overline{CLK0}$	Differential PECL clock input pair
5	V_{BB}	Voltage reference output
6, 7	CLK1, $\overline{CLK1}$	Differential PECL clock input pair
8	V_{EE}	Ground
9, 16, 25, 32	V_{CCO}	Output driver power supply voltages
10–15, 17–24, 26–31	Q0:9, $\overline{Q0:9}$	Differential PECL output pairs

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PTN1111BD	LQFP32	Plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm	SOT358-1

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{CC}	Supply voltage	–0.5 to +4.6	V
ESDHBM	Electrostatic discharge (Human Body Model; 1.5 kΩ, 100 pF)	>2	kV
ESDMM	Electrostatic discharge (Machine Model; 0 kΩ, 200 pF)	>200	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply voltage	2.375	3.8	V
V_{IR}	Receiver input voltage	V_{EE}	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C unless otherwise specified; V_{CC} = 3.3 V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{OH}	Output HIGH voltage	2.275	2.345	2.420	V
V_{OL}	Output LOW voltage	1.490	1.595	1.680	V
V_{IH}	Input HIGH voltage	2.135	–	2.420	V
V_{IL}	Input LOW voltage	1.490	–	1.825	V
V_{BB}	Output reference voltage	1.92	–	2.04	V
V_{CC}	Power supply voltage	2.375	–	3.8	V
I_{IH}	Input HIGH current	–	–	150	μA
I_{EE}	Power supply current, internal	–	80	120	mA
I_{CC}	Power supply current including load: 50 Ω to V_{CC} – 2.0 V	–	340	–	mA

NOTE:

1. These values are for V_{CC} = 3.3 V; PECL level specifications are referenced to V_{CC} and will track 1:1 with variation of V_{CC}.

AC ELECTRICAL CHARACTERISTICS

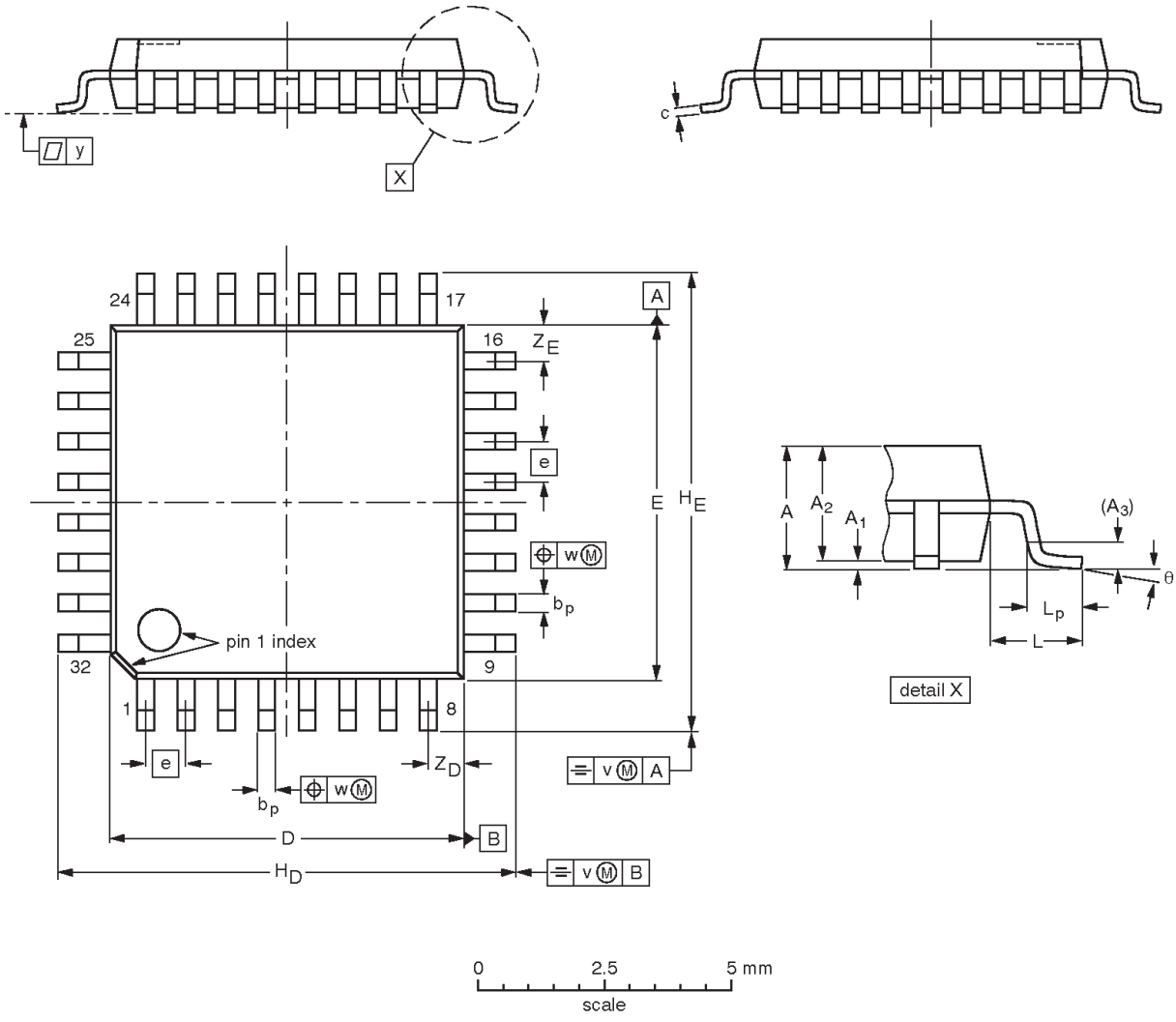
T_{amb} = –40°C to +85°C unless otherwise specified; $V_{CC} = V_{CCmin}$ to V_{CCmax}; V_{EE} = 0 V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay input (differential) to output	–	400	680	ps
	Propagation delay input (single-ended) to output	–	400	680	ps
t_{skew}	Clock output skew, within device	–	20	40	ps
	Clock output skew, part-to-part	–	80	110	ps
	Clock output pulse skew	–	50	160	ps
f_{MAX}	Maximum input frequency	–	1.5	–	GHz
t_{Pclk_set}	Propagation delay CLK_SEL transition to stable Qn/$\overline{Qn}$ output	–	5	10	ns
V_{PP}[1]	Input swing	0.5	0.8	1.3	V
t_r/t_f	Output rise/fall time at 20% and 80% intersects	–	200	–	ps

NOTE:

1. Required to maintain AC specifications. Actual device accepts V_{PP} of 100 mV or higher.

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1	136E03	MS-026				~~99-12-27~~ 00-01-19

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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