DATA SHEET

TDA3618JR
Multiple voltage regulator with switch and ignition buffers

Preliminary specification
Supersedes data of 1999 Sep 01
File under Integrated Circuits, IC01

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Philips
Semiconductors

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Multiple voltage regulator with switch and ignition buffers

TDA3618JR

FEATURES

General

- Extremely low noise behaviour and good stability with very small output capacitors
- Two V_P-state controlled regulators and a power switch
- Regulator 2, reset and ignition buffer operate during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range from −18 to +50 V
- Low reverse current of regulator 2
- Low quiescent current when regulator 1, regulator 3 and power switch are switched off
- Hold output for low V_P
- Hold output for regulators 1 and 3
- Hold output for foldback mode switch
- Hold output for load dump and temperature protection
- Reset and hold (open collector) outputs
- Adjustable reset delay time
- High ripple rejection
- Backup capacitor for regulator 2
- Two independent ignition buffers, one inverted and with open-collector output.

Protection

- Reverse polarity safe, down to −18 V
- Able to withstand voltages up to 18 V at the outputs and the supply line may be short-circuited
- ESD protected on all pins
- Thermal protections with hysteresis
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch at short-circuit
- The regulator outputs and the power switch are DC short-circuit safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3618JR is a multiple output voltage regulator with a power switch and ignition buffers, intended for use in car radios with or without a microcontroller. It contains:

- Two fixed voltage regulators with foldback current protection (regulators 1 and 3) and one fixed voltage regulator (regulator 2) intended to supply a microcontroller, that also operates during load dump and thermal shutdown
- A power switch with protection, operated by an enable input
- Reset and hold outputs that can be used to interface with the microcontroller; the reset signal can be used to wake up the microcontroller
- A supply pin that can withstand load dump pulses and negative supply voltages
- Regulator 2, which is switched on at a backup voltage greater than 6.5 V and off when the output voltage of regulator 2 drops below 1.9 V
- A provision for the use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage
- An inverted ignition 1 input with open-collector output stage
- An ignition 2 input Schmitt trigger with push-pull output stage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3618JR	DBS17P	plastic DIL-bent-SIL (special bent) power package; 17 leads (lead length 12 mm)	SOT475-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	operating	11	14.4	18	V
		reverse polarity; non-operating	–	–	–18	V
		regulator 2 on	2.4	14.4	50	V
		jump start for t ≤ 10 minutes	–	–	30	V
		load dump protection for t ≤ 50 ms and $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	310	400	µA
T_j	junction temperature		–	–	150	°C
Voltage regulators						
$V_{O(REG1)}$	output voltage of regulator 1	1 mA ≤ I_{REG1} ≤ 600 mA	8.5	9.0	9.5	V
$V_{O(REG2)}$	output voltage of regulator 2	0.5 mA ≤ I_{REG2} ≤ 150 mA; V_P = 14.4 V	4.75	5.0	5.25	V
$V_{O(REG3)}$	output voltage of regulator 3	1 mA ≤ I_{REG3} ≤ 750 mA	4.75	5.0	5.25	V
Power switch						
V_{drop}	drop-out voltage	I_{SW} = 1 A	–	0.45	0.7	V
		I_{SW} = 1.8 A	–	1	1.8	V
I_M	peak current		3	–	–	A

BLOCK DIAGRAM

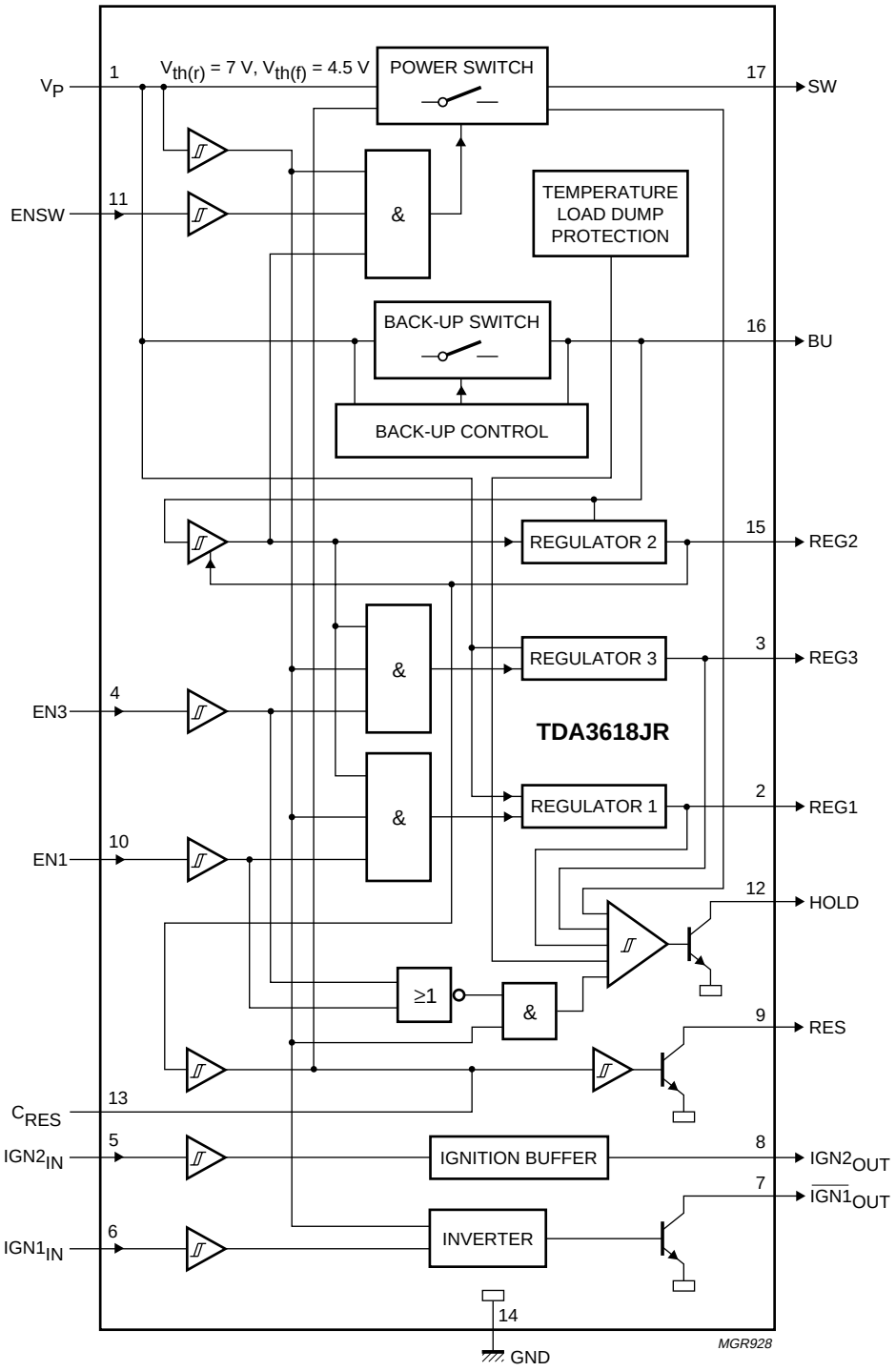


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
EN3	4	enable input regulator 3
$IGN2_{IN}$	5	ignition 2 input
$IGN1_{IN}$	6	ignition 1 input
$\overline{IGN1}_{OUT}$	7	ignition 1 output (active LOW)
$IGN2_{OUT}$	8	ignition 2 output
RES	9	reset output
EN1	10	enable input regulator 1
ENSW	11	enable input power switch
HOLD	12	hold output (active LOW)
C_{RES}	13	reset delay capacitor
GND	14	ground
REG2	15	regulator 2 output
BU	16	backup output
SW	17	power switch output

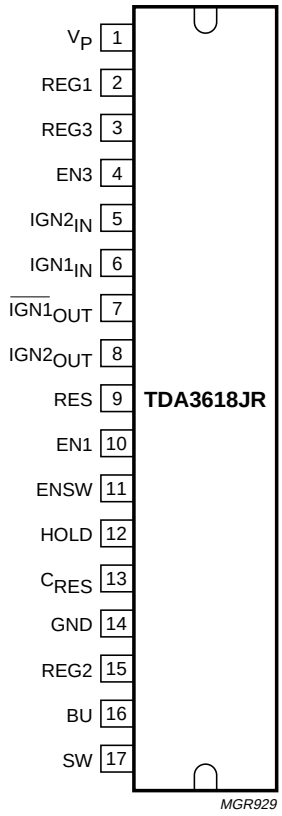


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3618JR is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of the low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3618JR.

Regulator 2 switches on when the backup voltage exceeds 6.5 V for the first time and switches off again when the output voltage of regulator 2 falls below 1.9 V (this is far below an engine start). When regulator 2 is switched on and its output voltage is within its voltage range, the reset output is enabled to generate a reset to the microcontroller. The reset cycle can be extended by an external capacitor at pin C_{RES}. The start-up feature is built-in to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge of the backup capacitor can be used to supply regulator 2 for a short period when the supply drops to 0 V (the time depends on the value of the storage capacitor).

The output stages of regulators 1 and 3 have an extremely low noise behaviour and good stability. These regulators are stabilized by using small output capacitors.

When both regulator 2 and the supply voltage ($V_P > 4.5$ V) are available, regulators 1 and 3 can be operated by means of enable inputs (pins EN1 and EN3 respectively).

Pin HOLD is normally HIGH and is active LOW. Pin HOLD is connected to an open-collector NPN transistor and must have an external pull-up resistor to operate. The hold output is controlled by a low voltage detection circuit which, when activated, pulls the warning output LOW (enabled). The detection outputs of the regulators are connected to an OR gate inside the IC such that the hold output is activated (goes LOW) when the regulator voltages of regulator 1 and/or regulator 3 are out of regulation for any reason. Each regulator enable input controls its own detection circuit, such that if a regulator is disabled or switched off, the detection circuit for that regulator is disabled.

The hold circuit is also controlled by the temperature and load dump protection. Activating the temperature or load dump protection causes a hold (LOW) during the time the protection is activated. When all regulators are switched off, pin HOLD is controlled by the battery line (pin V_P), temperature protection and load dump protection.

The hold output is enabled (LOW) at low battery voltages. This indicates that it is not possible to get regulator 1 into regulation when switching it on. The hold function includes hysteresis to avoid oscillations when the regulator voltage crosses the hold threshold. Pin HOLD also becomes LOW when the switch is in foldback protection mode; see Fig.4 for a timing diagram. The hold circuit block diagram is given in Fig.3.

The power switch can also be controlled by means of a separate enable input (pin ENSW).

All output pins are fully protected. The regulators are protected against load dump (regulators 1 and 3 switch off at supply voltages >18 V) and short-circuit (foldback current protection).

The switch contains a current protection. However, this protection is delayed at short-circuit by the reset delay capacitor. During this time, the output current is limited to a peak value of at least 3 A and continuous current of 2 A ($V_P \leq 18$ V).

In the normal situation, the voltage on the reset delay capacitor is approximately 3.5 V (depending on temperature). The switch output is approximately $V_P - 0.4$ V. At operational temperature, the switch can deliver at least 3 A. At high temperature, the switch can deliver approximately 2 A. During an overload condition or short-circuit ($V_{SW} < V_P - 3.7$ V), the voltage on the reset delay capacitor rises 0.6 V above the voltage of regulator 2. This rise time depends on the capacitor connected to pin C_{RES}. During this time, the switch can deliver more than 3 A. The charge current of the reset delay capacitor is typically 4 μA and the voltage swing approximately 1.5 V. When regulator 2 is out of regulation and generates a reset, the switch can only deliver 2 A and will go into the foldback protection without delay. At supply voltages >17 V, the switch is clamped at 16 V maximum (to avoid externally connected circuits being damaged by an overvoltage) and the switch will switch off at load dump.

Interfacing with the microcontroller (simple full or semi on/off logic applications) can be realized with two independent ignition Schmitt triggers and ignition output buffers (one open-collector and one push-pull output). Ignition 1 output is inverted.

The timing diagrams are shown in Figs 4 and 5.

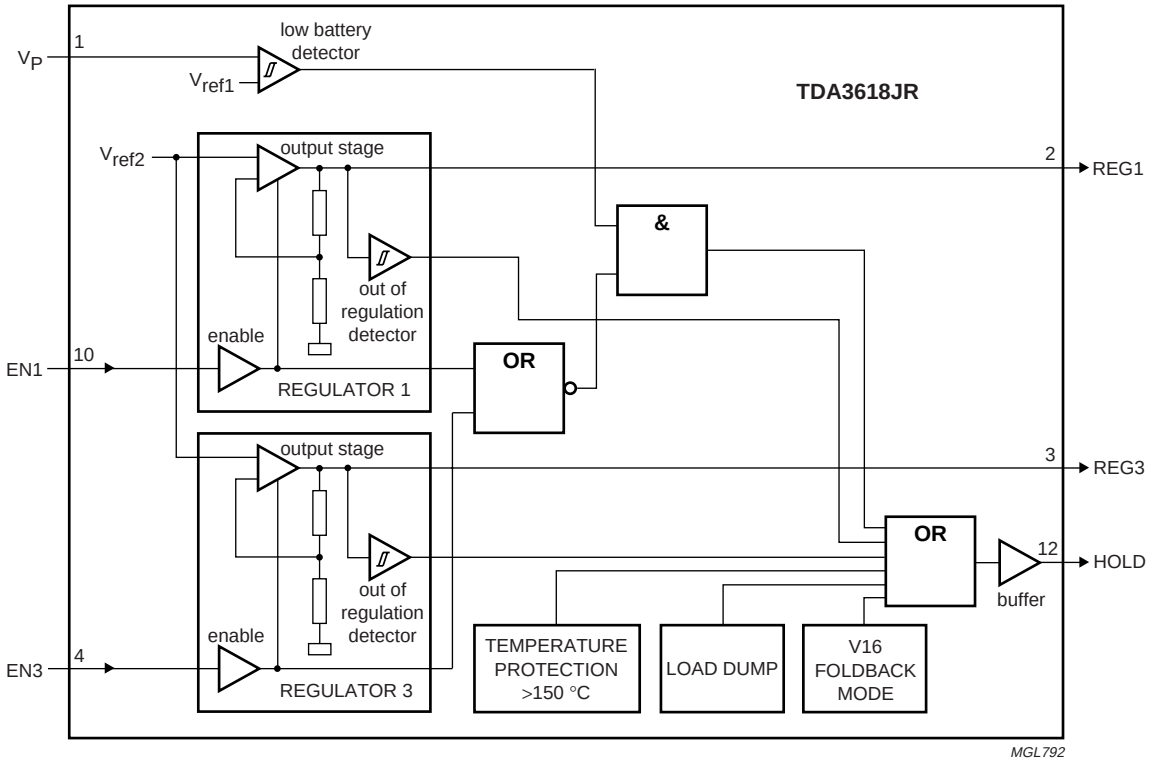


Fig.3 Block diagram of the hold circuit.

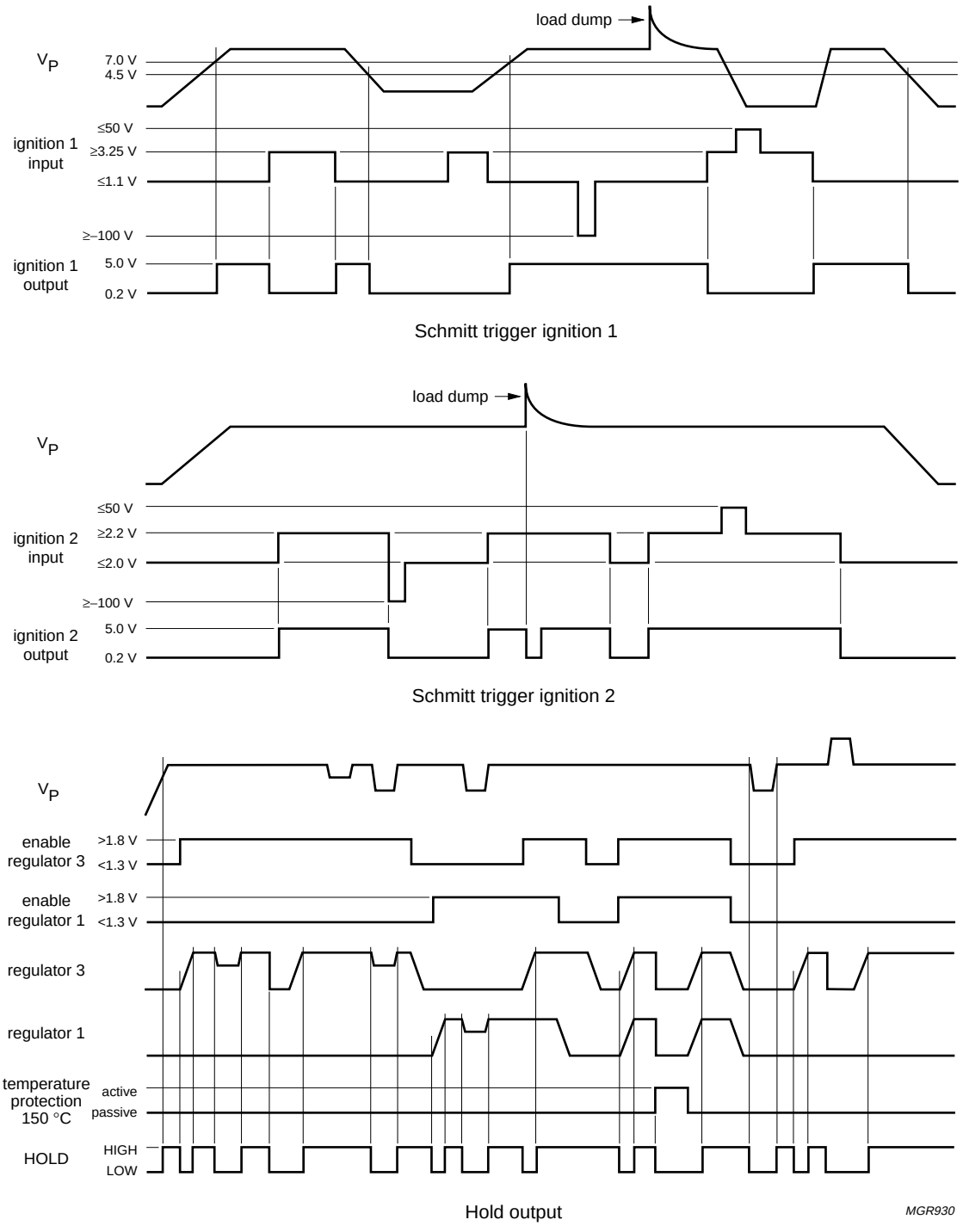
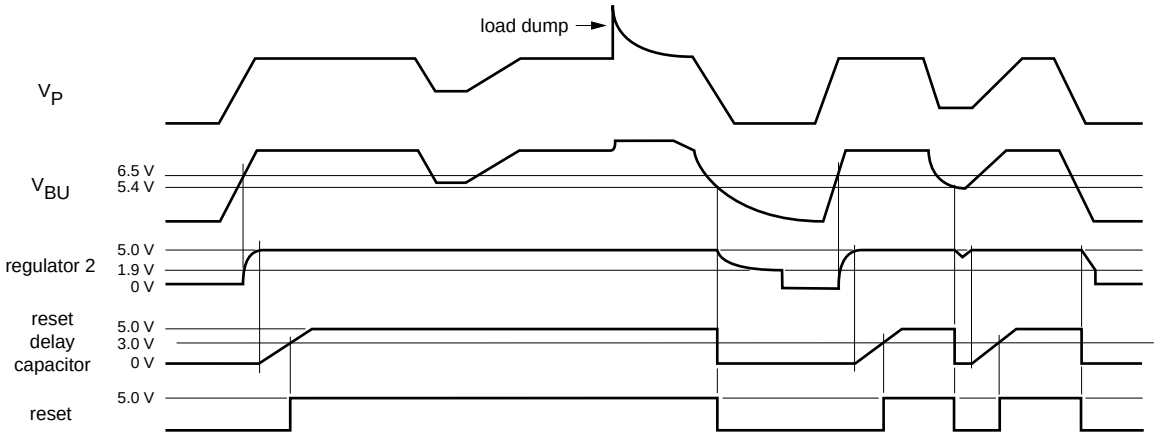
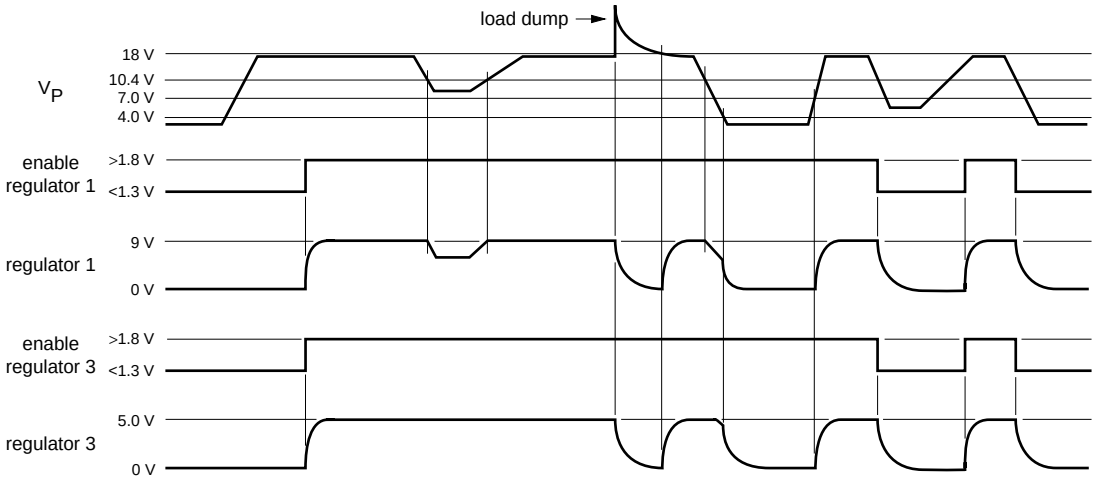


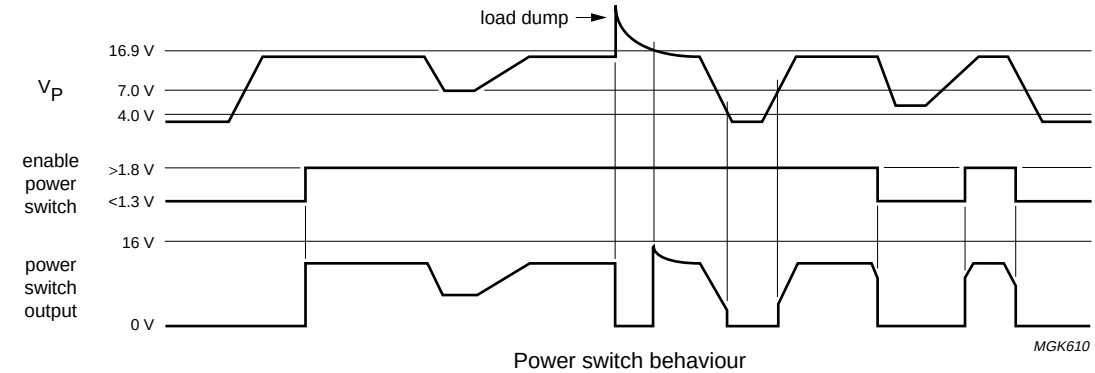
Fig.4 Timing diagram of ignition Schmitt triggers and hold output.



Backup Schmitt trigger and reset behaviour



V_P and enable Schmitt trigger



Power switch behaviour

Fig.5 Timing diagram of regulators and power switch.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		reverse polarity; non-operating	–	–18	V
		jump start; t ≤ 10 minutes	–	30	V
		load dump protection; t ≤ 50 ms; t_r ≥ 2.5 ms	–	50	V
P_{tot}	total power dissipation		–	62	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; see Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltages	operating	11	14.4	18	V
		regulator 2 on; note 1	2.4	14.4	18	V
		jump start; t ≤ 10 minutes	–	–	30	V
		load dump protection; t ≤ 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	V_P = 12.4 V; I_{REG2} = 0.1 mA; note 2	–	310	400	µA
		V_P = 14.4 V; I_{REG2} = 0.1 mA; note 2	–	315	–	µA
Schmitt trigger for regulator 1, regulator 3 and the power switch						
$V_{th(r)}$	rising threshold voltage		6.5	7.0	7.5	V
$V_{th(f)}$	falling threshold voltage		4.0	4.5	5.0	V
V_{hys}	hysteresis voltage		–	2.5	–	V
Schmitt trigger for regulator 2						
$V_{th(r)}$	rising threshold voltage		6.0	6.5	7.1	V
$V_{th(f)}$	falling threshold voltage		1.7	1.9	2.3	V
V_{hys}	hysteresis voltage		–	4.6	–	V
Schmitt trigger for enable inputs (regulator 1, regulator 3 and power switch)						
$V_{th(r)}$	rising threshold voltage		1.4	1.8	2.4	V
$V_{th(f)}$	falling threshold voltage		0.9	1.3	1.9	V
V_{hys}	hysteresis voltage	$I_{REG} = I_{SW}$ = 1 mA	–	0.5	–	V
I_{LI}	input leakage current	V_{EN} = 5 V	1	5	10	µA
Reset trigger level of regulator 2						
$V_{th(r)}$	rising threshold voltage	V_P rising; I_{REG1} = 50 mA; note 3	4.5	$V_{O(REG2)}$ – 0.15	$V_{O(REG2)}$ – 0.1	V
Schmitt triggers for HOLD output						
$V_{th(r)(REG1)}$	rising threshold voltage of regulator 1	V_P rising; note 3	–	$V_{O(REG1)}$ – 0.15	$V_{O(REG1)}$ – 0.075	V
$V_{th(f)(REG1)}$	falling threshold voltage of regulator 1	V_P falling; note 3	8.1	$V_{O(REG1)}$ – 0.35	–	V
$V_{hys(REG1)}$	hysteresis voltage due to regulator 1		–	0.2	–	V
$V_{th(r)(REG3)}$	rising threshold voltage of regulator 3	V_P rising; note 3	–	$V_{O(REG3)}$ – 0.15	$V_{O(REG3)}$ – 0.075	V
$V_{th(f)(REG3)}$	falling threshold voltage of regulator 3	V_P falling; note 3	4.1	$V_{O(REG3)}$ – 0.35	–	V
$V_{hys(REG3)}$	hysteresis voltage due to regulator 3		–	0.2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{th(r)(VP)}$	rising threshold voltage of supply voltage	V_{EN} = 0 V	9.1	9.7	10.3	V
$V_{th(f)(VP)}$	falling threshold voltage of supply voltage	V_{EN} = 0 V	9.0	9.4	9.8	V
$V_{hys(VP)}$	hysteresis voltage of supply voltage	V_{EN} = 0 V	–	0.3	–	V
Reset and hold buffer						
$I_{sink(L)}$	LOW-level sink current	$V_{RES} \leq 0.8$ V; $V_{HOLD} \leq 0.8$ V	2	–	–	mA
I_{LO}	output leakage current	V_P = 14.4 V; V_{RES} = 5 V; V_{HOLD} = 5 V	–	0.1	5	µA
t_r	rise time	note 4	–	7	50	µs
t_f	fall time	note 4	–	1	50	µs
Reset delay						
I_{ch}	charge current		2	4	8	µA
I_{dch}	discharge current		500	800	–	µA
$V_{th(r)(RES)}$	rising voltage threshold reset signal		2.5	3.0	3.5	V
$t_{d(RES)}$	delay time reset signal	C = 47 nF; note 5	20	35	70	ms
$V_{th(r)(SW)}$	rising voltage threshold switch foldback protection		–	$V_{O(REG2)}$	–	V
$t_{d(SW)}$	delay time switch foldback protection	C = 47 nF; note 6	8	17.6	40	ms
Regulator 1 (I_{REG1} = 5 mA; unless otherwise specified)						
$V_{O(off)}$	output voltage off		–	1	400	mV
$V_{O(REG1)}$	output voltage	1 mA $\leq I_{REG1} \leq$ 600 mA	8.5	9.0	9.5	V
		12 V $\leq V_P \leq$ 18 V	8.5	9.0	9.5	V
ΔV_{line}	line regulation	12 V $\leq V_P \leq$ 18 V	–	2	75	mV
ΔV_{load}	load regulation	1 mA $\leq I_{REG1} \leq$ 600 mA	–	20	100	mV
I_q	quiescent current	I_{REG1} = 600 mA	–	25	60	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_{drop}	drop-out voltage	I_{REG1} = 550 mA; V_P = 9.5 V; note 7	–	0.4	0.7	V
I_{lim}	current limit	$V_{O(REG1)}$ > 8.5 V; note 8	0.65	1.2	–	A
I_{sc}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 9	250	800	–	mA
Regulator 2 (I_{REG2} = 5 mA; unless otherwise specified)						
$V_{O(REG2)}$	output voltage	0.5 mA $\leq I_{REG2} \leq$ 300 mA	4.75	5.0	5.25	V
		8 V $\leq V_P \leq$ 18 V	4.75	5.0	5.25	V
		18 V $\leq V_P \leq$ 50 V; $I_{REG2} \leq$ 150 mA	4.75	5.0	5.25	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{line}	line regulation	6 V ≤ V_P ≤ 18 V	–	2	50	mV
		6 V ≤ V_P ≤ 50 V	–	15	75	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG2} ≤ 150 mA	–	20	50	mV
		1 mA ≤ I_{REG2} ≤ 300 mA	–	–	100	mV
SVRR	supply voltage ripple rejection	f = 3 kHz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_{drop}	drop-out voltage	I_{REG2} = 100 mA; V_P = 4.75 V; note 7	–	0.4	0.6	V
		I_{REG2} = 200 mA; V_P = 5.75 V; note 7	–	0.8	1.2	V
		I_{REG2} = 100 mA; V_{BU} = 4.75 V; note 10	–	0.2	0.5	V
		I_{REG2} = 200 mA; V_{BU} = 5.75 V; note 10	–	0.8	1.0	V
I_{lim}	current limit	$V_{O(REG2)}$ > 4.5 V; note 8	0.32	0.37	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 9	20	100	–	mA
Regulator 3 (I_{REG3} = 5 mA; unless otherwise specified)						
$V_{O(off)}$	output voltage off		–	1	400	mV
$V_{O(REG3)}$	output voltage	1 mA ≤ I_{REG3} ≤ 750 mA	4.75	5.0	5.25	V
		7 V ≤ V_P ≤ 18 V	4.75	5.0	5.25	V
ΔV_{line}	line regulation	7 V ≤ V_P ≤ 18 V	–	2	50	mV
ΔV_{load}	load regulation	1 mA ≤ I_{REG3} ≤ 750 mA	–	20	100	mV
I_q	quiescent current	I_{REG3} = 750 mA	–	19	45	mA
SVRR	supply voltage ripple rejection	f_i = 3 kHz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_{drop}	drop-out voltage	I_{REG3} = 500 mA; V_P = 5.75 V; note 7	–	1	1.5	V
I_{lim}	current limit	$V_{O(REG3)}$ > 4.5 V; note 8	0.80	0.90	–	A
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω; note 9	100	400	–	mA
Power switch						
V_{drop}	drop-out voltage	I_{SW} = 1 A; V_P = 13.5 V; note 11	–	0.45	0.70	V
		I_{SW} = 1.8 A; V_P = 13.5 V; note 11	–	1.0	1.8	V
I_{dc}	continuous current	V_P = 16 V; V_{SW} = 13.5 V	1.8	2.0	–	A
V_{clamp}	clamping voltage	V_P ≥ 17 V	13.5	15.0	16.0	V
I_M	peak current	V_P = 17 V; notes 6, 12 and 13	3	–	–	A
V_{fb}	flyback voltage behaviour	I_{SW} = −100 mA	–	V_P + 3	22	V
I_{sc}	short-circuit current	V_P = 14.4 V; V_{SW} < 1.2 V; note 13	–	0.8	–	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Backup switch						
I_{dc}	continuous current		0.3	0.35	–	A
V_{clamp}	clamping voltage	$V_P \geq 16.7$ V	–	–	16	V
I_r	reverse current	$V_P = 0$ V; $V_{BU} = 12.4$ V	–	–	–900	µA
Schmitt trigger for enable input of ignition 1						
$V_{th(r)}$	rising threshold voltage of ignition 1 input		2.75	3.25	3.75	V
$V_{th(f)}$	falling threshold voltage of ignition 1 input		0.8	–	1.3	V
V_{hys}	hysteresis voltage		1.5	–	–	V
I_{LI}	input leakage current	$V_{IGN1IN} = 5$ V	–	–	1.0	µA
$I_{I(clamp)}$	input clamping current	$V_{IGN1IN} > 50$ V	–	–	50	mA
$V_{IH(clamp)}$	HIGH-level input clamping voltage		V_P	–	50	V
$V_{IL(clamp)}$	LOW-level input clamping voltage		–0.6	–	0	V
Schmitt trigger for power supply of ignition 1						
$V_{th(r)}$	rising threshold voltage		6.5	7.0	7.5	V
$V_{th(f)}$	falling threshold voltage	note 14	4.0	4.5	5.0	V
Ignition 1 buffer						
V_{OL}	LOW-level output voltage	$I_{IGN1OUT} = 0$ mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	$I_{IGN1OUT} = 0$ mA	4.5	5.0	5.25	V
I_{OL}	LOW-level output current	$V_{IGN1OUT} \leq 0.8$ V	0.45	0.8	–	mA
I_{LO}	output leakage current	$V_{IGN1OUT} = 5$ V; $V_{IGN1IN} = 0$ V	–	–	1.0	µA
t_{PLH}	LOW-to-HIGH propagation time	V_{IGN1IN} falling from 3.75 to 0.8 V	–	–	500	µs
t_{PHL}	HIGH-to-LOW propagation time	V_{IGN1IN} rising from 0.8 to 3.75 V	–	–	500	µs
Schmitt trigger for enable input of ignition 2						
$V_{th(r)}$	rising threshold voltage of ignition 2 input	$V_P > 3.5$ V	1.9	2.2	2.5	V
$V_{th(f)}$	falling threshold voltage of ignition 2 input	$V_P > 3.5$ V	1.7	2.0	2.3	V
V_{hys}	hysteresis voltage	$V_P > 3.5$ V	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{IGN2IN} = 5$ V	–	–	1.0	µA
$I_{I(clamp)}$	input clamp current	$V_{IGN2IN} > 50$ V	–	–	50	mA
$V_{IH(clamp)}$	HIGH-level input clamping voltage		V_P	–	50	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IL(clamp)}$	LOW-level input clamping voltage		–0.6	–	0	V
Ignition 2 buffer						
V_{OL}	LOW-level output voltage	$I_{IGN2OUT}$ = 0 mA	0	0.2	0.8	V
V_{OH}	HIGH-level output voltage	$I_{IGN2OUT}$ = 0 mA	4.5	5.0	5.25	V
I_{OL}	LOW-level output current	$V_{IGN2OUT} \leq 0.8$ V	0.45	0.8	–	mA
I_{OH}	HIGH-level output current	$V_{IGN2OUT} \geq 4.5$ V	–0.45	–2.0	–	mA
I_{LO}	output leakage current (source)	$V_{IGN2OUT}$ = 5 V; V_{IGN2IN} = 5 V	–	–	1.0	µA
t_{PLH}	LOW-to-HIGH propagation time	V_{IGN2IN} rising from 1.7 to 2.5 V	–	–	500	µs
t_{PHL}	HIGH-to-LOW propagation time	V_{IGN2IN} falling from 2.5 to 1.7 V	–	–	500	µs

Notes

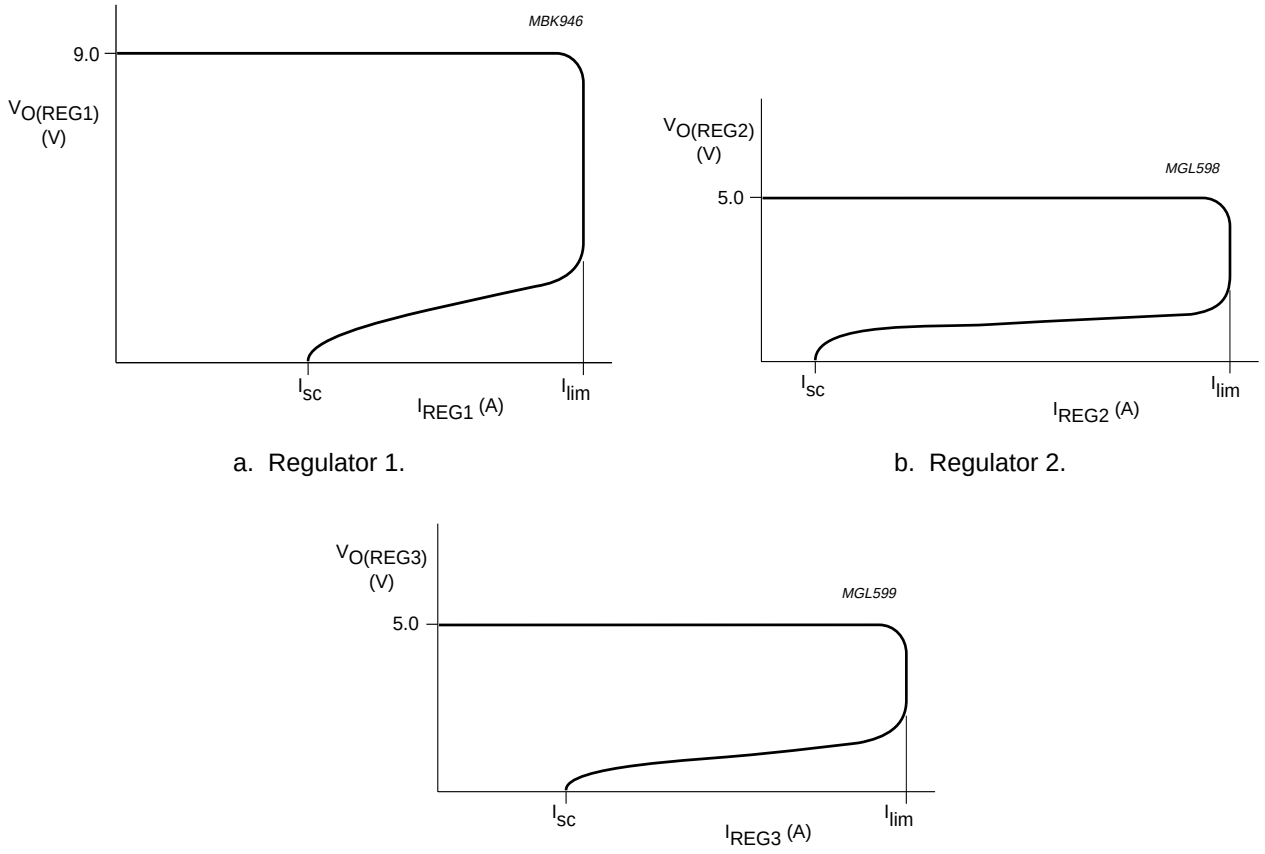
1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The quiescent current is measured in the standby mode with pins EN1, EN2 and ENSW connected to ground and $R_{L(REG2)} = \infty$; (see Fig.8).
3. The voltage of the regulator drops as a result of a V_P drop.
4. The rise and fall times are measured with a 10 kΩ pull-up resistor and a 50 pF load capacitor.
5. The delay time depends on the value of the capacitor connected to pin C_{RES}:

$$t_{d(RES)} = \frac{C}{I_{ch}} \times V_{th(r)(RES)} = C \times (750 \times 10^3) \text{ [s]}$$

6. The delay time depends on the value of the capacitor connected to pin C_{RES}:

$$t_{d(RES)} = \frac{C}{I_{ch}} \times (V_{OREG2)} - 3.5) = C \times (375 \times 10^3) \text{ [s]}$$

7. The drop-out voltage of regulators 1, 2 and 3 is measured between pins V_P and REGn.
8. At current limit, I_{lim} is held constant (see Fig.6 for the behaviour of I_{lim}).
9. The foldback current protection limits the dissipated power at short-circuit (see Fig.6).
10. The drop-out voltage is measured between pins BU and REG2.
11. The drop-out voltage of the power switch is measured between pins V_P and SW.
12. The maximum output current of the power switch is limited to 1.8 A when the supply voltage exceeds 18 V. A test-mode is built-in. The delay time of the power switch is disabled when a voltage of V_P + 1 V is applied to the switch-enable input.
13. At short-circuit, I_{sc} of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms. A test-mode is built-in. The delay time of the switch is disabled when a voltage of V_P + 1 V is applied to the switch-enable input.
14. $V_{IGN1OUT}$ = LOW for $V_{IGN1IN} > 1.2$ V or $V_{EN1} > 1.3$ V or $V_{EN3} > 1.3$ V or $V_{ENSW} > 1.3$ V.



a. Regulator 1.

b. Regulator 2.

c. Regulator 3.

Fig.6 Foldback current protection of the regulators.

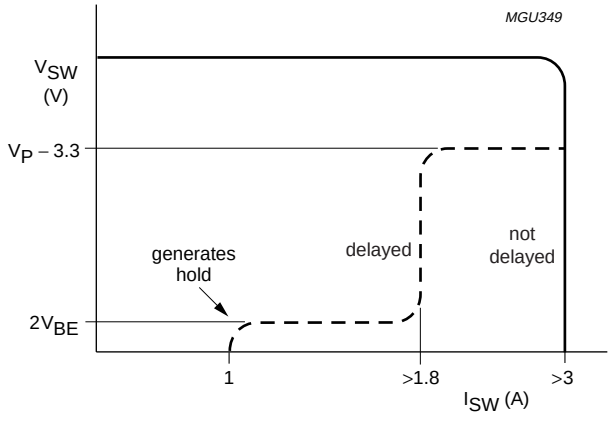


Fig.7 Current protection of the power switch.

TEST AND APPLICATION INFORMATION

Test information

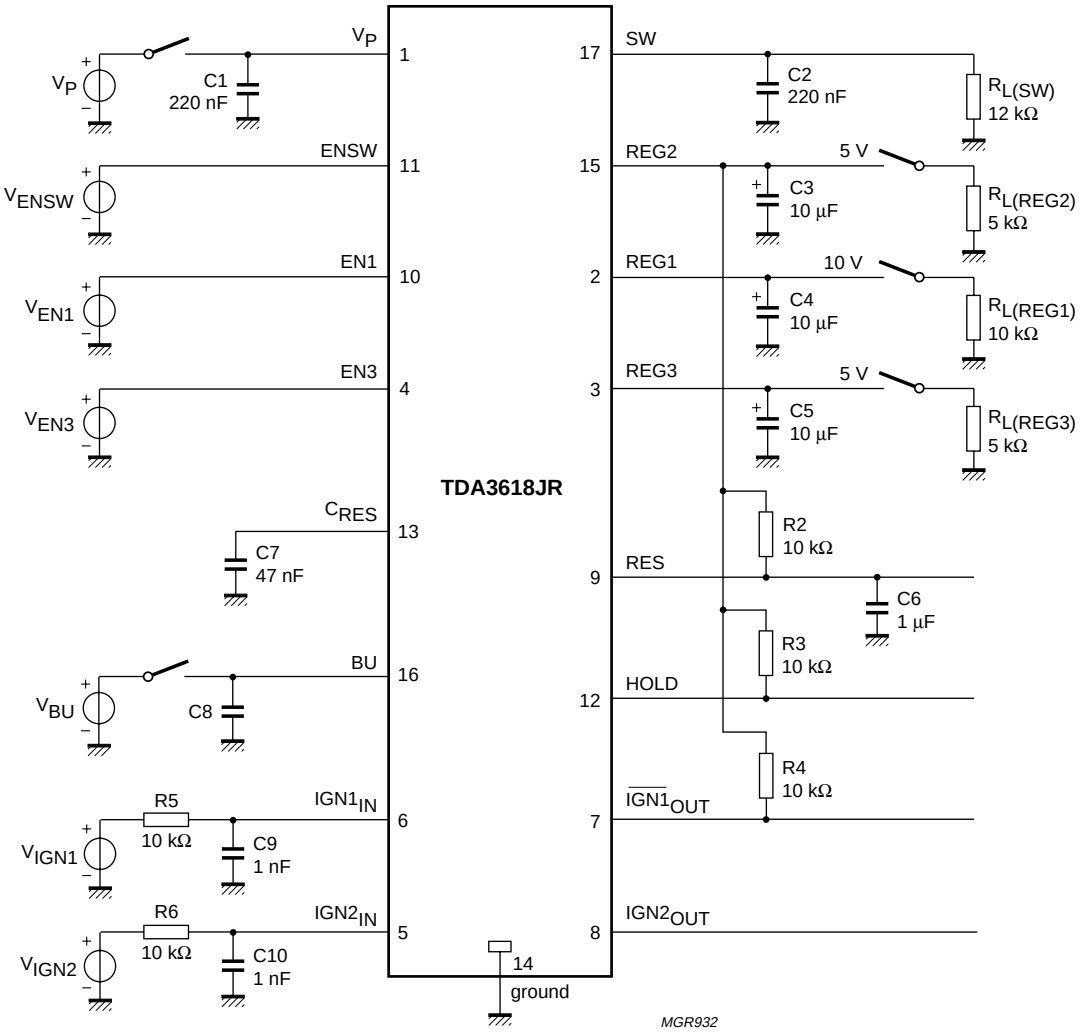


Fig.8 Test circuit.

Application information

NOISE

Table 1 Noise figures

REGULATOR	NOISE FIGURE (μV)(1)		
	C_o = 10 μF	C_o = 47 μF	C_o = 100 μF
1	170	130	110
2	180	120	100
3	100	70	65

Note

1. Measured at a bandwidth of 200 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by means of the output capacitors). When a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to pins 1 and 14 (supply and ground), the noise is minimal.

STABILITY

The regulators are stabilized with the externally connected output capacitors. The output capacitors can be selected using the graphs of Figs 9 and 10. When an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at a low temperature.

The two examples show how an output capacitor value is selected.

Example 1

Regulators 1 and 3 are stabilized with an electrolytic output capacitor of 220 μF (ESR = 0.15 Ω).
At T_{amb} = –30 °C the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω. The regulator will remain stable at T_{amb} = –30 °C (see Fig.9).

Example 2

Regulator 2 is stabilized with a 10 μF electrolytic capacitor (ESR = 3 Ω). At T_{amb} = –30 °C the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω. The regulator will be unstable at T_{amb} = –30 °C (see Fig.10).

Solution

To avoid problems with stability at low temperatures, the use of tantalum capacitors is recommended. Use a tantalum capacitor of 10 μF or a larger electrolytic capacitor.

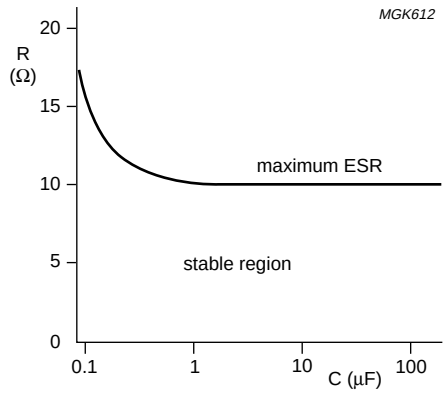


Fig.9 Curve for selecting the value of output capacitor for regulators 1 and 3.

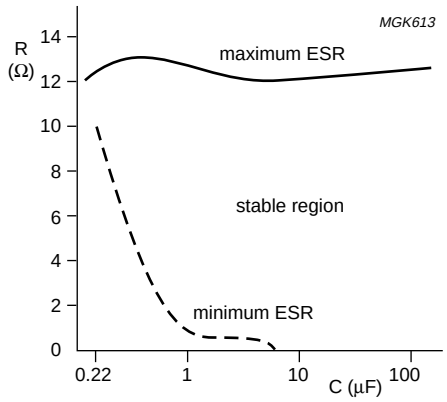
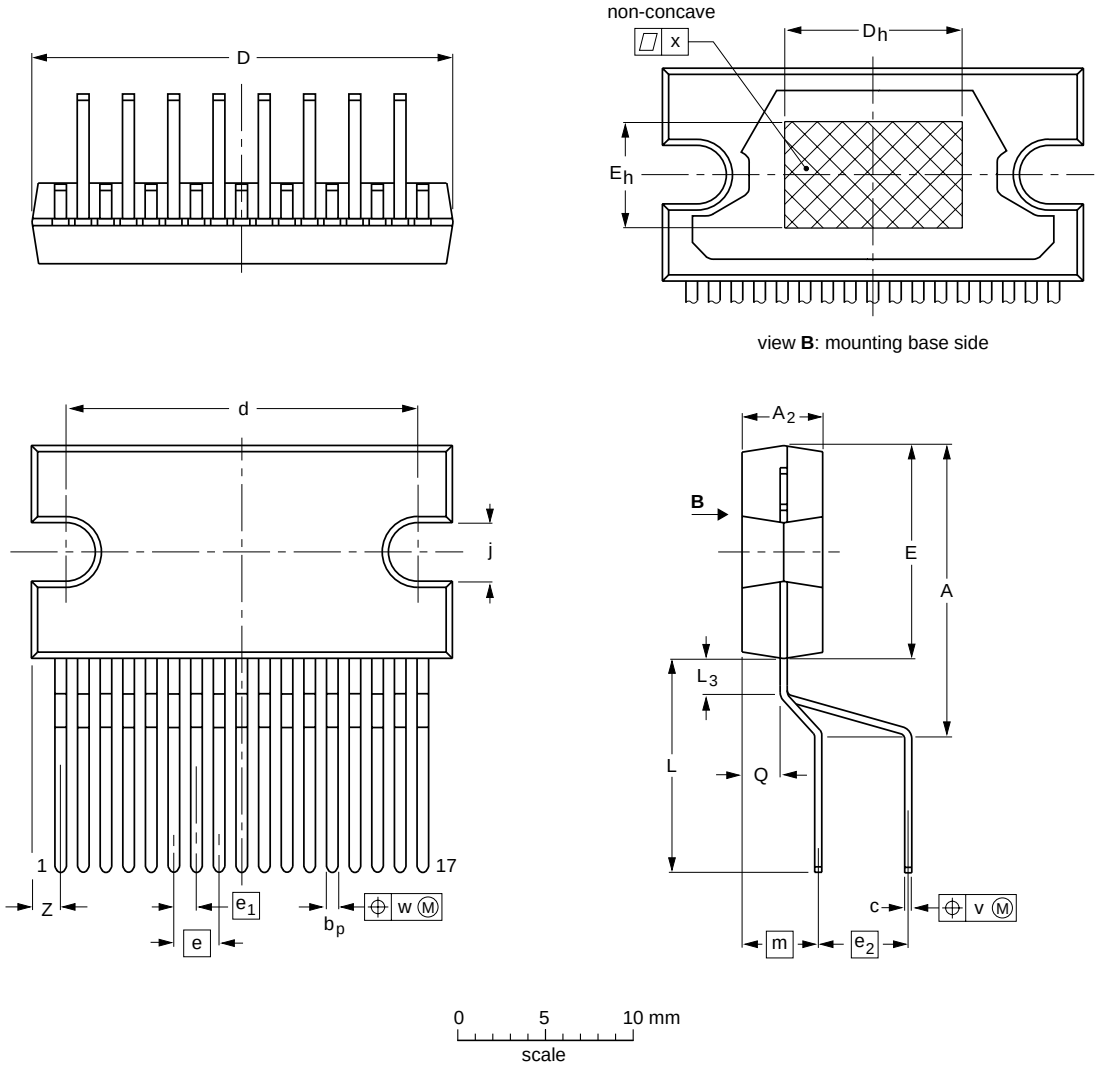


Fig.10 Curve for selecting the value of output capacitor for regulator 2.

PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL (special bent) power package; 17 leads (lead length 12 mm) **SOT475-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT475-1						~~97-05-20~~ 99-12-17

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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