NEC

MOS INTEGRATED CIRCUIT

μPD72107

LAP-B CONTROLLER

Link Access Procedure Balanced mode

The μPD72107 is an LSI that supports LAP-B protocol specified by the ITU-T recommended X.25 on a single chip.

FEATURES

- Complied with ITU-T recommended X.25 (LAP-B84 edition)
  - HDLC frame control
  - Sequence control
  - Flow control
- ITU-T recommended X.75 supported
- TTC standard JT-T90 supported
- Optional functions
  - Option frame
  - Global address frame
  - Error check deletion frame
- Powerful test functions
  - Data loopback function
  - Loopback test link function
  - Frame trace function
- Abundant statistical information
- Detailed mode setting function
- Modem control function
- On-chip DMAC (Direct Memory Access Controller)
  - 24-bit address
  - Byte/word transfer enabled (switch with external pin)
- Memory-based interface
  - Memory-based command
  - Memory-based status
  - Memory-based transmit/receive data
- MAX.4 Mbps serial transfer rate
- NRZ, NRZI coding

ORDERING INFORMATION

Part Number	Package
μPD72107CW	64-pin plastic shrink DIP (750 mils)
μPD72107GC-3B9	80-pin plastic QFP (14 x 14 mm)
μPD72107L	68-pin plastic QFJ (950 x 950 mils)

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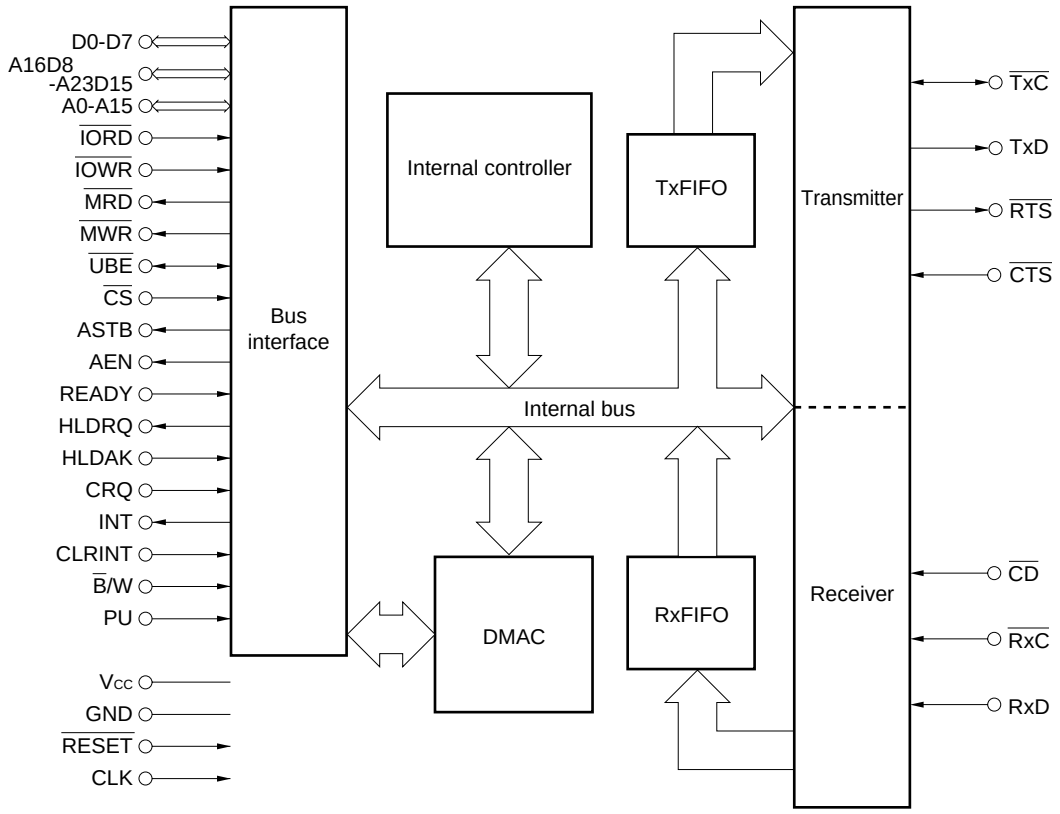
BLOCK DIAGRAM

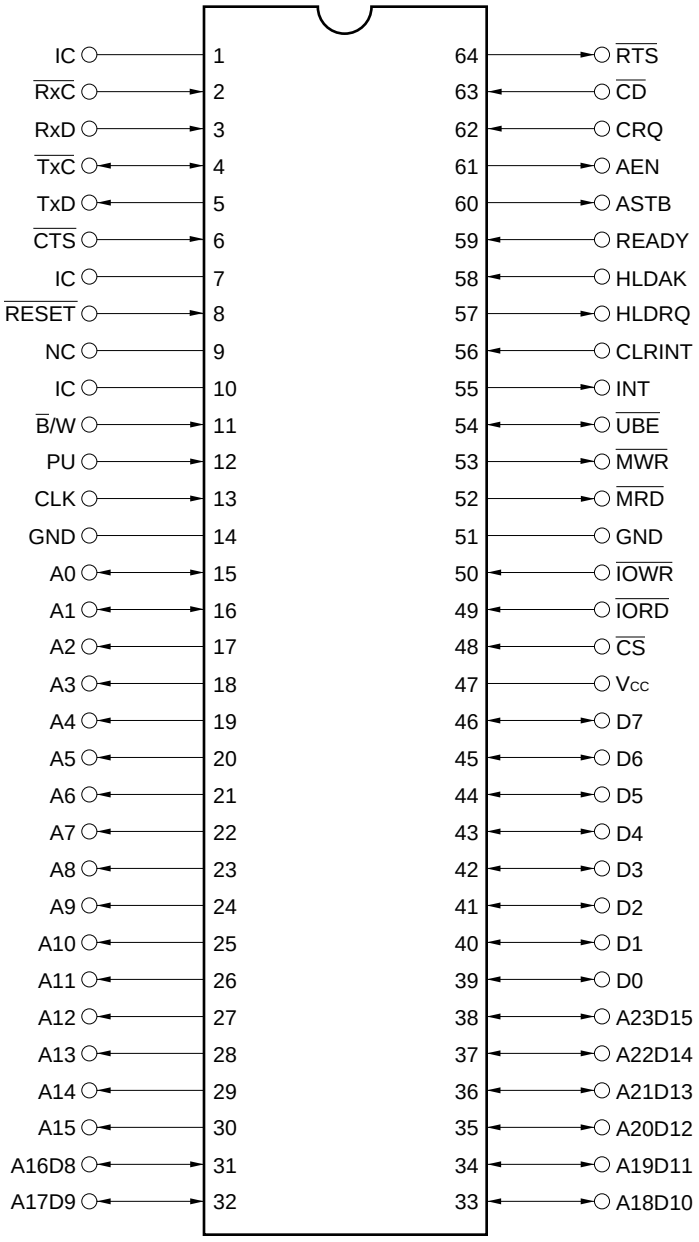


Name	Function
Bus interface	An interface between the μPD72107 and external memory or external host processor
Internal controller	Manages LAP-B protocol including control of the DMAC block, transmitter block, and receiver block
DMAC (Direct Memory Access Controller)	Controls the transfer of data on the external memory to the internal controller or transmitter block, and controls the writing of data in the internal controller or receiver block to the external memory
TxFIFO	A 16-byte buffer for when transmit data is sent from the DMAC to the transmitter block
RxFIFO	A 32-byte buffer for when receive data is sent from the receiver block to the DMAC
Transmitter	Converts the contents of TxFIFO into an HDLC frame and transmits it as serial data
Receiver	Receives HDLC frame and writes internal data to RxFIFO
Internal bus	An 8-bit address bus and 8-bit data bus that connect the internal controller, DMAC, FIFO, serial block, and bus interface block

PIN CONFIGURATION (Top View)

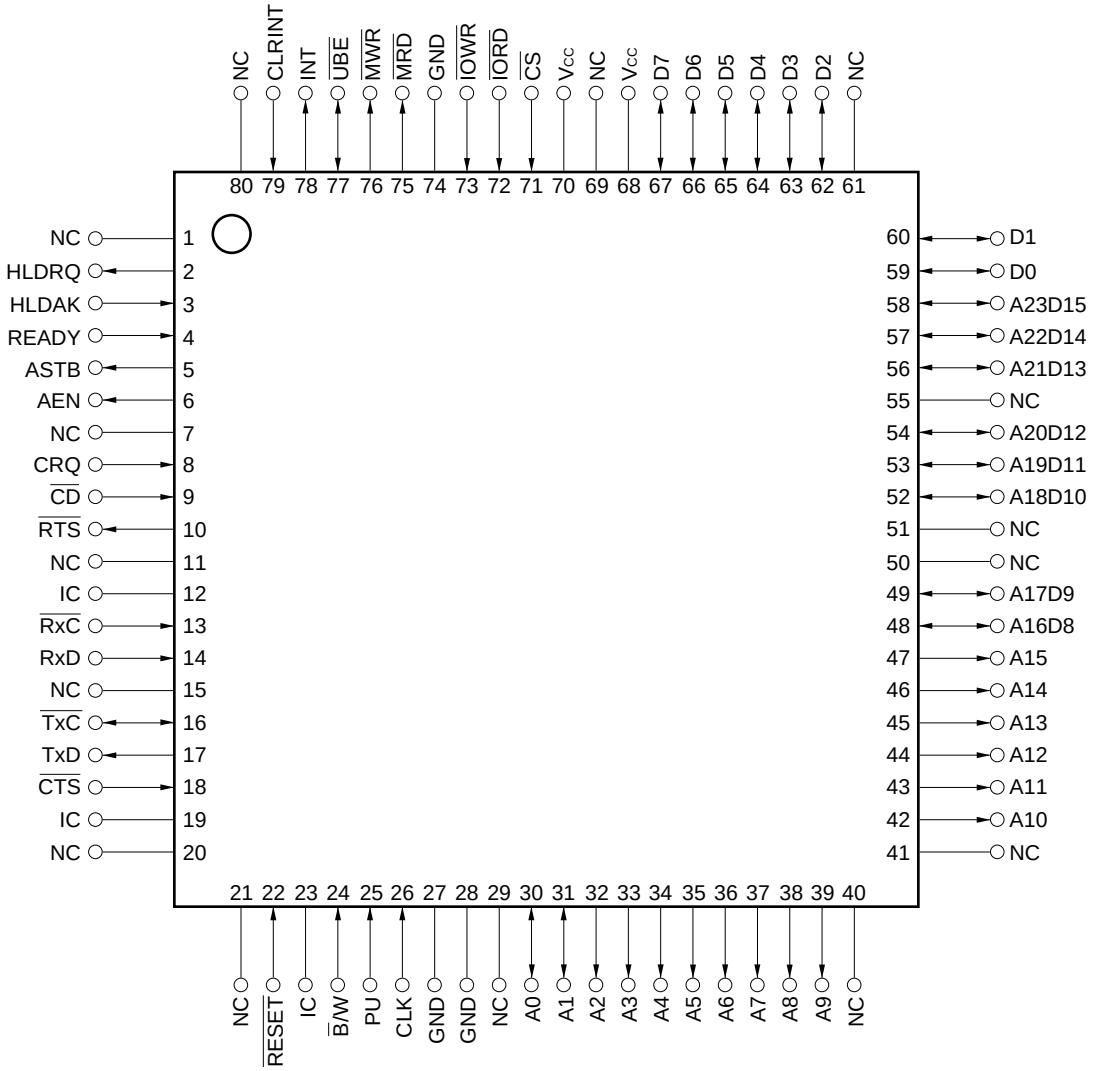
64-pin plastic shrink DIP (750 mils)

μPD72107CW



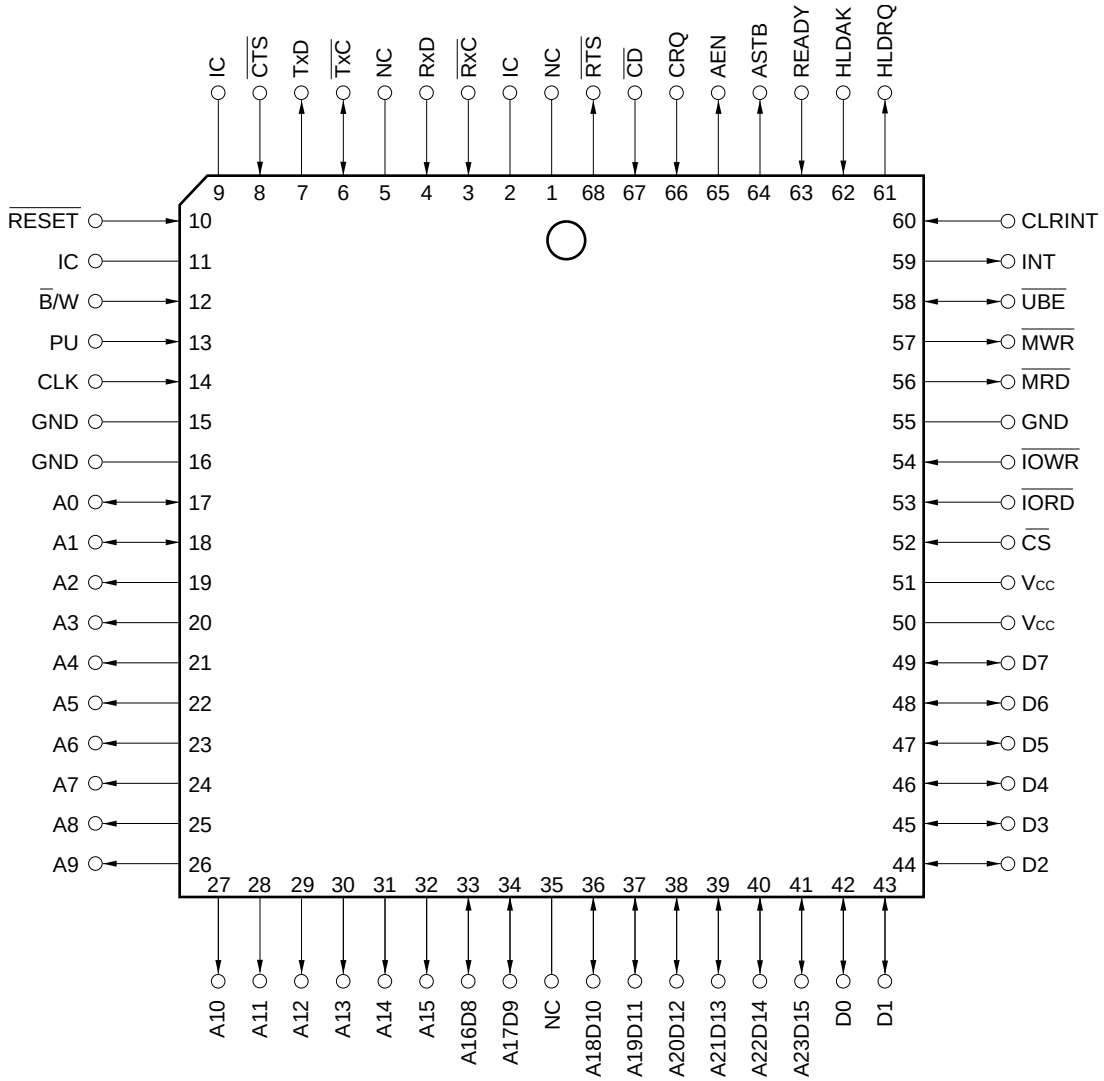
80-pin plastic QFP (14 × 14 mm)

μPD72107GC-3B9



68-pin plastic QFJ (950 × 950 mils)

μPD72107L



1. PINS

1.1 Pin Functions

Pin Name	SDIP Pin No.	QFP Pin No.	QFJ Pin No.	I/O	Active Level	Function
V_{CC}	47	68 70	50 51	–	–	+5 V power supply
GND	14 51	27 28 74	15 16 55	–	–	Ground (0 V) Note that there is more than one ground pin.
CLK (Clock)	13	26	14	I	–	System clock input Input clock of 1 MHz to 8.2 MHz.
$\overline{\text{RESET}}$ (Reset)	8	22	10	I	L	Initializes the internal μPD72107. Active width of more than 7 CLK clock cycles is required (clock input is required). After reset, this pin becomes a bus slave.
PU (Pull Up)	12	25	13	I	–	Pull up to high level when using in normal operation.
$\overline{\text{CS}}$ (Chip Select)	48	71	52	I	L	When bus master Set to disable.
						When bus slave Read/write operation from the host processor at low level is enabled.
$\overline{\text{MRD}}$ (Memory Read)	52	75	56	O 3-state	L	When bus master Reads the data of the external memory at low level.
						When bus slave High impedance
$\overline{\text{MWR}}$ (Memory Write)	53	76	57	O 3-state	L	When bus master Writes the data to the external memory at low level.
						When bus slave High impedance
$\overline{\text{IORD}}$ (I/O Read)	49	72	53	I	L	This pin is used when the external host processor reads the contents of the internal registers of the μPD72107.
$\overline{\text{IOWR}}$ (I/O Write)	50	73	54	I	L	This pin is used when the external host processor writes the data to the internal registers of the μPD72107.
ASTB (Address Strobe)	60	5	64	O	H	This pin is used to latch the address output from the μPD72107 externally.

<table>
<tr><th>Pin Name</th><th>SDIP Pin No.</th><th>QFP Pin No.</th><th>QFJ Pin No.</th><th>I/O</th><th>Active Level</th><th>Function</th></tr>
<tr><td>NC
(No Connection)</td><td>9</td><td>1, 7,
11, 15,
20, 21,
29, 40,
41, 50,
51, 55,
61, 69,
80</td><td>1
5
35</td><td>–</td><td>–</td><td>Use this pin open.</td></tr>
<tr><td>IC
(Internally
Connected)</td><td>1
7
10</td><td>12
19
23</td><td>2
9
11</td><td>–</td><td>–</td><td>Do not connect anything to this pin.</td></tr>
<tr><td>$\overline{\text{UBE}}$
(Upper Byte
Enable)</td><td>54</td><td>77</td><td>58</td><td>I/O
3-state</td><td>L/H</td><td>When bus master (output)
The signal output from this pin changes according to the input value of the $\overline{\text{B}}$/W pin.
• Byte transfer mode ($\overline{\text{B}}$/W = 0)
$\overline{\text{UBE}}$ is always high impedance.
• Word transfer mode ($\overline{\text{B}}$/W = 1)
Indicates that valid data is either in pins D0 to D7 or pins A16D8 to A23D15 (or both).
<table>
<tr><th>$\overline{\text{UBE}}$</th><th>A0</th><th>D0 to D7</th><th>A16D8 to A23D15</th></tr>
<tr><td>0</td><td>0</td><td>○</td><td>○</td></tr>
<tr><td>0</td><td>1</td><td>×</td><td>○</td></tr>
<tr><td>1</td><td>0</td><td>○</td><td>×</td></tr>
<tr><td>1</td><td>1</td><td>×</td><td>×</td></tr>
</table>
When bus slave (input)
$\overline{\text{UBE}}$ pin becomes input, and indicates that valid data is either in pins D0 to D7 or pins A16D8 to A23D15.
<table>
<tr><th>$\overline{\text{UBE}}$</th><th>A0</th><th>D0 to D7</th><th>A16D8 to A23D15</th></tr>
<tr><td>0</td><td>0</td><td>○</td><td>×</td></tr>
<tr><td>0</td><td>1</td><td>×</td><td>○</td></tr>
<tr><td>1</td><td>0</td><td>○</td><td>×</td></tr>
<tr><td>1</td><td>1</td><td>○</td><td>×</td></tr>
</table></td></tr>
</table>

Pin Name	SDIP Pin No.	QFP Pin No.	QFJ Pin No.	I/O	Active Level	Function
$\overline{B}$/W (Byte/Word)	11	24	12	I	L/H	Specifies the data bus that accesses the external memory when bus master. $\overline{B}$/W = 0 Byte units (8 bits) $\overline{B}$/W = 1 Word units (16 bits) After power-on, fix the status of the $\overline{B}$/W pin. In the case of word access, the lower data bus is the contents data of even addresses.
READY (Ready)	59	4	63	I	H	An input signal that is used to extend the $\overline{MRD}$ and $\overline{MWR}$ signal widths output by the μPD72107 to adapt to low-speed memory. When the READY signal is low level, the $\overline{MRD}$ and $\overline{MWR}$ signals maintain active low. Do not change the READY signal at any time other than the specified setup/ hold time.
HLDRQ (Hold Request)	57	2	61	O	H	A hold request signal to the external host processor. When a DMA operation is performed in the μPD72107, this signal is activated to switch from bus slave to bus master.
HLDAK (Hold Acknowledge)	58	3	62	I	H	A hold acknowledge signal from the external host processor. When the μPD72107 detects that this signal is active, the bus slave switches to bus master, and a DMA operation is started.
AEN (Address Enable)	61	6	65	O	H	When bus master, this signal enables the latched higher addresses and outputs them to system address bus. This signal is also used for disabling other system bus drivers.
A0, A1	15, 16	30, 31	17, 18	I/O 3-state	–	Bidirectional 3-state address lines. When bus master (output) Indicate the lower 2-bit addresses of memory access.
						When bus slave (input) Input addresses when the external host processor I/O accesses the μPD72107.
A2 to A15	17 to 30	32 to 47 (except 40, 41)	19 to 32	O 3-state	–	When bus master Output bit 2 to bit 15 of memory access addresses.
						When bus slave Become high impedance.

Pin Name	SDIP Pin No.	QFP Pin No.	QFJ Pin No.	I/O	Active Level	Function
A16D8 to A23D15	31 to 38	48 to 58 (except 50, 51, 55)	33 to 41 (except 35)	I/O 3-state	–	Bidirectional 3-state address/data buses. Multiplex pins of the higher 16 bits to 23 bits of addresses and the higher 8 bits to 15 bits of data.
D0 to D7	39 to 46	59 to 67 (except 61)	42 to 49	I/O 3-state	–	Bidirectional 3-state data buses. When bus master When writing to external memory, these pins become input if reading at output.
						When bus slave Usually, these pins become high impedance. When the external host processor reads I/O of the μPD72107, the internal register data is output.
CRQ (Command Request)	62	8	66	I	H	A signal requesting command execution to the μPD72107 by the external host processor. The μPD72107 starts fetching commands from on the external memory at the rising edge of this signal.
INT (Interrupt)	55	78	59	O	H	An interrupt signal from the μPD72107 to the external host processor.
CLRINT (Clear Interrupt)	56	79	60	I	H	A signal inactivating the INT signal being output by the μPD72107. The μPD72107 generates the CLRINT signal in the LSI internal circuit at the rising edge of this signal, and forcibly makes the INT output signal low.
$\overline{\text{CTS}}$ (Clear To Send)	6	18	8	I	–	A general-purpose input pin. The μPD72107 reports the "$\overline{\text{CTS}}$ pin change detection status" to the external host processor when the input level of this pin is changed in the general-purpose input/output pin support (setting RSSL to 1 by the "system initialization command"). The change of input level is recognized only when the same level is sampled twice in succession after sampling in 8-ms cycles and detecting the change. Moreover, when the external host processor issues a "general-purpose input/output pin read command" to the μPD72107, the μPD72107 reports the pin information of this pin to the external host processor by a "general-purpose input/output pin read response status". The change can be detected even in the clock input stop status of $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$.

Pin Name	SDIP Pin No.	QFP Pin No.	QFJ Pin No.	I/O	Active Level	Function
$\overline{\text{RTS}}$ (Request To Send)	64	10	68	O	–	A general-purpose output pin. The output value of this pin can be changed by issuing an "$\overline{\text{RTS}}$ pin write command" from the external host processor to the μPD72107. Moreover, when the external host processor issues a "general-purpose input/output pin read command" to the μPD72107, the μPD72107 reports the pin information of this pin to the external host processor by a "general-purpose input/output pin read response status".
$\overline{\text{CD}}$ (Carrier Detect)	63	9	67	I	–	A general-purpose input pin. The μPD72107 reports the "$\overline{\text{CD}}$ pin change detection status" to the external host processor when the input level of this pin is changed in the general-purpose input/output pin support (setting RSSL to 1 by the "system initialization command"). The change of input level is recognized only when the same level is sampled twice in succession after sampling in 8-ms cycles and detecting the change. Moreover, when the external host processor issues a "general-purpose input/output pin read command" to the μPD72107, the μPD72107 reports the pin information of this pin to the external host processor by a "general-purpose input/output pin read response status". The change can be detected even in the clock input stop status of $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$.
TxD (Transmit Data)	5	17	7	O	–	A serial transmit data output pin.
$\overline{\text{TxC}}$ (Transmit Clock)	4	16	6	I/O 3-state	–	When CLK is set to 01 or 10 by "operation mode setting LCW" (output) Outputs a clock that divides by 16 the input signal of the $\overline{\text{RxC}}$ pin or CLK pin made by the μPD72107. **Caution $\overline{\text{TxC}}$ becomes input because CLK = 00 is the default after reset. It becomes output after setting CLK to 01 or 10 by "operation mode setting LCW".**
						When CLK is set to 00 by "operation mode setting LCW" (input) Inputs transmit clock externally.

Remark LCW: abbreviation for Link Command Word

Pin Name	SDIP Pin No.	QFP Pin No.	QFJ Pin No.	I/O	Active Level	Function
RxD (Receive Data)	3	14	4	I	–	A serial receive data input pin.
$\overline{\text{RxC}}$ (Receive Clock)	2	13	3	I	–	When CLK is set to 01 or 10 by "operation mode setting LCW" Sixteen times the clock input of the transmit/receive clock for the on-chip DPLL of the μPD72107
						When CLK is set to 00 by "operation mode setting LCW" One time the clock input of the receive clock

Remark LCW: abbreviation for Link Command Word

1.2 Pin Status after Reset of μPD72107

The status of the output pins and input/output pins after reset in the μPD72107 is as shown in Table 1-1.

Table 1-1. Pin Status after Reset

Pin Number			Pin Name	I/O	During Reset
64-pin SDIP	80-pin QFP	68-pin QFJ			
4	16	6	$\overline{\text{TxC}}$	I/O[Note]	High impedance
5	17	7	TxD	O	H
15, 16	30, 31	17, 18	A0, A1	I/O[Note]	High impedance
17 to 30	32 to 47 (except 40, 41)	19 to 32	A2 to A15	O[Note]	High impedance
31 to 38	48 to 58 (except 50, 51, 55)	33 to 41 (except 35)	A16D8 to A23D15	I/O[Note]	High impedance
39 to 46	59 to 67 (except 61)	42 to 49	D0 to D7	I/O[Note]	High impedance
52	75	56	$\overline{\text{MRD}}$	O[Note]	High impedance
53	76	57	$\overline{\text{MWR}}$	O[Note]	High impedance
54	77	58	$\overline{\text{UBE}}$	I/O[Note]	High impedance
55	78	59	INT	O	L
57	2	61	HLDRQ	O	L
60	5	64	ASTB	O	L
61	6	65	AEN	O	L
64	10	68	$\overline{\text{RTS}}$	O	H

Note 3-state

Remarks 1. The status after reset is released is the same as the status during reset.

2. Input low level to the $\overline{\text{RESET}}$ pin for more than 7 clocks of the system clock.

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I		–0.5 to V_{DD} + 0.3	V
Output voltage	V_O		–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{ILC}	CLK pin	–0.5		+0.8	V
	V_{IL}	Other pins	–0.5		+0.8	V
Input voltage, high	V_{IHC}	CLK and PU pins	+3.3		V_{DD} + 0.3	V
	V_{IH}	Other pins	+2.2		V_{DD} + 0.3	V
Output voltage, low	V_{OL}	I_{OL} = 2.5 mA			0.4	V
Output voltage, high	V_{OH}	I_{OH} = –400 μA	0.7 × V_{DD}			V
Power supply current	I_{DD}	At operation		20	50	mA
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}			±10	μA

Capacitance (T_A = +25°C, V_{DD} = 0 V)

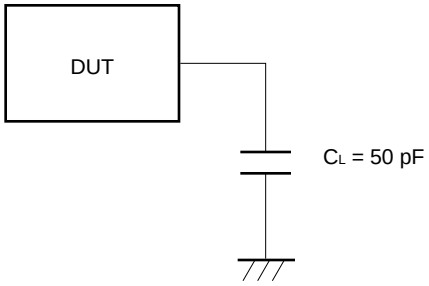
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz	–	8	15	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V	–	8	15	pF
I/O capacitance	C_{IO}		–	8	20	pF

AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

When bus master (1)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLK cycle time	t_{CYK}		121	1000	ns
CLK low-level time	t_{KKL}		50		ns
CLK high-level time	t_{KKH}		50		ns
CLK rise time	t_{KR}	1.5 – 3.0 V		10	ns
CLK fall time	t_{KF}	3.0 – 1.5 V		10	ns

Load condition

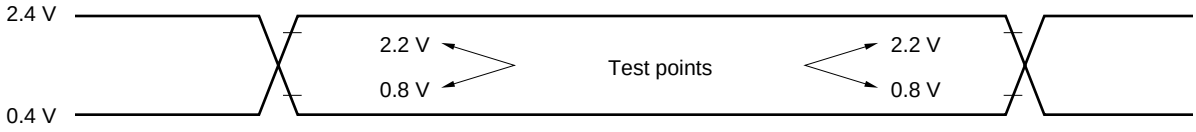


C_L includes jig capacitance.

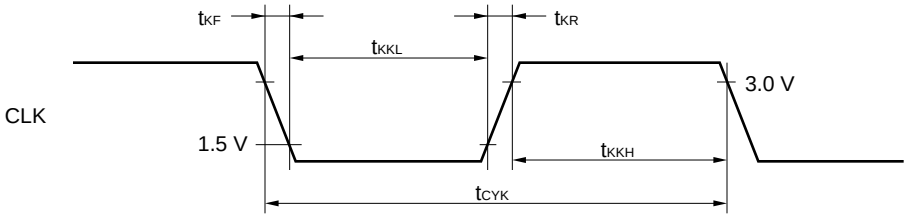
Caution If the load capacitance exceeds 50 pF due to the configuration of the circuit, keep the load capacitance of this device to within 50 pF by inserting a buffer or by some other means.

Remark DUT: device under test

AC test input/output waveform (except clock)



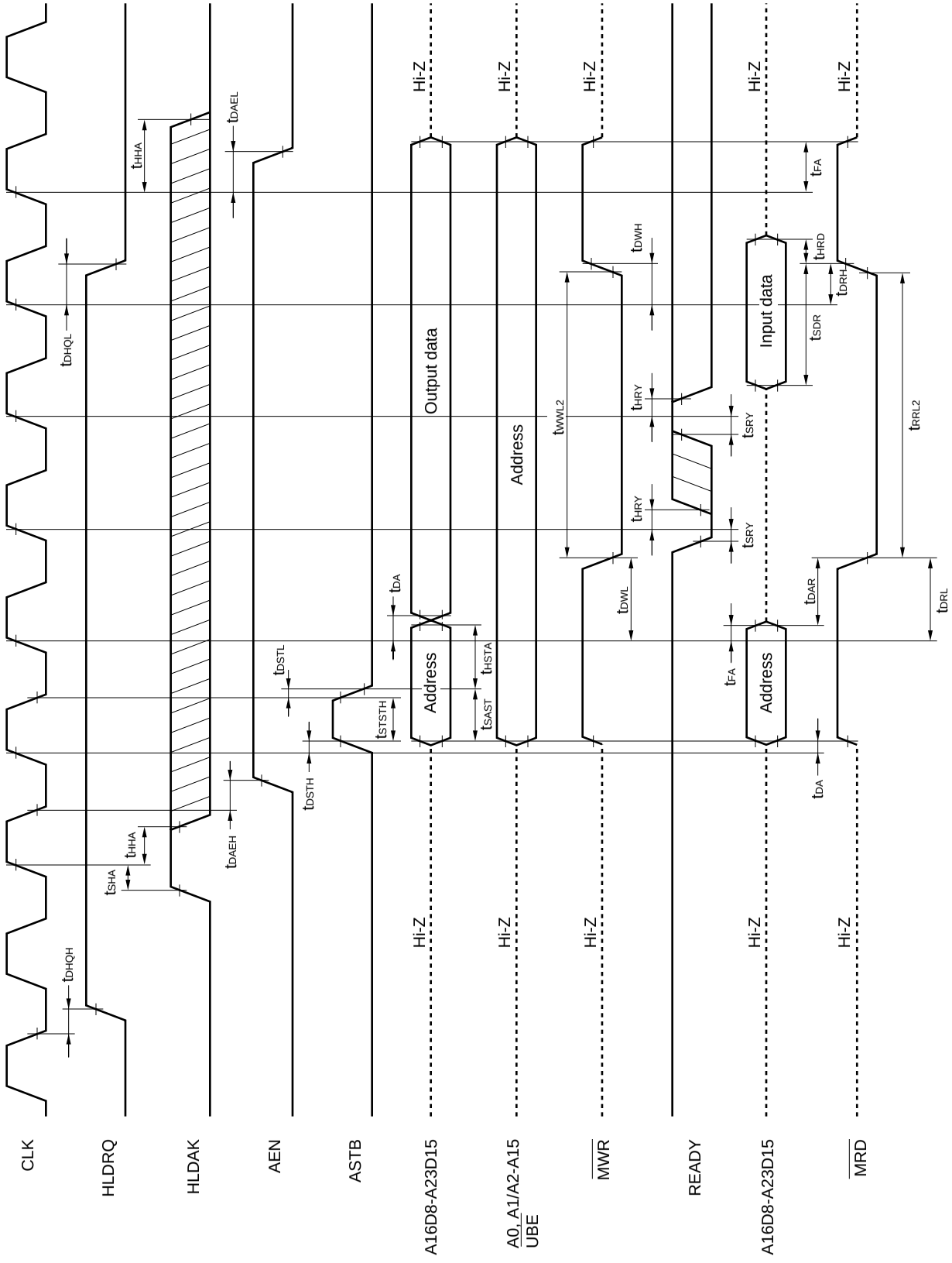
System clock



When bus master (2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
HLDRQ ↑ delay time (vs. CLK ↓)	t_{DHQH}			100	ns
HLDRQ ↓ delay time (vs. CLK ↑)	t_{DHQL}			100	ns
HLDAK setup time (vs. CLK ↑)	t_{SHA}		35		ns
HLDAK hold time (vs. CLK ↑)	t_{HHA}		20		ns
AEN ↑ delay time (vs. CLK ↓)	t_{DAEH}			100	ns
AEN ↓ delay time (vs. CLK ↑)	t_{DAEL}			100	ns
ASTB ↑ delay time (vs. CLK ↑)	t_{DSTH}			70	ns
ASTB high-level width	t_{STSTH}		t_{KKH}–15		ns
ASTB ↓ delay time (vs. CLK ↓)	t_{DSTL}			100	ns
ADR/$\overline{UBE}$/$\overline{MRD}$/$\overline{MWR}$ delay time (vs. CLK ↑)	t_{DA}			100	ns
ADR/$\overline{UBE}$/$\overline{MRD}$/$\overline{MWR}$ float time (vs. CLK ↑)	t_{FA}			70	ns
ADR setup time (vs. ASTB ↓)	t_{SAST}		t_{KKH}–35		ns
ADR hold time (vs. ASTB ↓)	t_{HSTA}		t_{KKL}–20		ns
$\overline{MRD}$ ↓ delay time (vs. ADR float)	t_{DAR}		0		ns
$\overline{MRD}$ ↓ delay time (vs. CLK ↑)	t_{DRL}			70	ns
$\overline{MRD}$ low-level width	t_{RRL2}		$2t_{CYK}$–50		ns
$\overline{MRD}$ ↑ delay time (vs. CLK ↑)	t_{DRH}			70	ns
Data setup time (vs. $\overline{MRD}$ ↑)	t_{SDR}		100		ns
Data hold time (vs. $\overline{MRD}$ ↑)	t_{HRD}		0		ns
$\overline{MWR}$ ↓ delay time (vs. CLK ↑)	t_{DWL}			70	ns
$\overline{MWR}$ low-level width	t_{WWL2}		$2t_{CYK}$–50		ns
$\overline{MWR}$ ↑ delay time (vs. CLK ↑)	t_{DWH}			70	ns
READY setup time (vs. CLK ↑)	t_{SRY}		35		ns
READY hold time (vs. CLK ↑)	t_{HRY}		20		ns

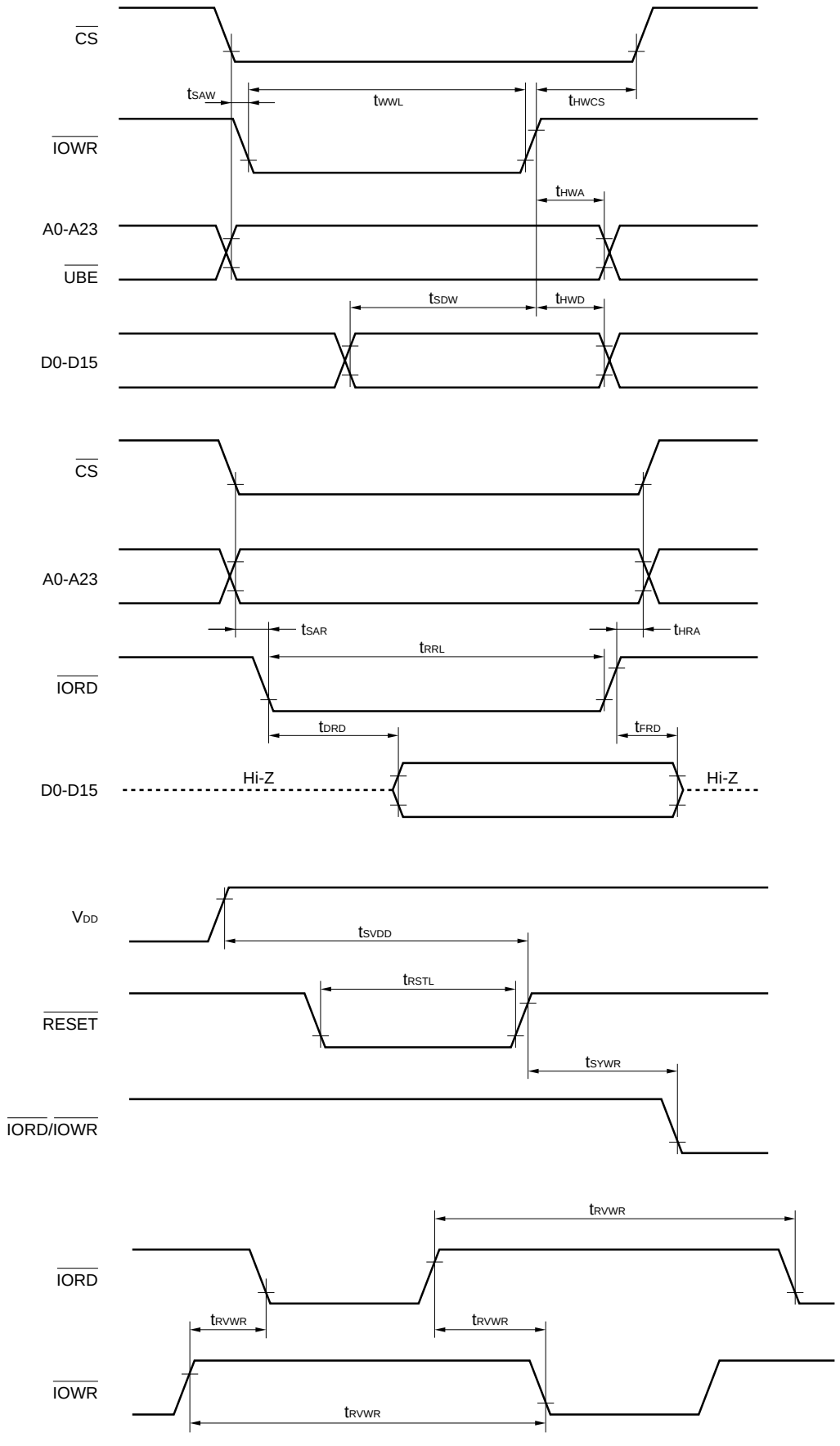
When bus master



When bus slave (1)

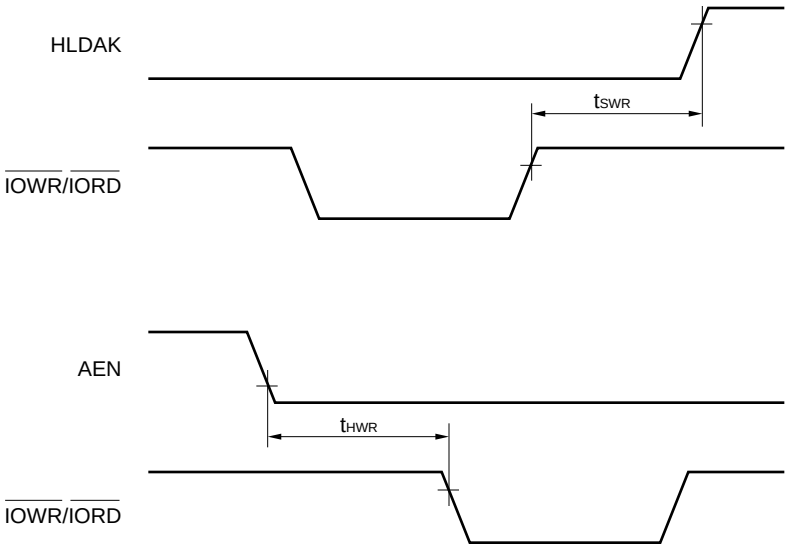
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{IOWR}$ low-level width	t_{WWL}		100		ns
$\overline{CS}$ low-level hold time (vs. $\overline{IOWR}$ ↑)	t_{HWCS}		0		ns
ADR/$\overline{UBE}$/$\overline{CS}$ low-level setup time (vs. $\overline{IOWR}$ ↓)	t_{SAW}		0		ns
ADR/$\overline{UBE}$ hold time (vs. $\overline{IOWR}$ ↑)	t_{HWA}		0		ns
Data setup time (vs. $\overline{IOWR}$ ↑)	t_{SDW}		100		ns
Data hold time (vs. $\overline{IOWR}$ ↑)	t_{HWD}		0		ns
$\overline{IORD}$ low-level width	t_{RRL}		150		ns
ADR/$\overline{CS}$ low-level setup time (vs. $\overline{IORD}$ ↓)	t_{SAR}		35		ns
ADR/$\overline{CS}$ low-level hold time (vs. $\overline{IORD}$ ↑)	t_{HRA}		0		ns
Data delay time (vs. $\overline{IORD}$ ↓)	t_{DRD}			120	ns
Data float time (vs. $\overline{IORD}$ ↑)	t_{FRD}		10	100	ns
$\overline{RESET}$ low-level width	t_{RSTL}		$7t_{CYK}$		ns
V_{DD} setup time (vs. $\overline{RESET}$ ↑)	t_{SVDD}		1000		ns
$\overline{RESET}$ ↑ –1st • $\overline{IOWR}$/$\overline{IORD}$	t_{SYWR}		$2t_{CYK}$		ns
$\overline{IOWR}$/$\overline{IORD}$ recovery time	t_{RVWR}		200		ns

When bus slave



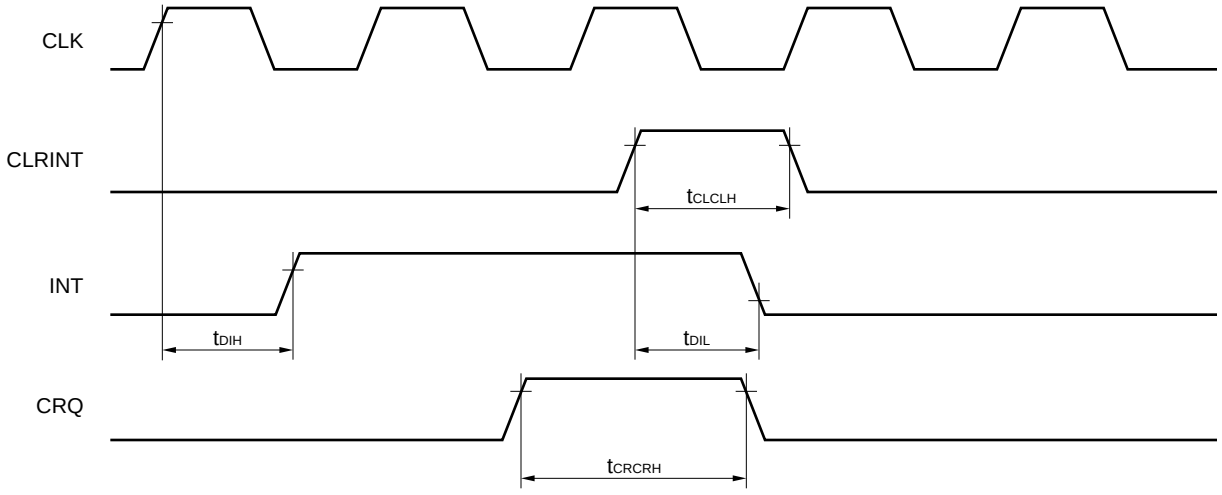
When bus slave (2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{IOWR}$/$\overline{IORD}$ high-level setup time (vs. HLDAK ↑)	t_{SWR}		–20		ns
$\overline{IOWR}$/$\overline{IORD}$ high-level hold time (vs. AEN ↓)	t_{HWR}		100		ns



When bus slave (3)

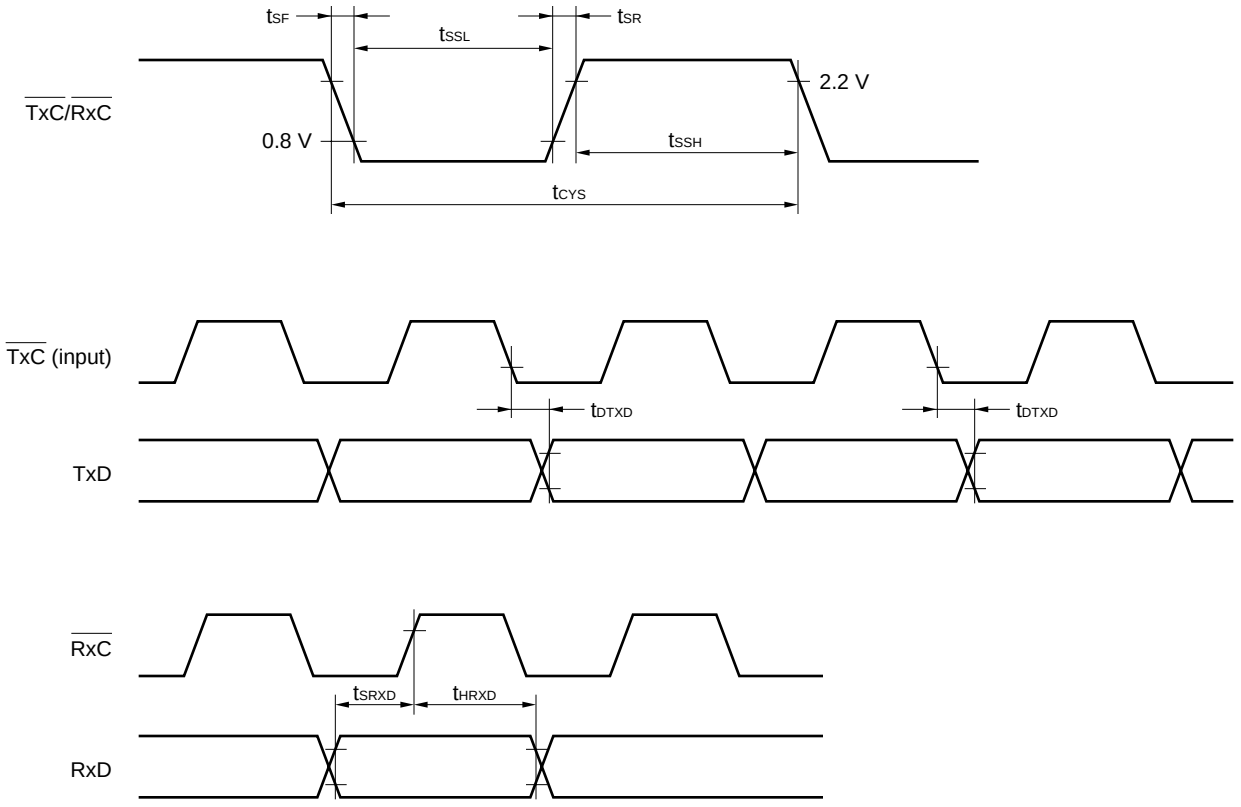
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLRINT high-level width	t_{CLCLH}		100		ns
INT ↑ delay time (vs. CLK ↑)	t_{DIH}			100	ns
INT ↓ delay time (vs. CLRINT ↑)	t_{DIL}			100	ns
CRQ high-level width	t_{CRCRH}		100		ns



Serial block (1)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{TxC}/\overline{RxC}$ cycle time	t_{CYS}	When on-chip DPLL is not used	250	DC	ns
$\overline{TxC}/\overline{RxC}$ low-level time	t_{SSL}		110		ns
$\overline{TxC}/\overline{RxC}$ high-level time	t_{SSH}		110		ns
$\overline{TxC}/\overline{RxC}$ rise time	t_{SR}			20	ns
$\overline{TxC}/\overline{RxC}$ fall time	t_{SF}			12	ns
TxD delay time (vs. $\overline{TxC}$ ↓)	t_{DTXD}			100	ns
RxD setup time (vs. $\overline{RxC}$ ↑)	t_{SRXD}		50		ns
RxD hold time (vs. $\overline{RxC}$ ↑)	t_{HRXD}		70		ns

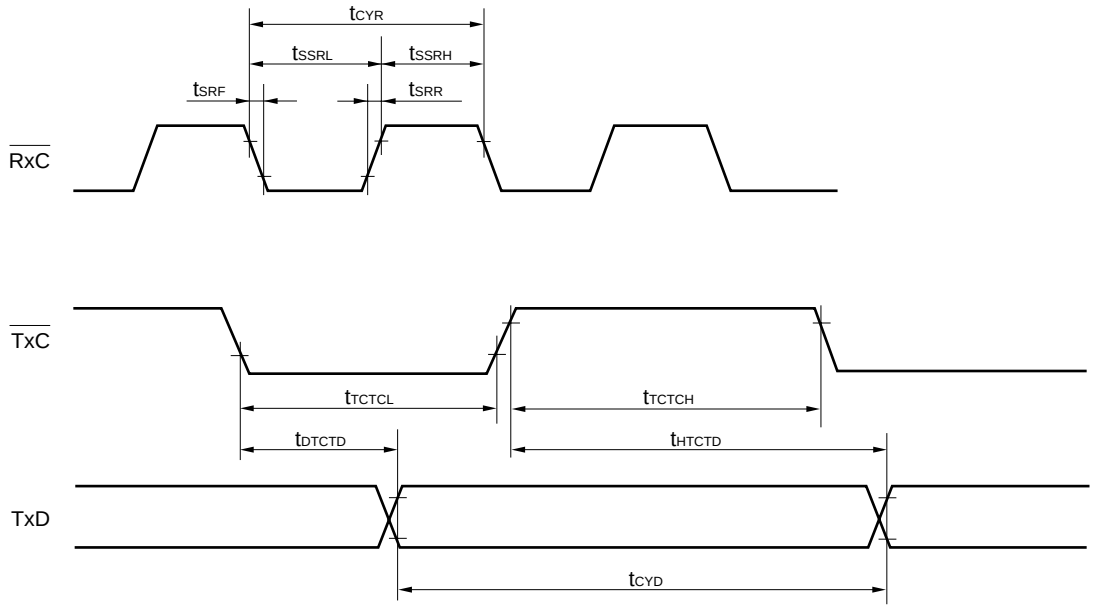
Serial clock (when on-chip DPLL is not used)



Serial block (2)

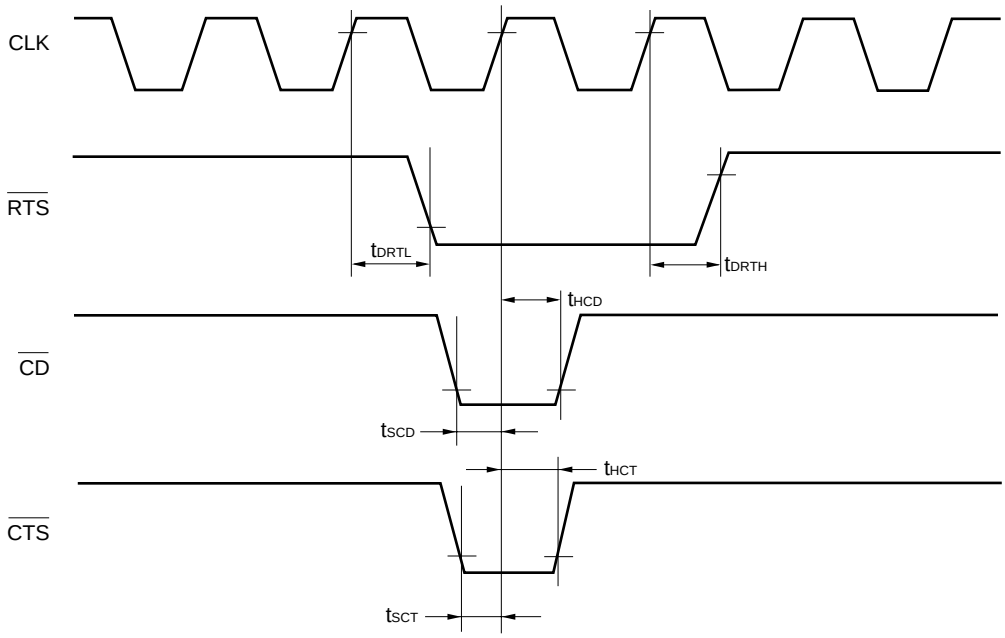
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RxC}}$ cycle time	t_{CYR}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)	30.3 125	 1000	ns
$\overline{\text{RxC}}$ low-level time	t_{SSRL}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)	10 50		ns
$\overline{\text{RxC}}$ high-level time	t_{SSRH}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)	10 50		ns
$\overline{\text{RxC}}$ rise time	t_{SRR}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)		5 10	ns
$\overline{\text{RxC}}$ fall time	t_{SRF}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)		5 10	ns
Transmit/receive data cycle	t_{CYD}	When on-chip DPLL is used (source clock = $\overline{\text{RxC}}$) When on-chip DPLL is used (source clock = CLK)	500 2000	 16000	ns
$\overline{\text{TxC}}$ low-level time	t_{TCTCL}	When on-chip DPLL is used	$0.5t_{CYD}$–25		ns
$\overline{\text{TxC}}$ high-level time	t_{TCTCH}		$0.5t_{CYD}$–25		ns
TxD delay time (vs. $\overline{\text{TxC}}$ ↓)	t_{DTCTD}			50	ns
TxD hold time (vs. $\overline{\text{TxC}}$ ↑)	t_{HTCTD}		$0.5t_{CYD}$–25		ns

Serial clock (when on-chip DPLL is used)



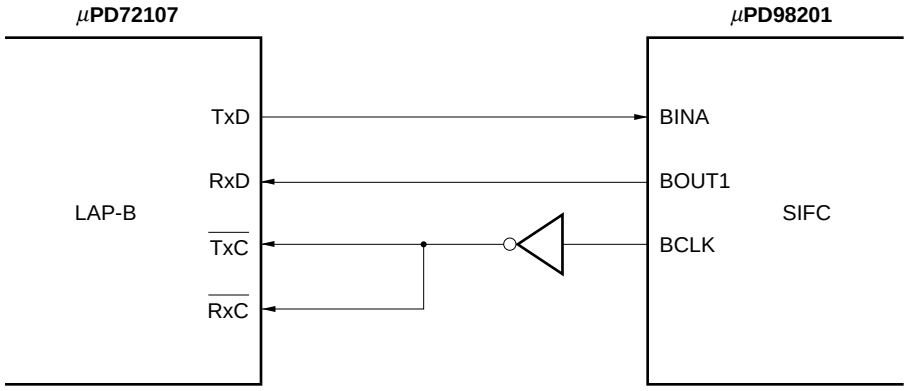
Serial block (3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{RTS}$ ↑ delay time (vs. CLK ↑)	t_{DRTH}			100	ns
$\overline{RTS}$ ↓ delay time (vs. CLK ↑)	t_{DRTL}			100	ns
$\overline{CD}$ setup time (vs. CLK ↑)	t_{SCD}		35		ns
$\overline{CD}$ hold time (vs. CLK ↑)	t_{HCD}		20		ns
$\overline{CTS}$ setup time (vs. CLK ↑)	t_{SCT}		35		ns
$\overline{CTS}$ hold time (vs. CLK ↑)	t_{HCT}		20		ns



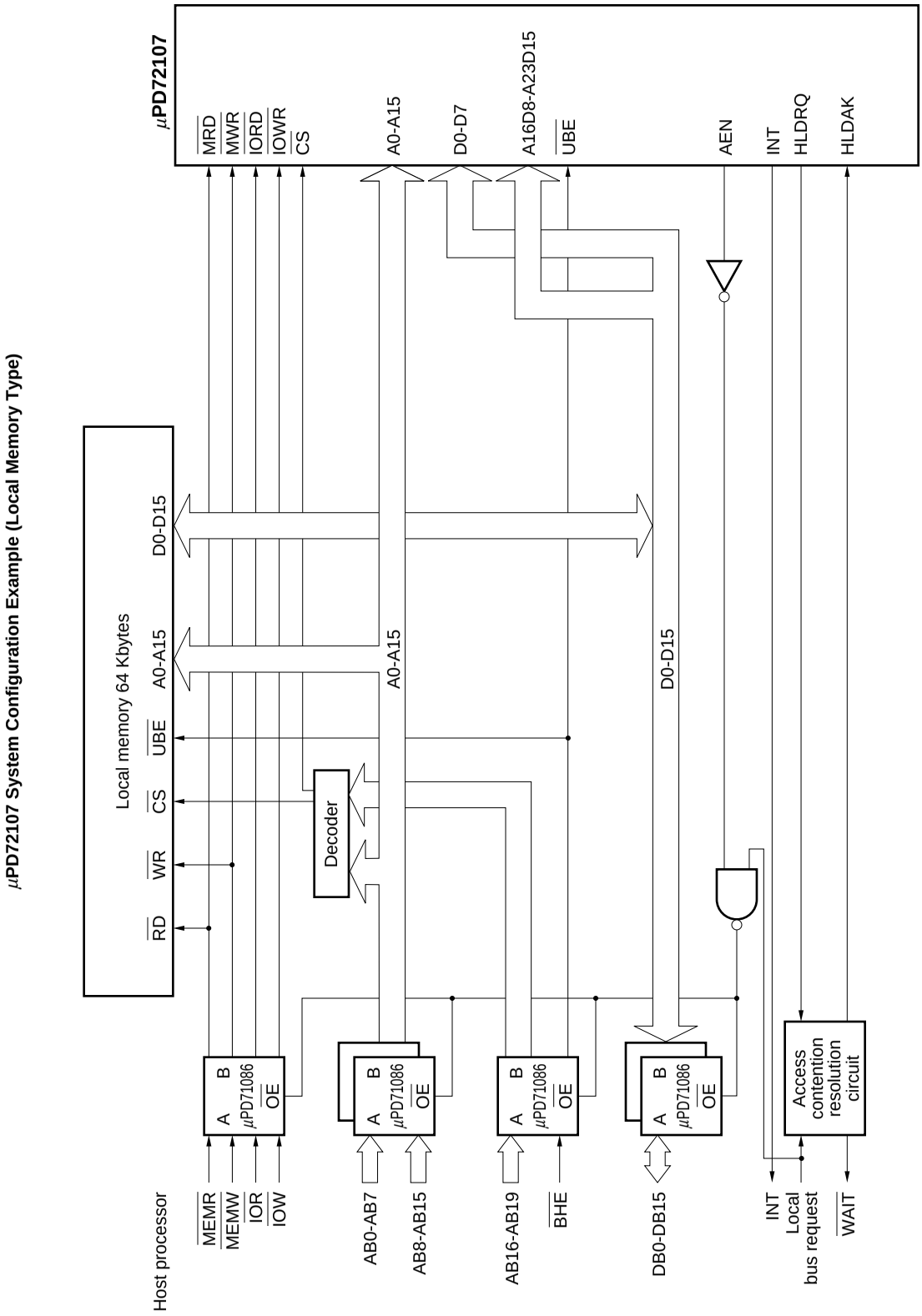
3. APPLICATION CIRCUIT EXAMPLE

(1) Connection with SIFC (μPD98201)

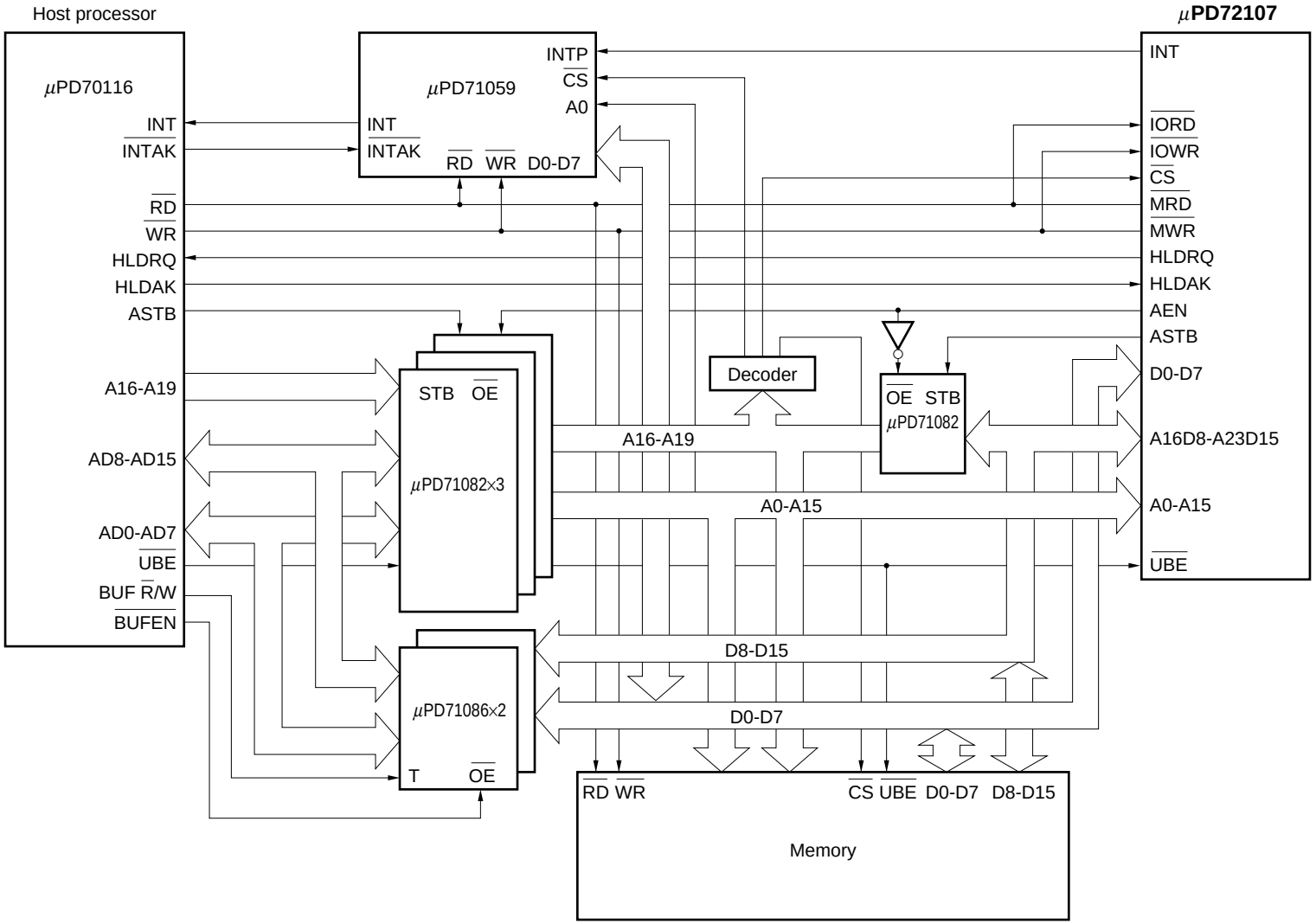


4. SYSTEM CONFIGURATION EXAMPLES

μPD72107 System Configuration Example (Local Memory Type)

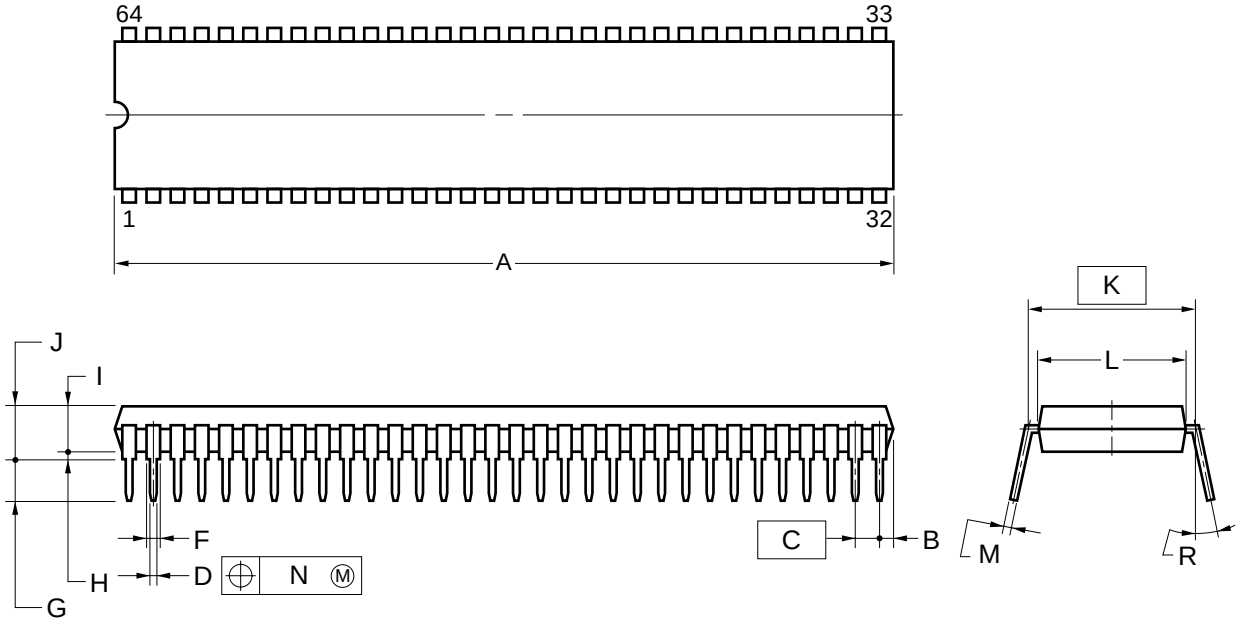


μPD72107 System Configuration Example (Main Memory Sharing Type)



5. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



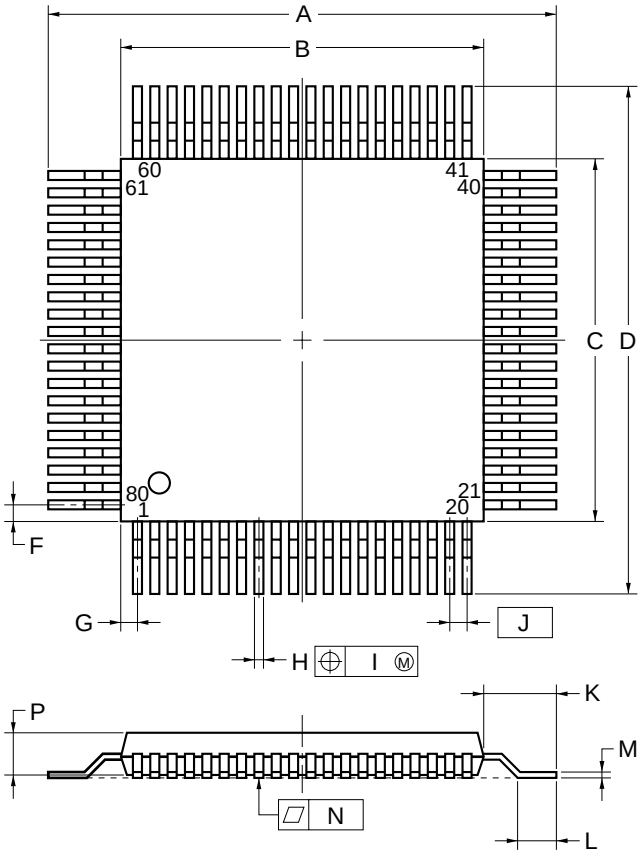
NOTES

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

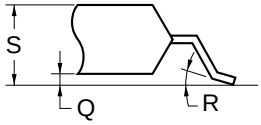
ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

P64C-70-750A,C-3

80 PIN PLASTIC QFP (14x14)



detail of lead end



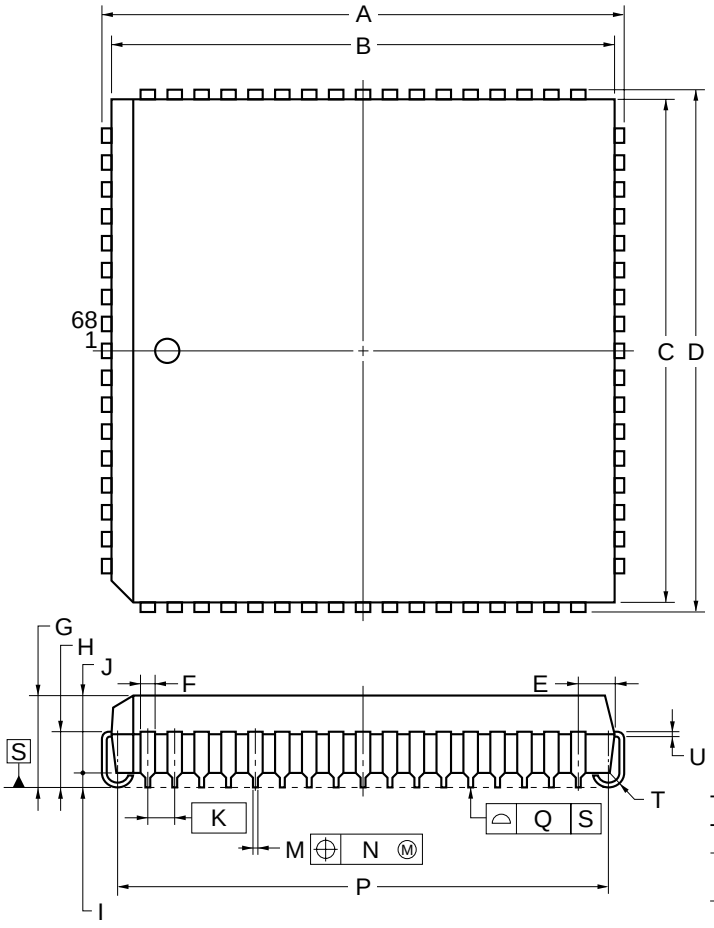
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-5

68 PIN PLASTIC QFJ (950 x 950 mil)



ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20±0.1	$0.953^{+0.004}_{-0.005}$
C	24.20±0.1	$0.953^{+0.004}_{-0.005}$
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4±0.1	$0.134^{+0.004}_{-0.005}$
K	1.27 (T.P.)	0.050 (T.P.)
M	0.42±0.08	$0.017^{+0.003}_{-0.004}$
N	0.12	0.005
P	23.12±0.2	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$

P68L-50A1-3

NOTES

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

6. RECOMMENDED SOLDERING CONDITIONS

The μPD72107 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Surface mounting type

- **μPD72107GC-3B9: 80-pin plastic QFP (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C, Time: 10 sec. Max., Count: one time, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Duration: 3 sec. Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

- **μPD72107L: 68-pin plastic QFJ (950 × 950 mils)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: one time	VP15-00-1
Partial heating	Pin temperature: 300°C Max., Duration: 3 sec. Max. (per pin row)	–

Insertion type

- **μPD72107CW: 64-pin plastic shrink DIP (750 mils)**

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C Max., Time: 10 sec. Max.
Partial heating	Pin temperature: 300°C Max., Duration: 3 sec. Max. (per a pin)

Caution Wave soldering must be applied only to pins. Be sure to avoid jet soldering the package body.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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