NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC659A

8-BIT A/D CONVERTER FOR VIDEO PROCESSING WITH REFERENCE GENERATOR AND CLAMP CIRCUIT

The μPC659A is a 8-bit A/D converter for video signal processing, the power consumption of which is lower than the μPC659. The high speed and high quality bipolar processing technology has enabled fast conversion rate and high resolution to be achieved. Conversion rate is up to 20 Msps (sampling per second) and linearity error within ±0.5 LSB while operating at low power consumption. Wide variety of application can be realized in digital application field such as digital TV system and high speed facsimile.

Also, this IC includes sample and hold circuit, clamp circuit and reference voltage generator, which enable simple external circuit to be constructed.

The μPC659A and the μPC659 are different in the number of clock pulses till transformed data is output after analog signal is captured. This should be taken into consideration when using the μPC659A instead of the μPC659. For details, refer to the timing chart.

FEATURES

- Resolution : 8-bit
- Conversion rate : 20 Msps
- Differential non-linearity : ±0.5 LSB MAX.
- Power supply : +5 V
- Analog input voltage : 1.0 V_{p-p}
- Power consumption : 215 mW TYP.
- Built-in circuit : Sample and hold circuit
  Clamp circuit (Clamp voltage and clamp pulse must be supplied.)
  Reference voltage generator (V_{RB} = 2.3 V, V_{RT} = 3.3 V TYP.)

ORDERING INFORMATION

Part Number	Package
μPC659AGS	24-pin plastic SOP (300 mil)

The information in this document is subject to change without notice.

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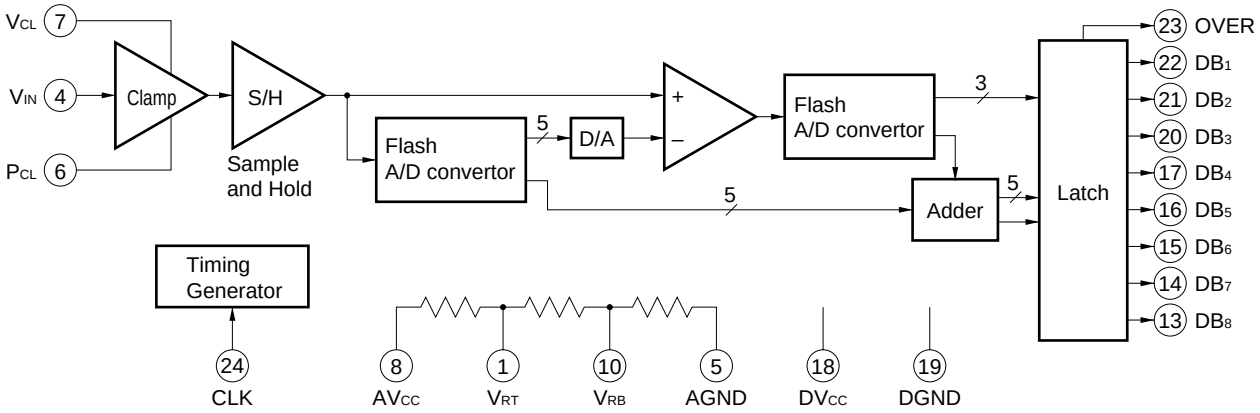
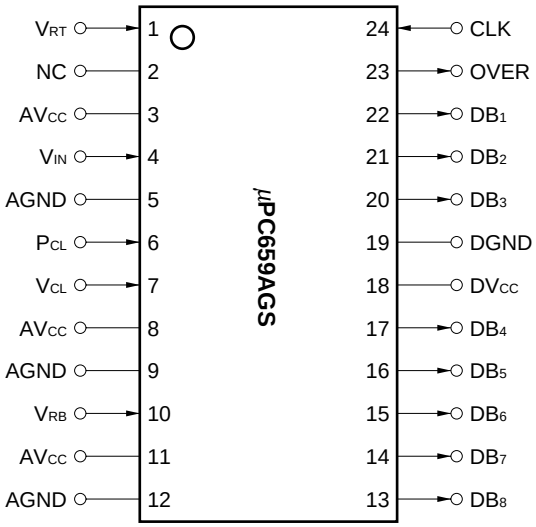
Date Published July 1997 N
Printed in Japan

The mark ★ shows major revised points.

BLOCK DIAGRAM

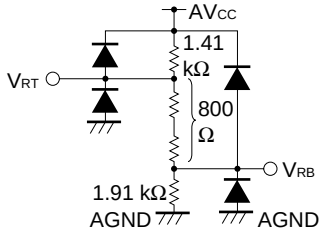
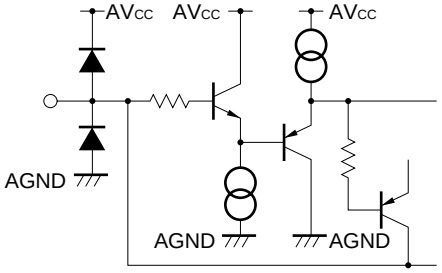
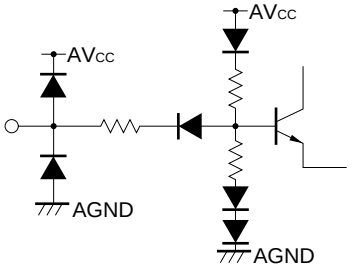
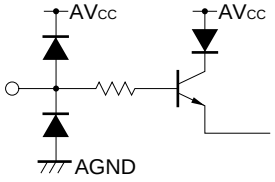
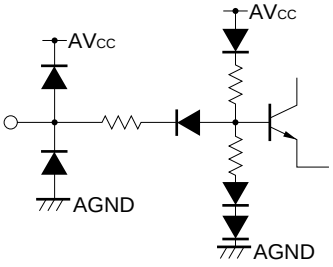


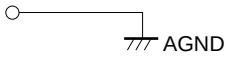
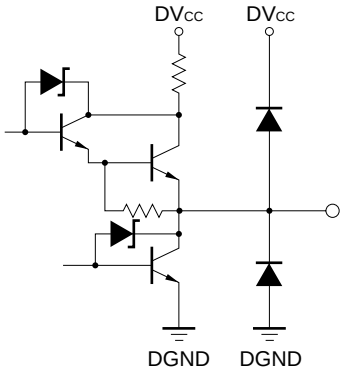
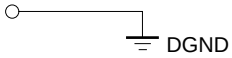
PIN CONFIGURATION (Top View)



AGND	:	Ground for Analog Circuit
AV_{CC}	:	Power Supply for Analog Circuit
CLK	:	Clock
DB_8 to DB_1	:	Digital Data Bus
DGND	:	Ground for Digital Circuit
DV_{CC}	:	Power Supply for Digital Circuit
NC	:	No Connection
OVER	:	Digital Over Range
P_{CL}	:	Clamp Pulse
V_{CL}	:	Clamp Voltage
V_{IN}	:	Analog Signal
V_{RB}	:	Reference Voltage (Bottom)
V_{RT}	:	Reference Voltage (Top)

PIN FUNCTIONS

Pin Name	Pin No.	Input/ Output	Function	Equivalent Circuit
V_{RT}	1	Input	Reference voltage (Top)	
V_{RB}	10	Input	Reference voltage (Bottom)	
V_{IN}	4	Input	Analog signal Input analog signal from this pin. The signal is read at rising edge of the clock. The clamp function also will be worked on this pin. So it's necessary to connect capacitance and low impedance signal source. The burst signal is protected at pedestal clamp because of soft clamp circuit.	
P_{CL}	6	Input	Clamp pulse Analog signal input from analog input pin is clamped to the voltage; V_{CL} according to the high level term of this pulse. During high level signal is input, analog input pin voltage is nearly clamped to voltage V_{CL}.	
V_{CL}	7	Input	Clamp voltage Set voltage at clamping analog input signal. Analog input signal is clamped nearly to this input voltage V_{CL} according to the clamp pulse P_{CL} high level period.	
CLK	24	Input	Clock Analog data acquisition and digital data out are synchronized with the rising edge of this clock.	
AV_{CC}	3, 8, 11	–	Power supply for analog circuit	

Pin Name	Pin No.	Input/ Output	Function	Equivalent Circuit
AGND	5, 9, 12	–	Ground for analog circuit	
DB_8 to DB_4 DB_3 to DB_1	13 to 17, 20 to 22	Output	Digital signal DB_8 is LSB, DB_1 is MSB.	
OVER	23	Output	Digital over range Overflow (active high).	
DV_{CC}	18	–	Power supply for digital circuit	
DGND	19	–	Ground for digital circuit	
NC	2	–	No Connection	

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	AV_{CC}, DV_{CC}	–0.3 to +6.0	V
Digital input voltage	V_{IND}	–0.3 to DV_{CC} + 0.3	V
Analog input voltage	V_{INA}	–0.3 to AV_{CC} + 0.3	V
Reference input voltage	V_{RT}, V_{RB}	–0.3 to AV_{CC} + 0.3	V
Clamp voltage	V_{CL}	–0.3 to AV_{CC} + 0.3	V
Clamp pulse input voltage	V_{PCL}	–0.3 to AV_{CC} + 0.3	V
★ Operating ambient temperature	T_A	–20 to +70	°C
Storage temperature	T_{stg}	–40 to +150	°C
Power dissipation	P_d	560	mW

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions (T_A = –20 to +70 °C)

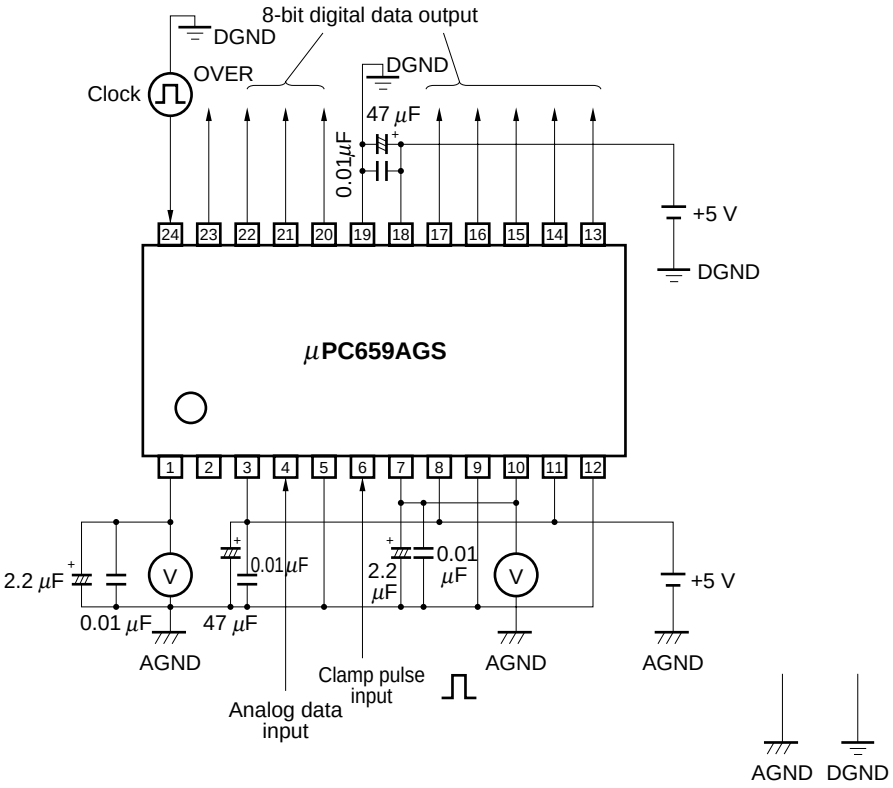
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{CC}, DV_{CC}	AGND=DGND = 0 V	4.7	5.0	5.3	V
★ Supply voltage difference	$\|AV_{CC}-DV_{CC}\|$	AGND=DGND = 0 V		0	0.1	V
Analog input voltage	V_{INA}	V_{CC} = 5.0 V	V_{RB} – 0.4		V_{RT} + 0.4	V
Clamp input voltage	V_{CL}	V_{CC} = 5.0 V	V_{RB} – 0.4		V_{RT} + 0.4	V
Sampling clock	f_{samp}		1		20	MHz
Sampling clock high level pulse width	t_{PWH}		25		500	ns
Sampling clock low level pulse width	t_{PWL}		25		500	ns
Clock input high level voltage	V_{CKH}		2.0			V
Clock input low level voltage	V_{CKL}				0.8	V
Clamp pulse width	t_{PWCL}		1.0			μs
Clamp pulse input high level voltage	V_{PCLH}		2.0			V
Clamp pulse input low level voltage	V_{PCLL}				0.8	V
Clamp capacitance	C_{CL}			10		μF
Maximum analog input frequency	f_{AIN}			8		MHz

DC Characteristics and AC Characteristics (T_A = –20 to +70 °C, AV_{CC} = DV_{CC} = 5.0 ±0.3 V)

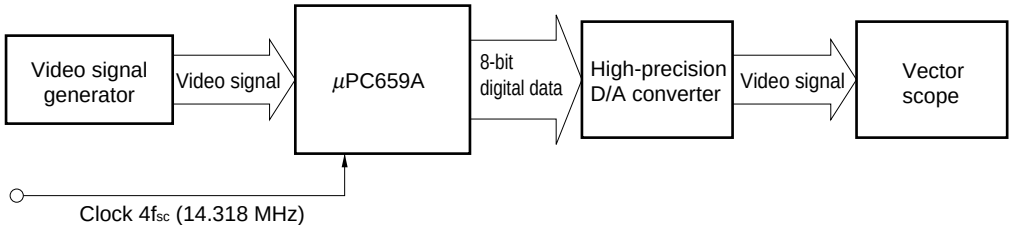
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{CC}	V_{CC} = 5.0 V, T_A = 25 °C	26	43	62	mA
Resolution	RES			8		bit
Non-linearity	NL	V_{CC} = 5.0 V, T_A = 25 °C V_{IN} = 1.0 V_{p-p}, f_{samp} = 20 MHz			±1.5	LSB
Differential non-linearity	DNL	V_{CC} = 5.0 V, T_A = 25 °C V_{IN} = 1.0 V_{p-p}, f_{samp} = 20 MHz			±0.5	LSB
Differential gain	DG	f_{samp} = 14.318 MHz NTSC ramp wave (40 IRE)		1.5	3	%
Differential phase	DP	f_{samp} = 14.318 MHz NTSC ramp wave (40 IRE)		0.8	3	deg
Digital data output delay time	t_D	Delay time from rising edge of sampling clock. DB_1 to DB_8, OVER, C_L = 15 pF	12	20	35	ns
Digital output low level voltage	V_{OL}	I_{OL} = 1.6 mA DB_1 to DB_8, OVER			0.4	V
Digital output high level voltage	V_{OH}	I_{OH} = –400 μA DB_1 to DB_8, OVER	2.7			V
Digital input low level current	I_{INDL}	V_{IN} = 0.8 V			–200	μA
Digital input high level current	I_{INDH}	V_{IN} = 2.0 V			10	μA
Analog input current	I_{INA}	Measure input current from analog input pin		10	35	μA
Reference voltage (Bottom)	V_{RB}	V_{CC} = 5.0 V	2.1	2.3	2.5	V
Reference voltage (Top)	V_{RT}	V_{CC} = 5.0 V	3.1	3.3	3.5	V
Analog input equivalent capacitance	C_{IN}	V_{IN} = V_{RB}		3		pF
Clock input equivalent capacitance	C_{CLK}			2		pF
Reference voltage (Difference)	V_{REF}	V_{RT} – V_{RB}, V_{CC} = 5.0 V		1		V

Caution The values of I_{CC} and t_D are different between the μPC659 and the μPC659A

Test Circuit

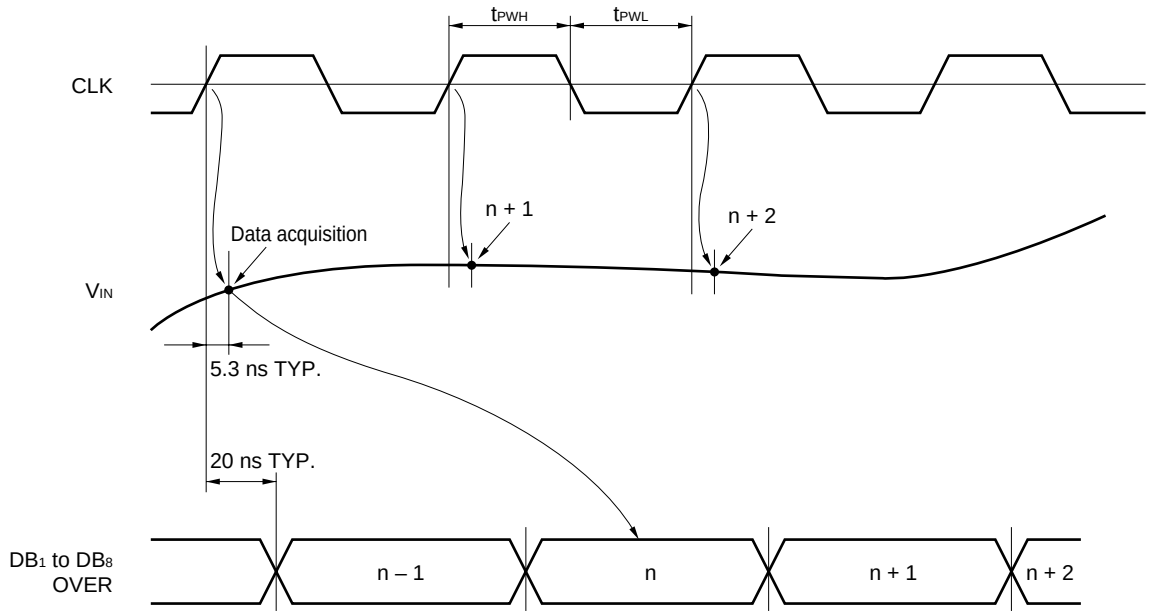


DG, DP Test Block



Remark The video signal from the video signal generator is NTSC, 40 IRE ramp signal.

Timing Chart



Analog signal is captured at the rising edge, and converted data will be output at the rising edge after 1 clock pulse[Note].

Note For the μPC659, 2 clock pulses.

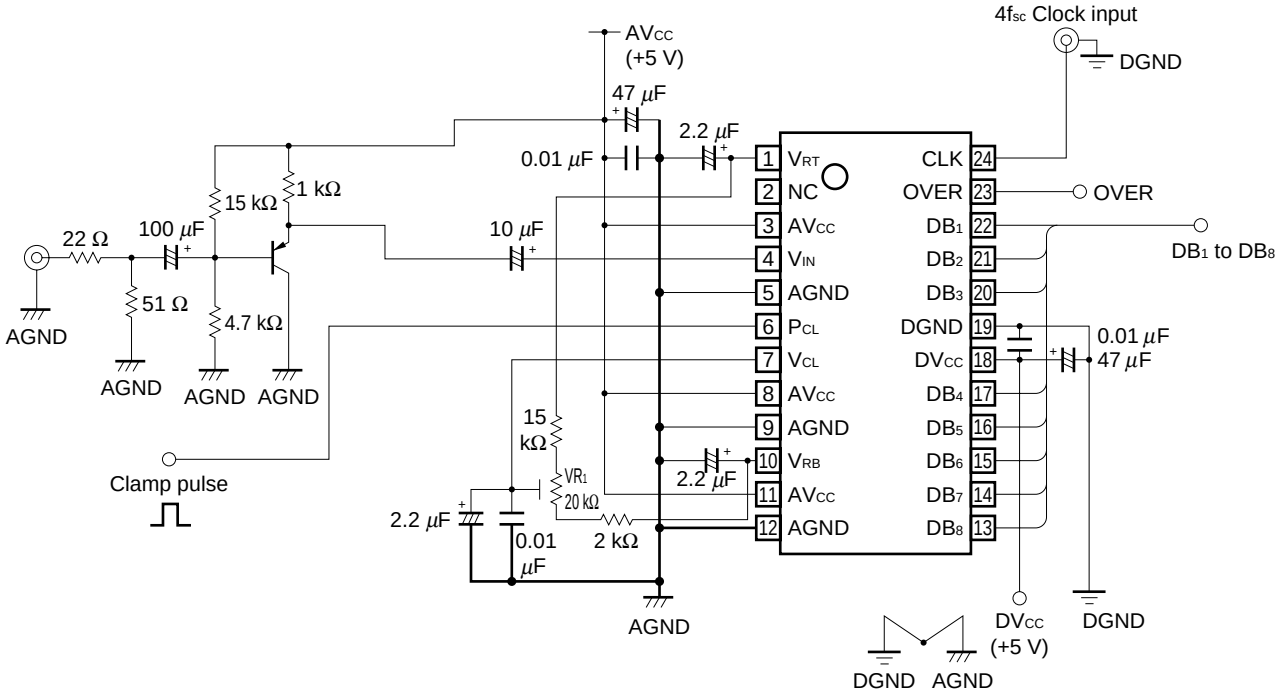
Caution The value of data output delay time (t_D) is different between the μPC659 and the μPC659A.

Output Code for Analog Input

Analog input	Output digital code								
	OVER	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)
V_{RB} to 1/2 LSB	0	0	0	0	0	0	0	0	0
1/2 LSB to (1 + 1/2) LSB	0	0	0	0	0	0	0	0	1
to	to	to	to	to	to	to	to	to	to
(254 + 1/2) LSB to (255 + 1/2) LSB	0	1	1	1	1	1	1	1	1
(255 + 1/2) LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to AV_{CC}	1	1	1	1	1	1	1	1	1

Remark $LSB \fallingdotseq \frac{V_{RT} - V_{RB}}{256} \fallingdotseq 3.906$ mV TYP., V_{RB} = 2.3 V TYP., V_{RT} = 3.3 V TYP.

APPLICATION CIRCUIT EXAMPLE



Remarks 1. VR_1: Clamp voltage adjustment

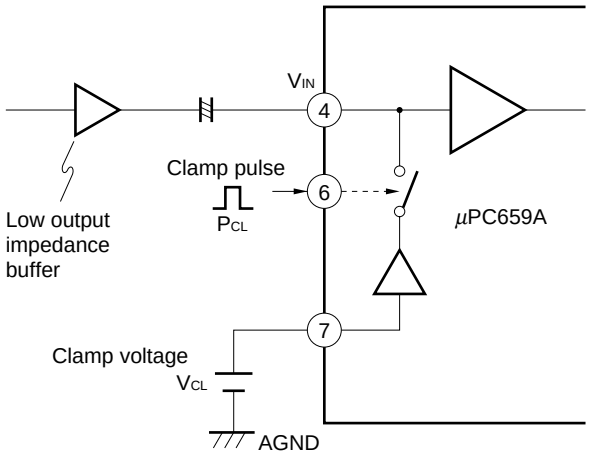
2. Must be thick line wiring for the power supply lines. And reduce the resistance and reactance ingredient.

AV_{CC} and DV_{CC} must be connected at one point.

AGND and DGND must be connected at one point.

ATTENTION FOR APPLICATION

- Converted data output
  Analog signal is captured at the rising edge, and converted data will be output at the rising edge after 1 clock pulse. For the μPC659, 2 clock pulses.
- Analog input terminal
  In case the pedestal level is clamped, the clamp circuit uses the soft clamp circuit to protect the burst level. However, if a high impedance output is connected to the V_{IN} pin (pin 4), the burst level will be reduced (for example, for an external impedance of 10 Ω, the burst level is reduced by approx. 3 %).
  Therefore, connect the lowest possible impedance signal to the analog signal input pin.



- If don's use the clamp circuit
  P_{CL} pin (pin 6) and GND must be short-circuit. And insert by-pass capacitor of about 0.1 μF between the V_{CL} pin (pin 7) and GND. Input analog signal to V_{IN} pin (pin 4).
  In case an external clamp circuit is used, connect the P_{CL} pin (pin 6) to GND, and leave the V_{CL} pin (pin 7) unconnected. Set the voltage of the V_{IN} pin (pin 4) between 2.3 V and 3.3 V.
- Clamp voltage
  There is a few difference clamp voltage between the supply clamp voltage V_{CL} (pin 7) and really clamp voltage.
  Really clamp voltage = $V_{CL} + \alpha$
  Take account of the α (about ±20 mV) at supply V_{CL} to pin 7.
- When reference voltage is set from external, V_{RB} (pin 10) = 2.3 V, V_{RT} (pin 1) = 3.3 V .
- Circuit current

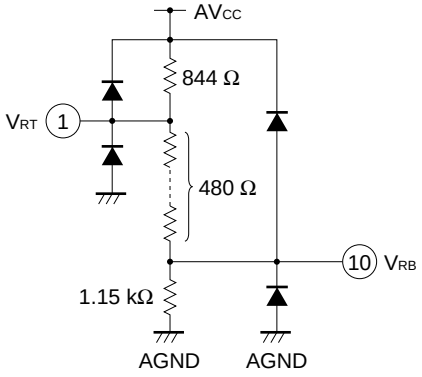
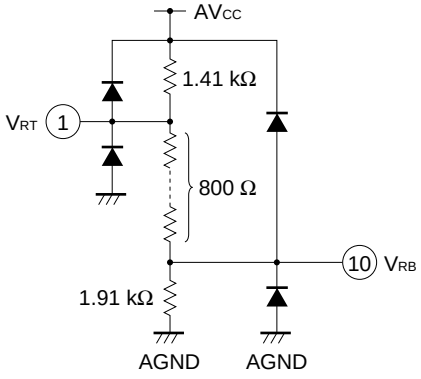
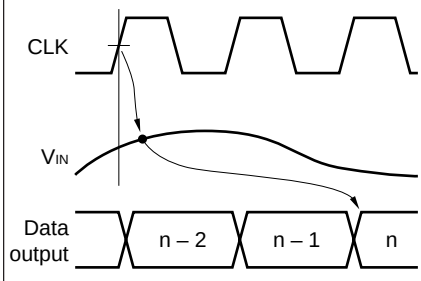
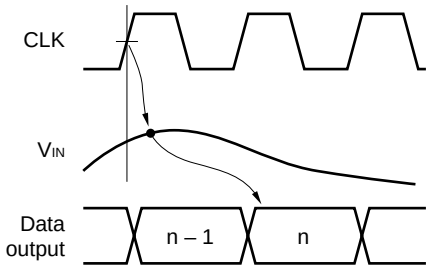
	TYP. (Unit: mA)
Analog circuit current	37
Digital circuit current	6
Sum	43

- Set the sampling clock frequency between 1 MHz and 20 MHz. If a frequency outside this range is used, the internal sample-and-hold circuit will not function properly.
- First apply 5 V to the AV_{CC} pins (pins 3 and 11) and the DV_{CC} pin (pin 18), then input the analog signal to the V_{IN} pin (pin 4). If the analog signal is input first, the output data may latch up.

DIFFERENCE BETWEEN THE μPC659 AND THE μPC659A

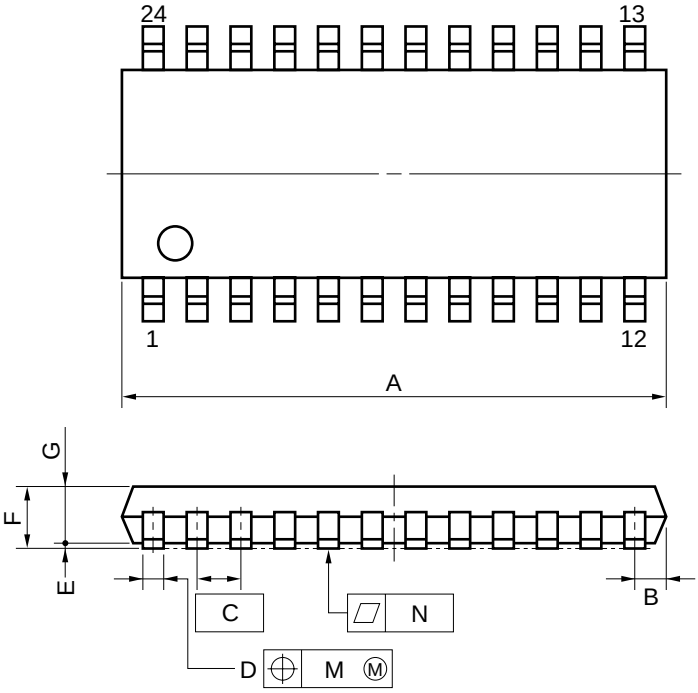
The following table shows the differences between the μPC659 and the μPC659A.

This should be taken into consideration when using the μPC659A instead of the μPC659.

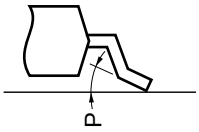
Parameter			μPC659	μPC659A
Supply current I_{CC} (V_{CC} = 5.0 V, T_A = 25 °C)		MIN.	50 mA	26 mA
		TYP.	79 mA	43 mA
		MAX.	110 mA	62 mA
Digital data output delay time t_D		TYP.	12 ns	20 ns
		MAX.	20 ns	35 ns
Internal reference resistance V_{RT} pin (pin 1), V_{RB} pin (pin 10)				
Timing chart				

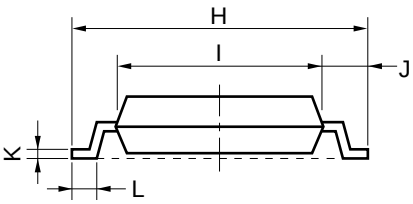
PACKAGE DRAWING

24 PIN PLASTIC SOP (300 mil)



detail of lead end





NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P24GM-50-300B-4

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface mount device

μPC659AGS : 24-pin plastic SOP (300 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 ˚C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 ˚C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
Vapor phase soldering	Peak temperature: 215 ˚C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 ˚C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Wave Soldering	Solder temperature: 260 ˚C or below, Flow time: 10 seconds or less, Pre-heating temperature: 120 ˚C or below (Package surface temperature), Maximum number of flow processes: 1 time.	WS60-00-1
Partial heating method	Pin terminal temperature: 300 ˚C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5