M66235FP

STANDARD CLOCK GENERATOR

DESCRIPTION

M66235 is produced using the silicon gate CMOS process. It is able to output clock input signal in sync with optional external trigger input signal.
It features excellent synchronizing precision (jitter) over a wide frequency band range.

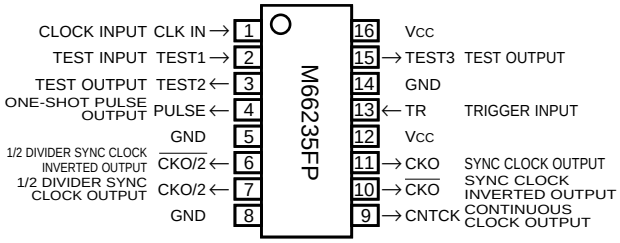
FEATURES

- 5V single power supply (5V ±5%)
- Frequency band: 25 ~ 52MHz
- Synchronizing precision (jitter): ±3ns
- Output types
  (1) Output of the same frequency as input clock, and its inversion
  (2) 1/2 divider clock output and its inversion
  (3) One-shot pulse output
  (4) Continuous clock output
- Noise in the positive direction to trigger input is removed by built-in noise killer circuit

APPLICATION

Clock phase control for horizontal synchronization

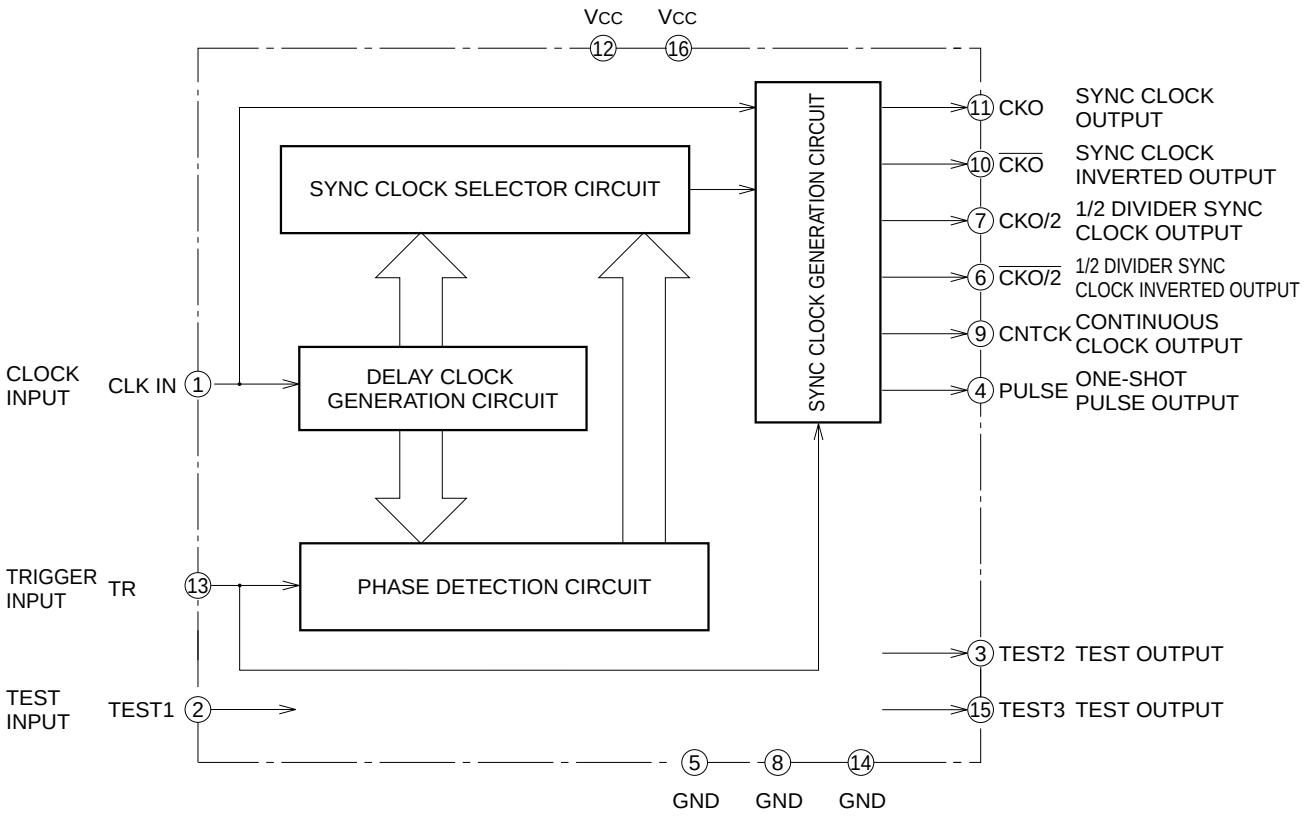
PIN CONFIGURATION (TOP VIEW)



Outline 16P2N-A

Note: Keep test pins (TEST 1 to 3) open.

BLOCK DIAGRAM



FUNCTION

M66235 standard clock generator outputs clock input signal, which is input to CLK IN, synchronously with optional trigger signal, which is input to TR.

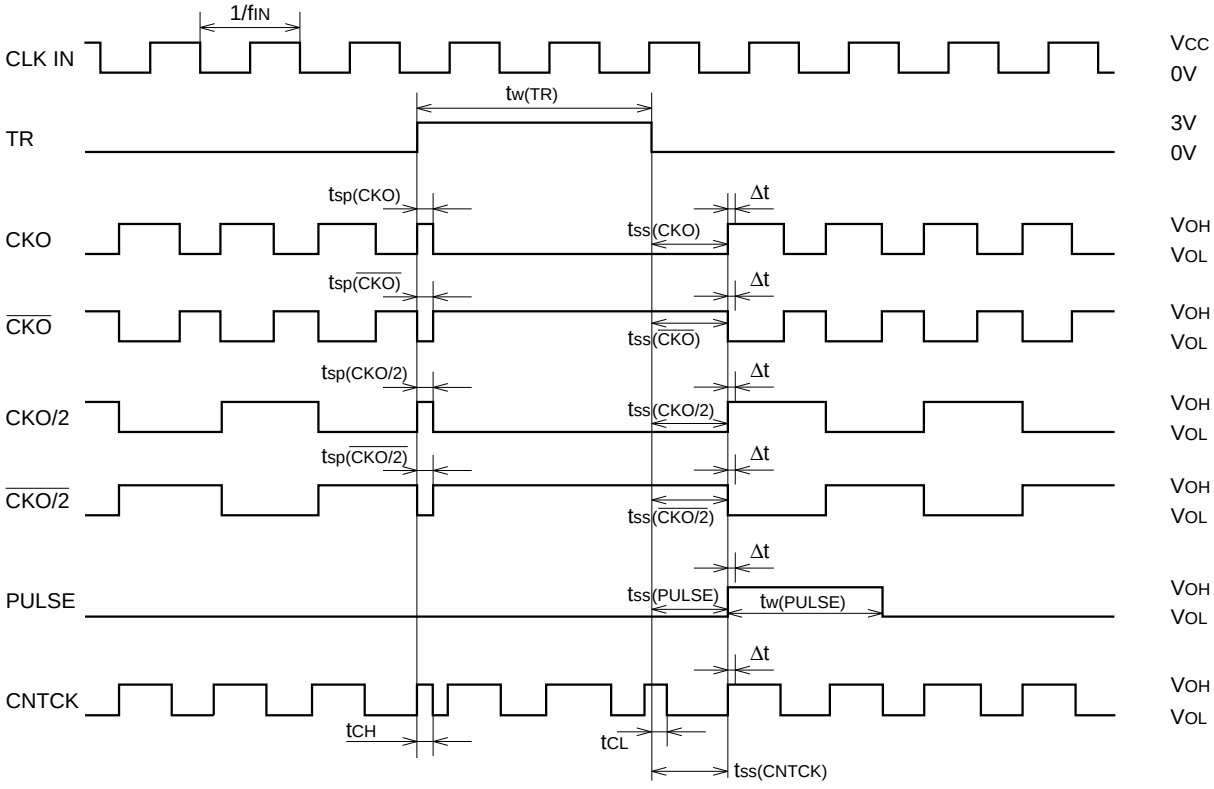
Sync clock output timing is determined by trigger input signal fall edge. Time-lag between trigger input signal fall edge and sync clock output equals the sum of clock input signal "L" pulse width and M66235 internal delay. Variation in this lag (Δt) is ± 3ns, ensuring excellent synchronizing accuracy.

There are six types of outputs: synchronous clock output (CKO), synchronous clock inverted output ($\overline{CKO}$), 1/2 divider synchronous clock output (CKO/2), 1/2 divider synchronous clock inverted output ($\overline{CKO/2}$), one-shot pulse output (PULSE) and continuous clock output (CNTCK).

From synchronous clock output (CKO), sync clock of the same frequency as clock input signal is output. From synchronous clock inverted output ($\overline{CKO}$), inverted signal of sync clock output from CKO is output. From 1/2 divider synchronous clock output (CKO/2), 1/2 divider signal of sync clock output from CKO is output. From 1/2 divider synchronous clock inverted output ($\overline{CKO/2}$), inverted signal of that output from CKO/2 is output.

From one-shot pulse output (PULSE), one-shot pulse which is almost equal to two cycles of clock input signal is output after trigger input signal falls. From continuous clock output (CNTCK), sync clock is output when trigger input signal is on "L" level; when trigger input signal is on "H" level, clock input signal, which is input to CLK IN, is output.

All these outputs but continuous clock output are suspended when trigger input signal is on "H" level: Synchronous clock output, 1/2 divider synchronous clock output and one-shot pulse output stay on "L" level, and synchronous clock inverted output and 1/2 divider synchronous clock inverted output stay on "H" level.



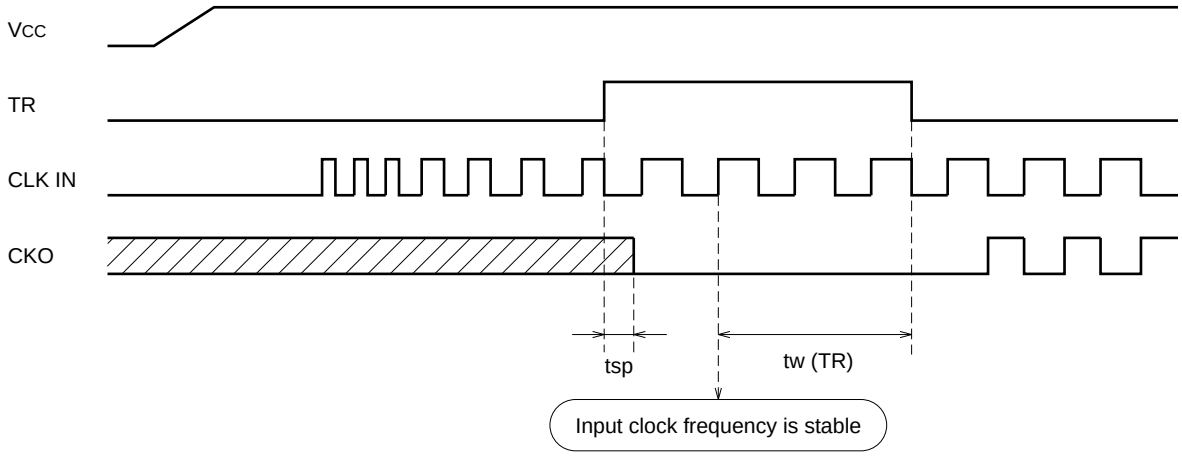
Note 1: tss (CKO, $\overline{CKO}$, CKO/2, $\overline{CKO/2}$ and PULSE) equals the sum of input clock "L" width and α . Value α refers to internal delay in M66235. Under environment where temperature and VCC do not change, value α and tss are kept constant. Dispersion of tss under such conditions is defined as Δt [synchronizing precision (jitter)].

Note 2: Outputs (CKO, $\overline{CKO}$, CKO/2, $\overline{CKO/2}$ PULSE and CNTCK) are unknown until trigger input TR reaches "H" level for the first time after power-on.

After Power-on Procedure

After power-on, M66235 status is unknown till the trigger input being set to the “H” level.
To get a accurate sync clock output, please keep a following procedure.

Please hold the trigger input “H” level during more than tw(TR) after the input clock frequency being stable.
Also, in case of changing the clock input frequency(f_{IN}), please keep the same procedure.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} +0.5	V
V_O	Output voltage		–0.5 ~ V_{CC} +0.5	V
P_d	Power dissipation	When mounted	750	mW
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage		0		V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ±5%, GND = 0V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	“H” input voltage	TR	2			V
V_{IL}	“L” input voltage				0.8	V
V_{IH}	“H” input voltage	CLK IN	0.8 × V_{CC}			V
V_{IL}	“L” input voltage				0.2 × V_{CC}	V
V_{OH}	“H” output voltage	GND = 0V, I_{OH} = –4mA	V_{CC} – 0.8			V
V_{OL}	“L” output voltage	GND = 0V, I_{OL} = 4mA			0.55	V
I_{CC} (s)	Supply current (static)	GND = 0V, V_I = V_{CC} or GND			50	µA
I_{CC} (a)	Supply current (active)	GND = 0V, f_{IN} = 52MHz, V_I = V_{CC} or GND			130	mA
I_{IH}	“H” input current	GND = 0V, V_I = V_{CC}			+1	µA
I_{IL}	“L” input current	GND = 0V, V_I = 0V			–1	µA
C_I	Input capacitance				10	pF

TIMING REQUIREMENTS (T_a = 0 ~ 70°C, V_{CC} = 5V ±5%, GND = 0V)

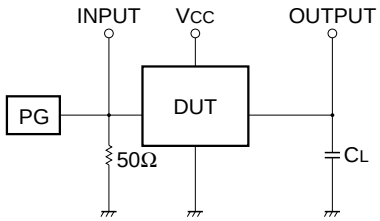
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{IN}	Clock input frequency		25		52	MHz
f_{DUTY}	Clock input duty		40		60	%
$t_{w(TR)}$	Trigger input “H” pulse width		200			ns
t_r	Clock input rise time				5	ns
t_f	Clock input fall time				5	ns

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ±5%, GND = 0V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Δt	Synchronizing precision (jitter)	C_L=15pF			±3	ns
$t_{ss(CKO)}$	Sync clock output start time				t_{Lp} + 50	ns
$t_{ss(\overline{CKO})}$	Sync clock inverted output start time					ns
$t_{ss(CKO/2)}$	1/2 divider sync clock output start time				t_{Lp} + 50	ns
$t_{ss(\overline{CKO/2})}$	1/2 divider sync clock inverted output start time					ns
$t_{ss(PULSE)}$	One-shot pulse output start time				t_{Lp} + 50	ns
$t_{ss(CNTCK)}$	Continuous clock output start time				t_{Lp} + 50	ns
$t_{sp(CKO)}$	Sync clock output stop time				40	ns
$t_{sp(\overline{CKO})}$	Sync clock inverted output stop time					ns
$t_{sp(CKO/2)}$	1/2 divider sync clock output stop time				40	ns
$t_{sp(\overline{CKO/2})}$	1/2 divider sync clock inverted output stop time					ns
$t_{w(PULSE)}$	One-shot pulse output width		2tp – 10		2tp + 10	ns
t_{CH}	Sync clock-Input clock switching time				40	ns
t_{CL}	Input clock-Sync clock switching time				30	ns
$f_{ODUTY(CKO)}$	Sync clock output duty		30		70	%
$f_{ODUTY(\overline{CKO})}$	Sync clock inverted output duty					%

- $t_p = 1/f_{IN}$, $t_{Lp} = t_p \times (100 - f_{DUTY})/100$
- Switching test waveform
  - Input pulse level CLK IN: 0 to V_{CC}
    TR: 0 to 3V
  - Input pulse rise time: 3ns
  - Input pulse fall time : 3ns
  - Criterial voltage
    - Input voltage CLK IN: V_{CC}/2
      TR: 1.3V
    - Output voltage: V_{CC}/2 for all outputs
- Capacitance: C_L includes stray wiring capacitance and probe input capacitance.

TEST CIRCUIT



TIMING DIAGRAM