NEC

MOS INTEGRATED CIRCUIT

μPD17P203A, 17P204

4-BIT SINGLE-CHIP MICROCONTROLLER WITH STATIC RAM AND 3-CHANNEL TIMER FOR INFRARED REMOTE CONTROLLER

DESCRIPTION

μPD17P203A and μPD17P204 are variations of μPD17203A and μPD17204 respectively and are equipped with a one-time PROM instead of an internal mask ROM.

μPD17P203A and μPD17P204 are suitable for evaluating a program when developing μPD17203A and μPD17204 systems respectively because the program can be written by the user.

When reading this document, also refer to the μPD17203A and μPD17204 Data Sheets.

FEATURES

- 17K architecture: General-purpose register format
- Pin-compatible (except for PROM programming function): μPD17P203A with μPD17203A
  μPD17P204 with μPD17204
- Internal one-time PROM: 4096 x 16 bits (μPD17P203A)
  7936 x 16 bits (μPD17P204)
- Static RAM: 16 Kbits (μPD17P203A)
  8 Kbits (μPD17P204)
- Power supply voltage: 2.9 to 5.5 V (at T_A = –20 to +75°C, f_X = 4MHz)
  2.0 to 5.5 V (at T_A = –20 to +75°C, f_{XT} = 32kHz)

The features of each product is shown in the following table:

Item	μPD17P203A-001 μPD17P204-001	μPD17P203A-002 μPD17P204-002	μPD17P203A-003 μPD17P204-003	μPD17203A μPD17204
Pull-up resistor of $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	On request (mask option)
Pull-up resistor of P0A and P0B pins		Provided		
Main clock oscillator circuit				
Subclock oscillator circuit		Not provided	Provided	

μPD17P203A and μPD17P204 are different from μPD17203A and μPD17204 respectively in the power supply voltage and the operating ambient temperature. Therefore, use μPD17P203A and μPD17P204 only for the system evaluation.

This document explains μPD17P204 as a typical product where no specification is made.

The information in this document is subject to change without notice.

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Date Published June 1995 P
Printed in Japan

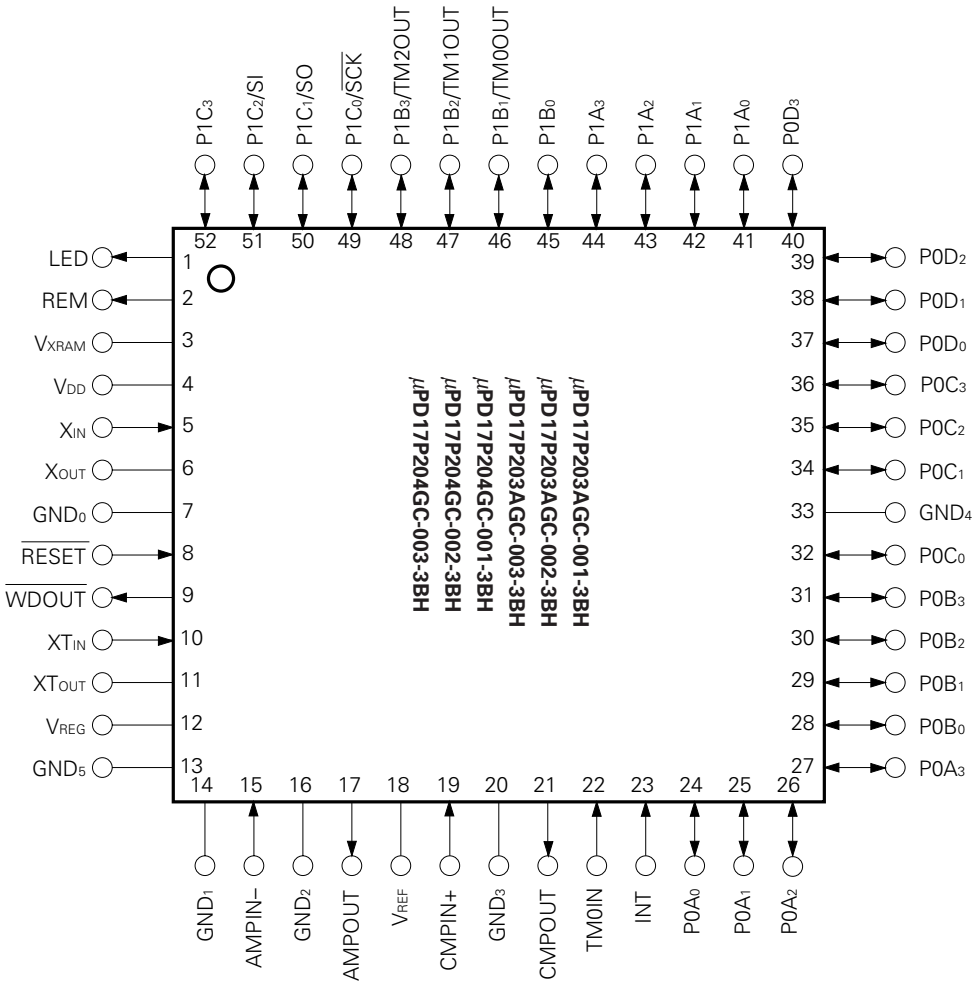
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD17P203AGC-001-3BH	52-pin plastic QFP (14 × 14 mm)
μPD17P203AGC-002-3BH	52-pin plastic QFP (14 × 14 mm)
μPD17P203AGC-003-3BH	52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-001-3BH	52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-002-3BH	52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-003-3BH	52-pin plastic QFP (14 × 14 mm)

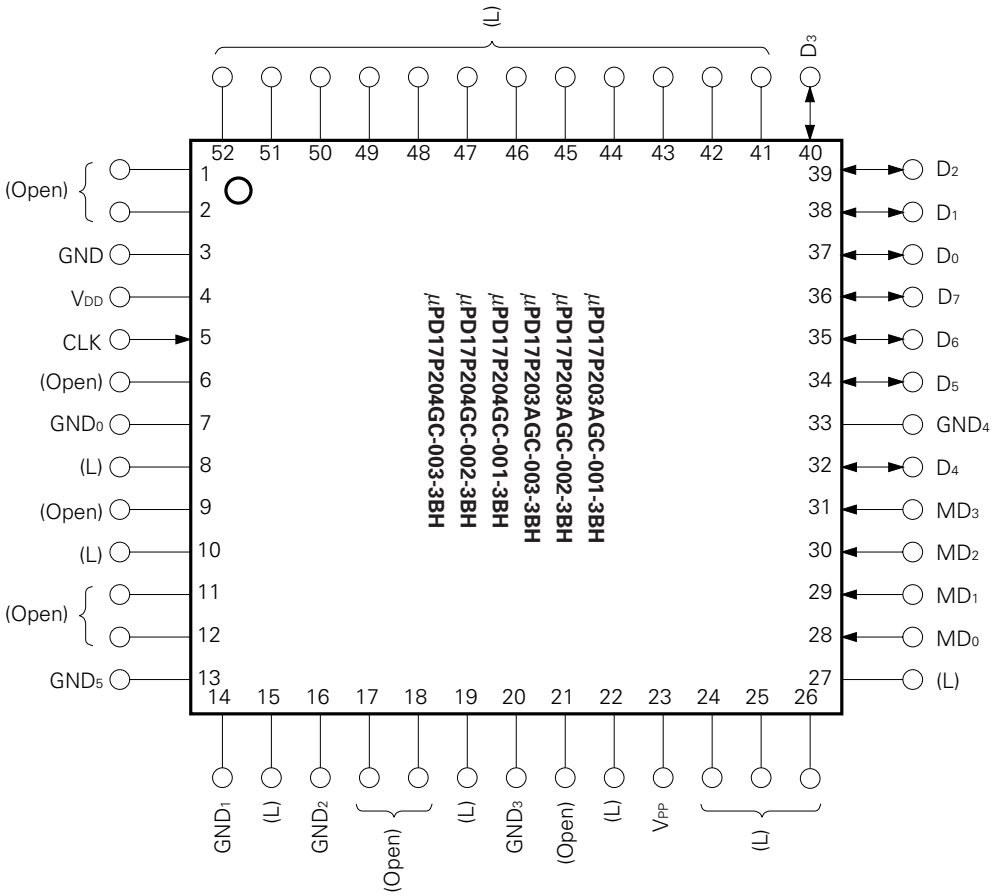
PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode



AMPIN–	:	Operational amplifier input
AMPOUT	:	Operational amplifier output
CMPIN+	:	Comparator input
CMPOUT	:	Comparator output
GND_0-GND_5	:	Ground
INT	:	External interrupt input
LED	:	Remote controller transmission output indicator
$P0A_0$-$P0A_3$	:	I/O port 0A
$P0B_0$-$P0B_3$	:	I/O port 0B
$P0C_0$-$P0C_3$	:	I/O port 0C
$P0D_0$-$P0D_3$	:	I/O port 0D
$P1A_0$-$P1A_3$	:	I/O port 1A
$P1B_0$-$P1B_3$	:	I/O port 1B
$P1C_0$-$P1C_3$	:	I/O port 1C
REM	:	Remote controller transmission output
$\overline{RESET}$	:	Reset input
$\overline{SCK}$	:	Serial clock input/output
SI	:	Serial data input
SO	:	Serial data output
TM0IN	:	Timer 0 input
TM0OUT	:	Timer 0 output
TM1OUT	:	Timer 1 output
TM2OUT	:	Timer 2 output
V_{DD}	:	Power supply
V_{REG}	:	Voltage regulator output
V_{REF}	:	Reference voltage output
V_{XRAM}	:	Static RAM (XRAM) power supply
$\overline{WDOUT}$	:	Overrun detection output
X_{IN}, X_{OUT}	:	Main clock oscillation use
XT_{IN}, XT_{OUT}	:	Subclock oscillation use

(2) PROM programming mode



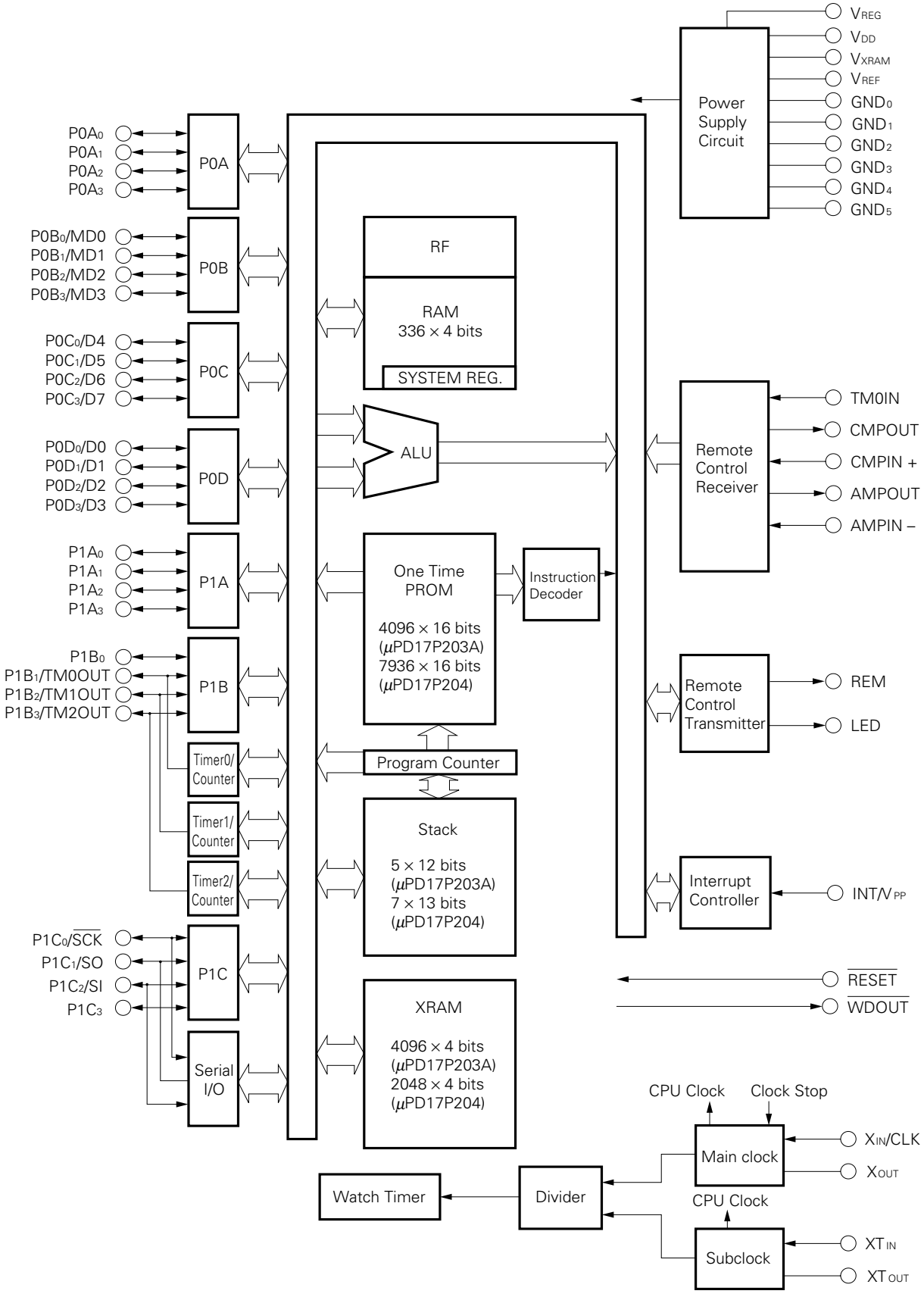
Caution Those enclosed in parentheses indicate the processing of the pins not used in PROM programming mode.

L : Ground these pins through a resistor (470Ω).

Open: Do not connect anything to these pins.

CLK	: PROM clock input	MD0-MD3	: PROM mode selection
D0-D7	: PROM data I/O	V_{DD}	: Power supply
GND, GND_0-GND_5	: Ground	V_{PP}	: Program power supply

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE

(1/2)

Pin No.	Symbol	Function	Output Format	At Reset
1	LED	Outputs NRZ signal in synchronization with infrared remote controller signal. Remains low while remote control carrier is output	CMOS push-pull	High-level output
2	REM	Outputs active-high infrared remote control signal	CMOS push-pull	Low-level output
3	V_{XRAM}	Supplies power to XRAM	–	–
4	V_{DD}	Positive power	–	–
5 6	X_{IN} X_{OUT}	Connect 4-MHz ceramic oscillator for main clock oscillation	–	(Oscillation stop)
7	GND_0	Ground	–	–
8	$\overline{RESET}$	Inputs low-active system reset signal. While this pin remains low level, oscillation of main clock stops. Pull-up resistor can also be connected by mask option (μPD17P203A-001 and μPD17P204-001 only).	–	–
9	$\overline{WDOUT}$	Outputs signal for detecting overrun. This pin outputs a low-level when an overflow in the watchdog timer or an overflow/underflow in the stack is detected. Connect this pin to the $\overline{RESET}$ pin.	N-ch open drain	High impedance ★
10 11	XT_{IN} XT_{OUT}	Connect 32-kHz crystal oscillator across these pins. When option not using subclock is selected, main clock is divided and is supplied to watch timer.	–	(Oscillation)
12	V_{REG}	Outputs signal from voltage regulator for subclock oscillator circuit. Connect external 0.1-μF capacitor.	–	–
13	GND_5	Ground	–	–
14	GND_1	Ground of operation amplifier	–	–
15	AMPIN-	Inverted input of operational amplifier	–	Input
16	GND_2	Ground of operational amplifier	–	–
17	AMPOUT	Output of operational amplifier	–	Output
18	V_{REF}	Outputs reference voltage of $1/2V_{DD}$. Connect external 0.1-μF capacitor.	–	–
19	CMPIN+	Non-inverted input of comparator. Output of this comparator can be obtained from CMPOUT.	–	Input
20	GND_3	Ground of operational amplifier	–	–

Remark GND_1-GND_3 are the ground pins of the operational amplifier.
Keep all these pins at the same potential to stabilize the operation of the operational amplifier.

(2/2)

Pin No.	Symbol	Function	Output Format	At Reset
21	CMPOUT	Comparator output. Externally connect CMPOUT and TM0IN when using microcontroller as teaching remote controller	–	Output
22	TM0IN	Clock input to timer 0. Input clock is sampled by internal clock and then input to envelope signal generator circuit, as well as to timer 0. By using timer 0 with timer 1, frequency of clock input to this pin can be measured.	–	Input
23	INT	External interrupt signal input pin	–	Input
24 to 27	$P0A_0$ to $P0A_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units. Pull-up resistor can be connected by mask option (μPD17P203A-001, -002 and μPD17P204-001, -002 only). When one or more of these pins goes low in standby mode standby mode is released.	CMOS push-pull	Input
28 to 31	$P0B_0$ to $P0B_3$			
32 34 to 36	$P0C_0$ $P0C_1$ to $P0C_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units.	N-ch open drain	Input
33	GND_4	Ground	–	–
37 to 40	$P0D_0$ to $P0D_3$	Constitute 4-bit I/O port, which can be set in input or output mode in 4-bit units.	N-ch open drain	Input
41 to 44	$P1A_0$ to $P1A_3$	Constitute 4-bit I/O port, which can be set in input or output mode in bitwise. Pull-up registor can be connected through program.	N-ch open drain	Input
45 46 47 48	$P1B_0$ $P1B_1$/TM0OUT $P1B_2$/TM1OUT $P1B_3$/TM2OUT	Port 1B or timer output • $P1B_0$-$P1B_3$ - 4-bit I/O port - Can be set in input/output mode in bitwise - Pull-up resistor can be connected through program • TM0OUT-TM2OUT - Timer output	N-ch open drain	Input ($P1B_0$-$P1B_3$)
49 50 51 52	$P1C_0$/$\overline{SCK}$ $P1C_1$/SO $P1C_2$/SI $P1C_3$	Port 1C or serial interface I/O • $P1C_0$-$P1C_3$ - 4-bit I/O port - Can be set in input/output mode in bitwise • $\overline{SCK}$, SO, SI - $\overline{SCK}$: serial clock I/O - SO : serial clock data output - SI : serial clock data input	CMOS push-pull	Input ($P1C_0$-$P1C_3$)

Caution For "A" standard products, note that standby mode is released when one or more of P0C and P0D pins goes high in standby mode.

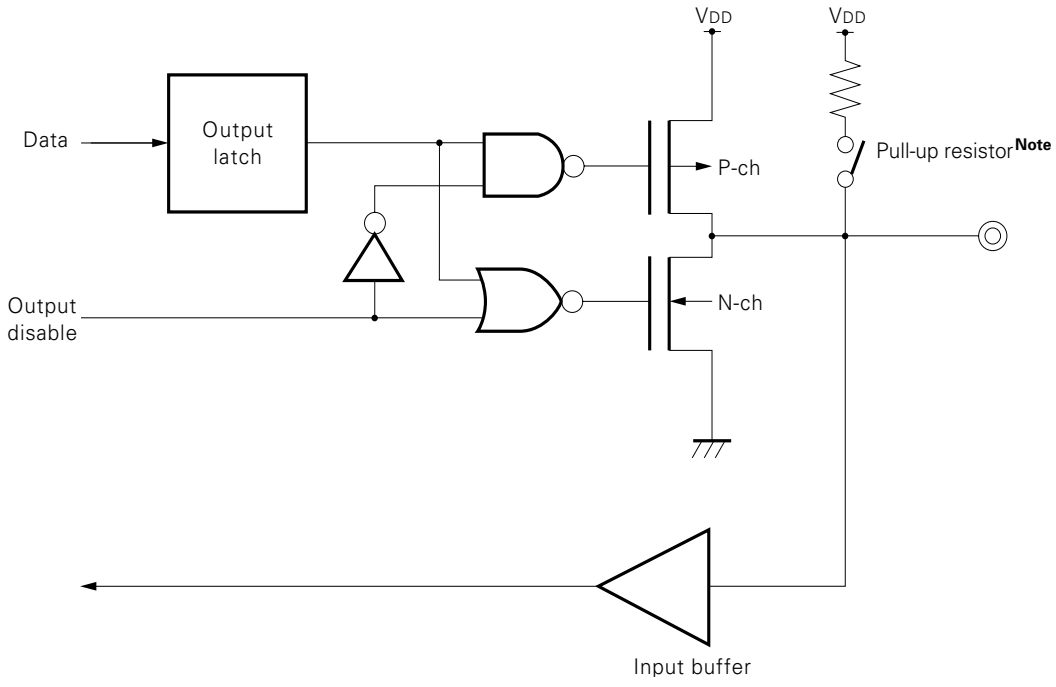
1.2 PROM PROGRAMMING MODE

Pin No.	Symbol	Function	Output Format	At Reset
3 7 13 14 16 20 33	GND GND_0 GND_5 GND_1 GND_2 GND_3 GND_4	Ground	–	–
4	V_{DD}	Positive power	–	–
5	CLK	Address updating clock input	–	Input
23	V_{PP}	Supplies program voltage. Apply 12.5V to this pin	–	–
28 to 31	MD_0 to MD_3	Selects PROM programming mode	–	Input
32, 34 to 36	D_4 to D_7	8-bit data I/O	CMOS push-pull	Input
37 to 40	D_0 to D_3			

1.3 PIN I/O CIRCUITS

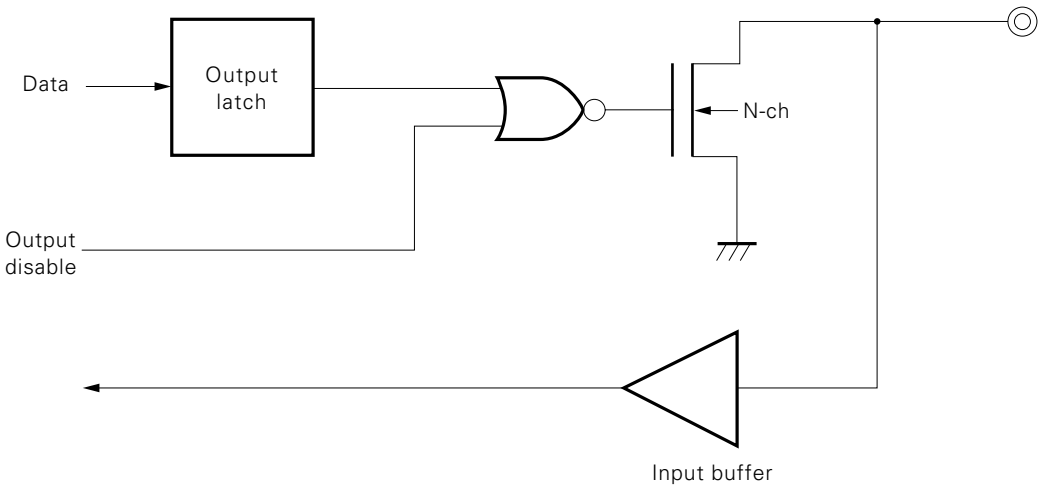
This section shows the I/O circuits of the μPD17P204 pins in simplified schematic diagrams.

(1) $P0A_0$-$P0A_3$, $P0B_0$/MD0-$P0B_3$/MD3

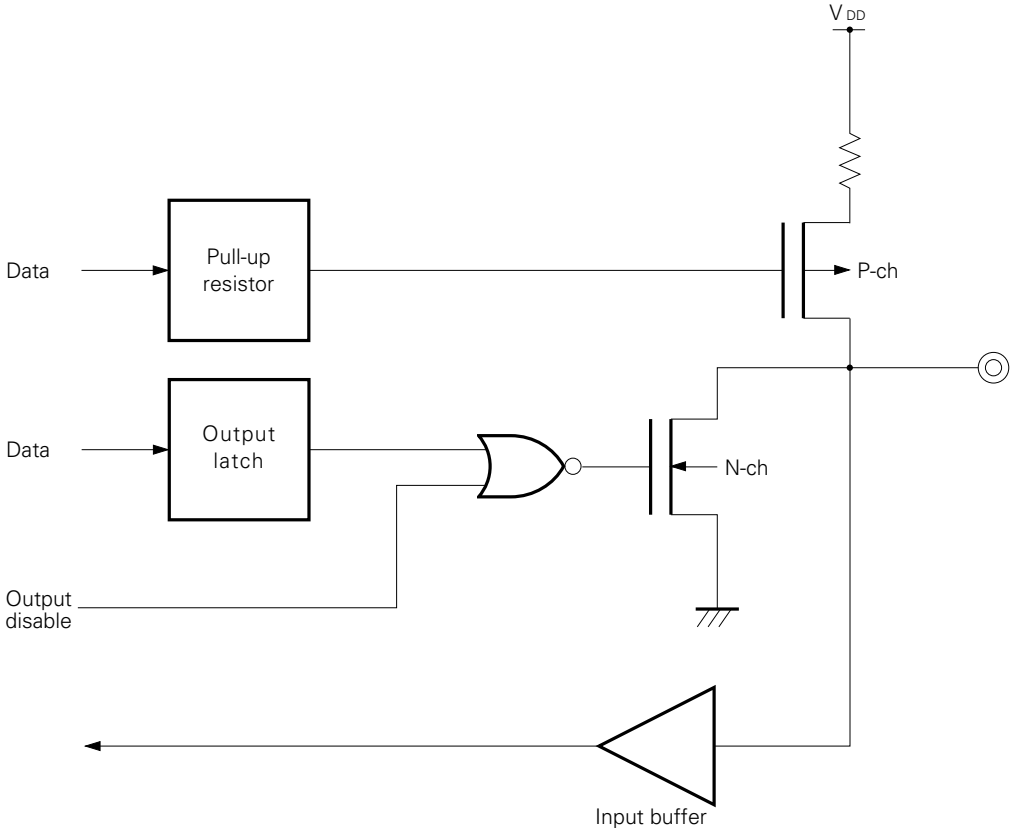


Note μPD17P203A-001, -002 and μPD17P204-001, -002 only.

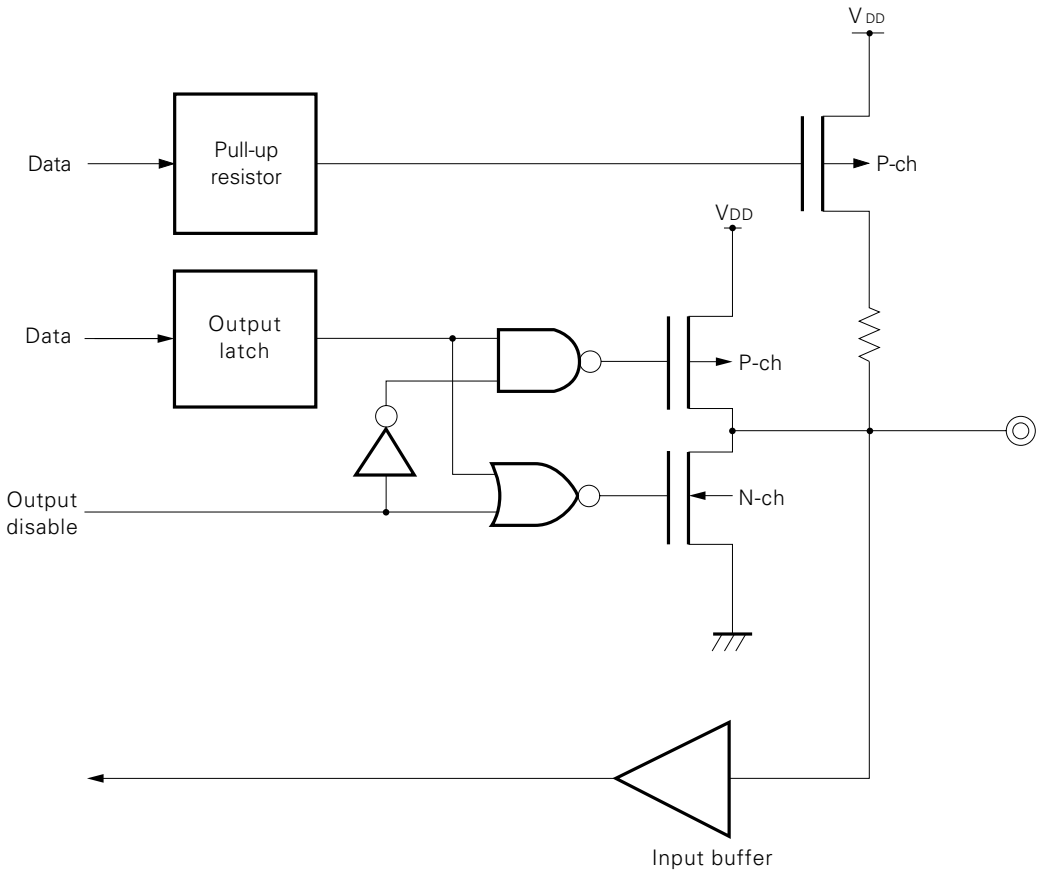
(2) $P0C_0/D4$-$P0C_3/D7$, $P0D_0/D0$-$P0D_3/D3$



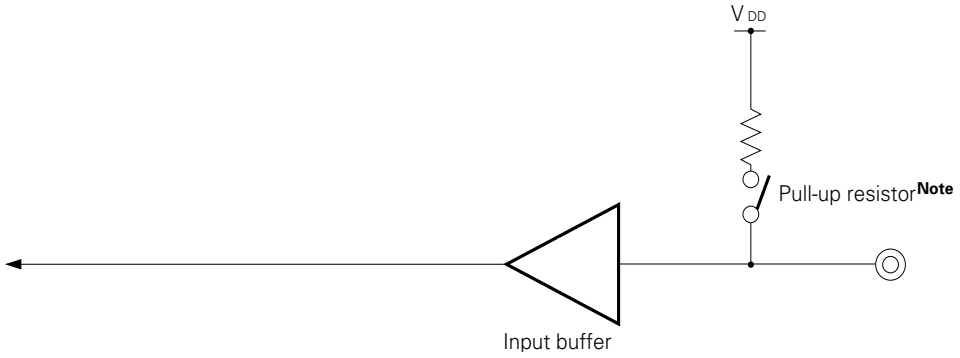
(3) $P1A_0$-$P1A_3$, $P1B_0$-$P1B_3$/TM2OUT



(4) $P1C_0/\overline{SCK}$-$P1C_3$



(5) $\overline{RESET}$



Note μPD17P203A-001 and μPD17P204-001 only

★ 1.4 PROCESSING OF UNUSED PINS

The following are recommended to process unused pins.

Table 1-1. Processing of Unused Pins

Pin	Recommended Connection
INT, TM0IN	Connect to V_{DD} or GND
$P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$	Input: Connect each pin to V_{DD} through resistor Output: Open (high-level output)
$P0C_0$-$P0C_3$, $P0D_0$-$P0D_3$ $P1A_0$-$P1A_3$, $P1B_0$-$P1B_3$	Input: Connect each pin to V_{DD} or GND through resistor Output: Open (low-level output)
$P1C_0$-$P1C_3$	Input: Connect each pin to V_{DD} or GND through resistor Ouput: Open
LED	Open
REM	Open
$\overline{WDOUT}$	Connect to GND
X_{IN}	
X_{OUT}	Connect to V_{DD}
XT_{IN}	Connect to GND
XT_{OUT}	Connect to V_{REG}
AMPIN–	Connect to GND or AMPOUT
AMPOUT, CMPOUT	Open
CMPIN+	Connect to GND
V_{REF}	Open

1.5 NOTES ON USING $\overline{\text{RESET}}$ AND INT PINS (NORMAL OPERATION MODE ONLY) ★

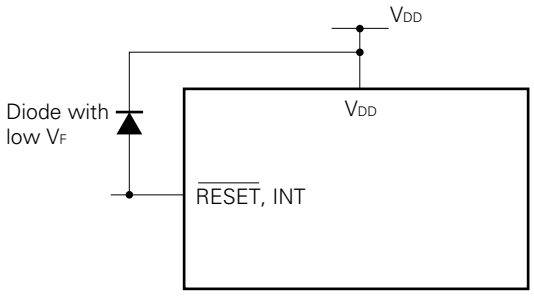
In addition to the functions shown in **1. PIN FUNCTIONS**, the $\overline{\text{RESET}}$ and INT pins also have a function to set a test mode (for IC testing) in which the internal operations of the μPD17P204 are tested.

When a voltage higher than V_{DD} is applied to either of these pins, the test mode is set. This means that, even during normal operation, the μPD17P204 may be set in the test mode if a noise exceeding V_{DD} is applied.

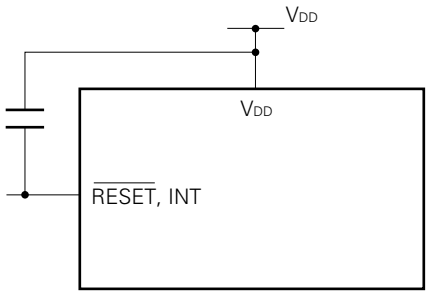
For example, if the wiring length of the $\overline{\text{RESET}}$ or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- Connect diode with low V_F between V_{DD} and $\overline{\text{RESET}}$/INT pin



- Connect capacitor between V_{DD} and $\overline{\text{RESET}}$/INT pin



2. DIFFERENCES BETWEEN MASK ROM PRODUCTS AND ONE-TIME PROM PRODUCTS

The μPD17P203A and μPD17203 are identical in the CPU functions and internal hardware peripherals except for that the μPD17P204 is provided with a PROM, which can be written by the user, in the place of the mask ROM of the μPD17204. The only differences between the two microcontrollers are therefore the program memory and mask option. The relation between the μPD17P204 and μPD17204 is the same as the relation between the μPD17P203A and μPD17203. **Note that the μPD17P203A and μPD17P204 is slightly different from the μPD17203A and μPD17204 respectively in electrical characteristics, such as supply voltage and supply current.** The following shows the differences between μPD17P203A and μPD17203A; μPD17P204 and μPD17204.

For the CPU functions and internal hardware peripherals of the μPD17203A and μPD17P204, therefore, refer to the Data Sheet of the μPD17203A and μPD17204.

<table>
<tr><th>Item \ Product</th><th>μPD17P203A-001</th><th>μPD17P203A-002</th><th>μPD17P203A-003</th><th>μPD17203A</th></tr>
<tr><td>Program memory</td><td colspan="3">• One-time PROM
• 0000H-0FFFH
• 4096x16 bits</td><td>• Mask ROM
• 0000H-0FFFH
• 4096x16 bits</td></tr>
<tr><td>Pull-up resistor of $\overline{\text{RESET}}$ pin</td><td rowspan="3">Provided</td><td>Not provided</td><td rowspan="2">Not provided</td><td rowspan="3">On request
(mask option)</td></tr>
<tr><td>Pull-up resistor of P0A and P0B pins</td><td rowspan="2">Provided</td></tr>
<tr><td>Main clock oscillator circuit</td></tr>
<tr><td>Subclock oscillator circuit</td><td>Not provided</td><td>Provided</td></tr>
<tr><td>V_{PP} pin, PROM program pins</td><td colspan="3">Provided</td><td>Not provided</td></tr>
<tr><td>Power supply voltage
(T_A = –20 to 75°C)</td><td colspan="3">V_{DD} = 2.9 to 5.5 V (at 4MHz)^{Note}</td><td>V_{DD} = 2.2 to 5.5 V
(at 4MHz)</td></tr>
<tr><td>Package</td><td colspan="4">52-pin plastic QFP</td></tr>
</table>

<table>
<tr><th>Item \ Product</th><th>μPD17P204-001</th><th>μPD17P204-002</th><th>μPD17P204-003</th><th>μPD17204</th></tr>
<tr><td>Program memory</td><td colspan="3">• One-time PROM
• 0000H-1EFFH
• 7936x16 bits</td><td>• Mask ROM
• 0000H-1EFFH
• 7936x16 bits</td></tr>
<tr><td>Pull-up resistor of $\overline{\text{RESET}}$ pin</td><td rowspan="3">Provided</td><td>Not provided</td><td rowspan="2">Not provided</td><td rowspan="3">On request
(mask option)</td></tr>
<tr><td>Pull-up resistor of P0A and P0B pins</td><td rowspan="2">Provided</td></tr>
<tr><td>Main clock oscillator circuit</td></tr>
<tr><td>Subclock oscillator circuit</td><td>Not provided</td><td>Provided</td></tr>
<tr><td>V_{PP} pin, PROM program pins</td><td colspan="3">Provided</td><td>Not provided</td></tr>
<tr><td>Power supply
(T_A = –20 to 75°C)</td><td colspan="3">V_{DD} = 2.9 to 5.5 V (at 4MHz)^{Note}</td><td>V_{DD} = 2.2 to 5.5 V
(at 4MHz)</td></tr>
<tr><td>Package</td><td colspan="4">52-pin plastic QFP</td></tr>
</table>

Note For details on the power supply voltage, refer to **4. ELECRICAL SPECIFICATIONS**.

3. ONE-TIME PROM (PROGRAM MEMORY) WRITING, READING, AND VERIFICATION

The program memory of 4096 x 16 bits (μPD17P203A) and 7936 x 16 bits (μPD17P204) one-time PROM are provided.

The following table lists the pins to be used for this PROM writing, reading or verification.

In PROM mode, no address input pin is used. Instead, the address is updated by the clock for input from the CLK pin.

Pin Name	Function
V_{PP}	Applies program voltage.
CLK	Inputs address update clock.
MD0-MD3	Selects operation mode.
D0-D7	Inputs and outputs 8-bit data.

3.1 OPERATION MODE FOR WRITING, READING, AND VERIFICATION OF PROGRAM MEMORY

If +6 V is applied to the V_{DD} and +12.5 V to the V_{PP} pin after μPD17P204 has been placed in the reset status for a fixed time (V_{DD} = 5V, $\overline{RESET}$ = 0V), μPD17P204 enters program memory write, read, or verify mode. The MD0 to MD3 pins are used to set the operation modes listed in the following table. Leave the pins not used for program memory writing, reading, or verification open or ground through pull-down resistors.

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	x	H	H	Program inhibit mode

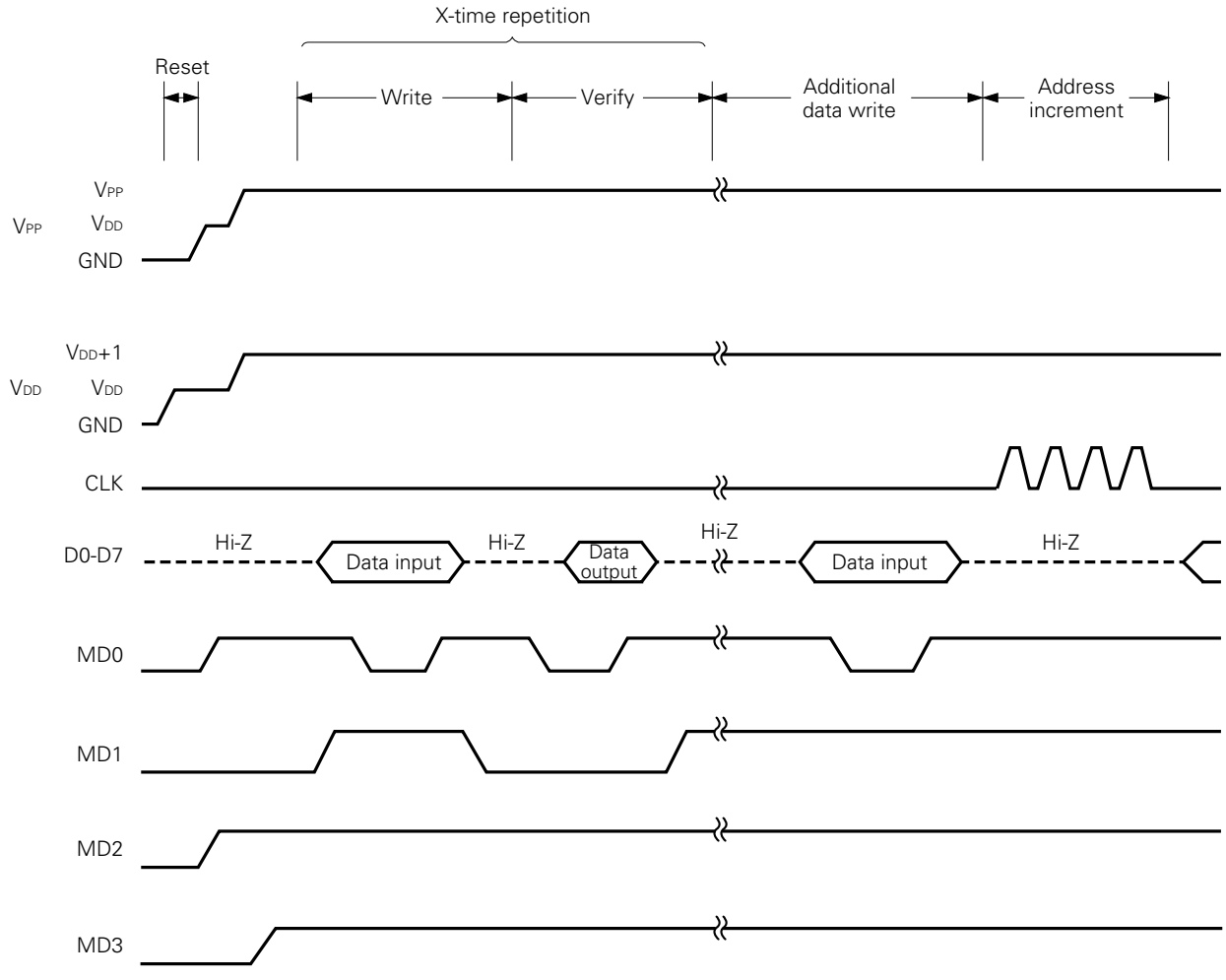
x: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 microseconds, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Write data in 1-millisecond write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (X) in steps (7) to (9)) times 1 milliseconds.
(11) Set program inhibit mode.
(12) Supply a pulse to the CLK pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power supply.

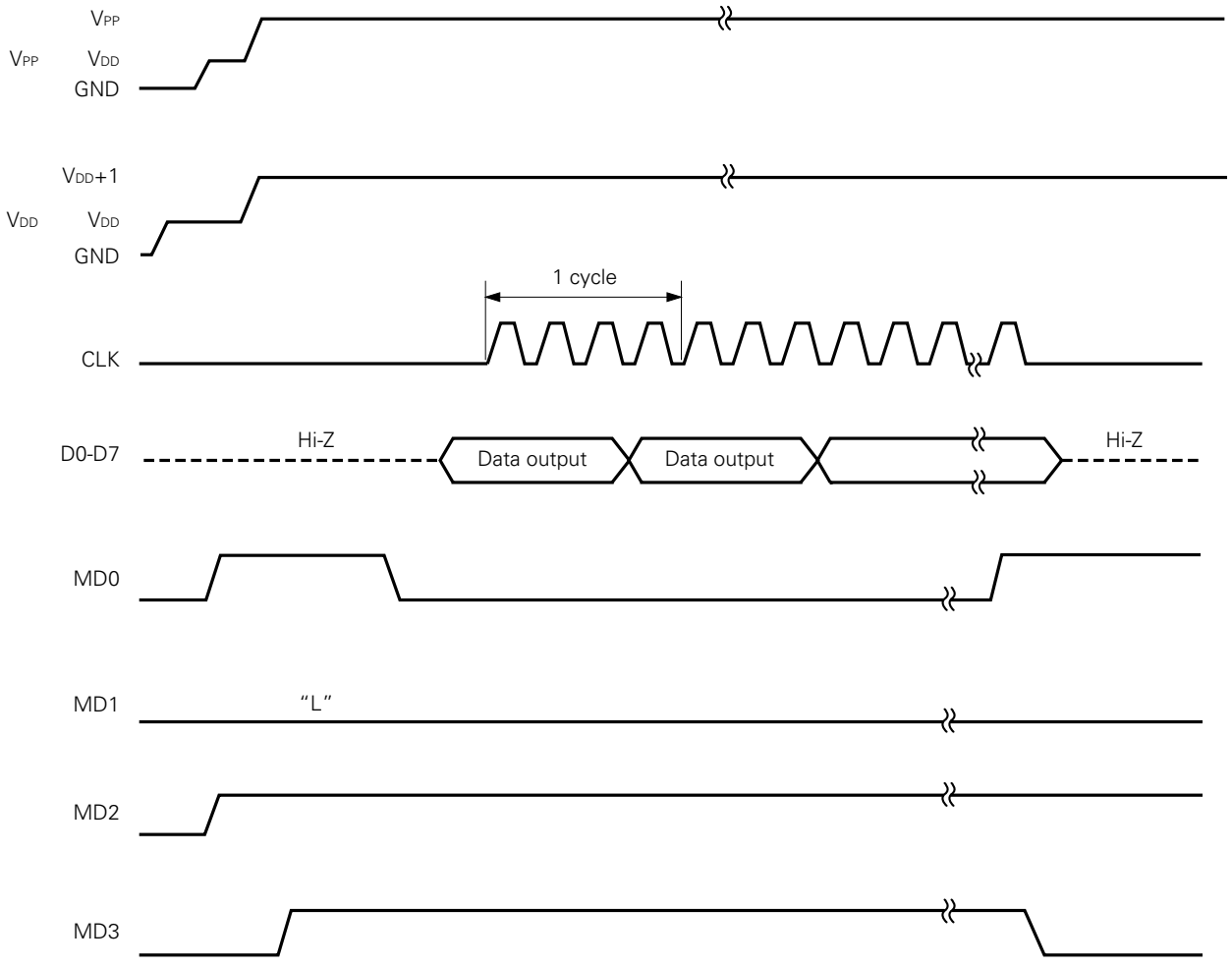
Steps (2) to (12) are illustrated below.



3.3 PROGRAM MEMORY READ PROCEDURE

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 microseconds, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the CLK pin four times.
(8) Set program inhibit mode.
(9) Set program memory address 0 clear mode.
(10) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



4. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Item	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH1}	REM pin	Peak value	–30	mA
	I_{OH2}		Effective value[Note]	–20	mA
	I_{OH3}	1 pin (except for REM pin)	Peak value	–7.5	mA
	I_{OH4}		Effective value[Note]	–5.0	mA
	I_{OH5}	Total (except for REM pin)	Peak value	–22.5	mA
	I_{OH6}		Effective value[Note]	–15.0	mA
Low-level output current	I_{OL1}	1 pin	Peak value	7.5	mA
	I_{OL2}		Effective value[Note]	5.0	mA
	I_{OL3}	Total	Peak value	30	mA
	I_{OL4}		Effective value[Note]	20	mA
Operating ambient temperature	T_A			–20 to +75	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Effective value = Peak value x $\sqrt{\text{Duty}}$

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

RECOMMENDED OPERATING RANGE (T_A = –20 to +75°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When the system clock is f_X = 4 MHz, T_A = –20 to 55°C	2.7	3.0	5.5	V
	V_{DD2}	When the system clock is f_X = 4 MHz	2.9	3.0	5.5	V
	V_{DD3}	When the system clock is f_X = 6 MHz, T_A = –20 to 50°C	4.75	5.0	5.5	V
	V_{DD4}	When the system clock is fXT = 32 kHz	2.0	3.0	5.5	V
Main clock oscillation frequency	f_X		1.0	4.0	8.0	MHz
Subclock oscillation frequency	f_{XT}			32.768		kHz

CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	INT, $\overline{\text{RESET}}$ pins			10	pF
	C_{PIN}	Other than INT, $\overline{\text{RESET}}$ pins			10	pF

DC CHARACTERISTICS

(V_{DD} = V_{XRAM} = 3 V, T_A = –20 to +75°C, f_X = 4 MHz, f_{XT} = 32 kHz)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	$\overline{RESET}$, INT pins		2.4		3.0	V
	V_{IH2}	Other than $\overline{RESET}$, INT pins		2.1		3.0	V
Low-Level Input Voltage	V_{IL1}	$\overline{RESET}$, INT pins		0		0.6	V
	V_{IL2}	Other than $\overline{RESET}$, INT pins		0		0.9	V
High-Level Input Current	I_{IH1}	INT	V_{IH} = 3 V			0.2	μA
	I_{IH2}	TM0IN	V_{IH} = 3 V			0.2	μA
	I_{IH3}	$\overline{RESET}$	V_{IH} = 3 V			0.2	μA
	I_{IH4}	P0A-P0D	V_{IH} = 3 V			0.2	μA
	I_{IH5}	P1A-P1C	V_{IH} = 3 V			0.2	μA
Low-Level Input Current	I_{IL1}	INT	V_{IL} = 0 V			–0.2	μA
	I_{IL2}	TM0IN	V_{IL} = 0 V			–0.2	μA
	I_{IL3}	$\overline{RESET}$	V_{IL} = 0 V, w/o pull-up resistors			–0.2	μA
	I_{IL4}		V_{IL} = 0 V, w/pull-up resistors	–30	–60	–120	μA
	I_{IL5}	P0A,P0B	V_{IL} = 0 V, w/o pull-up resistors			–0.2	μA
	I_{IL6}		V_{IL} = 0 V, w/pull-up resistors	–8	–15	–30	μA
	I_{IL7}	P0C,P0D	V_{IL} = 0 V			–0.2	μA
	I_{IL8}	P1A-P1C	V_{IL} = 0 V, w/o pull-up resistors			–0.2	μA
	I_{IL9}		V_{IL} = 0 V, w/pull-up resistors	–30	–60	–120	μA
High-Level Output Current	I_{OH1}	P0A,P0B	V_{OH} = 2.7 V	–0.6	–2.0	–4.0	mA
	I_{OH2}	P1C	V_{OH} = 2.7 V	–0.6	–2.0	–4.0	mA
	I_{OH3}	REM	V_{OH} = 1 V	–7.0	–15.0	–25.0	mA
	I_{OH4}	LED	V_{OH} = 2.7 V	–0.3	–1.0	–2.0	mA
	I_{OH5}	CMPOUT	V_{OH} = 2.7 V	–0.3	–1.0	–2.0	mA
Low-Level Output Current	I_{OL1}	P0A,P0B,P1C	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL2}	P0C,P0D,P1B	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL3}	P1A	V_{OL} = 0.3 V	1.5	4.5	7.5	mA
	I_{OL4}	REM	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL5}	LED,$\overline{WDOUT}$	V_{OL} = 0.3 V	0.5	1.5	2.5	mA ★
	I_{OL6}	CMPOUT	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
V_{REF} Output Voltage	V_{REF}	C = 0.1 μF, R = 82 KΩ		0.8	1.1	1.6	V
Supply Current	I_{DD1}	Operation mode	Generates both XT and X	0.5	2.0	4.0	mA
	I_{DD2}		Generates XT only		400	600	μA
	I_{DD3}	HALT mode	Generates both XT and X			2.0	mA
	I_{DD4}		Generates XT only		20	30	μA
XRAM Supply Current	I_{XRAM1}	Operation mode, V_{XRAM} = 3 V		3.0	5.0	7.0	μA
	I_{XRAM2}	HALT mode, V_{XRAM} = 3 V, T_A = 25°C			0.2	1.0	μA

XRAM LOW SUPPLY VOLTAGE DATA HOLDING CHARACTERISTICS

(T_A = –20 to +75°C, $V_{DD} \leq V_{XRAMDR}$)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Holding Voltage	V_{XRAMDR}		1.3		5.5	V

DC PROGRAMMING CHARACTERISTICS

(T_A = 25°C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.3 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than CLK	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} –0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Other than CLK	0		0.3 V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input Leakage Current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
High-Level Output Voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} Supply Current	I_{DD}				30	mA
V_{PP} Supply Current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP} and disconnect it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS

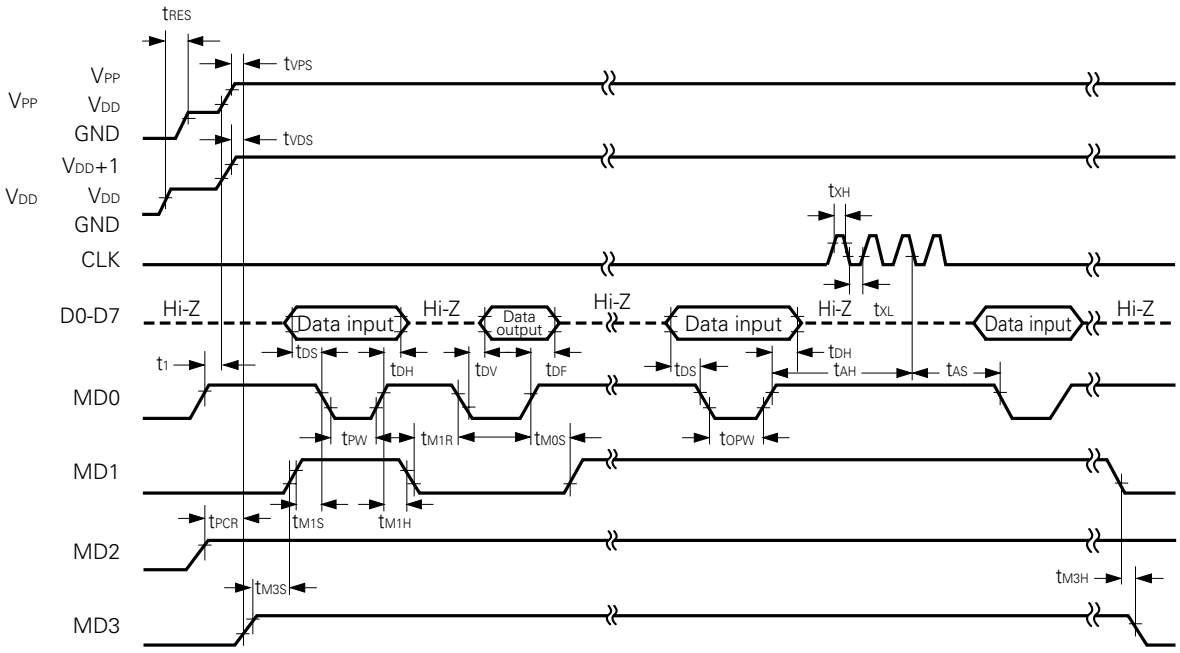
(T_A = 25°C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.3 V)

Item	Symbol	Note 1	Conditions	MIN.	TYP.	MAX.	Unit
Address Setup Time[Note 2] (vs.MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 Setup Time (vs. MD0↓)	t_{M1S}	t_{OES}		2			μs
Data Setup Time (vs. MD0↓)	t_{DS}	t_{DS}		2			μs
Address Hold Time[Note 2] (vs.MD0↑)	t_{AH}	t_{AH}		2			μs
Data Hold Time (vs. MD0↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑→ Data Output Float Delay Time	t_{DF}	t_{DF}		0		130	ns
V_{PP} Setup Time (vs. MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} Setup Time (vs. MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 Setup Time (vs. MD1↑)	t_{MOS}	t_{CES}		2			μs
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 Hold Time (vs. MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 Recovery Time (vs. MD0↓)	t_{M1R}	t_{OR}		2			μs
Program Counter Reset Time	t_{PCR}	–		10			μs
CLK Input High-/Low- Level Width	t_{XH},t_{XL}	–		0.125			μs
CLK Input Frequency	f_X	–				4.19	MHz
Initial Mode Set Time	t_I	–		2			μs
MD3 Setup Time (vs. MD1↑)	t_{M3S}	–		2			μs
MD3 Hold Time (vs. MD1↓)	t_{M3H}	–		2			μs
MD3 Setup Time (vs. MD0↓)	t_{M3SR}	–	When data is read from program memory	2			μs
Address[Note 2] → Data Output Delay Time	t_{DAD}	t_{ACC}	When data is read from program memory			2	μs
Address[Note 2] → Data Output Hold Time	t_{HAD}	t_{OH}	When data is read from program memory	0		130	ns
MD3 Hold Time (vs. MD0↑)	t_{M3HR}	–	When data is read from program memory	2			μs
MD3 ↓→ Data Output Float Delay Time	t_{DFR}	–	When data is read from program memory	2			μs
Reset Setup Time	t_{RES}			10			μs

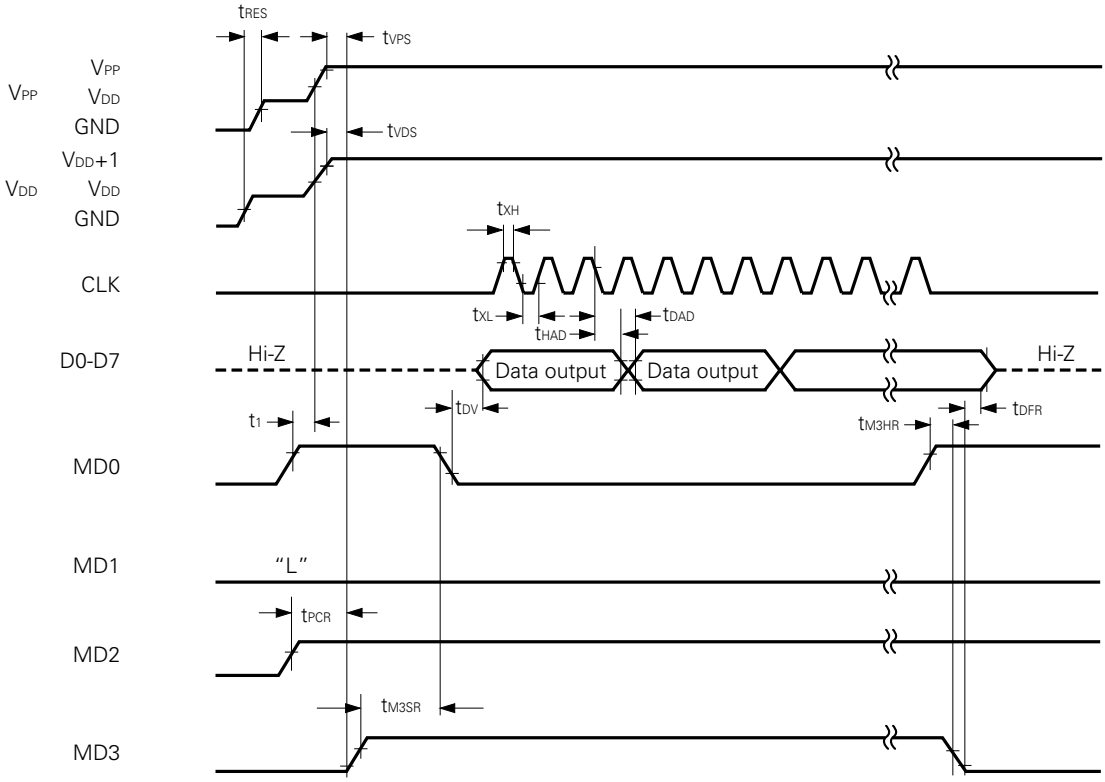
Notes **1.** These symbols are the corresponding μPD27C256 (maintenance product) symbols.

2. The internal address is incremented by 1 at the third falling edge of CLK (with four clocks constituting as one cycle). The internal address is not connected to any pin.

PROGRAM MEMORY WRITE TIMING

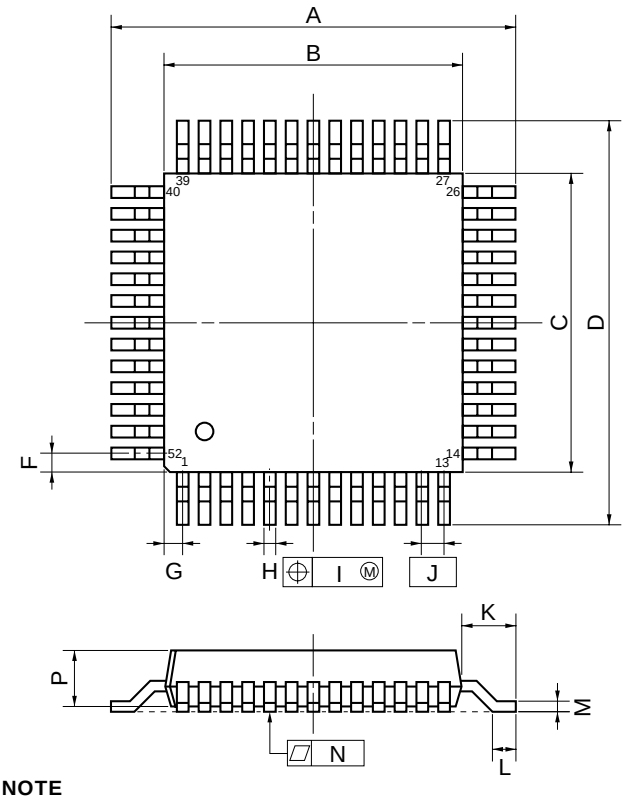


PROGRAM MEMORY READ TIMING

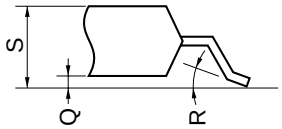


5. PACKAGE DRAWINGS ★

52 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.2	0.677±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S52GC-100-3BH-2

★ 6. RECOMMENDED SOLDERING CONDITIONS

Soldering must be performed under the following conditions.

For details of recommended conditions for surface mounting, refer to information document "Semiconductor device mounting technology manual" (IEI-1207).

For other soldering methods, please consult with NEC personnel.

Table 6-1. Soldering Conditions of Surface Mount Type

μPD17P203AGC-001-3BH : 52-pin plastic QFP (14 × 14 mm)
μPD17P203AGC-002-3BH : 52-pin plastic QFP (14 × 14 mm)
μPD17P203AGC-003-3BH : 52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-001-3BH : 52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-002-3BH : 52-pin plastic QFP (14 × 14 mm)
μPD17P204GC-003-3BH : 52-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min), Number of times: 2 max., Days: 7 days[Note] (after that, prebaking is necessary for 20 hours at 125°C) <Caution> (1) Start second reflow after device temperature (which has risen because of first reflow) has returned to room temperature. (2) Do not clean flux with water after first reflow.	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min), Number of times: 2 max., Days: 7 days[Note] (after that, prebaking is necessary for 20 hours at 125°C) <Caution> (1) Start second reflow after device temperature (which has risen because of first reflow) has returned to room temperature. (2) Do not clean flux with water after first reflow.	VP15-207-2
Pin part heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	——

Note The number of days the device can be stored after the dry pack was opened, under storage conditions of 25°C and 65% RH max.

Caution Do not use two or more soldering methods in combination (except the pin partial heating method).

APPENDIX A. MICROCONTROLLERS FOR LEARNING REMOTE CONTROLLER

Item \ Product		μPD17203A	μPD17P203A	μPD17204	μPD17P204
ROM Capacity		4096 x 16 bits (mask ROM)	4096 x 16 bits (one-time PROM)	7936 x 16 bits (mask ROM)	7936 x 16 bits (one-time PROM)
RAM Capacity		336 x 4 bits			
Static RAM Capacity		4096 x 4 bits		2048 x 4 bits	
Carrier Generator for Infrared Remote Controller		Provided			
Receiver Preamplifier for Infrared Remote Controller		Provided			
I/O Ports		28			
External Interrupt (INT)		1			
Timer		4 channels: 8-bit timer: 3 channels; Watch timer: 1 channel			
Watchdog Timer		Provided ($\overline{\text{WDOUT}}$ output)			
Serial Interface		1 channel			
Stack		5 levels (interrupt nesting: 3 levels)		7 levels (interrupt nesting: 3 levels)	
Standby Function		STOP and HALT modes			
Instruction Execution Time (supply voltage) T_A = –20 to +75°C	Main System Clock	4 μs at 4 MHz			
		(V_{DD} = 2.2 to 5.5V)	(V_{DD} = 2.9 to 5.5V[Note])	(V_{DD} = 2.2 to 5.5V)	(V_{DD} = 2.9 to 5.5V[Note])
	Sub-System Clock	488 μs at 32.768 kHz (V_{DD} = 2.0 to 5.5 V)			
Package		52-pin plastic QFP			

Note The supply voltage varies depending on the operating ambient temperature. For details, refer to **4. ELECTRICAL SPECIFICATIONS**.

★ APPENDIX B. DEVELOPMENT TOOLS

The following tools are readily available for μPD17P203A and μPD17P204 program development.

Hardware

Name	Outline
In-circuit emulators (IE-17K, IE-17K-ET[Note 1], EMU-17K[Note 2])	The IE-17K, IE-17K-ET, and EMU-17 are in-circuit emulators that can be commonly used with the 17K series products. The IE-17K and IE-17K-ET are connected to the host machine, which is a PC-9800 series product or IBM PC/AT™, via RS-232-C. The EMU-17K is inserted into an expansion slot of a PC-9800 series product. When these in-circuit emulators are used in combination with a system evaluation board (SE board) dedicated to each model of the device, they operate as the emulator dedicated to that model. A more sophisticated debugging environment can be created by using the man-machine interface software, SIMPLEHOST™. The EMU-17K has a function that allows you to check the contents of the data memory real-time.
SE board (SE-17204)	The SE-17204 is an SE board for the μPD17203A, 17P203A, 17204 and 17P204. It may be used alone to evaluated a system, or in combination with an in-circuit emulator for debugging.
Emulation Probe (EP-17203GC)	The EP-17203GC is an emulation probe for the μPD17203A, 17P203A, 17204 and 17P204. It connects an SE board and the user system. When used with the EV-9200G-52 this probe connects the SE board and the target system.
Conversion socket (EV-9200G-52[Note 3])	The EV-9200G-52 connects the EP-17203GC and the target system.
PROM programmer (AF-9703[Note 4], AF-9704[Note 4] AF-9705[Note 4], AF9706[Note 4])	The AF9703, AF9704, AF9705, and AF9706 are PROM programmers that can program the μPD17P203A and 17P204. When connected with programmer adapter AF-9808A, this PROM programmer can program the μPD17P203A and 17P204.
Program adapter (AF-9808B[Note 4])	The AF-9808A is an adapter for programming the μPD17P203AGC and 17P204GC and is used in combination with the AF-9703, AF-9704, AF-9705, and AF-9706.

Notes 1. Low-cost model: external power supply type

2. This is a product from I.C., Corp. For details, consult I.C.

3. One EV-9200G-52 is supplied with the EP-17203GC. Five EV-9200G-52s are optionally available as a set.

4. These are products from Ando Electric. For details, consult Ando Electric.

Software

Name	Outline Machine	Host	OS Media		Supply	Order Code
17K series assembler (AS17K)	AS17K is an assembler that can be used in common with the 17K series products. When developing the program of the μPD17P203A and 17P204, AS17K is used in combination with a device file (AS17203, AS17204).	PC-9800 series	MS-DOS™		5″ 2DH	μS5A10AS17K
					3.5″ 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5″ 2HC	μS7B10AS17K
					3.5″ 2HC	μS7B13AS17K
Device file (AS17203)	AS17203 is a device file for μPD17203A, and 17P203A, and it is used in combination with an assembler commonly used for the 17K series (AS17K).	PC-9800 series	MS-DOS		5″ 2HD	μS5A10AS17203
					3.5″ 2HD	μS5A13AS17203
		IBM PC/AT	PC DOS		5″ 2HC	μS7B10AS17203
					3.5″ 2HC	μS7B13AS17203
Device file (AS17204)	AS17204 is a device file for μPD17204 and 17P204, and it is used in combination with an assembler for the 17K series (AS17K).	PC-9800 series	MS-DOS		5″ 2HD	μS5A10AS17204
					3.5″ 2HD	μS5A13AS17204
		IBM PC/AT	PC DOS		5″ 2HC	μS7B10AS17204
					3.5″ 2HC	μS7B13AS17204
Support software (SIMPLEHOST)	SIMPLEHOST is a software package that enables man-machine interface on the Windows™ when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	MS-DOS	Windows	5″ 2HD	μS5A10IE17K
					3.5″ 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5″ 2HC	μS7B10IE17K
					3.5″ 2HC	μS7B13IE17K

Remark The corresponding OS versions are as follows:

OS	Version
MS-DOS	Ver. 3.30 to Ver. 5.00A[Note]
PC DOS	Ver. 3.1 to Ver. 5.0[Note]
Windows	Ver. 3.0 to Ver. 3.1

Note Ver. 5.00/5.00A of MS-DOS and Ver. 5.0 of PC DOS have a task swap function, but this function cannot be used with this software.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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