PMC-SIERRA

PM7347

S/UNI-
JET™

S/UNI®-JET

SATURN® USER NETWORK INTERFACE
for J2/E3/T3

Data Sheet

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Revision History

Issue No.	Issue Date	Details of Change
3	June 2001	Included Application examples, Description, and Functional Description, Functional Timing, Microprocessor Timing, and A.C. Timing sections. Completed Normal Mode Register and Operation sections.
		Changed all read-only "Reserved" bits to "Unused".
		Changed IDDOP values.
		Changed Thermal "Case" temperature to "Ambient", Section 11.
		Divided Pin Diagram into quadrants for readability.
2	March 2000	Preliminary label removed.
		S/UNI-JET errata added.
1	April 1999	Document created.

Table of Contents

List of Registers

List of Figures

List of Tables

1 Features

The S/UNI®-JET is a single chip Asynchronous Transfer Mode (ATM) User Network Interface (UNI) operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s that:

- Conforms to AF-Physical (PHY)-0054.000, AF-PHY-0034.000 and AF-PHY-0029.000.

- Implements ATM Direct Cell Mapping into DS1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.

- Provides a UTOPIA Level 2 compatible ATM-PHY Interface.

- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum User Network Interface Specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 and E3 transmission systems according to the ETSI 300-269 and ETSI 300-270.

- Supports Switched Multi-megabit Data Service (SMDS) and ATM mappings into various rate transmission systems as shown in Table 1:

Table 1   Supported Operating Formats

Rate	Format	Framer Only	SMDS PLCP Mapping	ATM Direct Mapping
T3 (44.736 Mbit/s)	C-bit Parity	YES	YES	YES
	M23	YES	YES	YES
E3 (34.368 Mbit/s)	G.751	YES	YES	YES
	G.832	YES	n/a	YES
J2 (6.312 Mbit/s)	G.704 & NTT	YES	n/a	YES
E1 (2.048 Mbit/s)	CRC-4	external	YES	YES
	PCM30	external	YES	YES
T1 (1.544 Mbit/s)	ESF	external	YES	YES
	SF	external	YES	YES
Arbitrary Cell Rate (up to 52 Mbit/s)		bypass	n/a	YES

- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.

- Provides on-chip DS3, E3 (G.751 and G.832), and J2 framers.

- Is configurable for sole DS3, E3, or J2 Framer use.

Note: When configured to operate as a DS3, E3, or J2 Framer, gapped transmit and receive clocks can be optionally generated for interface to devices which only need access to payload data bits.

- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s, which enables the S/UNI-JET to be used as an ATM cell delineator.

- Uses the PMC-Sierra™ PM4351 COMET, PM4341 T1XC and PM6341 E1XC T1 and E1 framer/line interface chips for DS1 and E1 applications.

- Provides programmable pseudo-random test pattern generation, detection, and analysis features.

- Provides integral transmit and receive HDLC controller with 128-byte FIFO depth.

- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.

- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.

- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

- Uses low power 3.3V CMOS technology with 5V tolerant inputs.

- Is available in a 256-pin SBGA package (27mm x 27mm).

The receiver section of the S/UNI-JET:

- Provides frame synchronization for the M23 or C-bit parity DS3 applications and alarm detection. Also:
  - ° Accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events.
  - ° Detects far end alarm channel codes.
  - ° Provides an integral HDLC receiver to terminate the path maintenance data link.

- Provides frame synchronization for the G.751 or G.832 E3 applications and alarm detection. Also:
  - ° Accumulates line code violations, framing errors, parity errors, and FEBE events.
  - ° Detects the Trail Trace in G.832, the Trail Trace is detected.
  - ° Provides an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.

- Provides frame synchronization for G.704 and NTT 6.312 Mbit/s J2 applications and alarm detection. Also:
  - ° Accumulates line code violations, framing errors, and CRC parity errors.
  - ° Provides an integral HDLC receiver to terminate the data link.

- Provides frame synchronization, cell delineation and extraction for DS3, G.751 E3, G.832 E3, and G.704 and NTT J2 ATM direct-mapped formats.

- Provides PLCP frame synchronization, path overhead extraction, and cell extraction for DS1 PLCP, DS3 PLCP, E1 PLCP, and G.751 E3 PLCP formatted streams.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the receive path with parity support, and multi-PHY (Level 2) control signals.

- Provides ATM framing using cell delineation. Note: ATM cell delineation may optionally be disabled to allow passing of all cell bytes regardless of cell delineation status.

- Provides cell descrambling, header check sequence (HCS) error detection, idle cell filtering, header descrambling (for use with PPP packets), and accumulates the number of received idle cells, the number of received cells written to the FIFO, and the number of HCS errors.

- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cell FIFOs.

- Provides a receive HDLC controller with a 128-byte FIFO to accumulate data link information.

- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.

- Provides programmable pseudo-random test-sequence detection (up to $2^{32}-1$ bit length patterns conforming to ITU-T O.151 standards) and analysis features.

The transmitter section of the S/UNI-JET:

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. Also:
  - ° Optionally inserts far end alarm channel codes.
  - ° Provides an integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. Also:
  - ° Inserts the Trail Trace for G.832
  - ° Provides an integral HDLC transmitter to insert either the Network Requirement or the General Purpose data link.

- Provides frame insertion for G.704 6.312 Mbit/s J2 applications, alarm insertion, and diagnostic features, and also an integral HDLC transmitter to insert the path maintenance data link.

- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based PLCP formats, and also alarm insertion and diagnostic features.

- Provides a 50 MHz 8-bit wide or 16-bit wide Utopia FIFO buffer in the transmit path with parity support and multi-PHY (Level 2) control signals.

- Provides optional ATM cell scrambling, header scrambling (for use with PPP packets), HCS generation/insertion, programmable idle cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

- Provides a four cell FIFO for rate decoupling between the line and a higher layer processing entity. FIFO latency may be reduced by changing the number of operational cells in the FIFO.

- Provides a transmit HDLC controller with a 128-byte FIFO.

- Provides an 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.

- Provides programmable pseudo-random test sequence generation (up to $2^{32}-1$ bit length sequences conforming to ITU-T O.151 standards). Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

The bypass and loopback features of the S/UNI-JET:

- Allow bypassing of the DS3, E3, and J2 framers to enable transmission system sublayer processing by an external device.

- Allow bypassing of the PLCP and ATM functions to enable use of the S/UNI-JET as a DS3, E3, or J2 framer.

- Provide diagnostic loopbacks, line loopbacks, and payload loopbacks.

2 Applications

- ATM or SMDS Switches, Multiplexers, and Routers

- SONET/SDH Mux E3/DS3 Tributary Interfaces

- PDH Mux J2/E3/DS3 Line Interfaces

- DS3/E3/J2 Digital Cross Connect Interfaces

- DS3/E3/J2 PPP Internet Access Interfaces

- DS3/E3/J2 Frame Relay Interfaces

- DSLAM Uplinks

3   References

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- ANSI T1.107a - 1990, "Digital Hierarchy - Supplement to Formats Specifications (DS3 Format Applications)".

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- ANSI T1.646 - 1995, "Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM".

- ATM Forum - ATM User-Network Interface Specification, V3.1, October, 1995.

- ATM Forum - "UTOPIA, An ATM PHY Interface Specification, Level 2, Version 1", June, 1995.

- ATM Forum, af-PHY-0034.000, "E3 (34,368 kbps) Physical Layer Interface", August, 1995.

- ATM Forum, af-PHY-0054.000, "DS3 Physical Layer Interface Specification", January, 1996.

- ATM Forum, af-PHY-0029.000, "6,312 Kbps UNI Specification, Version 1.0", June 1995.

- Bell Communications Research, TA-TSY-000773 - "Local Access System Generic Requirements, Objectives, and Interface in Support of Switched Multi-megabit Data Service" Issue 2, March 1990 and Supplement 1, December 1990.

- ETS 300 269 Draft Standard T/NA(91)17 - "Metropolitan Area Network Physical Layer Convergence Procedure for 2.048 Mbit/s", April 1994.

- ETS 300 270 Draft Standard T/NA(91)18 - "Metropolitan Area Network Physical Layer Convergence Procedure for 34.368 Mbit/s", April 1994.

- ITU-T Recommendation O.151 - "Error Performance Measuring Equipment Operating at the Primary Rate and Above", October, 1992.

- ITU-T Recommendation I.432 - "B-ISDN User-Network Interface - Physical Layer Specification", 1993

- ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

- ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.

- ITU-T Recommendation G.751 - CCITT Blue Book Fasc. III.4, "Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order Bit Rate of 139,264 kbit/s and Using Positive Justification", 1988.

- ITU-T Draft Recommendation G.775 - "Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria", October 1993.

- ITU-T Recommendation G.804 - "ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)", 1993.

- ITU-T Recommendation G.832 - "Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures", 1993.

- ITU-T Recommendation Q.921 - "ISDN User-Network Interface - Data Link Layer Specification", March, 1993.

- NTT Technical Reference, "NTT Technical Reference for High-Speed Digital Leased Circuit Services", 1991.

4 Definitions

The following table defines the abbreviations for the S/UNI-JET.

AIC	Application Identification Channel
AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
BIP	Bit Interleaved Parity
CMOS	Complementary Metal Oxide Semiconductor
COFA	Change of Frame Alignment
CPERR	Path Parity Error
CRC	Cyclic Redundancy Check
DSLAM	DSL Access Multiplexer
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
EXZS	Excess Zeros
F-bit	Framing Bit
FAS	Framing Alignment Signal
FEAC	Far-End Alarm Control
FEBE	Far-End Block Error
FERF	Far End Receive Failure
FERR	Framing Bit Error
FIFO	First-In First-Out
HCS	Header Check Sequence
HDLC	High-level Data Link Control
ISDN	Integrated Services Digital network
ITU	International Telecommunications Union
JTAG	Joint Test Action Group
LCD	Loss of Cell Delineation
LCV	Line Code Violation
LOF	Loss of Frame
LOS	Loss of Signal
NRZ	Non Return to Zero
OOF	Out of Frame
PERR	Parity Error
PHY	Physical Layer
PLCP	Physical Layer Convergence Procedure
PMDL	Path Maintenance Data Link
PMON	Performance Monitor
POS	Packet Over SONET
PPP	Point-to-Point Protocol

RAI	Receive Alarm Indication
RBOC	Bit Oriented Code Detector
RDLC	Data Link Receiver
RED	Receive Error Detection
SBGA	Super Ball Grid Array
SCI-PHY^{TM}	SATURN® Compatible Interface Specification for PHY and ATM layer devices
SMDS	Switched Multi-Megabit Data Service
SONET	Synchronous Optical Network
TAP	Test Access Port
TSB	Telecom System Block
TTB	Trail Trace Buffer

5   Application Examples

The S/UNI-JET is configurable as:

- An ATM device

- A J2/E3/T3 framer

- A cell processor

As an ATM-PHY layer device, the S/UNI-JET connects on the line side to one J2/E3/T3 line interface unit and on the system side, it interfaces with an ATM layer device, such as the PM7322 RCMP-800, over an 8- or 16-bit wide UTOPIA Level 2 interface. Refer to Figure 1.

Figure 1   S/UNI-JET Operating as an ATM PHY in an ATM Switch
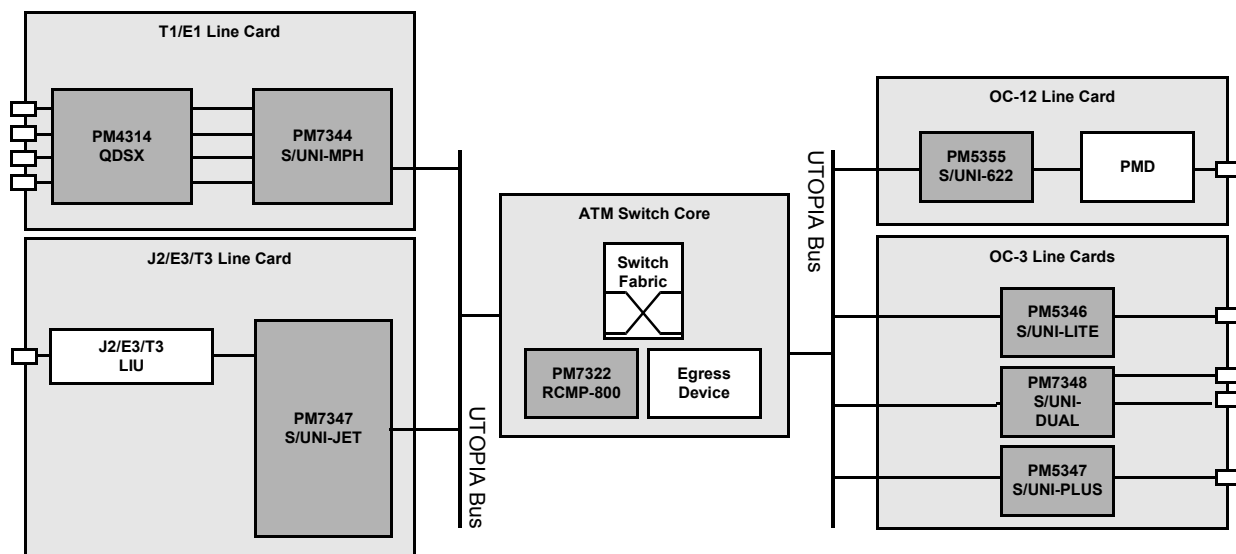
As a J2/E3/T3 framer, the S/UNI-JET can be used in router, frame relay switch, and multiplexer applications. Refer to Figure 2.

Figure 2 S/UNI-JET Operating as a Framer Device in Frame Relay Equipment

Access Side   Uplink Side
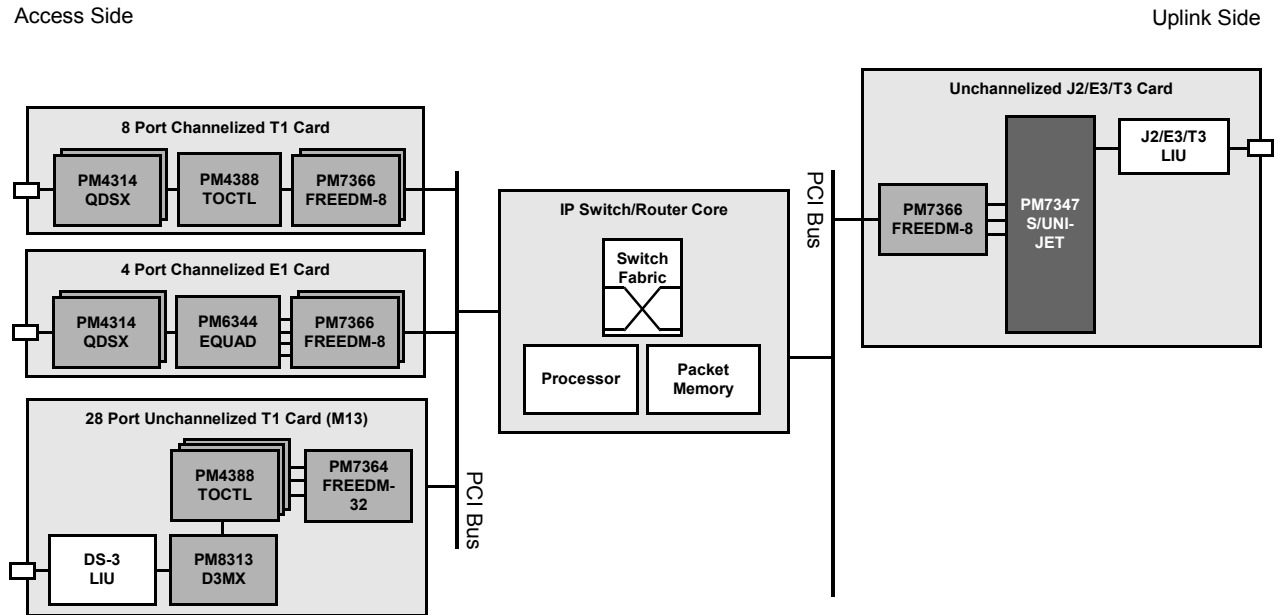
In an unchannelized J2/E3/T3 line card, the S/UNI-JET directly connects to one PM7366 FREEDM-8 HDLC controller. Each FREEDM-8 can process two high-speed links such as T3 and E3, or can process up to eight lower speed links such as J2. The S/UNI-JET gaps all the overhead bits so that only the payload data is passed to and from FREEDM-8. On the line side, the S/UNI-JET is connected to one J2/E3/T3 line interface unit. On the system side, the S/UNI-JET interfaces with a data link device over a serial bit interface.

6   Block Diagram

Figure 3   Block Diagram
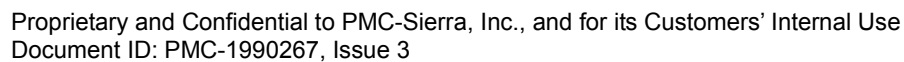
7   Description

The PM7346 S/UNI-JET is an ATM physical layer processor with integrated DS3, E3, and J2 framers. It supports PLCP sublayer DS1, DS3, E1, and E3 processing and ATM cell delineation.

The S/UNI-JET contains:

- An Integral DS3 framer that provides DS3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a.

- An Integral E3 framer that provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751.

- An Integral J2 framer that provide J2 framing in accordance with ITU-T Recommendation G.704 and I.432.

When configured for various transmission system sublayer processing, the S/UNI-JET accepts and outputs the appropriate type of bipolar and unipolar signals as described in Table 2:

Table 2   Transmission System Sublayer Processing Acceptance and Output

Transmission System Sublayer Processing	Acceptance and Output
DS3	Accepts and outputs both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.
E3	Accepts and outputs both HDB3-encoded bipolar and unipolar signals compatible with G.751 and G.832 applications.
J2	Accepts and outputs both B8ZS-encoded bipolar and unipolar signals compliant with G.704 and NTT 6.312 Mbit/s applications.
DS1, or E1	Accepts and outputs outputs unipolar signals with appropriate clock and frame pulse signals for physical sublayer processing.
Other transmission systems	Provides a generic interface for physical sublayer processing.

In the DS3 receive direction, the S/UNI-JET frames to DS3 signals with a maximum average reframe time of 1.5 ms and detects line code violations (LCV), loss of signal (LOS), framing bit errors, parity errors, path parity errors, alarm indication signals (AIS), far end receive failure (FERF), and idle code. The DS3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the Path Maintenance Data Link (PMDL) and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for PMDL support. Valid bit-oriented codes in the FEAC channels are also detected and are available through the microprocessor port.

Table 3   Summary of Receive Detection Features

Transmission System Sublayer Processing	Transmit or Receive	Detected Features
DS3	Receive	LCV, LOS, framing bit errors, parity errors, path parity errors, AIS, FERF, and idle code
E3	Receive	LCV, LOS, framing bit errors, AIS, and RAI

Transmission System Sublayer Processing	Transmit or Receive	Detected Features
J2	Receive	LCV, LOS, LOF, framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and RAI

In the E3 receive direction, the S/UNI-JET frames to G.751 and G.832 E3 signals with a maximum average reframe times of 135 µs for G.751 frames and 250 µs for G.832 frames. LCVs, LOS, framing bit errors, AIS, and remote alarm indication (RAI) are detected. Further, when processing G.832 formatted data, parity errors, far end receive failure, and far end block errors are also detected; and the Trail Trace message can be extracted and made available through the microprocessor port. HDLC receivers are provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

In the J2 receive direction, the S/UNI-JET frames to G.704 6.312 MHz signals with a maximum average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 bits to rule out 99.9% of all static mimic framing patterns is available with a maximum average reframe time of 10.22 ms when operating with a 10^{-4} bit error rate. The alternate framing algorithm can be selected by the CRC_REFR bit in the J2-FRMR Configuration Register. LCV, LOS, loss of frame (LOF), framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and RAI are detected. HDLC receivers are provided for Data Link support.

Error event accumulation is also provided by the S/UNI-JET. Framing bit errors, LCV, parity errors, path parity errors, and far end block errors (FEBE) are accumulated, when appropriate, in saturating counters for DS3, E3, and J2 frames. LOF detection for DS3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1ms, 2ms, and 3ms.

In the DS3 transmit direction, the S/UNI-JET inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for the insertion of FEAC channels and the PMDL in the appropriate overhead bits. AIS can be inserted by using internal register bits and other status signals such as the idle signal can be inserted when enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit parity application.

In the E3 transmit direction, the S/UNI-JET inserts E3 framing in either G.832 or G.751 format. When enabled for G.832 operation, an HDLC transmitter is provided so that the Network Requirement or General Purpose Data Link is inserted into the appropriate overhead bits. The AIS and other status signals can be inserted by internal register bits.

In the J2 transmit direction, the S/UNI-JET inserts J2 6.312 Mbit/s G.704 framing. HDLC transmitters are provided the Data Links are inserted. CRC-5 check bits are calculated and inserted into the J2 multiframe. External pins are provided so that any of the overhead bits within the J2 frame can be overwritten.

The S/UNI-JET also supports diagnostic options that allow it to insert, when appropriate, the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, LCV, all-zeros, AIS, RAIs, and Remote End Alarms.

The S/UNI-JET provides cell delineation for ATM cells using the PLCP framing format, or by using the header check sequence octet in the ATM cell header as specified by ITU-T Recommendation I.432. DS1, DS3, E1, and E3-based PLCP frame formats can be processed. Non-PLCP-based cell delineation is done with either bit, nibble, or byte-wide search algorithms depending on the line interface used. An interface consistent with the generic physical interface defined by ITU-T Recommendation I.432 is provided for arbitrary rates up to 52 Mbit/s. This interface is used for PHY layer support for transmission systems that do not have an associated PLCP sublayer, or to provide an efficient means of directly mapping ATM cells to existing transmission system formats (such as DS3 and DS1).

In the PLCP receive direction, framing, path overhead extraction, and cell extraction is provided. BIP-8 error events, frame octet error events, and FEBE events are accumulated.

In the PLCP transmit direction, the S/UNI-JET provides overhead insertion using inputs or internal registers, DS3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion, and automatic FEBE insertion. Diagnostic features for BIP-8 error, framing error and FEBE insertion are also supported.

In the cell receive path, idle cells may be dropped according to a programmable filter. By default, incoming cells with single bit HCS errors are corrected and written to the FIFO buffer. Optionally, cells can be dropped upon detection of a HCS error. Cell delineation may optionally be disabled to allow all cells to pass, regardless of cell delineation status. The ATM cell payloads are optionally descrambled. ATM cell headers may optionally be descrambled (for use with PPP packets). Assigned cells containing no detectable HCS errors are written to a FIFO buffer. Cell data is read from the FIFO using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} and Utopia Level 2-compatible interface. Cell data parity is also provided. Counts of error-free assigned cells, and cells containing HCS errors are accumulated independently for performance monitoring purposes.

In the cell transmit path, cell data is written to a FIFO buffer using a synchronous 50 MHz 8-bit wide or 16-bit wide SCI-PHY^{TM} compatible interface. Cell data parity is also examined for errors. Idle cells are automatically inserted when the FIFO contains less than one full cell. HCS generation, cell payload scrambling, and cell header scrambling (for use with PPP packets) are optionally provided. Counts of transmitted cells are accumulated for performance monitoring purposes.

Both receive and transmit cell FIFOs provide buffering for four cells. The FIFOs provide the rate matching interface between the higher layer ATM entity and the S/UNI-JET.

The S/UNI-JET is configured, controlled, and monitored by a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked with this interface.

The S/UNI-JET requires a software initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 13.1 of this document for the details on how to program this sequence.

8 Pin Diagram

The S/UNI-JET is packaged in a 256-pin SBGA package with a body size of 27 mm by 27 mm and a pin pitch of 1.27 mm.

Quadrant A11/A20 to K11/K20

	20	19	18	17	16	15	14	13	12	11	
A	VSS	VSS	VSS	TDATI[10]	TDATI[14]	D[1]	D[5]	VSS	A[3]	A[7]	A
B	VSS	VDD	VDD	TDATI[9]	TDATI[13]	D[0]	D[4]	A[0]	A[2]	A[6]	B
C	VSS	VDD	VDD	TDATI[7]	TDATI[11]	TDATI[15]	D[2]	D[6]	A[1]	A[5]	C
D	TDAT[3]	TDAT[4]	TDAT[6]	NC	TDAT[8]	TDAT[12]	VDD	D[3]	D[7]	A[4]	D
E	TFCLK	TDAT[0]	TDAT[2]	TDAT[5]							E
F	TADR[0]	TADR[1]	TADR[2]	TDAT[1]							F
G	TSOC	TPRTY	VDD	VDD		**Bottom View**					G
H	BIAS	TCA	TENB	VDD		**(Top Left)**					H
J	VSS	NC	NC	DTCA							J
K	VSS	NC	PHY_ADR[2]	VDD							K
	20	19	18	17	16	15	14	13	12	11	

Quadrant A1/A10 to K1/K10

	10	9	8	7	6	5	4	3	2	1	
A	VSS	VSS	ALE	INTB	TRSTB	TOHM/TNEG	RCLK	VSS	VSS	VSS	A
B	A[9]	A[10]	WRB	TDO	TCK	TCLK	NC	VDD	VDD	VSS	B
C	A[8]	CSB	RSTB	TMS	TPOS/TDATO	RLCV/RNEG/ROHM	NC	VDD	VDD	VSS	C
D	VDD	RDB	TDI	VDD	RPOS/RDATI	NC	BIAS	NC	NC	VSS	D
E							NC	VSS	VSS	VSS	E
F							VSS	VSS	NC	NC	F
G		**Bottom View**					VDD	NC	VSS	VSS	G
H		**(Top Right)**					VSS	TOH	TOHCLK	VSS	H
J							TOHINS	TOHFP	ROH	ROHFP	J
K							ROHCLK	VSS	VSS	NC	K
	10	9	8	7	6	5	4	3	2	1	

Quadrant L11/L20 to Y11/Y20

	20	19	18	17	16	15	14	13	12	11	
L	PHY_ADR[1]	PHY_ADR[0]	ATMB	DRCA	**Bottom View** (Bottom Left)						L
M	NC	NC	NC	RSOC							M
N	VSS	RCA	RENB	RADR[1]							N
P	RFCLK	RADR[2]	RADR[0]	VDD							P
R	VDD	VDD	RPRTY	RDAT[13]							R
T	RDAT[15]	RDAT[14]	RDAT[12]	RDAT[9]							T
U	RDAT[11]	RDAT[10]	RDAT[8]	BIAS	RDAT[6]	RDAT[2]	VDD	TPOHCLK	REF8KO/ RPOHFP/ RFPO/ RMFPO	VDD	U
V	VSS	VDD	VDD	RDAT[7]	RDAT[3]	TICLK	TPOHINS	RPOH/ ROVRHD	VSS	NC	V
W	VSS	VDD	VDD	RDAT[5]	RDAT[1]	TIOHM/ TFPI/ TMFPI	TPOHFP/ TFPO/ TMFPO/ TGAPCLK/ TCELL	RPOHCLK/ RSCLK/ RGAPCLK	VSS	VSS	W
Y	VSS	VSS	VSS	RDAT[4]	RDAT[0]	TDATI/ TPOH	LCD/ RDATO	VSS	VSS	VSS	Y
	20	19	18	17	16	15	14	13	12	11	

Quadrant L1/L10 to Y1/Y10

	10	9	8	7	6	5	4	3	2	1	
L	**Bottom View**						VDD	NC	NC	VSS	L
M	(Bottom Right)						VSS	NC	NC	VSS	M
N							NC	NC	NC	VSS	N
P							VDD	VSS	NC	NC	P
R							NC	NC	NC	VSS	R
T							NC	REF8KI	NC	NC	T
U	NC	VSS	NC	VDD	NC	NC	BIAS	NC	NC	FRMSTAT	U
V	NC	VSS	NC	NC	VSS	NC	NC	VDD	VDD	VSS	V
W	NC	VSS	VSS	NC	VSS	VSS	NC	VDD	VDD	VSS	W
Y	NC	NC	VSS	NC	NC	VSS	NC	VSS	VSS	VSS	Y
	10	9	8	7	6	5	4	3	2	1	

9 Pin Description

Pin Name	Type	Pin No.	Function
TPOS TDATO	Output	C6	The Transmit Digital Positive Pulse (TPOS) contains the positive pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail output format is selected. The Transmit Data (TDATO) contains the transmit data stream when the single-rail (unipolar) output format is enabled or when a non-DS3/E3/J2 based transmission system is selected. The TPOS/TDATO pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-JET Transmit Configuration Register. Output signal polarity control is provided by the TPOSINV bit in the S/UNI-JET Transmit Configuration Register. Both TPOS and TDATO are updated on the falling edge of TCLK by default, and may be configured for update on the rising edge of TCLK through the TCLKINV bit in the S/UNI-JET Transmit Configuration Register. Also, both TPOS and TDATO can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-JET Transmit Configuration Register.
TNEG TOHM	Output	A5	The Transmit Digital Negative Pulse (TNEG) contains the negative pulses transmitted on the B3ZS-encoded DS3, HDB3-encoded E3, or B8ZS-encoded J2 transmission system when the dual-rail NRZ output format is selected. The Transmit Overhead Mask (TOHM) indicates the position of overhead bits (non-payload bits) in the transmission system stream aligned with TDATO. TOHM indicates the location of the M-frame boundary for DS3, the position of the frame boundary for E3, and the position of the multi-frame boundary for J2 when the single-rail (unipolar) NRZ input format is enabled. When a PLCP formatted signal is transmitted, TOHM is set to logic one once per transmission frame, and indicates the DS1 or E1 frame alignment. When a non-PLCP, non-DS3, non-E3, or non-J2 based signal is transmitted, TOHM is a delayed version of the TIOHM input, and indicates the position of each overhead bit in the transmission frame. TOHM is updated on the falling edge of TCLK. The TNEG/TOHM pin function selection is controlled by the TFRM[1:0] and the TUNI bits in the S/UNI-JET Transmit Configuration Register. Output signal polarity control is provided by the TNEGINV bit in the S/UNI-JET Transmit Configuration Register.

Pin Name	Type	Pin No.	Function
			By default, both TNEG and TOHM are updated on the falling edge of TCLK and can be enabled for update on the rising edge of TCLK. This sampling is controlled by the TCLKINV bit in the S/UNI-JET Transmit Configuration Register. Also, both TNEG and TOHM can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-JET Transmit Configuration Register.
TCLK	Output	B5	The Transmit Output Clock (TCLK) provides the transmit direction timing. TCLK is a buffered version of TICLK and can be enabled to update the TPOS/TDATO and TNEG/TOHM outputs on its rising or falling edge.
RPOS RDATI	Input	D6	The Receive Digital Positive Pulse (RPOS) contains the positive pulses received on the B3ZS-encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected. The Receive Data (RDATI) contains the data stream when the single-rail (unipolar) NRZ input format is enabled or when a non-DS3/E3/J2 based transmission system is being processed (for example, RDATI may contain a DS1 or E1 stream). The RPOS/RDATI pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-JET Configuration Register and by the UNI bits in the DS3 FRMR, the E3 FRMR, or the J2 FRMR Configuration Register. Both RPOS and RDATI are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-JET Receive Configuration Register. Note: Signal polarity control is provided by the RPOSINV bit in the S/UNI-JET Receive Configuration Register.

Pin Name	Type	Pin No.	Function
RNEG	Input	C5	The Receive Digital Negative Pulse (RNEG) contains the negative pulses received on the B3ZS encoded DS3, the HDB3-encoded E3, or the B8ZS-encoded J2 transmission system when the dual-rail NRZ input format is selected.
RLCV			The Receive LCV (RLCV) contains LCV indications when the single-rail (unipolar) NRZ input format is enabled for DS3, E3, or J2 applications. Each LCV is represented by an RCLK period-wide pulse.
ROHM			When a DS1 or E1 PLCP or ATM direct-mapped signal is received, Receive Overhead Mask (ROHM) is pulsed once per transmission frame, and indicates the DS1 or E1 frame alignment relative to the RDATI data stream. When an alternate frame-based signal is received, ROHM indicates the position of each overhead bit in the transmission frame.
			The RNEG/RLCV/ROHM pin function selection is controlled by the RFRM[1:0] bits in the S/UNI-JET Receive Configuration Register, the UNI bits in the DS3 FRMR, E3 FRMR, or J2 FRMR Configuration Register, and the PLCPEN and EXT bits in the SPLR Configuration Register.
			RNEG, RLCV, and ROHM are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-JET Receive Configuration Register.
			Note: Signal polarity control is provided by the RNEGINV bit in the S/UNI-JET Receive Configuration Register.
RCLK	Input	A4	The Receive Clock (RCLK) provides the receive direction timing. RCLK is the externally recovered transmission system baud rate clock that samples the RPOS/RDATI and RNEG/RLCV/ROHM inputs on its rising or falling edge.
TOHINS	Input	J4	The Transmit DS3/E3/J2 Overhead Insertion (TOHINS) controls the insertion of the DS3, E3, or J2 overhead bits from the TOH input.
			When TOHINS is high, the associated overhead bit in the TOH stream is inserted in the transmitted DS3, E3, or J2 frame. When TOHINS is low, the DS3, E3, or J2 overhead bit is generated and inserted internally.
			TOHINS is sampled on the rising edge of TOHCLK. If TOHINS is a logic one, the TOH input has precedence over the internal datalink transmitter, or any internal register bit setting.

Pin Name	Type	Pin No.	Function
TOH	Input	H3	When configured for DS3 operation, Transmit DS3/E3/J2 Overhead Data (TOH) contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream.
			When configured for G.832 E3 operation, TOH contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream.
			When configured for G.751 E3 operation, TOH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream.
			When configured for J2 operation, TOH contains the overhead bits (TS97, TS98, Framing, X_{1-3}, A, M, E_{1-5}) that may be inserted in the transmit J2 stream.
			If TOHINS is a logic one, the TOH input has precedence over the internal datalink transmitter, or any other internal register bit setting. TOH is sampled on the rising edge of TOHCLK.
TOHFP	Output	J3	The Transmit DS3/E3/J2 Overhead Frame Position (TOHFP) is used to align the individual overhead bits in the transmit overhead data stream, TOH, to the DS3 M-frame or the E3 frame.
			For DS3, TOHFP is high during the X1 overhead bit position in the TOH stream. For G.832 E3, TOHFP is high during the first bit of the FA1 byte. For G.751 E3, TOHFP is high during the RAI overhead bit position in the TOH stream. For J2, TOHFP is high during the first bit of timeslot 97 in the first frame of a 4-frame multiframe).
			TOHFP is updated on the falling edge of TOHCLK.
TOHCLK	Output	H2	The Transmit DS3/E3/J2 Overhead Clock (TOHCLK) is active when a DS3, E3, or J2 stream is being processed. TOHCLK is nominally a 526 kHz clock for DS3, a 1.072 MHz clock for G.832 E3, a 1.074 MHz clock for G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2.
			TOHFP is updated on the falling edge of TOHCLK. TOH, and TOHINS are sampled on the rising edge of TOHCLK.
REF8KI	Input	T3	The PLCP frame rate is locked to an external 8 kHz reference applied on Reference 8 kHz Input (REF8KI). An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate.
			The REF8KI input must transition high once every 125 µs for correct operation. The REF8KI input is treated as an asynchronous signal and must be "glitch-free". If the LOOPT register bit is logic one, the PLCP frame rate is locked to the RPOHFP signal instead of the REF8KI input.

Pin Name	Type	Pin No.	Function
TPOHINS	Input	V14	The Transmit Path Overhead Insertion (TPOHINS) controls the insertion of PLCP overhead octets on the TPOH input. When TPOHINS is logic one, the associated overhead bit in the TPOH stream is inserted in the transmit PLCP frame. When TPOHINS is logic zero, the PLCP path overhead bit is generated and inserted internally. TPOHINS is sampled on the rising edge of TPOHCLK. Note: When operating in G.751 E3 PLCP mode, bits 8, 7, and 6 of the C1 octet should not be manipulated.
TPOH TDATI	Input	Y15	The Transmit PLCP Overhead Data (TPOH) valid when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is logic zero. TPOH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) which may be inserted in the transmit PLCP frame. The octet data on TPOH is shifted in order from the most significant bit (bit 1) to the least significant bit (bit 8). TPOH is sampled on the rising edge of TPOHCLK. The Framer Transmit Data (TDATI) contains the serial data to be transmitted when the S/UNI-JET is configured as a DS3, E3, or J2 framer device for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register. TDATI is sampled on the rising edge of TICLK if the TXGAPEN register bit in the S/UNI-JET Configuration 2 Register is logic zero. If TXGAPEN is logic one, then TDATI is sampled on the falling edge of TGAPCLK.

Pin Name	Type	Pin No.	Function
TPOHFP	Output	W14	The Transmit Path Overhead Frame Position (TPOHFP) is valid when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is logic zero. The TPOHFP output locates the individual PLCP path overhead bits in the transmit overhead data stream, TPOH. TPOHFP is logic one while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TPOH stream.
			TPOHFP is updated on the falling edge of TPOHCLK.
TFPO			The Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register to logic one and the TXGAPEN bit in the S/UNI-JET Configuration Register to logic zero.
			TFPO pulses high for 1 out of every 85 clock cycles when configured for DS3, giving a free-running mark for all overhead bits in the frame. TFPO pulses high for 1 out of every 1536 clock cycles when configured for G.751 E3, giving a free-running reference G.751 indication. TFPO pulses high for 1 out of every 4296 clock cycles when configured for G.832 E3, giving a free-running reference G.832 frame indication. TFPO pulses high for 1 out of every 789 clock cycles when configured for J2, giving a free-running reference frame indication.
TMFPO			TMFPO pulses high for 1 out of every 4760 clock cycles when configured for DS3, giving a free-running reference M-frame indication. TMFPO pulses high for 1 out of every 3156 clock cycles when configured for J2, giving a free-running reference multi-frame indication. TMFPO behaves the same as TFPO for E3 applications.
			TFPO and TMFPO are updated on the rising edge of TICLK or RCLK if loop-timed.
TGAPCLK			The Framer Gapped Transmit Clock (TGAPCLK) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register and the TXGAPEN bit in the S/UNI-JET Configuration 2 Register.
			TGAPCLK is derived from the transmit reference clock TICLK or from the receive clock if loop-timed. The overhead bit (gapped) positions are generated internal to the device. TGAPCLK is held high during the overhead bit positions. This clock is useful for interfacing to devices which source payload data only.
			TGAPCLK is used to sample TDATI.

Pin Name	Type	Pin No.	Function
TCELL			The Transmit Cell Indication (TCELL) is valid when the TCELL bit in the S/UNI-JET Miscellaneous Register is set. TCELL pulses once for every cell (idle or assigned) transmitted. TCELL is updated using timing derived from the transmit input clock (TICLK), and is active for a minimum of 8 TICLK periods (or 8 RCLK periods if loop-timed).
TPOHCLK	Output	U13	The Transmit PLCP Overhead Clock (TPOHCLK) is active when PLCP processing is enabled. TPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, and a 576 kHz clock for an G.751 E3 based PLCP frame. TPOHFP is updated on the falling edge of TPOHCLK. TPOH and TPOHINS are sampled on the rising edge of TPOHCLK.
TIOHM	Input	W15	The Transmit Input Overhead Mask (TIOHM) is valid only if the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is logic zero. TIOHM indicates the position of overhead bits when not configured for DS1, DS3, E1, E3, or J2 transmission system streams. TIOHM is delayed internally to produce the TOHM output. When configured for operation over a DS1, a DS3, an E1, an E3, or a J2 transmission system sublayer, TIOHM is not required, and should be set to logic zero. When configured for other transmission systems, TIOHM is set to logic one for each overhead bit position. TIOHM is set to logic zero if the transmission system does not contain overhead bits. TIOHM is sampled on the rising edge of TICLK. The Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register to logic one.
TFPI			TFPI indicates the position of all overhead bits in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame. TFPI is not required to pulse at every frame boundary in E3 or J2 modes.
TMFPI			TMFPI indicates the position of the first bit in each DS3 M-frame, the first bit in each E3 frame, or the first framing bit in each J2 multiframe. TMFPI is not required to pulse at every multiframe boundary. TFPI/TMFPI is sampled on the rising edge of TICLK.

Pin Name	Type	Pin No.	Function
TICLK	Input	V15	The Transmit Input Clock (TICLK) provides the transmit direction timing. TICLK is the externally generated transmission system baud rate clock. It is internally buffered to produce the transmit clock output, TCLK, and can be enabled to update the TPOS/TDATO and TNEG/TOHM outputs on the TICLK rising edge. The TICLK maximum frequency is 52 MHz.
ROHFP	Output	J1	The Receive DS3/E3/J2 Overhead Frame Position (ROHFP) locates the individual overhead bits in the received overhead data stream, ROH. ROHFP is high during the X1 overhead bit position in the ROH stream when processing a DS3 stream. ROHFP is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFP is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFP is high during the first bit in Timeslot 97 in the first frame of the 4-frame multiframe when processing a J2 stream. ROHFP is updated on the falling edge of ROHCLK.
ROH	Output	J2	The Receive DS3/E3/J2 Overhead Data (ROH) contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream. It also contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 stream, the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream, and the overhead bits (Framing, X_{1-3}, A, M, E_{1-5}) extracted from the received J2 stream. ROH is updated on the falling edge of ROHCLK.
ROHCLK	Output	K4	The Receive DS3/E3/J2 Overhead Clock (ROHCLK) is active when a DS3, E3, or J2 stream is being processed. ROHCLK is nominally a 526 kHz clock when processing DS3, a 1.072 MHz clock when processing G.832 E3, a 1.074 MHz clock when processing G.751 E3, and a gapped 6.312 MHz clock with an average frequency of 168 kHz for J2. ROH and ROHFP are updated on the falling edge of ROHCLK.

Pin Name	Type	Pin No.	Function
REF8KO RPOHFP RFPO RMFPO	Output	U12	The Reference 8kHz Output (REF8KO) is an 8kHz reference derived from the receive clock (RCLK). A free-running divide-down counter is used to generate REF8KO so it will not "glitch" on reframe actions. REF8KO will pulse high for approximately one RCLK cycle every 125 µs. REF8KO should be treated as a "glitch-free" asynchronous signal. The Receive PLCP Overhead Frame Position (RPOHFP) locates the individual PLCP path overhead bits in the receive overhead data stream, RPOH. RPOHFP is logic one while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK. RPOHFP is available when the PLCPEN register bit is logic one in the SPLR Configuration Register. The Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO) is valid when the S/UNI-JET is configured to be in framer only mode. The 8KREFO bit must be set to logic zero in the S/UNI-JET Configuration Register. RFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-subframe, the first bit in each G.751 E3 or G.832 E3 frame, or the first framing bit in each J2 frame RMFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-frame, the first bit in each G.751 or G.832 E3 multiframe, or the first framing bit in each J2 multiframe. RFPO/RMFPO is updated on either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the S/UNI-JET Receive Configuration Register.
RPOH ROVRHD	Output	V13	The Receive PLCP Overhead Data (RPOH) contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) extracted from the received PLCP frame when the PLCP layer is in-frame. When the PLCP layer is in the LOF state, RPOH is forced to all ones. The octet data on RPOH is shifted out in order from the most significant bit (bit 1) to the least significant bit (bit 8). RPOH is updated on the falling edge of RPOHCLK. The Framer Receive Overhead Indication (ROVRHD) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register. ROVRHD will be high whenever the data on RDATO corresponds to an overhead bit position. ROVRHD is updated on the either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the S/UNI-JET Receive Configuration Register.

Pin Name	Type	Pin No.	Function
RPOHCLK	Output	W13	The Receive PLCP Overhead Clock (RPOHCLK) is active when PLCP processing is enabled. The frequency of this signal depends on the selected PLCP format. RPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, or a 576 kHz clock for a G.751 E3 based PLCP frame.
			RPOHFP and RPOH are updated on the falling edge of RPOHCLK.
RSCLK			The Framer Recovered Clock (RSCLK) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration Register.
			RSCLK is the recovered clock and timing reference for RDATO, RFPO/RMFPO, and ROVRHD.
RGAPCLK			The Framer Recovered Gapped Clock (RGAPCLK) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register and the RXGAPEN bit in the S/UNI-JET Configuration 2 Register.
			RGAPCLK is the recovered clock and timing reference for RDATO. RGAPCLK is held high for bit positions which correspond to overhead.
LCD	Output	Y14	The Loss of Cell Delineation (LCD) is an active high signal which is asserted while the ATM cell processor has detected a Loss of Cell Delineation defect. The FRMRONLY bit in the S/UNI-JET Configuration 1 Register must be set to logic zero for LCD to be valid.
RDATO			The Framer Receive Data (RDATO) is valid when the S/UNI-JET is configured as a DS3, E3, or J2 framer for non-ATM applications by setting the FRMRONLY bit in the S/UNI-JET Configuration 1 Register.
			RDATO is the received data aligned to RFPO/RMFPO and ROVRHD. RDATO is updated on the active edge (as set by the RSCLKR register bit) of RSCLK or RGAPCLK.
FRMSTAT	Output	U1	Framer Status (FRMSTAT) is an active high signal that can be configured to show when one of the J2, E3, DS3, or PLCP framers have detected certain conditions. The FRMSTAT output can be programmed via the STATSEL[2:0] bits in the S/UNI-JET Configuration 2 Register to indicate: E3/DS3 LOF or J2 extended LOF, E3/DS3 OOF or J2 LOF, PLCP LOF, PLCP OOF, AIS, LOS, and DS3 Idle. FRMSTAT should be treated as a "glitch-free" asynchronous signal.
ATM8	Input	L18	The ATM Interface Bus Width Selection (ATM8) input pin determines whether the S/UNI-JET works with a 8-bit wide interface (RDAT[7:0] and TDAT[7:0]) or a 16-bit wide interface (RDAT[15:0] and TDAT[15:0]).
			If ATM8 is set to logic one, then the 8-bit wide interface is chosen. If ATM8 is set to logic zero, then the 16-bit wide interface is chosen.

Pin Name	Type	Pin No.	Function
TDAT[15] TDAT[14] TDAT[13] TDAT[12] TDAT[11] TDAT[10] TDAT[9] TDAT[8] TDAT[7] TDAT[6] TDAT[5] TDAT[4] TDAT[3] TDAT[2] TDAT[1] TDAT[0]	Input	C15 A16 B16 D15 C16 A17 B17 D16 C17 D18 E17 D19 D20 E18 F17 E19	The Transmit Cell Data Bus (TDAT[15:0]) carries the ATM cell octets that are written to the transmit FIFO. TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs. The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. When configured for the 8-bit wide interface, TDAT[15:8] are not used and should be tied to ground.
TPRTY	Input	G19	The Transmit Bus Parity (TPRTY) signal indicates the parity of the TDAT[15:0] or TDAT[7:0] bus. If configured for the 8-bit bus (via the ATM8 input pin), then parity is calculated over TDAT[7:0]. If configured for the 16-bit bus, then parity is calculated over TDAT[15:0]. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. Odd or even parity selection is made using the TPTYP register bit. TPRTY is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs.
TSOC	Input	G20	The Transmit Start of Cell (TSOC) signal marks the start of cell on the TDAT bus. When TSOC is high, the first word of the cell structure is present on the TDAT bus. It is not necessary for TSOC to be present for each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is sampled on the rising edge of TFCLK and is considered valid only when TENB is simultaneously asserted and the S/UNI-JET has been selected via the TADR[2:0] inputs.
TENB	Input	H18	The Transmit Multi-PHY Write Enable (TENB) signal is an active low input which is used along with the TADR[2:0] inputs to initiate writes to the transmit FIFO. When sampled low using the rising edge of TFCLK, the word on the TDAT bus is written into the transmit FIFO selected by the TADR[2:0] address bus. When sampled high using the rising edge of TFCLK, no write is performed, but the TADR[2:0] address is latched to identify the transmit FIFO to be accessed. A complete 53-octet cell must be written to the transmit FIFO before it is inserted into the transmit stream. Idle cells are inserted when a complete cell is not available.

Pin Name	Type	Pin No.	Function
TADR[2] TADR[1] TADR[0]	Input	F18 F19 F20	The Transmit Address (TADR[2:0]) bus is used for device selection and device polling in accordance with the Utopia Level 2 standard.
			When TADR[2:0] is set to the same value as the PHY_ADR[2:0] inputs than the transmit interface of this S/UNI-JET is either being selected or polled.
			Note: The null-PHY address 7H is an invalid address and cannot be used to select the S/UNI-JET.
			TADR[2:0] is sampled on the rising edge of TFCLK.
TCA	Output	H19	The Transmit Multi-PHY Cell Available (TCA) signal indicates when a cell is available in the transmit FIFO for the device selected by TADR[2:0].
			When high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full or that the corresponding transmit FIFO is full. TCA will transition low on the rising edge of TFCLK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0) if the device being polled is the same as the selected device.
			To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three, or four cells. Note: Regardless of what fill level TCA is set to indicate "full" at, the transmit cell processor can store four complete cells.
			TCA is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched (by TFCLK) from the TADR[2:0] inputs.
			The polarity of TCA (with respect the the description above) is inverted when the TCAINV register bit is set to logic one.
TFCLK	Input	E20	The Transmit FIFO Write Clock (TFCLK) is used to write ATM cells to the four-cell transmit FIFOs. TFCLK cycles at a 52 MHz or lower instantaneous rate.

Pin Name	Type	Pin No.	Function
DTCA	Output	J17	The Direct Access Transmit Cell Available (DTCA) output signals indicate when a cell is available in the transmit FIFO.
			When high, DTCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. DTCA can be configured to indicate either that the corresponding transmit FIFO is near full and can accept no more than four writes or that the corresponding transmit FIFO is full. DTCA will thus transition low on the rising edge of TFCLK which samples Payload byte 43 (TCALEVEL0=0) or 47 (TCALEVEL0=1) for the 8-bit interface (ATM8=1), or the rising edge of TFCLK which samples Payload word 19 (TCALEVEL0=0) or 23 (TCALEVEL0=1) for the 16-bit interface (ATM8=0).
			To reduce FIFO latency, the FIFO depth at which DTCA indicates "full" can be set to one, two, three or four cells. Note: Regardless of what fill level DTCA is set to indicate "full" at, the transmit cell processor can store four complete cells.
			The polarity of DTCA (with respect to the description above) is inverted when the TCAINV register bit is set to logic one.
			The DTCA outputs can be used to support Utopia Direct Access mode.
RDAT[15] RDAT[14] RDAT[13] RDAT[12] RDAT[11] RDAT[10] RDAT[9] RDAT[8] RDAT[7] RDAT[6] RDAT[5] RDAT[4] RDAT[3] RDAT[2] RDAT[1] RDAT[0]	Output	T20 T19 R17 T18 U20 U19 T17 U18 V17 U16 W17 Y17 V16 U15 W16 Y16	The Receive Cell Data Bus (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive ATM FIFO selected by RADR[2:0]. RDAT[15:0] is tri-stated when RENB is high. RDAT[15:0] is updated on the rising edge of RFCLK.
			The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. RDAT[15:8] will remain tri-stated if ATM8 is set to logic one.
			RDAT[15:0] is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.

Pin Name	Type	Pin No.	Function
RPRTY	Output	R18	The Receive Parity (RPRTY) signal indicates the parity of the RDAT bus. The S/UNI-JET can be configured to operate with an 8-bit wide or 16-bit wide ATM data interface via the ATM8 input pin. In the 8-bit mode, RPRTY reflects the parity of RDAT[7:0]. In the 16-bit mode, RPRTY reflects the parity of RDAT[15:0]. Odd or even parity selection is made using the RXPTYP register bit. RPRTY is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.
RSOC	Output	M17	The Receive Start of Cell (RSOC) signal marks the start of cell on the RDAT bus. RSOC marks the start of the cell on the RDAT bus. RSOC is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched from the RADR[2:0] inputs when RENB is high.
RENB	Input	N18	The Receive Multi-PHY Read Enable (RENB) signal is used to initiate reads from the receive FIFO. When sampled low using the rising edge of RFCLK, a byte is read (if one is available) from the receive FIFO selected by the RADR[2:0] address bus and output on the RDAT bus. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[15:0], RPRTY, and RSOC are tri-stated, and the address on RADR[2:0] is latched to select the device or port for the next ATM FIFO access. RENB must operate in conjunction with RFCLK to access the FIFOs at a high enough rate to prevent FIFO overflows. The ATM layer device may de-assert RENB at anytime it is unable to accept another byte.
RADR[2] RADR[1] RADR[0]	Input	P19 N17 P18	The Receive Address (RADR[2:0])] bus is used for device selection and device polling in accordance with the Utopia Level 2 standard. When RADR[2:0] is set to the same value as the PHY_ADR[2:0] inputs than the receive interface of this S/UNI-JET is either being selected or polled. Note: The null PHY address 7H is an invalid address and cannot be used to select the S/UNI-JET. RADR[2:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
RCA	Output	N19	The Receive Multi-PHY Cell Available (RCA) signal indicates when a cell is available in the receive FIFO for the device selected by RADR[2:0].
			RCA can be configured to be de-asserted when either zero or four bytes remain in the selected/addressed FIFO. RCA will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0) if the PHY being polled is the same as the selected device.
			RCA is tri-stated when either the null-PHY address (7H) or an address not matching the address space set by PHY_ADR[2:0] is latched (by RFCLK) from the RADR[2:0] inputs.
			The polarity of RCA (with respect to the description above) is inverted when the RCAINV register bit is set to logic one.
RFCLK	Input	P20	The Receive FIFO Read Clock (RFCLK) signal is used to read ATM cells from the receive FIFOs. RFCLK must cycle at a 52 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflows.
DRCA	Output	L17	The Direct Access Receive Cell Available (DRCA) output signals indicate when a cell is available in the receive FIFO.
			DRCA can be configured to be de-asserted when either zero or four bytes remain in the FIFO. DRCA will thus transition low on the rising edge of RFCLK after Payload byte 48 (RCALEVEL0=1) or 43 (RCALEVEL0=0) is output for the 8-bit interface (ATM8=1), or after Payload word 24 (RCALEVEL0=1) or 19 (RCALEVEL0=0) is output for the 16-bit interface (ATM8=0).
			The DRCA outputs can be used to support Utopia Direct Access mode.
PHY_ADR[2] PHY_ADR[1] PHY_ADR[0]	Input	K18 L20 L19	The Device Identification Address (PHY_ADR[2:0]) inputs represent the address space which this S/UNI-JET occupies.
			When the PHY_ADR[2:0] inputs match the TADR[2:0] or RADR[2:0] inputs, then this S/UNI-JET is selected for transmit or receive ATM access.
			Note: The null-PHY address 7H is an invalid address and will not select the S/UNI-JET. The S/UNI-JET can be used directly in applications requiring 7 or fewer ports. Applications requiring more than 7 ports may require external decoding of the Utopia address to avoid bus contention.
CSB	Input	C9	The Active low Chip Select (CSB) signal must be low to enable S/UNI-JET register accesses. If CSB is not used, (RDB and WRB determine register reads and writes) then it should be tied to an inverted version of RSTB.

Pin Name	Type	Pin No.	Function
WRB	Input	B8	The Active low Write Strobe (WRB) signal is pulsed low to enable a S/UNI-JET register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input	D9	The Active low Read Enable (RDB) signal is pulsed low to enable a S/UNI-JET register read access. The S/UNI-JET drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	D12 C13 A14 B14 D13 C14 A15 B15	The Bi-directional Data Bus (D[7:0]) is used during S/UNI-JET register read and write accesses.
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B9 B10 C10 A11 B11 C11 D11 A12 B12 C12 B13	The Address Bus (A[10:0]) selects specific registers during S/UNI-JET register accesses.
RSTB	Input	C8	The Active low Reset (RSTB) signal is set low to asynchronously reset the S/UNI-JET. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
ALE	Input	A8	The Address Latch Enable (ALE) is active-high and latches the address bus A[10:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-JET to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	A7	The Active low Open-Drain Interrupt (INTB) signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note: The INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
TCK	Input	B6	The Test Clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	C7	The Test Mode Select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	D8	The Test Data Input (TDI) signal carries test data into the S/UNI-JET via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

Pin Name	Type	Pin No.	Function
TDO	Output	B7	The Test Data Output (TDO) signal carries test data out of the S/UNI-JET via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	A6	The Active low Test Reset (TRSTB) signal provides an asynchronous S/UNI-JET test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note: If not used, TRSTB must be connected to the RSTB input.
BIAS	Input	H20 U17 D4 U4	When tied to +5V, the +5V Bias (BIAS) input is used to bias the wells in the input and I/O pads so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When tied to VDD, the inputs and bi-directional inputs will only tolerate input levels up to VDD.
VDD[1] VDD[2] VDD[3] VDD[4] VDD[5] VDD[6] VDD[7] VDD[8] VDD[9] VDD[10] VDD[11] VDD[12] VDD[13] VDD[14] VDD[15] VDD[16] VDD[17] VDD[18] VDD[19] VDD[20] VDD[21] VDD[22] VDD[23] VDD[24] VDD[25] VDD[26] VDD[27] VDD[28] VDD[29] VDD[30] VDD[31] VDD[32]	Power	B2 B3 B18 B19 C2 C3 C18 C19 D7 D10 D14 G4 G17 G18 H17 K17 L4 P4 P17 R19 R20 U7 U11 U14 V2 V3 V18 V19 W2 W3 W18 W19	The DC Power pins should be connected to a well-decoupled +3.3V DC supply.

Pin Name	Type	Pin No.	Function
VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49]	Ground	A1 A2 A3 A9 A10 A13 A18 A19 A20 B1 B20 C1 C20 D1 E1 E2 E3 F3 F4 G1 G2 H1 H4 J20 K2 K3 K20 L1 M1 M4 N1 N20 P3 R1 U9 V1 V6 V9 V12 V20 W1 W5 W6 W8 W9 W11 W12 W20 Y1	The DC Ground pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59]	Ground	Y2 Y3 Y5 Y8 Y11 Y12 Y13 Y18 Y19 Y20	The DC Ground pins should be connected to GND.
NC[1] NC[2] NC[3] NC[4] NC[5] NC[6] NC[7] NC[8] NC[9] NC[10] NC[11] NC[12] NC[13] NC[14] NC[15] NC[16] NC[17] NC[18] NC[19] NC[20] NC[21] NC[22] NC[23] NC[24] NC[25] NC[26] NC[27] NC[28] NC[29] NC[30] NC[31] NC[32] NC[33] NC[34] NC[35] NC[36] NC[37] NC[38] NC[39] NC[40] NC[41] NC[42] NC[43] NC[44]	No Connect	B4 C4 D2 D3 D5 D17 E4 F1 F2 G3 J18 J19 K1 K19 L2 L3 M2 M3 M18 M19 M20 N2 N3 N4 P1 P2 R2 R3 R4 T1 T2 T4 U2 U3 U5 U6 U8 U10 V4 V5 V7 V8 V10 V11	These pins are No-Connects

Pin Name	Type	Pin No.	Function
NC[45] NC[46] NC[47] NC[48] NC[49] NC[50] NC[51] NC[52]	No Connect	W4 W7 W10 Y4 Y6 Y7 Y9 Y10	These pins are No-Connects

Notes

1. All S/UNI-JET inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

2. All S/UNI-JET outputs and bi-directionals have at least 3 mA drive capability. The data bus outputs, D[7:0], have 3 mA drive capability. The FIFO interface outputs, RDAT[15:0], RPRTY, RCA, DRCA, RSOC, TCA, and DTCA, have 12 mA drive capability. The outputs TCLK, TPOS/TDATO, TNEG/TOHM, TPOHFP/TFPO/TMFPO/TGAPCLK, LCD/RDATO, RPOH/ROVRHD, RPOHCLK/RSCLK/RGAPCLK, and REF8KO/RPOHFP/RFPO/RMFPO have 6 mA drive capability. All other outputs have 3 mA drive capability.

3. Inputs RSTB, ALE, TMS, TDI, and TRSTB have internal pull-up resistors.

4. RSTB, TRSTB, TMS, TDI, TCK, REF8KI, TFCLK, RFCLK, TICLK, and RCLK are schmitt trigger input pads.

5. The VSS [59:1] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-JET.

6. The VDD[32:1] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be used and must all connect to a common +3.3 V or ground rail, as appropriate.

7. During power-up and power-down, the voltage on the BIAS pin must be kept equal to or greater than the voltage on the VDD [32:1] pins, to avoid damage to the device.

10   Functional Description

The S/UNI-JET contains the following blocks:

- DS3, E3, J2 Framer

- DS3, E3, J2 Transmitter

- RBOC Bit oriented code detector and XBOC Bit oriented code detector

- RDLC PMDL receiver and TDPR PMDL transmitter

- PMON Performance monitor and CPPM Cell and PLCP performance monitor

- SPLR PLCP layer receiver and SPLT SMDS PLCP Layer Transmitter

- ATMF ATM cell delineator

- PRGD Pseudo-random sequence generator/detector

- RXCP Receive cell processor and TXCP Transmit cell processor

- RXFF Receive FIFO and TXFF Transmit FIFO

- TTB Trail trace buffer

- JTAG Test access port

10.1   DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates the circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. This block is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of LCV (LCV). The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A LOS defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm simultaneously examines five F-bit candidates. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal such as, the M-bits, M1, M2, and M3 are following the 010 pattern. If the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bit, framing is declared and out-of-frame (OOF) is removed. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An OOF defect is detected when three F-bit errors out of eight or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in three out of four consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration Register. The three out of eight consecutive F-bits OOF ratio provides more robust operation, in the presence of a high bit error rate, than the three out of 16 consecutive F-bits ratio. Either OOF criteria allows an OOF defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, LCV, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and FEBEs are indicated. These error indications, as well as the LCV and excessive zeros indication, are accumulated over one second intervals with the Performance Monitor (PMON). Note: The framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the AIS, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm uses a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010.. for AIS, 1100.. for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones).

Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms, that is, 1.5 times the maximum average reframe time. RED, AIS, or IDLE are removed when the respective counter decrements to zero. DS3 LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

Valid X-bits are extracted by the T3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic zero (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic one (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for two M-frames before being reported within the DS3 FRMR Status Register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an OOF.

When the C-bit parity application is enabled, both the FEAC channel and the PMDL are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the PMDL are received by the Data Link Receiver (RDLC).

The T3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The T3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the ROHCLK, and ROHFP outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

10.2   E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. For the G.751 format, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. For the G.832 format, the E3-FRMR expects to see the selected framing pattern error-free for two consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected:

In G.832 E3 format, the E3-FRMR extracts:

- The Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block.

- The FERF bit and indicates an alarm when the FERF bit is a logic one for three or five consecutive frames. The FERF indication is removed when the FERF bit is a logic zero for three or five consecutive frames.

- The FEBE bit and outputs it for accumulation in PMON.

- The Payload Type bits and buffers them so that they can be read by the microprocessor.

- The Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for three or five consecutive frames.

- The Network Operator byte and presents it as a serial stream for further processing by the RDLC block when the RNETOP bit in the S/UNI-JET Data Link and FERF Control Register is logic one. The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. All eight bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RDLC.

- The General Purpose Communication Channel byte and presents it to the RDLC when the RNETOP bit in the S/UNI-JET Data Link and FERF Control Register is logic zero The byte is also brought out on the ROH[x] output with an associated clock on ROHCLK[x].

In G.751 E3 mode, the E3-FRMR extracts:

- The RAI bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic one for three or five consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic zero for three or five consecutive frames.

- The National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RDLC when the RNETOP bit in the S/UNI-JET Data Link and FERF Control Register is logic zero. The bit is also brought out on the ROH[x] output with an associated clock on ROHCLK[x]. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream to the ATMF/SPLR block. For G.751 mode, the tributary justification bits can be optionally identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares OOF alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the OOF indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than eight zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than five zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

LOS is declared when no marks have been received for 32 consecutive bit periods. LOS de-asserted after 32 bit periods during which there is no sequence of four consecutive zeros.

E3 LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

10.3   J2 Framer

The J2-FRMR integrates circuitry to decode a unipolar or B8ZS encoded signal and frame to the resulting 6312 kbps J2 bit stream. Having found frame, the J2-FRMR extracts a variety of overhead and datalink information from the J2 bit stream.

The J2 format consists of 789-bit frames, each 125 µs long, consisting of 96 bytes of payload, 2 reserved bytes, and five F-bits. The frames are grouped into 4-frame multiframes. The multiframe format is described in Table 4.

Table 4   Multiframe Format

Bit #	1-8	..	761-768	769-776	777-784	785	786	787	788	789
1	TS1[1:8]	..	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	1	0	0	m
2	TS1[1:8]	..	TS96[1:8]	TS97[1:8]	TS98[1:8]	1	0	1	0	0
3	TS1[1:8]	..	TS96[1:8]	TS97[1:8]	TS98[1:8]	x1	x2	x3	a	m
4	TS1[1:8]	..	TS96[1:8]	TS97[1:8]	TS98[1:8]	e1	e2	e3	e4	e5

Notes

1.   *TS1 . TS96* are the byte interleaved payloads.

8.   *TS97*, *TS98* are reserved channels for signaling.

9.   The Frame Alignment Signal is represented as binary ones and zeroes.

10.   *m* is a 4-kHz datalink.

11.   *x1*, *x2*, and *x3* are spare bits, usually logic one.

12.   *a* is the remote LOF alarm bit, active high.

13.   *e1.e5* represent the CRC-5 check sequence. The entire 3156-bit multiframe, including the CRC-5 check sequence, should have a remainder of 0 when divided by $x^5 + x^4 + x^2 + 1$.

The J2-FRMR frames to a J2 signal with an average reframe time of 5.07 ms. An alternate framing algorithm that uses the CRC-5 check to detect static mimic patterns is also available. Once in frame, the J2-FRMR provides indications of frame and multiframe boundaries, and marks overhead bits, x-bits, m-bits, and reserved channels (TS97 and TS98). Indications of LOS, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided, and may be accumulated by the PMON (with the exception of change of frame alignment). Maskable interrupts are available to alert the microprocessor to the occurrence of any of these events. In addition to marking x-bit values, J2-FRMR provides microprocessor access to the x-bits, and will optionally generate an interrupt when any of the x-bits change state. The m-bits and the associated clock are can either be extracted through the RDLC or through the ROH[x] and ROHCLK[x] output pins of the S/UNI-JET . The m-bits are also presented to the RBOC for detection of any generic bit-oriented codes.

The J2-FRMR detects status signals such as Physical AIS, Payload AIS, RAI in m-bits, and Remote LOF (a-bit). It also optionally generates an interrupt when any of these status signals change.

J2 LOS is declared when no marks have been received for one of 15, 31, 63, or 255 consecutive bit periods. J2 LOS is cleared when either 15, 31, 63, or 255 consecutive bit periods have passed without detection of excessive zeros (meaning eight or more consecutive zeros) as required by ITU-T G.775.

J2 LOF is declared when seven or more consecutive multiframes with errored framing patterns are received. The J2 LOF is cleared when three or more consecutive multiframes with correct framing patterns are received. Also available are framing algorithms that take into account the CRC calculation. These framing algorithms are described in the following section.

J2 Physical Layer AIS is declared when two or less zeros are detected in a sequence of 3156 bits. It is cleared when three or more zeros is detected in a sequence of 3156 bits as required by ITU-T G.775.

J2 Payload AIS is detected when the incoming J2 payload has two or less zeros in a sequence of 3072 bits. It is cleared when three or more zeros are detected in a sequence of 3072 bits.

Note: The J2-FRMR may be forced to re-frame by microprocessor control. Similarly, the microprocessor may disable the J2-FRMR from reframing due to framing bit errors.

You can configure the J2-FRMR and mask or acknowledge all sources of interrupts through the internal registers. These internal registers are accessed from a generic microprocessor bus.

10.3.1   J2 Frame Find Algorithms

The J2-FRMR searches for frame alignment using one of two algorithms, as selected by the CRC_REFR bit in the J2-FRMR Configuration Register.

When the CRC_REFR bit is set to logic zero, the J2-FRMR uses only the frame alignment sequence to find frame, searching for three consecutive correct frame alignment sequences. The frame find block searches for the entire 9-bit sequence (spread over two multiframes) at the same time, greatly reducing the time required to find frame alignment. The framing process with CRC-REFR cleared is illustrated in Figure 4.

Figure 4   Framing algorithm (CRC_REFR = 0)
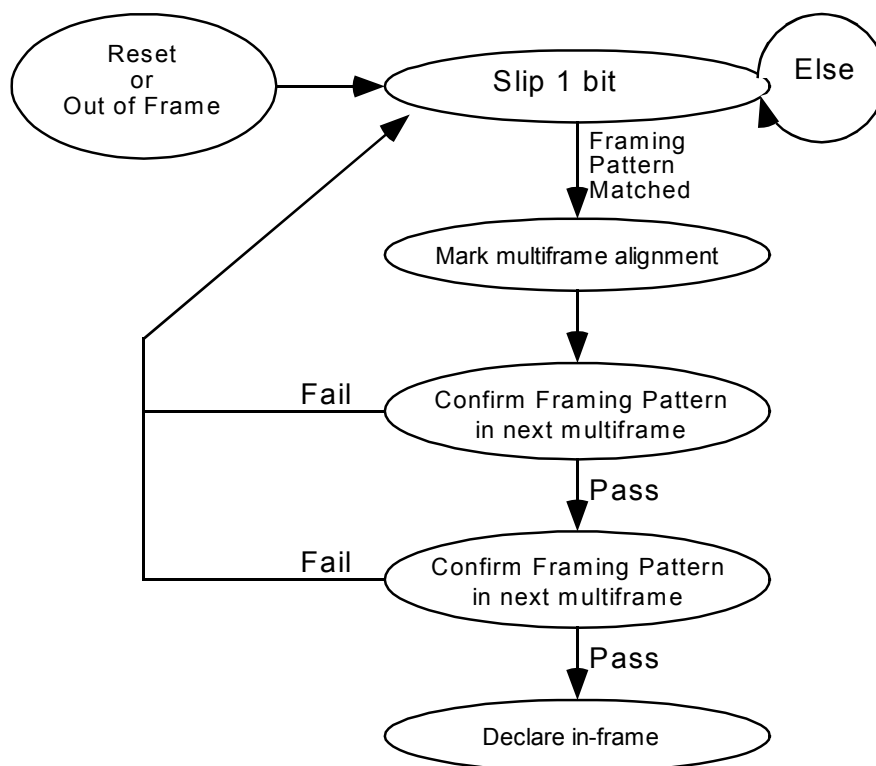
Using this algorithm, the J2-FRMR will on average find frame in 5.07 ms when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns.

When the CRC_REFR bit is set to logic one, in addition to requiring three consecutive correct framing patterns, the J2-FRMR requires that the first two CRC-5 checks be correct, or a reframe is initiated. To speed up the process, the CRC-5 and frame alignment checks are run concurrently, as illustrated in Figure 5.

Figure 5 Framing Algorithm (CRC_REFR = 1)
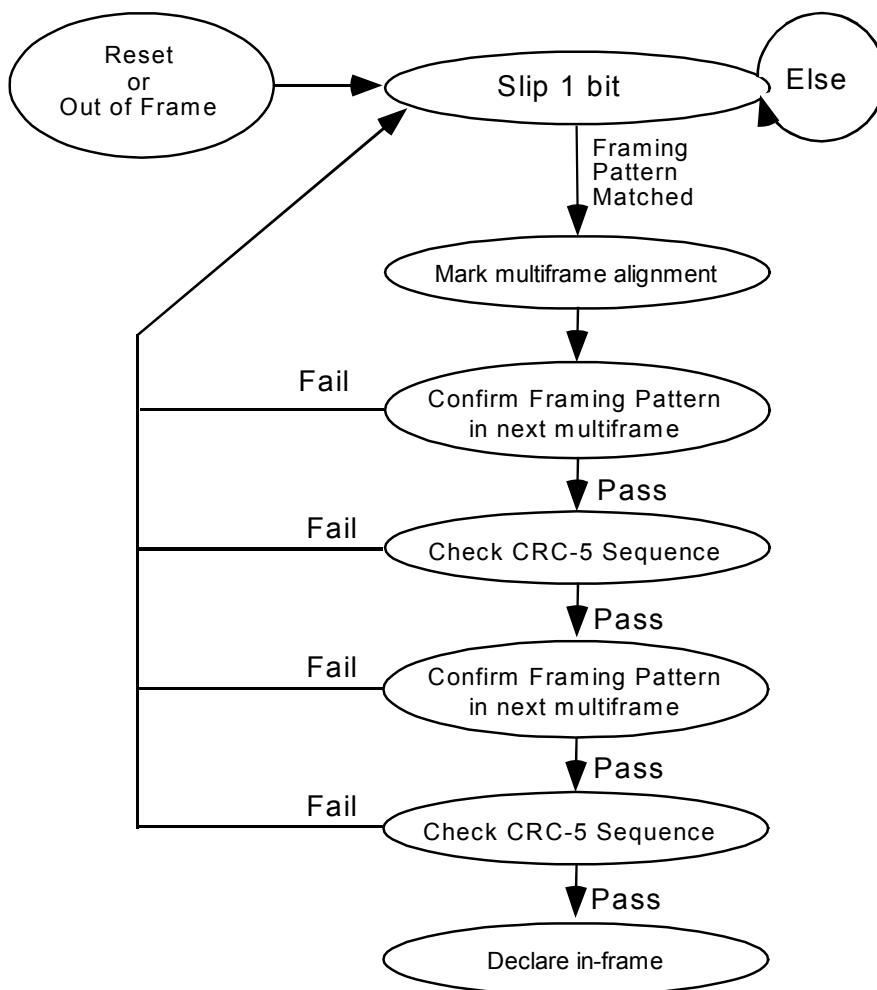
Using this algorithm, the J2-FRMR will find frame in 10.22 ms, on average when starting the search in the worst possible position, given a 10^{-4} error rate and no static mimic patterns. The algorithm will reject 99.90% of mimic patterns. Further protection against mimic patterns is available by monitoring the rate of CRC-5 errors.

Once frame alignment is found, the block sets the LOF indication low, indicates a change of frame alignment (if it occurred). The block declares LOF alignment if 7 consecutive FASs have been received in error. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of 1.65 years. The Frame Find Block can be forced to initiate a frame search at any time when the REFRAME bit in the J2-FRMR configuration. Conversely, when the FLOCK bit is set to logic one, the J2-FRMR will never declare LOF or search for a new frame alignment due to excess framing bit errors.

J2 extended LOF detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1 ms, 2 ms, or 3 ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an OOF condition and integrates down when the framer de-asserts the OOF condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is de-asserted.

10.4   RBOC Bit-Oriented Code Detector

Note: The Bit-Oriented Code Detector is only used in DS3 C-bit Parity or J2 mode.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the DS3 C-bit parity far-end alarm and control (FEAC) channel or in the J2 datalink signal stream. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

BOCs are received on the FEAC channel as 16-bit sequences each consisting of eight ones, a zero, six code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for eight out of 10 times or for four out of five times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values that are different from the detected code are received in a moving window of 10 code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all-ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

10.5   RDLC PMDL Receiver

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-JET Data Link and FERF/RAI Control Register), the E3 G.751 Network Use bit, or the J2 m-bit Data Link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits that indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end-of-message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

10.6   PMON Performance Monitor Accumulator

The PMON Block interfaces directly with either the DS3 Framer (T3-FRMR) to accumulate LCV events, parity error (PERR) events, path parity error (CPERR) events, FEBE events, excess zeros (EXZS), and framing bit error (FERR) events using the saturating counters:

- The E3 Framer (E3-FRMR) to accumulate LCV, PERR (in G.832 mode), FEBE and FERR events, or

- The J2 Framer (J2-FRMR) to accumulate LCVs, CRC errors (in the PERR counter), Framing bit errors (FERR), and excess zeros (EXZS).

The PMON stops accumulating error signals from the E3, DS3, or J2 Framers once frame synchronization is lost.

When an accumulation interval is signaled by a write to the PMON Register address space or a write to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register, the PMON transfers the current counter values into microprocessor-accessible holding registers and resets the counters to begin collecting error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt will be generated if it has been enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. Also provided is a register to indicate changes in the PMON counters since the last accumulation interval.

10.7   SPLR PLCP Layer Receiver

The PLCP Layer Receiver (SPLR) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 PLCP frame processing. The SPLR provides framing for PLCP based transmission formats.

The SPLR frames to DS1, DS3, E1, and G.751 E3 based PLCP frames with maximum average reframe times of 635 µs, 22 µs, 483 µs, and 32 µs respectively. Framing is declared (OOF is removed) upon finding two valid, consecutive sets of framing (A1 and A2) octets and two valid and sequential path overhead identifier (POHID) octets. While framed, the A1, A2, and POHID octets are examined. OOF is declared when an error is detected in both the A1 and A2 octets or when two consecutive POHID octets are found in error. LOF is declared when an OOF state persists for more than 25 ms, 1 ms, 20 ms, or 1 ms for DS1, DS3, E1, or G.751 E3 PLCP formats respectively. If the OOF events are intermittent, the LOF counter is decremented at a rate 1/12 (DS3 PLCP), 1/10 (E1, DS1 PLCP) or 1/9(G.751 E3 PLCP) of the incrementing rate. LOF is thus removed when an in-frame state persists for more than 250 ms for a DS1 signal, 12 ms for a DS3 signal, 200 ms for an E1 signal, or 9 ms for a G.751 E3 signal. When LOF is declared, PLCP reframe is initiated.

When in frame, the SPLR extracts the path overhead octets and outputs them bit serially on output RPOH, along with the RPOHCLK and RPOHFP outputs. Framing octet errors and path overhead identifier octet errors are indicated as frame errors. Bit interleaved parity errors and FEBEs are indicated. The yellow signal bit is extracted and accumulated to indicate yellow alarms. Yellow alarms are declared when 10 consecutive yellow signal bits are set to logic one. It is removed when 10 consecutive received yellow signal bits are set to logic zero. The C1 octet is examined to maintain nibble alignment with the incoming transmission system sublayer bit stream.

10.8   ATMF ATM Cell Delineator

The ATM Cell Delineator (ATMF) Block integrates circuitry to support HCS-based cell delineation for non-PLCP based transmission formats. The ATMF block accepts a bit serial cell stream from an upstream transmission system sublayer entity (such as the T3-FRMR, E3-FRMR, or J2-FRMR Block) and performs cell delineation to locate the cell boundaries. For PLCP applications, ATM cell positions are fixed relative to the PLCP frame, but the ATMF still performs cell delineation to locate the cell boundaries.

Cell delineation is the process of framing to ATM cell boundaries using the HCS field found in the ATM cell header. The HCS is a CRC-8 calculation over the first four octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The ATMF performs a sequential bit-by-bit, a nibble-by-nibble (DS-3 direct mapped), or a byte-by-byte (J2 and E3 direct-mapped) hunt for a correct HCS sequence. This state is referred to as the HUNT state. When receiving a bit serial cell stream from an upstream transmission-system sublayer entity, the bit, nibble, or byte boundaries are determined from the location of the overhead.

When a correct HCS is found, the ATMF locks on the particular cell boundary and assumes the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells. At that point a transition back to the HUNT state is executed. If an incorrect HCS is not found in this PRESYNC period then a transition to the SYNC state is made. In this state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Figure 6.

Figure 6   Cell delineation State Diagram
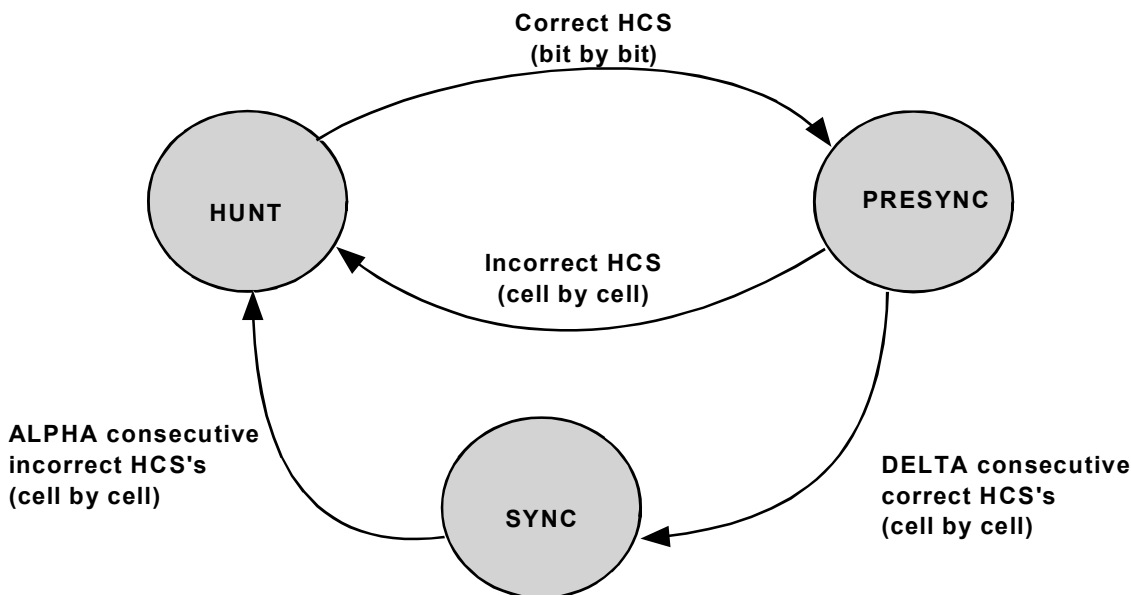
The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432. These values result in a maximum average time to frame of 127 μs for a DS3 stream carrying ATM cells directly mapped into the DS3 information payload.

LCD is detected by counting the number of incorrect cells while in the HUNT state. The counter value is stored in the RXCP-50 LCD Count Threshold Register. The threshold has a default value of 360 which results in:

- A DS3 application detection time of 3.5 ms.

- An E3 G.832 application detection time of 4.5 ms.

- An E3 G.751 application detection time of 5.0 ms.

- A J2 application time of 24.8ms, an E1 application detection time of 77 ms.

- A DS1 application detection time of 100 ms.

If the counter value is set to zero, the LCD output signal is asserted for every incorrect cell.

10.9   PRGD Pseudo-Random Sequence Generator/Detector

The Pseudo-Random Sequence Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Two types of test patterns (pseudo-random and repetitive) conform to ITU-T O.151.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. The PRGD can also insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern. The PRGD can perform an auto-synchronization to the expected pattern, and generate interrupts on detection and loss of the specified pattern. The PRGD can accumulate the total number of bits received and the total number of bit errors in two saturating 32-bit counters. The counters accumulate over an interval defined by writes to the S/UNI-JET Identification/Master Reset, and Global Monitor Update Register (006H) or by writes to any PRGD accumulation register. When an accumulation is forced by either method, then the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation. In addition to the two counters, a record of the 32 bits received immediately prior to the accumulation is available.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. Should it fail to find such a pattern, it will continue loading and checking until it finds a repetitive pattern. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences. Whenever a PRGD accumulation is forced, the PRGD stores a snapshot of the 32 bits received immediately prior to the accumulation. This snapshot may be examined in order to determine the exact nature of the repetitive pattern received by PRGD.

The pseudo-random or repetitive pattern can be inserted/extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

10.10   RXCP-50 Receive Cell Processor

The Receive Cell Processor (RXCP-50) Block integrates circuitry to support:

- Scrambled or unscrambled cell payloads.

- Scrambled or unscrambled cell headers.

- HCS verification.

- Idle cell filtering.

- Performance monitoring.

The RXCP-50 operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the LOF state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP-50 descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells can optionally be descrambled also. Note: Cell payload scrambling is enabled by default in the S/UNI-JET as required by ITU-T Recommendation I.432, but may be disabled to ensure backwards compatibility with older equipment.

The HCS is a CRC-8 calculation over the first four octets of the ATM cell header. The RXCP-50 verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP-50 can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and the cell header. Filtering according to a particular HCS and the GFC, PTI, and CLP bits of the ATM cell header is programmable through the RXCP-50 Registers. Note: The VCI and VPI bits must be all logic zero. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells can be blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' Registers are programmed with a certain blocking pattern. ATM Idle cells are filtered by default. For ATM cells, null or idle cells are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first four octets followed by the valid HCS octet.

While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 7.

Figure 7   HCS Verification State Diagram
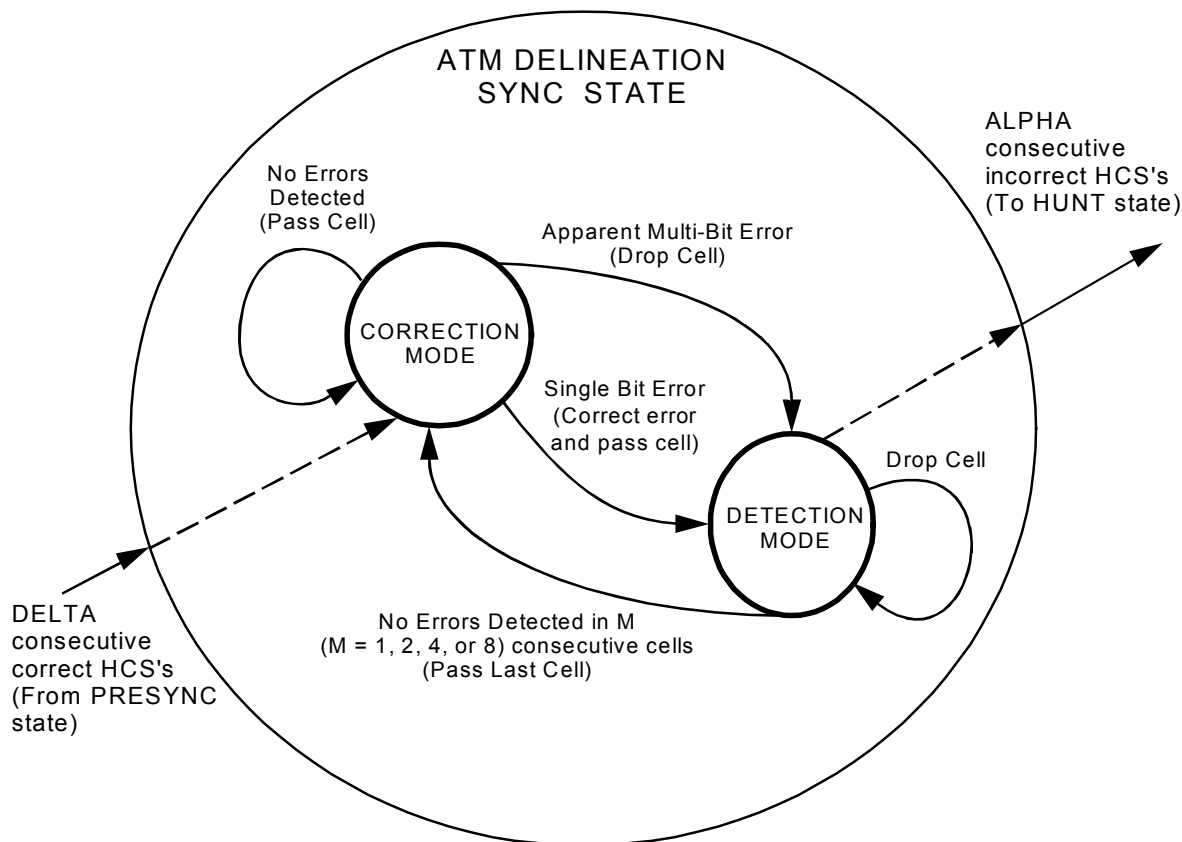
In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP-50 can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with a correct HCS. The mth cell is not discarded (see Figure 7). Note: The dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state.

Cell delineation can optionally be disabled, allowing the RXCP-50 to pass all data bytes it receives.

10.11 RXFF Receive FIFO

The Receive FIFO (RXFF) provides FIFO management and the S/UNI-JET receive cell interface. The receive FIFO contains four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

The general management functions of the RXFF are:

- Filling the receive FIFO.

- Indicating when the receive FIFO contains cells.

- Maintaining the receive FIFO read and write pointers.

- Detecting FIFO overrun and underrun conditions.

The FIFO interface is "UTOPIA Level 2"-compliant. It accepts a read clock (RFCLK) and read enable signal (RENB). The receive FIFO output bus (RDAT[15:0]) is tri-stated when RENB is logic one or if the PHY device address (RADR[4:0]) selected does not match this device's address. The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA and DRCA[4:1]) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA (and DRCA[x]) status changes from available to unavailable when the FIFO is either empty (RCALEVEL0=1) or near empty (RCALEVEL0 is logic zero).

The interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA (or DRCA[x]) is a logic zero will output invalid data.

10.12 CPPM Cell and PLCP Performance Monitor

The Cell and PLCP Performance Monitor (CPPM) Block interfaces directly to the SPLR to accumulate bit interleaved parity error events, framing octet error events, and FEBE events in saturating counters. When the PLCP framer (SPLR) declares LOF, the following are not counted: bit interleaved parity error events, framing octet error events, FEBE events, HCS error events.

When an accumulation interval is signaled by a write to the CPPM register address space or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register, the CPPM transfers the current counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

10.13 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the AIS, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits, and FEBE indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The PMDLmessages are sourced by the TDPR data link transmitter. These overhead signals can also be overwritten by using the TOH[x] and TOHINS[x] inputs.

When enabled for M23 operation, the C-bits are forced to logic one with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, LCV, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

10.14 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats and an alignment pulse applied to it by the SPLT block. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following format or mode.

In G.832 E3 format, the E3-TRAN:

- Inserts the BIP-8 byte calculated over the preceding frame.

- Inserts the Trail Trace bytes through the Trail Trace Buffer (TTB) block.

- Inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared.

- Inserts the FEBE bit, which is set to logic one when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic zero.

- Inserts the Payload Type bits based on the register value set by the microprocessor.

- Inserts the Tributary Unit multiframe indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor.

- Inserts the Timing Marker bit via a register bit.

- Inserts the Network Operator (NR) byte from the TDPR block when the TNETOP bit in the S/UNI-JET Data Link and FERF Control Register is logic one; otherwise, the NR byte is set to all ones. The NR byte can be overwritten by using the TOH[x] and TOHINS[x] input pins. All eight bits of the Network Operator byte are available for use as a datalink.

- Inserts the General Purpose Communication Channel (GC) byte from the TDPR block when the TNETOP bit in the S/UNI-JET Data Link and FERF Control Register is logic zero; otherwise, the byte is set to all ones. The GC byte can be overwritten by using the TOH[x] and TOHINS[x] input pins.

In G.751 E3 mode, the E3-TRAN :

- Inserts the RAI bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF.

- Inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the TDPR block as configured by the TNETOP bit in the S/UNI-JET Data Link and FERF Control Register and the NATUSE bit in the E3 TRAN Configuration Register.

- Optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single LCV for diagnostic purposes. Most of the overhead bits can be overwritten by using the TOH[x] and TOHINS[x] input pins.

10.15 J2 Transmitter

The J2 Transmitter (J2-TRAN) Block integrates circuitry required to insert the overhead bits into an J2 bit stream and produce a B8ZS-encoded signal. The J2-TRAN is directly compatible with the framing format specified in G.704 and NTT Technical Reference for High-Speed Digital Leased Circuit Services.

The J2-TRAN generates the frame alignment signal and inserts it into the incoming serial stream. All overhead and status bits in each frame format can be individually controlled by either register bits or by the transmit overhead stream.

The J2-TRAN inserts:

- The CRC-5 bits calculated over the preceding multiframe.

- The x-bits through microprocessor programmable register bits.

- The a-bit through a microprocessor programmable register bit.

- The m-bit data link through the TDPR block.

- Payload AIS or physical layer AIS through microprocessor programmable register bits.

- RAI over the m-bits, overwriting HDLC frames, by using the XBOC block or through automatic activation upon detection of certain remote alarm conditions.

The J2-TRAN allows overwriting of any of the overhead bits by using the TOH[x], TOHINS[x], TOHFP[x], and TOHCLK[x] overhead signals. Further, the J2-TRAN can provide insertion of single bit errors in the framing pattern or in the CRC-5 bits, and insertion of single LCV for diagnostic purposes.

10.16 XBOC Bit Oriented Code Generator

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity FEAC channel. A BOC is a 16-bit sequence consisting of eight ones, a zero, six code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111.

The code to be transmitted is programmed by writing the XBOC Code Register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

10.17 TDPR PMDL Transmitter

The Path Maintenance Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity PMDLin DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, the National Use bit datalink in G.751 E3, or the m-bit datalink in J2. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT FCS can be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the TDPR Transmit Data Register. The TDPR automatically begins transmission of data once at least one complete packet is written into its FIFO. All complete packets of data will be transmitted if no error condition occurs. After the last data byte of a packet, the CRC FCS (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. The TDPR will also force transmission of the FIFO data once the FIFO depth has surpassed the programmable upper limit threshold.

Transmission commences regardless of whether or not a packet has been completely written into the FIFO. The user must be careful to avoid overfilling the FIFO. Underruns can only occur if the packet length is greater than the programmed upper limit threshold because, in such a case, transmission will begin before a complete packet is stored in the FIFO.

An interrupt can be generated once the FIFO depth has fallen below a user-configured lower threshold as an indicator for the user to write more data. Interrupts can also be generated if the FIFO underflows while transmitting a packet when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort sequences (01111111 sequence where the 0 is transmitted first) can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified by the UDR register bit. An abort sequence will also be transmitted if the user overflows the FIFO with a packet of length greater than 128 bytes. Overflows where other complete packets are still stored in the FIFO will not generate an abort. Only the packet which caused the overflow is corrupted and an interrupt is generated to the user by the OVR register bit. The other packets remain unaffected.

When the TDPR is disabled, a logic one (Idle) is inserted in the PMDL.

10.18   SPLT SMDS PLCP Layer Transmitter

The SMDS PLCP Layer Transmitter (SPLT) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 based PLCP frame insertion.

The SPLT automatically inserts the framing (A1, A2) and path overhead identification (POHID) octets and provides registers or automatic generation of the F1, B1, G1, M2, M1, and C1 octets.

Registers are provided for the path user channel octet (F1) and the path status octet (G1). The bit interleaved parity octet (B1) and the FEBE subfield are automatically inserted.

The DQDB management information octets, M1 and M2 are generated. The type 0 and type 1 patterns described in TA-TSY-000772 are automatically inserted. The type 1 page counter may be reset using a register bit in the SPLT Configuration Register. Note: This feature is not required for the ATM Forum compliant DS3 UNI. For this application, the M1 and M2 octets must be set to all zeros.

The PLCP transmit frame C1 cycle/stuff counter octet and the transmit stuffing pattern can be referenced to the REF8KI input pin. Alternately, a fixed stuffing pattern may be inserted into the C1 cycle/stuff counter octet. A looped timing operating mode is provided where the transmit PLCP timing is derived from the received timing. In this mode, the C1 stuffing is generated based on the received stuffing pattern as determined by the SPLR block. When DS1 or E1 PLCP format is enabled, the pattern 00H is inserted.

When DS3 PLCP format is enabled, the C1 octet indicates the phase of the 375 µs nibble stuffing opportunity cycle. During frame one of the three frame cycle, the pattern FFH is inserted in the C1 octet, indicating a 13 nibble trailer length. During frame two, the pattern 00H is inserted, indicating a 14 nibble trailer length. During frame three, the pattern 66H or 99H is inserted, indicating a 13 or 14 nibble trailer length respectively.

When configured for G.751 E3 PLCP frame format, the C1 octet is used to indicate the number of octets stuffed in the trailer. The Table 5 shows the C1 octet pattern for each of the possible octet stuff lengths:

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Document ID: PMC-1990267, Issue 3

Table 5   C1 Octet Pattern

Stuff Length	C1(Hex)
17	3B
18	4F
19	75
20	9D
21	A7

The SPLT block generates a stuff length pattern of 18, 19, or 20 octets determined by the phase alignment of the start of the G.751 E3 frame and the start of the E3 PLCP frame. The REF8KI input is provisioned to loop time the PLCP transmit frame to an externally applied 8 kHz reference.

The Zn, growth octets are set to 00H. The Zn octets may be inserted from an external device via the path overhead stream input, TPOH.

10.19   TXCP-50 Transmit Cell Processor

The Transmit Cell Processor (TXCP-50) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP-50 scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells may also be scrambled. Note: Cell payload scrambling may be disabled in the S/UNI-JET, although it is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface. However, to ensure backwards compatibility with older equipment, the payload scrambling may be disabled.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP-50 inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48-octet information field is programmed with an 8-bit repeating pattern using an internal register.

10.20   TXFF Transmit FIFO

The Transmit FIFO (TXFF) provides FIFO management and the S/UNI-JET transmit cell interface. The transmit FIFO contains four cells. The FIFO depth may be programmed to four, three, two, or one cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

The general management functions of the TXFF include:

- Emptying cells from the transmit FIFO.

- Indicating when the transmit FIFO is full.

- Maintaining the transmit FIFO read and write pointers.

- Detecting a FIFO overrun condition.

The FIFO interface is "UTOPIA Level 2" compliant and accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, and the parity bit (TPRTY), and the ATM device address (TADR[4:0]) when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA and DTCA[4:1]), which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is logic zero) or when the FIFO is full (when TCALEVEL0 is logic one) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA and DTCA[x] indicates "full" can be set to one, two, three, or four cells by the FIFODP[1:0] bits of TXCP-50 Configuration 2 Register. If the programmed depth is less than four, more than one cell may be written after TCA or DTCA[x] is asserted as the TXCP-50 still allows four cells to be stored in its FIFO. This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA or DTCA[x] is logic zero are not processed. The TXFF automatically transmits idle cells until a full cell is available to be transmitted.

10.21 TTB Trail Trace Buffer

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream. The message is used by the OS to prevent delivery of traffic from the wrong source and is 16 bytes in length.

The 16-byte message is framed by the PTI Multiframe Alignment Signal (TMFAS = 'b10000000 00000000). One bit of the TMFAS is placed in the most significant bit of each message byte. In the receive direction, the trail trace message is extracted from the serial overhead stream output by the E3-FRMR. The extracted message is stored in the internal RAM for review by an external microprocessor. By default, the TTB will write the byte of a 16-byte message with its most significant bit set high to the first location in the RAM. The extracted trail trace message is checked for consistency between consecutive multiframes. A message received unchanged three or five times (programmable) is accepted for comparison with the copy previously written into the internal RAM by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched messages. In the transmit direction, the TTB sources the trail trace message from the internal RAM for insertion into the TR byte by the E3-TRAN.

The TTB also extracts the Payload Type label carried in the MA byte of the G.832 E3 stream. The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source. The Payload Type label is check for consistency between consecutive multiframes. A Payload Type label received unchanged for five frames is accepted for comparison with the copy previously written into the TTB by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

10.22 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE, and STCTEST instructions are supported.

The S/UNI-JET identification code is 073460CD hexadecimal.

10.23 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. Normal mode registers are required for normal operation. Test mode registers are used to enhance the testability of the S/UNI-JET.

With the exception of the S/UNI-JET Identification Register, all register descriptions can be found in the S/UNI-JET datasheet (PMC-1990267).

The register set is accessed as described in Table 6.

Table 6   Register Memory Map

Address	Register
000H-2FFH	Reserved
300H	S/UNI-JET Configuration 1
301H	S/UNI-JET Configuration 2
302H	S/UNI-JET Transmit Configuration
303H	S/UNI-JET Receive Configuration
304H	S/UNI-JET Data Link and FERF/RAI Control
305H	S/UNI-JET Interrupt Status
006H	S/UNI-JET Identification, Master Reset, and Global Monitor Update
306H	S/UNI-JET Reserved
307H	S/UNI-JET Clock Activity Monitor and Interrupt Identification
308H	SPLR Configuration
309H	SPLR Interrupt Enable
30AH	SPLR Interrupt Status
30BH	SPLR Status
30CH	SPLT Configuration
30DH	SPLT Control
30EH	SPLT Diagnostics and G1 Octet
30FH	SPLT F1 Octet
310H	PMON Change of PMON Performance Meters
311H	PMON Interrupt Enable/Status
312H-313H	PMON Reserved
314H	PMON LCV Event Count LSB
315H	PMON LCV Event Count MSB
316H	PMON Framing Bit Error Event Count LSB
317H	PMON Framing Bit Error Event Count MSB
318H	PMON Excessive Zeros Count LSB
319H	PMON Excessive Zeros Count MSB

Address	Register
31AH	PMON Parity Error Event Count LSB
31BH	PMON Parity Error Event Count MSB
31CH	PMON Path Parity Error Event Count LSB
31DH	PMON Path Parity Error Event Count MSB
31EH	PMON FEBE/J2-EXZS Event Count LSB
31FH	PMON FEBE/J2-EXZS Event Count MSB
320H	CPPM Reserved
321H	CPPM Change of CPPM Performance Meter
322H	CPPM BIP Error Count LSB
323H	CPPM BIP Error Count MSB
324H	CPPM PLCP Framing Error Event Count LSB
325H	CPPM PLCP Framing Error Event Count MSB
326H	CPPM PLCP FEBE Count LSB
327H	CPPM PLCP FEBE Count MSB
328H-32FH	CPPM Reserved
330H	DS3 FRMR Configuration
331H	DS3 FRMR Interrupt Enable
332H	DS3 FRMR Interrupt Status
333H	DS3 FRMR Status
334H	DS3 TRAN Configuration
335H	DS3 TRAN Diagnostics
336H-337H	DS3 TRAN Reserved
338H	E3 FRMR Framing Options
339H	E3 FRMR Maintenance Options
33AH	E3 FRMR Framing Interrupt Enable
33BH	E3 FRMR Framing Interrupt Indication and Status
33CH	E3 FRMR Maintenance Event Interrupt Enable
33DH	E3 FRMR Maintenance Event Interrupt Indication
33EH	E3 FRMR Maintenance Event Status
33FH	E3 FRMR Reserved
340H	E3 TRAN Framing Options
341H	E3 TRAN Status and Diagnostic Options
342H	E3 TRAN BIP-8 Error Mask
343H	E3 TRAN Maintenance and Adaptation Options
344H	J2 FRMR Configuration
345H	J2 FRMR Status
346H	J2 FRMR Alarm Interrupt Enable
347H	J2 FRMR Alarm Interrupt Status
348H	J2 FRMR Error/X-bit Interrupt Enable

Address	Register
349H	J2 FRMR Error/X-bit Interrupt Status
34AH-34BH	J2 FRMR Reserved
34CH	J2 TRAN Configuration
34DH	J2 TRAN Diagnostics
34EH	J2 TRAN TS97 Signaling
34FH	J2 TRAN TS98 Signaling
350H	RDLC Configuration
351H	RDLC Interrupt Control
352H	RDLC Status
353H	RDLC Data
354H	RDLC Primary Address Match
355H	RDLC Secondary Address Match
356H	RDLC Reserved
357H	RDLC Reserved
358H	TDPR Configuration
359H	TDPR Upper Transmit Threshold
35AH	TDPR Lower Interrupt Threshold
35BH	TDPR Interrupt Enable
35CH	TDPR Interrupt Status/UDR Clear
35DH	TDPR Transmit Data
35EH-35FH	TDPR Reserved
360H	RXCP-50 Configuration 1
361H	RXCP-50 Configuration 2
362H	RXCP-50 FIFO/UTOPIA Control & Config
363H	RXCP-50 Interrupt Enables and Counter Status
364H	RXCP-50 Status/Interrupt Status
365H	RXCP-50 LCD Count Threshold (MSB)
366H	RXCP-50 LCD Count Threshold (LSB)
367H	RXCP-50 Idle Cell Header Pattern
368H	RXCP-50 Idle Cell Header Mask
369H	RXCP-50 Corrected HCS Error Count
36AH	RXCP-50 Uncorrected HCS Error Count
36BH	RXCP-50 Received Cell Count LSB
36CH	RXCP-50 Received Cell Count
36DH	RXCP-50 Received Cell Count MSB
36EH	RXCP-50 Idle Cell Count LSB
36FH	RXCP-50 Idle Cell Count
370H	RXCP-50 Idle Cell Count MSB
371H-37FH	RXCP-50 Reserved

Address	Register
380H	TXCP-50 Configuration 1
381H	TXCP-50 Configuration 2
382H	TXCP-50 Transmit Cell Status
383H	TXCP-50 Interrupt Enable/Status
384H	TXCP-50 Idle Cell Header Control
385H	TXCP-50 Idle Cell Payload Control
386H	TXCP-50 Transmit Cell Counter LSB
387H	TXCP-50 Transmit Cell Counter
388H	TXCP-50 Transmit Cell Counter MSB
389H-38FH	TXCP-50 Reserved
390H	TTB Control Register
391H	TTB Trail Trace Identifier Status
392H	TTB Indirect Address Register
393H	TTB Indirect Data Register
394H	TTB Expected Payload Type Label Register
395H	TTB Payload Type Label Control/Status
396H-397H	TTB Reserved
398H	RBOC Configuration/Interrupt Enable
399H	RBOC Status
39AH	XBOC Code
39BH	S/UNI-JET Misc.
39CH	S/UNI-JET FRMR LOF Status.
3A0H	PRGD Control
3A1H	PRGD Interrupt Enable/Status
3A2H	PRGD Length
3A3H	PRGD Tap
3A4H	PRGD Error Insertion
3A5H-3A7H	PRGD Reserved
3A8H	PRGD Pattern Insertion Register #1
3A9H	PRGD Pattern Insertion Register #2
3AAH	PRGD Pattern Insertion Register #3
3ABH	PRGD Pattern Insertion Register #4
3ACH	PRGD Pattern Detector Register #1
3ADH	PRGD Pattern Detector Register #2
3AEH	PRGD Pattern Detector Register #3
3AFH	PRGD Pattern Detector Register #4
3B0H-3FFH	S/UNI-JET Reserved
400H	S/UNI-JET Master Test Register
401H-40BH	Reserved for S/UNI-JET Test

Address	Register
40CH	S/UNI-JET Identification Register
40DH - 7FFH	Reserved for S/UNI-JET Test

Notes

1. For all register accesses, CSB must be low.

2. Writing any value to any of the PMON(314H to 31FH), RXCP-50(369H to 370H) or TXCP-50(386H to 388H) counter holding registers will latch the current count value to the holding registers. To ensure that the transfer was completed a wait function must be performed via software as indicated by the specific count registers being latched. Each of the above mentioned registers have a specified clock cycle completion requirement that is stated in the specific count registers description. For example the LCV PMON count of registers 314H and 315H specifies that it takes three RCLK cycles to complete a transfer of the current count value to the count holding registers. Other registers may specify a different clock cycle requirement for the three different operational modes of the JET: DS3, E3 and J2.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the S/UNI-JET . Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

- Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

- All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-JET to determine the programming state of the block.

- Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

- Writing into read-only normal mode register bit locations does not affect S/UNI-JET operation unless otherwise noted.

- Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-JET operates as intended, reserved register bits must only be written with the suggested logic levels. Similarly, writing to reserved registers should be avoided.

- The S/UNI-JET requires a software initialization sequence in order to guarantee proper device operation and long term reliability. Please refer to Section 13.1 of this document for the details on how to program this sequence.

Register 300H: S/UNI-JET Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	8KREFO	1
Bit 6	R/W	DS27_53	1
Bit 5	R/W	TOCTA	0
Bit 4	R/W	FRMRONLY	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	LLOOP	0
Bit 1	R/W	DLOOP	0
Bit 0	R/W	PLOOP	0

PLOOP

The PLOOP bit controls the DS3, E3, or J2 payload loopback. When a logic zero is written to PLOOP, DS3, E3, or J2 payload loopback is disabled. When a logic one is written to PLOOP, the DS3, E3, or J2 overhead bits are regenerated and inserted into the received DS3, E3, or J2 stream and the resulting stream is transmitted. Setting the PLOOP bit disables the effect of the TICLK bit in the S/UNI-JET Transmit Configuration Register, thereby forcing flow-through timing. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-JET Transmit Configuration and Receive Configuration Registers, respectively, must be set to the same value for PLOOP to work properly.

DLOOP

The DLOOP bit controls the diagnostic loopback. When a logic zero is written to DLOOP, diagnostic loopback is disabled. When a logic one is written to DLOOP, the transmit data stream is looped in the receive direction. The TFRM[1:0] and RFRM[1:0] bits in the S/UNI-JET Transmit Configuration and Receive Configuration Registers, respectively, must be set to the same value for DLOOP to work properly. The DLOOP should not be set to a logic one when either the PLOOP, LLOOP, or LOOPT bit is a logic one. When in DS3, E3, or J2 modes, the TUNI register bit in the S/UNI-JET Transmit Configuration Register should be set to the same value as the UNI bit in the DS3, E3, or J2 FRMR Registers.

LLOOP

The LLOOP bit controls the line loopback. When a logic zero is written to LLOOP, line loopback is disabled. When a logic one is written to LLOOP, the stream received on RPOS/RDATI and RNEG/RLCV/ROHM is looped to the TPOS/TDATO and TNEG/TOHM outputs. Note: The TPOS, TNEG, and TCLK outputs are referenced to RCLK when LLOOP is logic one.

LOOPT

The LOOPT bit selects the transmit timing source. When a logic one is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock (RCLK) is used as the transmit timing source. The transmit nibble stuffing is derived from the nibble stuffing in the receive PLCP frame (for DS3 or E3 PLCP frame transmission). The FIXSTUFF bit must be set to logic zero if the LOOPT bit is set to logic one. When a logic zero is written to LOOPT, the transmit clock (TICLK) is used as the transmit timing source. The nibble stuffing is derived from the REF8KI input, or is fixed internally as determined by the FIXSTUFF bit in the SPLT Configuration Register (for DS3 or E3 PLCP frame transmission only). Setting the LOOPT bit disables the effect of the TICLK and TXREF bits in the S/UNI-JET Transmit Configuration and S/UNI-JET Configuration 2 Registers respectively, thereby forcing flow-through timing.

FRMRONLY

The FRMRONLY bit controls whether the S/UNI-JET is operating solely as a DS3, E3, or J2 framer/transmitter. If FRMRONLY is set to logic one, the PLCP, and ATM blocks are disabled and the RDATO, REF8KO/RFPO/RMFPO, RSCLK, ROVRHD, TFPO/TMFPO, TFPI/TMFPI, and TDATI I/O pins are enabled. The ATM interface inputs are ignored and the outputs are tri-stated. If FRMRONLY is set to logic zero, the PLCP and ATM blocks are enabled and the LCD, RPOH, RPOHCLK, RPOHFP, TPOH, TIOHM, and TPOHFP I/O pins are enabled and the ATM interface inputs and outputs are enabled.

TOCTA

The TOCTA bit enables octet-alignment or nibble-alignment of the transmit cell stream to the transmission overhead when the arbitrary transmission format is chosen (TFRM[1:0] = 11 binary and SPLT Configuration register bit EXT = 1). This bit has no effect when DS3, G.751 E3, G.832 E3, J2, T1, or E1 formats are selected since octet or nibble alignment is specified for these formats. When the arbitrary transmission format is chosen and TOCTA is set to logic one, the ATM cell nibbles or octets are aligned to the arbitrary transmission format overhead boundaries (as set by the TIOHM input). Nibble alignment is chosen if the FORM[1:0] bits in the SPLT Configuration are set to 00. Byte alignment is chosen if these FORM[1:0] bits are set to any other value. The number of TICLK periods between transmission format overhead bit positions must be divisible by four (for nibble alignment) or eight (for byte alignment). When TOCTA is set to logic zero, no octet alignment is performed , and there is no restriction on the number of TICLK periods between transmission format overhead bit positions.

DS27_53

The DS27_53 bit is used to select between the long data structure (27-byte words in 16-bit mode and 53-byte words in 8-bit mode) and the short data structure (26-byte words in 16-bit mode and 52-byte words in 8-bit mode) on the ATM interface. When DS27_53 is set to logic one, the RXCP-50 and TXCP-50 blocks are configured to operate with the long data structure; when DS27_53 is set to logic zero, the RXCP-50 and TXCP-50 are configured to operate with the short data structure.

8KREFO

The 8KREFO bit is used, in conjunction with the PLCPEN bit in the SPLR Configuration Register to select the function of the REF8KO/RPOHFP/RFPO/RMFPO[x] output pin. When PLCPEN is logic one, the RPOHFP function will be selected and 8KREFO has no effect. (Note: RPOHFP is inherently an 8kHz reference). If PLCPEN is logic zero and if 8KREFO becomes logic one, then an 8 kHz reference will be derived from the RCLK[x] signal and output on REF8KO. If 8KREFO and PLCPEN are both logic zero, then the RXMFPO register bit in the S/UNI-JET Configuration 2 Register will select either the RFPO or RMFPO function.

Register 301H: S/UNI-JET Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	STATSEL[2]	0
Bit 6	R/W	STATSEL[1]	0
Bit 5	R/W	STATSEL[0]	0
Bit 4	R/W	TXMFPI	0
Bit 3	R/W	TXGAPEN	0
Bit 2	R/W	RXGAPEN	0
Bit 1	R/W	TXMFPO	0
Bit 0	R/W	RXMFPO	0

RXMFPO

The RXMFPO bit controls which of the outputs RMFPO or RFPO is valid. If RXMFPO is a logic one, then RMFPO will be available. If RXMFPO is a logic zero, then RFPO will be available. This bit is effective only if the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is a logic one.

TXMFPO

The TXMFPO bit controls which of the outputs TMFPO[4:1] or TFPO[4:1] is valid. If TXMFPO is a logic one, then TMFPO[4:1] will be available. If TXMFPO is a logic zero, then TFPO[4:1] will be available. This bit is effective only if the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is a logic one. The TXGAPEN bit takes precedence over the TXMFPO bit.

RXGAPEN

The RXGAPEN bit configures the S/UNI-JET to enable the RGAPCLK[x] outputs. When RXGAPEN is a logic one, then the RGAPCLK[x] output is enabled. When RXGAPEN is a logic zero, then the RSCLK[x] output is enabled. The FRMRONLY register bit must be a logic one for RXGAPEN to have effect.

TXGAPEN

The TXGAPEN bit configures the S/UNI-JET to enable the TGAPCLK[x] outputs. When TXGAPEN is a logic one, the TGAPCLK[x] output is enabled. When TXGAPEN is a logic zero, then either the TFPO[x] or TMFPO[x] output is enabled, depending on the setting of the TXMFPO register bit. The FRMRONLY register bit must be a logic one for TXGAPEN to have effect.

TXMFPI

The TXMFPI bit controls which of the inputs TMFPI or TFPI is valid. If TXMFPI is a logic one, then TMFPI will be expected. If TXMFPI is a logic zero, then TFPI will be expected. This bit is effective only if the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is a logic one.

STATSEL[2:0]

The STATSEL[2:0] bits are used to select the function of the FRMSTAT output. The selection is shown in Table 7:

Table 7   STATSEL[2:0] Options

STATSEL[2:0]	FRMSTAT output pin indication function
000	E3/DS3 LOF or J2 extended LOF (integration periods are selected by the LOFINT[1:0] register bits in the S/UNI-JET Receive Configuration Register)
001	PLCP LOF
010	E3/DS3 OOF or J2 LOF
011	PLCP OOF
100	AIS
101	LOS
110	DS3 Idle
111	Reserved

Register 302H: S/UNI-JET Transmit Configuration

Bit	Type	Function	Default
Bit 7	R/W	TFRM[1]	0
Bit 6	R/W	TFRM[0]	0
Bit 5	R/W	TXREF	0
Bit 4	R/W	TICLK	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	TCLKINV	0
Bit 1	R/W	TPOSINV	0
Bit 0	R/W	TNEGINV	0

TNEGINV

The TNEGINV bit provides polarity control for outputs TNEG/TOHM. When a logic zero is written to TNEGINV, the TNEG/TOHM output is not inverted. When a logic one is written to TNEGINV, the TNEG/TOHM output is inverted. The TNEGINV bit setting does not affect the loopback data in diagnostic loopback.

TPOSINV

The TPOSINV bit provides polarity control for outputs TPOS/TDATO. When a logic zero is written to TPOSINV, the TPOS/TDATO output is not inverted. When a logic one is written to TPOSINV, the TPOS/TDATO output is inverted. The TPOSINV bit setting does not affect the loopback data in diagnostic loopback.

TCLKINV

The TCLKINV bit provides polarity control for output TCLK. When a logic zero is written to TCLKINV, TCLK is not inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the falling edge of TCLK. When a logic one is written to TCLKINV, TCLK is inverted and outputs TPOS/TDATO and TNEG/TOHM are updated on the rising edge of TCLK.

TUNI

The TUNI bit enables the S/UNI-JET to transmit unipolar or bipolar DS3, E3, or J2 data streams. When a logic one is written to TUNI, the S/UNI-JET transmits unipolar DS3, E3, or J2 data on TDATO. When TUNI is logic one, the TOHM output indicates the start of the DS3 M-Frame (the X1 bit), the start of the E3 frame (bit 1 of the frame), or the first framing bit of the J2 multiframe. When a logic zero is written to TUNI, the S/UNI-JET transmits B3ZS-encoded DS3 data, HDB3-encoded E3 data, or B8ZS-encoded J2 data on TPOS and TNEG. The TUNI bit has no effect if TFRM[1:0] is set to 11 binary as the output data is automatically configured for unipolar format.

TICLK

The TICLK bit selects the transmit clock used to update the TPOS/TDATO and
TNEG/TOHM outputs. When a logic zero is written to TICLK, the buffered version of the
input transmit clock, TCLK, is used to update TPOS/TDATO and TNEG/TOHM on the edge
selected by the TCLKINV bit. When a logic one is written to TICLK, TPOS/TDATO and
TNEG/TOHM are updated on the rising edge of TICLK, eliminating the flow-through TCLK
signal. The TICLK bit has no effect if the LOOPT, LLOOP, or PLOOP bit is a logic one.

TXREF

The TXREF register bit determines if TICLK[1] and TIOHM/TFPI/TMFPI[1] should be used
as the reference transmit clock and overhead/frame pulse, respectively, instead of TICLK and
TIOHM/TFPI/TMFPI. If TXREF is set to a logic one, then TICLK[1] and
TIOHM/TFPI/TMFPI[1] will be used as the reference transmit clock and overhead/frame
pulse, respectively. If TXREF is set to a logic zero, then TICLK and TIOHM/TFPI/TMFPI
will be used as the reference transmit clock and overhead/frame pulse, respectively, for
quadrant X. If loop-timing is enabled (LOOPT = 1), the TXREF bit has no effect on the
corresponding quadrant. Note: When TXREF is set to logic one, the unused TICLK and
TIOHM/TFPI/TMFPI should be tied to power or ground, not left floating.

TFRM[1:0]

The TFRM[1:0] bits determine the frame structure of the transmitted signal. Refer to Table 8:

Table 8   TFRM[1:0] Transmit Frame Structure Configurations

TFRM[1:0]	Transmit Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBIT bit in the DS3 TRAN Configuration Register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 TRAN Framing Options Register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format - If the EXT bit in the SPLT Configuration Register is a logic zero, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLT Configuration Register) and TIOHM should be tied low. If EXT is a logic one, then the arbitrary framing format is selected and overhead positions are indicated by the TIOHM input pin.

Register 303H: S/UNI-JET Receive Configuration

Bit	Type	Function	Default
Bit 7	R/W	RFRM[1]	0
Bit 6	R/W	RFRM[0]	0
Bit 5	R/W	LOFINT[1]	0
Bit 4	R/W	LOFINT[0]	0
Bit 3	R/W	RSCLKR	0
Bit 2	R/W	RCLKINV	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RNEGINV	0

RNEGINV

The RNEGINV bit provides polarity control for input RNEG/RLCV/ROHM. When a logic zero is written to RNEGINV, the input RNEG/RLCV/ROHM is not inverted. When a logic one is written to RNEGINV, the input RNEG/RLCV/ROHM is inverted. The RNEGINV bit setting does not affect the loopback data in diagnostic loopback.

RPOSINV

The RPOSINV bit provides polarity control for input RPOS/RDATI. When a logic zero is written to RPOSINV , the input RPOS/RDATI is not inverted. When a logic one is written to RPOSINV , the input RPOS/RDATI is inverted. The RPOSINV bit setting does not affect the loopback data in diagnostic loopback.

RCLKINV

The RCLKINV bit provides polarity control for input RCLK. When a logic zero is written to RCLKINV, RCLK is not inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the rising edge of RCLK. When a logic one is written to RCLKINV, RCLK is inverted and inputs RPOS/RDATI and RNEG/RLCV/ROHM are sampled on the falling edge of RCLK.

RSCLKR

The RSCLKR bit is in effect only when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set to logic one. When RSCLKR is a logic one, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the rising edge of RSCLK. When RSCLKR is a logic zero, the RDATO, RFPO/RMFPO, and ROVRHD outputs are updated on the falling edge of RSCLK. If the RXGAPEN bit is a logic one, then RSCLKR affects RGAPCLK in the same manner as it affects RSCLK.

LOFINT[1:0]

The LOFINT[1:0] bits determine the integration period used for asserting and de-asserting E3 and DS3 LOF or J2 extended LOF on the FRMLOF register bit of the S/UNI-JET FRMR LOF Status Register (x9CH) and on the FRMSTAT[4:1] output pins (if this function is enabled by the STATSEL[2:0] register bits of the S/UNI-JET Configuration 2 Register). The integration times are selected as shown in Table 9:

Table 9 LOF[1:0] Integration Period Configuration

LOFINT[1:0]	Integration Period
00	3 ms
01	2 ms
10	1 ms
11	Reserved

RFRM[1:0]

The RFRM[1:0] bits determine the expected frame structure of the received signal. Refer to Table 10:

Table 10 RFRM[1:0] Receive Frame Structure Configurations

RFRM[1:0]	Expected Receive Frame Structure
00	DS3 (C-bit parity or M23 depending on the setting of the CBE bit in the DS3 FRMR Configuration Register)
01	E3 (G.751 or G.832 depending on the setting of the FORMAT[1:0] bits in the E3 FRMR Framing Options Register)
10	J2 (G.704 and NTT compliant framing format)
11	DS1/E1/Arbitrary framing format (When EXT in the SPLR Configuration Register is a logic zero, then DS1 or E1 direct-mapped or PLCP framing is selected (via the PLCPEN and FORM[1:0] bits in the SPLR Configuration Register) and the frame alignment is indicated by the ROHM[x] input pin. When EXT is a logic one, then the arbitrary framing format is selected and overhead bit positions are indicated by the ROHM[x] input pin.)

Register 304H: S/UNI-JET Data Link and FERF/RAI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEN	1
Bit 6	R/W	AISEN	1
Bit 5	R/W	RBLEN	1
Bit 4	R/W	OOFEN	1
Bit 3	R/W	LOSEN	1
Bit 2	R/W	TNETOP	0
Bit 1	R/W	RNETOP	0
Bit 0	R/W	DLINV	0

DLINV

> The DLINV bit provides polarity control for the DS3 C-bit Parity PMDL, which is located in the three C-bits of M-subframe 5. When a logic one is written to DLINV, the PMDL is inverted before being processed. The rationale behind this bit is to safe-guard the S/UNI-JET in case the inversion is required in the future. Currently, the ANSI standard T1.107 specifies that the C-bits, which carry the PMDL, be set to all-zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all-zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully.

RNETOP

> The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RDLC. When RNETOP is logic one, the NR byte is extracted from the G.832 stream and terminated by RDLC. When RNETOP is logic zero, the GC byte is extracted from the G.832 stream and terminated by RDLC. Both the NR byte and the GC byte are extracted and output on the ROH pin for external processing.

TNETOP

> The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, TDPR. When TNETOP is logic one, the NR byte is inserted into the G.832 stream through the TDPR block; the GC byte of the G.832 E3 stream is sourced by through the TOH and TOHINS pins. If TOH and TOHINS are not active, then an all-ones signal will be inserted into the GC byte. When TNETOP is logic zero, the GC byte is inserted into the G.832 stream through the TDPR block; the NR byte of the G.832 E3 stream is sourced by the TOH and TOHINS pins. If TOH and TOHINS are not active, then an all-ones signal will be inserted into the NR byte.

For G.751 E3 streams, the National Use bit is sourced by the TDPR block if TNETOP and the NATUSE bit (from the E3 TRAN Configuration Register 341H) are both logic zero. If either TNETOP or NATUSE is logic one, the National Use bit will be sourced from the NATUSE register bit in Register 341H.

If the S/UNI-JET is configured for DS3 or J2 operation, TNETOP has no effect. The DS3 C-bit Parity and J2 datalink is inserted into the DS3 or J2 stream through the internal HDLC transmitter TDPR.

The TOH and TOHINS input pins can be used to overwrite the values of these overhead bits in the transmit stream.

LOSEN

The LOSEN bit enables the receive LOS indication to automatically generate a FERF indication in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When LOSEN is logic one, assertion of the LOS indication by the framer causes a FERF (RAI in G.751 or J2 mode) to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic zero, assertion of the LOS indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code Register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

OOFEN

The OOFEN bit enables the receive OOF indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates when the E3 or J2 framer is selected or when the DS3 framer is selected and the RBLEN bit is logic zero. When OOFEN is logic one, assertion of the OOF indication by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic zero, assertion of the OOF indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code Register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

RBLEN

The RBLEN bit enables: the receive RED alarm (persistent OOF) indication to automatically generate a FERF indication in the DS3 transmit stream, or a BIP8 error detection in the E3 G.832 Framer to generate a FEBE indication in the E3 G.832 transmit stream, or an LOF to generate a RLOF indication (A-bit) in the J2 transmit stream. When the E3 G.751 framer is selected, this bit has no effect.

When RBLEN is logic one, TFRM[1:0] is 00 binary, and RFRM[1:0] is 00 binary, assertion of the RED indication by the framer causes a FERF to be transmitted by DS3_TRAN for the duration of the RED assertion. Also, for DS3 frame format, the OOFEN bit is internally forced to logic zero when RBLEN is logic one. When RBLEN is logic zero, assertion of the RED indication does not cause transmission of a FERF.

When RBLEN is logic one, TFRM[1:0] is 01 binary, and RFRM[1:0] is 01 binary, any BIP8 error indication by the E3 G.832 framer causes a FEBE to be generated by the E3 G.832 TRAN. When RBLEN is logic zero, BIP8 errors detected by the E3 framer do not cause FEBEs to be generated by the E3_TRAN.

When RBLEN is logic one, TFRM[1:0] is 10 binary, and RFRM[1:0] is 10 binary, any LOF error indication by the J2 framer causes the RLOF bit (also known as the A bit) to be set in the J2 transmit stream. When RBLEN is logic zero, LOF errors detected by the J2 framer do not cause the RLOF bit to be set in the transmit stream.

AISEN

The AISEN bit enables the RAI signal to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2). When AISEN is logic one, assertion of the AIS indication (physical AIS for J2) by the framer causes a FERF/RAI to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic zero, assertion of the AIS indication does not cause transmission of a FERF/RAI.

Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code Register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

LCDEN

The LCDEN bit enables the receive-out-of-cell-delineation indication to automatically generate a FERF indication (RAI in G.751 or J2 mode) in the transmit stream. This bit operates regardless of framer selected (DS3, E3, or J2) but only in ATM mode. When LCDEN is logic one, assertion of the LCD indication by the receive FIFO causes a FERF/RAI to be transmitted by the transmitter for the duration of the LCD assertion. When LCDEN is logic zero, assertion of the LCD indication does not cause transmission of a FERF/RAI. Note: For the RAI to be automatically transmitted when in J2 format, the FEAC[5:0] bits in the XBOC Code Register must all be set to logic one. If the XBOC FEAC code is to be transmitted in J2 mode, LOSEN, OOFEN, AISEN, and LCDEN should all be set to logic zero.

Register 305H: S/UNI-JET Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPLRI/TTBI	X
Bit 6	R	TXCP50I	X
Bit 5	R	RXCP50I	X
Bit 4	R	RBOCI/PRGDI	X
Bit 3	R	FRMRI/LOFI	X
Bit 2	R	PMONI	X
Bit 1	R	TDPRI	X
Bit 0	R	RDLCI	X

SPLRI/TTBI, TXCP50I, RXCP50I, RBOCI/PRGDI, FRMRI/LOFI, PMONI, TDPRI, RDLCI

These bits are interrupt status indicators that identify the block that is the source of a pending interrupt. The SPLRI/TTBI bit will be logic one if either the SPLR or the TTB block has produced the interrupt. The RBOCI/PRGDI bit will be logic one if either the RBOC or PRGD block has produced the interrupt. The FRMRI/LOFI will be logic one if either the FRMR (J2, E3, or T3 - whichever one is enabled) or the E3, T3, or J2 Extended LOF signal (FRMLOFI from Register x9CH) is the source of the interrupt. This register is typically used by interrupt service routines to determine the source of a S/UNI-JET interrupt.

Register 006H: S/UNI-JET Identification, Master Reset, and Global Monitor Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	1
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	0
Bit 3	R	TYPE[0]	0
Bit 2	R	Unused	X
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register is used for global performance monitor updates, global software resets, and for device identification. Writing any value except 80H into this register initiates latching of all performance monitor counts in the PMON, RXCP-50, and TXCP-50 blocks in all four quadrants of the S/UNI-JET. The TIP register bit is used to signal when the latching is complete.

The CPPM Counter Registers are *not* latched by writing to Register 006H. Counters in the CPPM can only be updated by writing to CPPM register addresses (322H – 32FH).

ID[1:0]

The ID[1:0] bits allows software to identify the version level of the S/UNI-JET.

TYPE[3:0]

The TYPE[3:0] bits allow software to identify this device as the S/UNI-JET member of the S/UNI family of products.

RESET

The RESET bit allows software to asynchronously reset the S/UNI-JET. The software reset is equivalent to setting the RSTB input pin low, except that the S/UNI-JET Master Test Register is not affected. When a logic one is written to RESET, the S/UNI-JET is reset. When a logic zero is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

Register 307H: S/UNI-JET Clock Activity Monitor and Interrupt Identification

Bit	Type	Function	Default
Bit 7	R	INT	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RCLKA	X
Bit 2	R	TICLKA	X
Bit 1	R	TFCLKA	X
Bit 0	R	RFCLKA	X

RFCLKA

The RFCLKA bit monitors for low-to-high transitions on the RFCLK input. RFCLKA is set low when this register is read and is set high on a rising edge of RFCLK.

TFCLKA

The TFCLKA bit monitors for low-to-high transitions on the TFCLK input. TFCLKA is set low when this register is read and is set high on a rising edge of TFCLK.

TICLKA

The TICLKA bit monitors for low-to-high transitions on the TICLK input. TICLKA is set low when this register is read and is set high on a rising edge of TICLK.

RCLKA

The RCLKA bit monitors for low-to-high transitions on the RCLK input. RCLKA is set low when this register is read and is set high on a rising edge of RCLK.

INT

When the INT bit is set to logic one, the S/UN-JET has generated the interrupt. The particular block(s) the device that generated the interrupt can be identified by reading the S/UNI-JET Interrupt Status Register. When the INT bit is set to logic zero, then the device has not generated an interrupt. Note: The INT bit is valid only in register address 307H.

Register 308H: SPLR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REFRAME	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter to be supported using the ROHM[x] input. When a logic zero is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter is synchronized to the transmission system frame alignment using the ROHM[x] (for DS1 or E1 ATM direct-mapped formats), or by the integral framer block (for the DS3, J2, E3 G.751, or E3 G.832 formats).

When a logic one is written to EXT, indications on ROHM identify each transmission system overhead bit.

PLCPEN

The PLCPEN bit enables PLCP framing. When a logic one is written to PLCPEN, PLCP framing is enabled. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic zero is written to PLCPEN, PLCP related functions in the SPLR block are disabled. PLCPEN must be programmed to logic zero for E3 G.832, J2, and arbitrary framing formats.

REFRAME

The REFRAME bit is used to trigger reframing. When a logic one is written to REFRAME, the S/UNI-JET is forced out of PLCP frame and a new search for frame alignment is initiated. Note: Only a logic zero to logic one transition of the REFRAME bit triggers reframing; multiple write operations are required to ensure such a transition.

Reserved

All Reserved bits must be set to logic zero for proper operation.

FORM[1:0]

The FORM[1:0] bits select the PLCP frame format as shown below. These bits must be set to "11" if E1 direct mapped mode is being used (PLCPEN=0 and EXT=1). Refer to Table 11.

Table 11   SPLR FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	E3 G.751
1	0	DS1
1	1	E1

Register 309H: SPLR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FEBEE	0
Bit 5	R/W	COLSSE	0
Bit 4	R/W	BIPEE	0
Bit 3	R/W	FEE	0
Bit 2	R/W	YELE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit enables interrupt generation when a PLCP OOF defect is declared or removed. The interrupt is enabled when a logic one is written.

LOFE

The LOFE bit enables interrupt generation when a PLCP LOF defect is declared or removed. The interrupt is enabled when a logic one is written.

YELE

The YELE bit enables interrupt generation when a PLCP yellow alarm defect is declared or removed. The interrupt is enabled when a logic one is written.

FEE

The FEE bit enables interrupt generation when the S/UNI-JET detects a PLCP framing octet error. The interrupt is enabled when a logic one is written.

BIPEE

The BIPEE bit enables interrupt generation when the S/UNI-JET detects a PLCP bit interleaved parity error. The interrupt is enabled when a logic one is written.

COLSSE

The COLSSE bit enables interrupt generation when the S/UNI-JET detects a change of PLCP link status. The interrupt is enabled when a logic one is written.

FEBEE

The FEBEE bit enables interrupt generation when the S/UNI-JET detects a PLCP FEBE. The interrupt is enabled when a logic one is written.

Register 30AH: SPLR Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FEBEI	X
Bit 5	R	COLSSI	X
Bit 4	R	BIPEI	X
Bit 3	R	FEI	X
Bit 2	R	YELI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The OOFI bit is set to logic one when a PLCP OOF defect is detected or removed. The OOF defect state is contained in the SPLR Status Register. The OOFI bit position is set to logic zero when this register is read.

LOFI

The LOFI bit is set to logic one when a PLCP LOF defect is detected or removed. The LOF defect state is contained in the SPLR Status Register. The LOFI bit position is set to logic zero when this register is read.

YELI

The YELI bit is set to logic one when a PLCP yellow alarm defect is detected or removed. The yellow alarm defect state is contained in the SPLR Status Register. The YELI bit position is set to logic zero when this register is read.

FEI

The FEI bit is set to logic one when a PLCP framing octet error is detected. A framing octet error is generated when one or more errors are detected in the framing alignment octets (A1, and A2), or the path overhead identification octets. The FEI bit position is set to logic zero when this register is read.

BIPEI

The BIPEI bit is set to logic one when a PLCP bit interleaved parity (BIP) error is detected. BIP errors are detected using the B1 byte in the PLCP path overhead. The BIPEI bit position is set to logic zero when this register is read.

COLSSI

The COLSSI bit is set to logic one when a PLCP change of link status signal code is detected. The link status signal code is contained in the path status octet (G1). Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. A change of link status event occurs when two consecutive and identical link status codes are received that differ from the current code. The COLSSI bit position is set to logic zero when this register is read.

FEBEI

The FEBEI bit is set to logic one when a PLCP FEBE (FEBE) is detected. FEBE errors are indicated in the PLCP path status octet (G1). The FEBEI bit position is set to logic zero when this register is read.

Register 30BH: SPLR Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LSS[2]	X
Bit 5	R	LSS[1]	X
Bit 4	R	LSS[0]	X
Bit 3		Unused	X
Bit 2	R	YELV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit indicates the current PLCP OOF defect state. When an error is detected in both the A1 and A2 octets or when an error is detected in two consecutive path overhead identifier octets, OOFV is set to logic one. When the S/UNI-JET has found two valid, consecutive sets of A1 and A2 octets with two valid and sequential path overhead identifier octets, the OOFV bit is set to logic zero.

LOFV

The LOFV bit indicates the current PLCP LOF defect state. The LOF defect state is an integrated version of the OOF defect state. The declaration/removal times for the LOF defect state depends on the selected PLCP format. These are summarized in Table 12:

Table 12   PLCP LOF Declaration/Removal Times

PLCP Format	Declaration (ms)	Removal (ms)
DS3	1	12
E3 G.751	1.12	10
DS1	25	250
E1	20	200

If the OOF defect state is transient, the LOF counter is decremented at a rate 1/12 (DS3 PLCP) or 1/10 (DS1 or E1 PLCP) or 1/9 (G.751 E3 PLCP) of the incrementing rate.

YELV

The YELV bit indicates the current PLCP yellow alarm defect state. YELV is set to a logic one when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic one. YELV is set to a logic zero when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic zero.

LSS[2:0]

The LSS[2:0] bits contain the current link status signal code. Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. LSS[2:0] is updated when two consecutive and identical link status signal codes are received.

Register 30CH: SPLT Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	M1TYPE	0
Bit 4	R/W	M2TYPE	0
Bit 3	R/W	FIXSTUFF	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT

The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, J2, E3 G.751, or E3 G.832 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter and must be supported using the TIOHM input. When a logic zero is written to EXT, input transmission system overhead (for DS1, DS3, E1, J2, E3 G.751, and E3 G.832 formats) is indicated using the internal timeslot counter. This counter "flywheels" to create the appropriate transmission system alignment. This alignment is indicated on the TOHM output. When a logic one is written to EXT, indications on TIOHM identify each transmission system overhead bit. These indications flow through the S/UNI-JET and appear on the TOHM output where they mark the transmission system overhead placeholder positions in the TDATO stream. EXT should only be set to logic one if the TFRM[1:0] bits in the S/UNI-JET Transmit Configuration Register are both set to logic one and the arbitrary framing format is desired.

PLCPEN

The PLCPEN bit enables PLCP frame insertion. When a logic one is written to PLCPEN, DS3, E3 G.751, DS1, or E1 PLCP framing is inserted. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic zero is written to PLCPEN, PLCP related functions in the SPLT block are disabled. The PLCPEN bit must be set to logic zero for G.832 E3, J2, and arbitrary framing formats.

FIXSTUFF

The FIXSTUFF bit controls the transmit PLCP frame octet/nibble stuffing used for DS3 and G.751 E3 PLCP frame formats. When a logic zero is written to FIXSTUFF, stuffing is determined by the REF8KI input. When a logic one is written to FIXSTUFF and the DS3 PLCP frame format is enabled, a nibble is stuffed into the 13 nibble trailer twice every three stuff opportunities (i.e. 13, 14, 14 nibbles). This stuff ratio provides for a nominal PLCP frame rate of 125.0002366 μs (an error of 1.9 ppm). When the G.751 E3 PLCP frame format is enabled, 18, 19 or 20 octets are stuffed into the trailer depending on the alignment of the G.751 E3 frame, and the G.751 E3 PLCP frame. This yields a nominal PLCP frame rate of 125 μs.

M2TYPE

The M2TYPE bit selects the type of code transmitted in the M2 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic zero is written to M2TYPE, the fixed pattern type 0 code is transmitted in the M2 octet. When a logic one is written to M2TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M2 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

M1TYPE

The M1TYPE bit selects the type of code transmitted in the M1 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic zero is written to M1TYPE, the fixed pattern type 0 code is transmitted in the M1 octet. When a logic one is written to M1TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M1 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

FORM[1:0]

When EXT = 0 and PLCPEN = 0, the FORM[1:0] bits and the TFRM[1:0] bits in the S/UNI-JET Transmit Configuration Register select the ATM direct-mapped transmission frame format as shown below. When EXT = 0 and PLCPEN = 1, the FORM[1:0] bits along with the TFRM[1:0] bits select the transmission and PLCP frame format as shown below. When EXT = 1 and TOCTA = 1, then the FORM[1:0] bits control the cell alignment with respect to the transmission overhead given on TIOHM as shown in Table 13. The FORM bits have no effect if EXT = 1 and TOCTA = 0.

Table 13 SPLT FORM[1:0] Configurations

FORM[1]	FORM[0]	PLCP or ATM direct-mapped Framing Format / Cell alignment
0	0	DS3 / nibble
0	1	E3 or J2 / byte

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FORM[1]	FORM[0]	PLCP or ATM direct-mapped Framing Format / Cell alignment
1	0	DS1 / byte
1	1	E1 / byte

Register 30DH: SPLT Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SRCZN	0
Bit 5	R/W	SRCF1	0
Bit 4	R/W	SRCB1	0
Bit 3	R/W	SRCG1	0
Bit 2	R/W	SRCM1	0
Bit 1	R/W	SRCM2	0
Bit 0	R/W	SRCC1	0

SRCC1

The SRCC1 bit value ORed with input TPOHINS selects the source for the C1 octet on a bit by bit basis. If the OR results in a logic zero, the C1 bit position is derived internally as specified by the FIXSTUFF bit in the SPLT Configuration Register. If the OR results in a logic one, the C1 bit position is inserted with the value sampled on TPOH.

SRCM2

The SRCM2 bit value ORed with input TPOHINS selects the source for the M2 octet on a bit by bit basis. If the OR results in a logic zero, the M2 bit position is derived internally as specified by the M2TYPE bit in the SPLT Configuration Register. If the OR results in a logic one, the M2 bit position is inserted with the value sampled on TPOH. The M2 octet is set to logic zero (as required by the ATM Forum User Network Interface specification) by writing this bit position with a logic one, and connecting the TPOH input to VSS.

SRCM1

The SRCM1 bit value ORed with input TPOHINS selects the source for the M1 octet on a bit by bit basis. If the OR results in a logic zero, the M1 bit position is derived internally as specified by the M1TYPE bit in the SPLT Configuration Register. If the OR results in a logic one, the M1 bit position is inserted with the value sampled on TPOH. The M1 octet is set to logic zero (as required by the ATM Forum User Network Interface specification) by writing this bit position with a logic one, and connecting the TPOH input to VSS.

SRCG1

The SRCG1 bit value ORed with input TPOHINS selects the source for the G1 octet on a bit by bit basis. If the OR results in a logic zero, the G1 bit position is derived internally as required. If the OR results in a logic one, the G1 bit position is inserted with the value sampled on TPOH.

SRCB1

The SRCB1 bit value ORed with input TPOHINS selects the source for the B1 octet on a bit by bit basis. If the OR results in a logic zero, the internally calculated bit interleaved parity value is inserted in the B1 bit position. If the OR results in a logic one, the B1 bit position is inserted with the value sampled on TPOH.

SRCF1

The SRCF1 bit value ORed with input TPOHINS selects the source for the F1 octet on a bit by bit basis. If the OR results in a logic zero, the F1 bit position is determined by the SPLT F1 Octet Register. If the OR results in a logic one, the F1 bit position is inserted with the value sampled on TPOH.

SRCZN

The SRCZN bit value ORed with input TPOHINS selects the source for the Zn octets (where n=1 to 4 for the DS1 or E1 PLCP frame formats, n=1 to 6 for the DS3 PLCP frame format, and n=1 to 3 for the G.751 E3 PLCP frame format) on a bit by bit basis. If the OR results in a logic zero, the Zn bit position is forced to a logic zero. If the OR results in a logic one, the Zn bit position is inserted with the value sampled on TPOH.

Register 30EH: SPLT Diagnostics and G1 Octet

Bit	Type	Function	Default
Bit 7	R/W	DPFRM	0
Bit 6	R/W	DAFRM	0
Bit 5	R/W	DB1	0
Bit 4	R/W	DFEBE	0
Bit 3	R/W	YEL	0
Bit 2	R/W	LSS[2]	0
Bit 1	R/W	LSS[1]	0
Bit 0	R/W	LSS[0]	0

LSS[2:0]

The LSS[2:0] bits control the value inserted in the link status signal code bit positions of the path status octet (G1). These bits should be written with logic zero when implementing an ATM Forum UNI-compliant DS3 interface.

YEL

The YEL bit controls the yellow signal bit position in the path status octet (G1). When a logic one is written to YEL, the PLCP yellow alarm signal is transmitted.

DFEBE

The DFEBE bit controls the insertion of FEBEs in the PLCP frame. When DFEBE is written with a logic one, a single FEBE is inserted each PLCP frame. When DFEBE is written with a logic zero, FEBEs are indicated based on receive PLCP bit interleaved parity errors.

DB1

The DB1 bit controls the insertion of bit interleaved parity (BIP) errors in the PLCP frame. When DB1 is written with a logic one, a single BIP error is inserted in each PLCP frame. When DB1 is written with a logic zero, the bit interleaved parity is calculated and inserted normally.

DAFRM

The DAFRM bit controls the insertion of frame alignment pattern errors. When DAFRM is written with a logic one, a single bit error is inserted in each A1 octet, and in each A2 octet. When DAFRM is written with a logic zero, the frame alignment pattern octets are inserted normally.

DPFRM

The DPFRM bit controls the insertion of parity errors in the path overhead identification (POHID) octets. When DPFRM is written with a logic one, a parity error is inserted in each POHID octet. When DPFRM is written with a logic zero, the POHID octets are inserted normally.

Register 30FH: SPLT F1 Octet

Bit	Type	Function	Default
Bit 7	R/W	F1[7]	0
Bit 6	R/W	F1[6]	0
Bit 5	R/W	F1[5]	0
Bit 4	R/W	F1[4]	0
Bit 3	R/W	F1[3]	0
Bit 2	R/W	F1[2]	0
Bit 1	R/W	F1[1]	0
Bit 0	R/W	F1[0]	0

F1[7:0]

The F1[7:0] bits contain the value inserted in the path user channel octet (F1). F1[7] is the most significant bit, and is transmitted first. F1[0] is the least significant bit and is the last bit transmitted in the octet.

Register 310H: Change of PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH

The FEBECH bit is set to logic one if one or more FEBE events (or J2 EXZS events when the J2 framing format is selected) have occurred during the latest PMON accumulation interval.

CPERRCH

The CPERRCH bit is set to logic one if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH

The PERRCH bit is set to logic one if one or more parity error events (or J2 CRC-5 errors) have occurred during the latest PMON accumulation interval.

EXZS

The EXZS bit is set to logic one if one or more summed LCV events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH

The FERRCH bit is set to logic one if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH

The LCVCH bit is set to logic one if one or more LCV events have occurred during the latest PMON accumulation interval.

Register 311H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR

The OVR bit indicates the overrun status of the PMON holding registers. A logic one in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic zero indicates that no overrun has occurred. This bit is reset to logic zero when this register is read.

INTR

The INTR bit indicates the current status of the interrupt signal. A logic one in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic zero indicates that no transfer has occurred. The INTR bit is set to logic zero when this register is read.

INTE

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic one is written to INTE, the interrupt generation is enabled.

Register 314H: PMON LCV Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 315H: PMON LCV Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]

LCV[15:0] represents the number of DS3, E3, or J2 LCV errors that have been detected since the last time the LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes three RCLK cycles to complete.

Register 316H: PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

317H: PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]

> FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 or J2 framing pattern errors, that have been detected since the last time the framing error counter was polled.

> The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK cycles to complete in DS3 mode and three RCLK cycles to complete in E3 and J2 mode.

> This counter is paused when the corresponding framer has lost frame alignment.

Register 318H: PMON Excessive Zero Count LSB

Bit	Type	Function	Default
Bit 7	R	EXZS[7]	X
Bit 6	R	EXZS[6]	X
Bit 5	R	EXZS[5]	X
Bit 4	R	EXZS[4]	X
Bit 3	R	EXZS[3]	X
Bit 2	R	EXZS[2]	X
Bit 1	R	EXZS[1]	X
Bit 0	R	EXZS[0]	X

Register 319H: PMON Excessive Zero Count MSB

Bit	Type	Function	Default
Bit 7	R	EXZS[15]	X
Bit 6	R	EXZS[14]	X
Bit 5	R	EXZS[13]	X
Bit 4	R	EXZS[12]	X
Bit 3	R	EXZS[11]	X
Bit 2	R	EXZS[10]	X
Bit 1	R	EXZS[9]	X
Bit 0	R	EXZS[8]	X

EXZS[15:0]

> In DS3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic one in the DS3 FRMR Additional Configuration Register. This register accumulates summed LCV when the EXZSO is logic zero. The count of summed LCV is defined as the number of DS3 information blocks (85 bits) that contain one or more LCV since the last time the summed LCV counter was polled.

> The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). Such a write transfers the internally accumulated count to the EXZS Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK cycles to complete in DS3 mode and a maximum of 500 RCLK cycles to complete in G.832 E3 mode.

Register 31AH: PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 31BH: PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]

PERR[15:0] represents the number of DS3 P-bit errors, the number of E3 G.832 BIP-8 errors or the number of J2 CRC-5 errors that have been detected since the last time the parity error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK cycles to complete in DS3 mode and three RCLK cycles to complete in E3 and J2 mode.

This counter is paused when the corresponding framer has lost frame alignment.

Register 31CH: PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 31DH: PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]

When configured for DS3 applications, CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled.

This counter is forced to zero when the S/UNI-JET is configured for either J2 and E3 applications.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 255 RCLK cycles to complete.

This counter is paused when the corresponding framer has lost frame alignment.

Register 31EH: PMON FEBE/J2-EXZS Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE/J2-EXZS[7]	X
Bit 6	R	FEBE/J2-EXZS[6]	X
Bit 5	R	FEBE/J2-EXZS[5]	X
Bit 4	R	FEBE/J2-EXZS[4]	X
Bit 3	R	FEBE/J2-EXZS[3]	X
Bit 2	R	FEBE/J2-EXZS[2]	X
Bit 1	R	FEBE/J2-EXZS[1]	X
Bit 0	R	FEBE/J2-EXZS[0]	X

Register 31FH: PMON FEBE/J2-EXZS Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE/J2-EXZS[13]	X
Bit 4	R	FEBE/J2-EXZS[12]	X
Bit 3	R	FEBE/J2-EXZS[11]	X
Bit 2	R	FEBE/J2-EXZS[10]	X
Bit 1	R	FEBE/J2-EXZS[9]	X
Bit 0	R	FEBE/J2-EXZS[8]	X

FEBE/J2-EXZS[13:0]

> FEBE/J2-EXZS[13:0] represents the number of DS3 or E3 G.832 FEBEs that have been
> detected since the last time the FEBE error counter was polled.
>
> In J2 mode, FEBE/J2-EXZS[13:0] represents the number of Excessive Zeros (EXZS is a
> string of eight or more consecutive zeros) that have occurred during the previous
> accumulation interval.
>
> The counter (and all other counters in the PMON) is polled by writing to any of the PMON
> register addresses (314H to 31FH) or to the S/UNI-JET Identification, Master Reset, and
> Global Monitor Update Register (006H). Such a write transfers the internally accumulated
> count to the FEBE Event Count Registers and simultaneously resets the internal counter to
> begin a new cycle of error accumulation. This transfer and reset is carried out in a manner
> that coincident events are not lost. The transfer takes 255 RCLK cycles to complete in DS3
> mode and three RCLK cycles to complete in E3 and J2 mode.

Register 321H: CPPM Change of CPPM Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBECH	X
Bit 1	R	FECH	X
Bit 0	R	BIPECH	X

BIPECH

> The BIPECH bit is set to logic one if one or more PLCP bit interleaved parity error events have occurred since the last CPPM accumulation interval.

FECH

> The FECH bit is set to logic one if one or more PLCP frame alignment pattern octet errors, or path overhead identification octet errors have occurred since the last CPPM accumulation interval.

FEBECH

> The FEBECH bit is set to logic one if one or more PLCP FEBE events have occurred since the last CPPM accumulation interval.

Register 322H: CPPM B1 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	B1E[7]	X
Bit 6	R	B1E[6]	X
Bit 5	R	B1E[5]	X
Bit 4	R	B1E[4]	X
Bit 3	R	B1E[3]	X
Bit 2	R	B1E[2]	X
Bit 1	R	B1E[1]	X
Bit 0	R	B1E[0]	X

Register 323H: CPPM B1 Error Count MSB

Bit	Type	Function	Default
Bit 7	R	B1E[15]	X
Bit 6	R	B1E[14]	X
Bit 5	R	B1E[13]	X
Bit 4	R	B1E[12]	X
Bit 3	R	B1E[11]	X
Bit 2	R	B1E[10]	X
Bit 1	R	B1E[9]	X
Bit 0	R	B1E[8]	X

B1E[15:0]

> B1E[15:0] represents the number of PLCP bit interleaved parity (BIP) errors that have been detected since the last time the B1 error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (322H – 32FH). Such a write transfers the internally accumulated count to the B1 Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 μs for the DS3 bit rate; 1.95μs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. B1 errors are not accumulated when the S/UNI-JET has declared a PLCP LOF defect state.

Register 324H: CPPM Framing Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 325H: CPPM Framing Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[11:0]

> FE[11:0] represents the number of PLCP framing pattern octet errors and path overhead identification octet errors that have been detected since the last time the framing error event counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (322H – 32FH). Such a write transfers the internally accumulated count to the Framing Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. Framing error errors are not accumulated when the S/UNI-JET has declared a PLCP LOF defect state.

Register 326H: CPPM FEBE Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 327H: CPPM FEBE Count MSB

Bit	Type	Function	Default
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[15:0]

FEBE[15:0] represents the number of PLCP FEBEs (FEBE) that have been detected since the last time the FEBE error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses (322H – 32FH). Such a write transfers the internally accumulated count to the FEBE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 67 RCLK periods (1.5 µs for the DS3 bit rate; 1.95µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. FEBE errors are not accumulated when the S/UNI-JET has declared a PLCP LOF defect state.

Register 330H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE

The CBE bit enables the DS3 C-bit parity application. When a logic one is written to CBE, C-bit parity mode is enabled. When a logic zero is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, FEBEs are accumulated.

AISC

The AISC bit controls the algorithm used to detect the AIS (AIS). When a logic one is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic zero is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic zero is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR

The REFR bit initiates a DS3 reframe. When a logic one is written to REFR, the S/UNI-JET is forced OOF, and a new search for frame alignment is initiated. Note: Only a low-to-high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI

The UNI bit configures the S/UNI-JET to accept either dual-rail or single-rail receive DS3 streams. When a logic one is written to UNI, the S/UNI-JET accepts a single-rail DS3 stream on RDATI. The S/UNI-JET accumulates LCV on the RLCV input. When a logic zero is written to UNI, the S/UNI-JET accepts B3ZS-encoded dual-rail data on RPOS and RNEG.

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M3O8

The M3O8 bit controls the DS3 OOF decision criteria. When a logic one is written to M3O8, DS3 OOF is declared when three of eight framing bits (F-bits) are in error. When a logic zero is written to M3O8, the three of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic one, M-bit errors are disabled from causing an OOF; the LOF criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic zero, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic zero, an OOF can occur when one or more M-bit errors occur in three out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic one, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic zero, the detection time is 13.5 ms.

AISPAT

The AISPAT bit controls the pattern used to detect the AIS (AIS). When a logic one is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010.. is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic zero is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 331H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE

The LOSE bit enables interrupt generation when a DS3 LOSdefect is declared or removed. The interrupt is enabled when a logic one is written.

OOFE

The OOFE bit enables interrupt generation when a DS3 OOF defect is declared or removed. The interrupt is enabled when a logic one is written.

AISE

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic one is written.

IDLE

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic one is written.

FERFE

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic one is written.

CBITE

The CBITE bit enables interrupt generation when the S/UNI-JET detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic one is written.

REDE

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status Register. When REDE is set to logic one, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE

The COFAE bit enables interrupt generation when the S/UNI-JET detects a DS3 change of frame alignment. The interrupt is enabled when a logic one is written.

Register 331H: DS3 FRMR Additional Configuration Register

(ACE=1 in Register 333H)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

DALGO

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic one, a valid B3ZS signature is declared and three zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic zero, a valid B3ZS signature is declared and the three zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to LCV indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic one, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic zero, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic one, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic zero, every occurrence of three consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every three consecutive zeros). Refer to Table 14.

EXZSO

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic one, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic zero, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or three consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one. Refer to Table 14.

BPVO

The BPVO bit enables only bipolar violations to indicate LCV and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic one, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic zero, both BPVs not part of a valid B3ZS signature, and either three consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter. Refer to Table 14.

Table 14   DS3 FRMR EXZS/LCV Count Configurations

Register Bit			Counter Function	
EXZSO	BPVO	EXZDET	PMON EXZ Count	PMON LCV Count
0	0	0	Summed LCVs	BPVs & every 3 consecutive zeros
0	0	1	Summed LCVs	BPVs & every string of more than 3 consecutive zeros
0	1	0	Reserved	Reserved
0	1	1	Reserved	Reserved
1	0	0	Summed excessive zeros	BPVs & every 3 consecutive zeros
1	0	1	Summed excessive zeros	BPVs & every string of 3+ consecutive zeros
1	1	0	Summed excessive zeros	Only BPVs
1	1	1	Summed excessive zeros	Only BPVs

AISONES

The AISONES bit controls the pattern used to detect the AIS (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration Register are logic zero; if either AISPAT or AISC are logic one, the AISONES bit is ignored. When a logic zero is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111..) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic one is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111..) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized in Table 15:

Table 15   DS3 FRMR AIS Configurations

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic zero; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic zero, and X-bits=1. This can be detected by setting both AISPAT and AISC high, and declaring AIS only when AISV=1 and FERFV=0 (Register x33H).
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 332H: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI

The LOSI bit is set to logic one when a LOS defect is detected or removed. The LOSI bit position is set to logic zero when this register is read.

OOFI

The OOFI bit is set to logic one when an OOF defect is detected or removed. The OOFI bit position is set to logic zero when this register is read.

AISI

The AISI bit is set to logic one when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic zero when this register is read.

IDLI

The IDLI bit is set to logic one when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic zero when this register is read.

FERFI

The FERFI bit is set to logic one when a FERF defect is detected or removed. The FERFI bit position is set to logic zero when this register is read.

CBITI

The CBITI bit is set to logic one when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic zero when this register is read.

REDI

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status Register. When the REDI bit is a logic one, a change in the RED state has occurred. When the REDI bit is logic zero, no change in the RED state has occurred.

COFAI

The COFAI bit is set to logic one when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic zero when this register is read.

Register 333H: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV

The LOSV bit indicates the current LOS defect state. LOSV is a logic one when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic zero when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV

The OOFV bit indicates the current DS3 OOF defect state. When the S/UNI-JET has lost frame alignment and is searching for the new alignment, OOFV is set to logic one. When the S/UNI-JET has found frame alignment, the OOFV bit is set to logic zero.

AISV

The AISV bit indicates the AIS state. When the S/UNI-JET detects the AIS maintenance signal, AISV is set to logic one.

IDLV

The IDLV bit indicates the IDLE signal state. When the S/UNI-JET detects the IDLE maintenance signal, IDLV is set to logic one.

FERFV

The FERFV bit indicates the current far end receive failure defect state. When the S/UNI-JET detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic one. When the S/UNI-JET detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic zero.

CBITV

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic one (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic zero (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic one, the DS3 FRMR frame alignment acquisition circuitry has been OOF for 2.23ms (or for 13.5ms when FDET is logic zero). When the REDV bit is logic zero, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE

The ACE bit selects the Additional Configuration Register. This register is located at address 331H, and is only accessible when the ACE bit is set to logic one. When ACE is set to logic zero, the Interrupt Enable Register is accessible at address 331H.

Register 334H: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	CBIT	0

CBIT

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic one, C-bit parity is enabled, and the S/UNI-JET modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the FEBE indication, and the path parity. When CBIT is written with a logic zero, the M23 application is selected, and each C-bit is set to logic one by the S/UNI-JET except for the first C-bit of the frame, which is forced to toggle every frame. Note: The C-bits may be modified as required using the DS3 overhead access port (TOH) regardless of the setting of this bit.

FERF

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic one, the X1 and X2 overhead bit positions are set to logic zero. When FERF is written with a logic zero, the X1 and X2 overhead bit positions in the DS3 stream are set to logic one.

IDL

The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic one, the DS3 payload is overwritten with the repeating pattern 1100.. The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic zero, the idle signal is not inserted.

AIS

The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic one, the DS3 payload is overwritten with the repeating pattern 1010.. The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are controlled by the CBTRAN bit in this register. When AIS is written with a logic zero, the AIS signal is not inserted.

CBTRAN

The CBTRAN bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic zero, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic one, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Reserved

The reserved bit must be programmed to logic zero for proper operation.

Register 335H: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE

The DFEBE bit controls the insertion of FEBEs in the DS3 stream. When DFEBE is written with a logic one, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic zero. When DFEBE is written with a logic zero, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic one, the P-bits are inverted before insertion. When DPERR is written with a logic zero, the parity is calculated and inserted normally.

DCPERR

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic one and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic zero, the path parity is calculated and inserted normally.

DMERR

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic one, the M-bits are inverted before insertion. When DMERR is written with a logic zero, the M-bits are inserted normally.

DFERR

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic one, the F-bits are inverted before insertion. When DFERR is written with a logic zero, the F-bits are inserted normally.

DLCV

The DLCV bit controls the insertion of a single LCV in the DS3 stream. When DLCV is written with a logic one, a LCV is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the LCV to be inserted. For example, LCV may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the LCV.

DLOS

The DLOS bit controls the insertion of LOSin the DS3 stream. When DLOS is written with a logic one, the data on outputs TPOS/TDATO and TNEG/TOHM is forced to continuous zeros.

Register 338H: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 7	Unused	X	
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR

A transition from logic zero to logic one in the REFR bit position forces the E3 Framer to initiate a search for frame alignment. The bit must be cleared to logic zero, then set to logic one again to initiate subsequent searches for frame alignment.

REFRDIS

The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic one in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic zero allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. The FORMAT[1:0] bits select one of two framing formats. Refer to Table 16.

Table 16   E3 FRMR FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI

> The UNI bit selects the mode of the receive data interface. When UNI is logic one, the E3-FRMR expects unipolar data on the RDATI input and accepts LCV indications on the RLCV input. When UNI is logic zero, the E3-FRMR expects bipolar data on the RPOS and RNEG inputs and decodes the pulses according to the HDB3 line code.

Reserved

> The Reserved bit must be programmed to logic zero for proper operation.

Register 339H: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET

The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic one, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic zero, the Timing Marker bit must be in the same state for three consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET

The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the RAI (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic one, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic zero, the FERF, or RAI, bit must be in the same state for three consecutive frames.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic one, the justification service bits and the tributary justification bits are indicated as payload to the SPLR. When PYLD&JUST is logic zero, the justification service and tributary justification bits are indicated as overhead to SPLR. For G.751 ATM applications, this bit must be set to logic one for correct cell mapping.

WORDERR

The WORDERR bit selects whether the framing bit error indication pulses accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic one, the FERR indication to PMON pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic zero, the FERR indication to PMON pulses for each and every framing bit error that occurs; PMON accumulates all framing bit errors.

Reserved

The Reserved bit must be set to logic zero for proper operation.

WORDBIP

The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic one, the parity error indication to the E3 TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic zero, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs. For G.832 applications, this bit should be set to logic one.

Register 33AH: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit is an interrupt enable. When OOFE is logic one, a change of state of the OOF status generates an interrupt and sets the INTB output to logic zero. When OOFE is logic zero, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE

The COFAE bit is an interrupt enable. When COFAE is logic one, a change of frame alignment generates an interrupt and sets the INTB output to logic zero. When COFAE is logic zero, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE

The LCVE bit is an interrupt enable. When LCVE is logic one, detection of a LCV generates an interrupt and sets the INTB output to logic zero. When LCVE is logic zero, occurrences of LCV are disabled from causing interrupts on the INTB output.

LOSE

The LOSE bit is an interrupt enable. When LOSE is logic one, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic zero. When LOSE is logic zero, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE

The CZDE bit is an interrupt enable. When CZDE is logic one, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets the INTB output to logic zero. When CZDE is logic zero, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 33BH: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF

The OOF bit indicates the current state of the E3-FRMR. When OOF is logic one, the E3-FRMR is OOF alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic zero, the E3-FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic one, but the setting may change prior to the register being read.

LOS

The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic one, the E3-FRMR has received 32 consecutive RCLK cycles with no occurrences of bipolar data on RPOS and RNEG. When LOS is logic zero, the FRMR is receiving valid bipolar data. When the E3-FRMR has declared LOS, the LOS indication is set to logic zero (de-asserted) when the E3-FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic zero if the UNI bit is logic one. During reset, LOS is set to logic zero, but the setting may change prior to the register being read.

OOFI

A logic one OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic zero upon the completion of the register read. When OOFI is logic zero, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI

The COFAI bit indicates that a change of frame alignment between the previous alignment and the newly found alignment has occurred. When COFAI is logic one, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic zero upon the completion of the register read. When COFAI is logic zero, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI

The LCVI bit indicates that a LCV has occurred. When LCVI is logic one, a LCV on the RPOS and RNEG inputs was detected since the last time this register was read. The LCVI bit is cleared to logic zero upon the completion of the register read. When LCVI is logic zero, it indicates that no LCV was detected since the last register read. When the UNI bit in the Framing Options Register is logic one, the LCVI is forced to logic zero.

LOSI

The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic one, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic zero upon the completion of the register read. When LOSI is logic zero, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options Register is logic one, the LOSI is forced to logic zero.

CZDI

The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic one, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic zero upon the completion of the register read. When CZDI is logic zero, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options Register is logic one, the CZDI indication is forced to logic zero.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2,3,4,5,6 of this register) are cleared to logic zero after the register is read; the INTB output is also cleared to logic one if the interrupt was generated by any of these five events.

Register 33CH: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE

> The NATUSEE bit is an interrupt enable. When NATUSEE is logic one, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic zero, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE

> The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic one, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic zero, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE

> The PTYPEE bit is an interrupt enable. When PTYPEE is logic one, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic zero, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE

> The FEBEE bit is an interrupt enable. When FEBEE is logic one, an interrupt is generated on the INTB output when the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic zero, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE

The FERFE bit is an interrupt enable. When FERFE is logic one, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the RAI bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic zero, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE

The AISDE bit is an interrupt enable. When AISDE is logic one, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic zero, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE

The PERRE bit is an interrupt enable. When PERRE is logic one, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic zero, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE

The FERRE bit is an interrupt enable. When FERRE is logic one, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic zero, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 33DH: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	FunctioIn	Defaut
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI

The NATUSEI bit is a transition Indication. When NATUSEI is logic one, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic zero, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI

The TIMEMKI bit is a transition indication. When TIMEMKI is logic one, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic zero, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI

The PTYPEI bit is a transition indication. When PTYPEI is logic one, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic zero, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI

The FEBEI bit is a transition indication. When FEBEI is logic one, a change of state of the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic zero, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI

The FERFI bit is a transition indication. When FERFI is logic one, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the RAI bit (bit 12 of the frame in G.751) has occurred. When FERFI is logic zero, no changes in the state of the FERF or RAI bit has occurred since the last time this register was read.

AISDI

The AISDI bit is a transition indication. When AISDI is logic one, a change in state of the AISD indication has occurred. When AISDI is logic zero, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI

The PERRI bit is an event indication. When PERRI is logic one, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic zero, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI

The FERRI bit is an event indication. When FERRI is logic one, the occurrence of one or more framing bit error has been detected. When FERRI is logic zero, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic zero after the register is read; the INTB output is also cleared to logic one if the interrupt was generated by any of the Maintenance Event outputs.

Register 33EH: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE

The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK

The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]

The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or three times in rapid succession to ensure a coherent binary value.

FEBE

The FEBE bit reflects the state of the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF

The FERF bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the RAI bit (bit 11 of the frame in G.751) when the value has been the same for either three or 5 consecutive frames.

AISD

The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic one, less than eight zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the FRMR is OOF alignment. When AISD is logic zero, eight or more zeros (in G.832 mode), or 5 or more zeros (in G.751 mode), were detected during one complete frame period, or the FRMR has found frame alignment.

Register 340H: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]

The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

Table 17   E3 TRAN FORMAT[1:0] Configurations

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

Reserved

The Reserved bit must be programmed to logic zero for correct operation.

Register 341H: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PYLD&JUST	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE

The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the internal HDLC transmitter (if TNETOP is set to logic one). When TNETOP is logic zero, the NATUSE bit controls the value of the National Use bit. When NATUSE is logic one, the National Use bit (bit 12 in G.751) is forced to logic one regardless of the bit input from the internal HDLC transmitter or the setting of TNETOP. When NATUSE is logic zero, the National Use bit is set to the value sampled from the internal HDLC transmitter if TNETOP is logic zero. Otherwise, the National Use bit will be set to logic zero. If the E3 TRAN is configured for G.832 mode, this bit is ignored.

TAIS

The TAIS bit enables AIS signal transmission. When TAIS is logic one, the all 1's AIS signal is transmitted. When TAIS is logic zero, the normal data is transmitted.

Reserved

The Reserved bit must be programmed to logic zero for proper operation.

DLCV

The DLCV bit selects whether a LCV is generated for diagnostic purposes. When DLCV changes from logic zero to logic one, single LCV is generated; in HDB3, the LCV is generated by causing a bipolar violation pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must be first be written to logic zero and then to logic one again.

DFERR

The DFERR bit selects whether the framing pattern is corrupted for diagnostic purposes. When DFERR is logic one, the framing pattern inserted into the output data stream is inverted. When DFERR is logic zero, the unaltered framing pattern inserted into the output data stream.

CPERR

The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic one, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask Register and inserted into the G.832 EM byte. When CPERR is logic zero, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask Register, and inserted into the EM byte.

PYLD&JUST

The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing modes G.751 is indicated as overhead or payload. When PYLD&JUST is logic one, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic zero, the justification service and tributary justification bits are indicated as overhead. For G.751 ATM applications, this bit must be set to logic one for correct cell mapping.

Register 342H: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]

The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to eight BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic one in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the Status and Diagnostic Options Register can be used.

Register 343H: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK

The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic one, the Timing Marker bit in the MA byte is set to logic one. When TIMEMK is set to logic zero, the Timing Marker bit in the MA byte is set to logic zero.

TUMFRM[1:0]

The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multiframe bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte). These bits are logically ORed with the TUMFRM[1:0] overhead signals from the TOH input before being inserted in the MA byte.

PTYPE[2:0]

The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte).

FEBE

The FEBE bit reflects the value to be inserted in the FEBE indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indications generated by the FRMR for any detected BIP-8 errors. When the FEBE bit is logic one, bit 2 of the G.832 MA byte is set to logic one; when the FEBE bit is logic zero, any BIP-8 error indications from the FRMR causes bit 2 of the MA byte to be set to logic one.

FERF/RAI

The FERF/RAI bit reflects the value to be inserted in the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the RAI bit (bit 11 of the frame in G.751). The FERF/RAI bit is logically ORed with the LOS, OOF, AIS, and LCD indications from the E3 FRMR and RXCP-50 when the LOSEN, OOFEN, AISEN, and LCDEN register bits (in the S/UNI-JET Data Link and FERF/RAI Control Register) are set to logic one respectively. When the OR of the two signals is logic one, the FERF or RAI bit in the frame is set to logic one; when neither signal is logic one, the FERF or RAI bit is set to logic zero.

Register 344H: J2-FRMR Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UNI	0
Bit 5	R/W	REFRAME	0
Bit 4	R/W	FLOCK	0
Bit 3	R/W	CRC_REFR	0
Bit 2	R/W	SFRME	0
Bit 1	R/W	LOSTHR[1]	1
Bit 0	R/W	LOSTHR[0]	1

UNI

When the UNI bit is set to logic zero, the J2-FRMR expects unipolar data on the RDATI input and LCV indications on the RLCV input. When UNI is logic zero, the J2-FRMR expects bipolar B8ZS encoded data on the RPOS and RNEG inputs. When UNI is set to logic one, then the LOS, LOSI, and EXZI indications cannot be used.

REFRAME

Writing the REFRAME bit logic one forces the J2-FRMR to declare LOF, and begin searching for a new alignment. In order to force another reframe, REFRAME must be written with logic zero, and then logic one again.

FLOCK

When the FLOCK bit is set to logic one, the J2-FRMR is prevented from declaring LOF and searching for a new frame alignment due to framing-pattern errors. In this case, the J2-FRMR will only search for frame alignment when the REFRAME register bit transitions from logic zero to logic one.

CRC_REFR

When the CRC Reframe Enable bit is set to logic one, an alternate framing algorithm is enabled, which uses the CRC-5 check to detect framing to a mimic pattern in the payload or signaling bits. The framer, once it has seen at least one correct framing pattern, begins looking for correct CRC-5s as well. If it observes three consecutive correct framing patterns, and two correct CRC-5 sequences, then frame is declared. Otherwise, a reframe is initiated. When CRC_REFR is set to logic zero, the framing algorithm simply searches for three consecutive correct framing patterns.

SFRME

When the Single Framing Bit Error (SFRME) bit is set to logic one, then the J2-FRMR will indicate (to the PMON) a single framing error for every J2 multi-frame which contains one or more framing errors. When the SFRME bit is set to logic zero, the J2-FRMR will identify every framing error to the PMON.

LOSTHR[1:0]

The LOS Threshold bits select the number of consecutive zeroes required before the J2-FRMR will declare LOS, and the number of bit periods without an occurrence of excess zeroes that must pass before the J2-FRMR will de-assert LOS. The thresholds are described in Table 18:

Table 18   J2 FRMR LOS Threshold Configurations

LOSTHR[1]	LOSTHR[0]	Threshold
0	0	15
0	1	31
1	0	63
1	1	255

Thus, if LOSTHR[1:0] = 11 binary, LOS will be declared after the 255th consecutive binary zero, and de-asserted when 255 bit periods have passed without an occurrence of a string of eight or more consecutive zeroes.

Register 345H: J2-FRMR Status

Bit	Type	Function	Default
Bit 7	R	LOS	X
Bit 6	R	LOF	X
Bit 5		Unused	X
Bit 4	R	RAI	X
Bit 3	R	RLOF	X
Bit 2		Unused	X
Bit 1	R	PHYAIS	X
Bit 0	R	PLDAIS	X

LOS, LOF, RAI, RLOF, PHYAIS, PLDAIS

These register bits reflect the current state of the LOS, LOF, RAI (RAI), Remote LOF (RLOF, also known as the a-bit), Physical AIS (PHYAIS), and Payload AIS (PLDAIS) conditions.

Register 346H: J2-FRMR Alarm Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOSE	0
Bit 6	R/W	LOFE	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	RAIE	0
Bit 3	R/W	RLOFE	0
Bit 2	R/W	RLOF_THR	1
Bit 1	R/W	PHYAISE	0
Bit 0	R/W	PLDAISE	0

LOSE

When LOSE is logic one, the J2-FRMR will generate an interrupt when the LOS condition changes state. Note: The LOS bit is not valid when the UNI bit is set in the J2-FRMR Configuration Register.

LOFE

When LOFE is logic one, the J2-FRMR will generate an interrupt when LOF changes state.

COFAE

When COFAE is logic one, the J2-FRMR will generate an interrupt when a change of frame alignment occurs.

RAIE

When RAIE is logic one, the J2-FRMR will generate an interrupt when RAI changes state.

RLOFE

When RLOFE is logic one, the J2-FRMR will generate an interrupt when RLOF changes state.

RLOF_THR

The RLOF Threshold bit determines the number of consecutive a-bits that are required for the state of RLOF to change. When RLOF_THR is logic zero, RLOF is asserted when the a-bit has been logic one for three consecutive frames, and de-asserted when the a-bit has been logic zero for three consecutive frames. When RLOF_THR is logic one, RLOF is asserted when the a-bit has been logic one for five consecutive frames, and de-asserted when the a-bit has been logic zero for five consecutive frames. The default setting is that five consecutive a-bits are required.

PHYAISE

When PHYAISE is logic one, the J2-FRMR will generate an interrupt when a change is detected in the Physical AIS condition.

PLDAISE

When PLDAISE is logic one, the J2-FRMR will generate an interrupt when a change is detected in the Payload AIS condition.

Register 347H: J2-FRMR Alarm Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LOSI	X
Bit 6	R	LOFI	X
Bit 5	R	COFAI	X
Bit 4	R	RAII	X
Bit 3	R	RLOFI	X
Bit 2		Unused	X
Bit 1	R	PHYAISI	X
Bit 0	R	PLDAISI	X

LOSI

The LOSI bit is set to logic one if a change occurs in the LOS condition. LOSI is cleared when this register is read.

LOFI

The LOFI bit is set to logic one if a change occurs in the state of LOF. LOFI is cleared when this register is read.

COFAI

The COFAI bit is set to logic one if a change in frame alignment occurs. COFAI is cleared when this register is read.

RAII

The RAII bit is set to logic one if a change in the value of RAI occurs. RAII is cleared when this register is read.

RLOFI

The RLOFI bit is set to logic one if a change in the value of RLOF occurs. RLOFI is cleared when this register is read.

PHYAISI

The PHYAISI bit is set to logic one if a change in the condition of PHYAIS occurs. PHYAISI is cleared when this register is read.

PLDAISI

The PLDAISI bit is set to logic one if a change in the condition of PLDAIS occurs. PLDAISI is cleared when this register is read.

Register 348H: J2-FRMR Error/Xbit Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	CRCEE	0
Bit 6	R/W	FRMEE	0
Bit 5	R/W	BPVE	0
Bit 4	R/W	EXZE	0
Bit 3	R/W	XBITE	0
Bit 2		Unused	X
Bit 1	R/W	XBIT_DEB	0
Bit 0	R/W	XBIT_THR	0

CRCEE

When CRCEE is logic one, the J2-FRMR will generate an interrupt if a multiframe fails its CRC-5 check.

FRMEE

When FRMEE is logic one, the J2-FRMR will generate an interrupt upon the reception of an errored framing bit.

BPVE

When BPVE is logic one, the J2-FRMR will generate an interrupt upon the reception of a bipolar violation which is not part of a valid B8ZS code (when UNI is set to logic zero in the J2-FRMR Configuration Register) or on the reception of a logic one on RLCV (when UNI is set to logic one).

EXZE

When EXZE is logic one, the J2-FRMR will generate an interrupt upon the reception of a string of eight-or-more consecutive zeroes. EXZE has no effect when UNI is set to logic one in the J2-FRMR Configuration Register.

XBITE

When XBITE is logic one, the J2-FRMR will generate an interrupt when any of the x-bits (X1, X2, X3) change state. Because the XBIT interrupt is generated when the x-bit indications change, the interrupt is debounced along with them via the XBIT_DEB and XBIT_THR bits.

XBIT_DEB

When XBIT_DEB is set to logic zero, the x-bit indications in the J2-FRMR Error/Xbit
Interrupt Status Register reflect the most recent value of the x-bits. When XBIT_DEB is set
to logic one, the x-bit indications change value only when an x-bit has maintained its value
for three or five consecutive multiframes, depending on the setting of XBIT_THR.

XBIT_THR

When XBIT_THR is set to logic one, then XBIT_THR controls the debouncing threshold of
the x-bit indications in the J2-FRMR Error/Xbit Interrupt Status Register. When XBIT_THR
is logic zero, the threshold is set to three consecutive multiframes; when XBIT_THR is logic
one, the threshold is set to five consecutive multiframes.

Register 349H: J2-FRMR Error/Xbit Interrupt Status

Bit	Type	Function	Default
Bit 7	R	CRCEI	X
Bit 6	R	FRMEI	X
Bit 5	R	BPVI	X
Bit 4	R	EXZI	X
Bit 3	R	XBITI	X
Bit 2	R	X3	X
Bit 1	R	X2	X
Bit 0	R	X1	X

CRCEI

The CRCEI bit is set to logic one if a failed CRC-5 check occurs. CRCEI is cleared when this register is read.

FRMEI

The FRMEI bit is set to logic one if an errored framing bit occurs. FRMEI is cleared when this register is read.

BPVI

The BPVI bit is set to logic one if a bipolar violation that is not part of a valid B8ZS code occurs (when UNI is logic zero in the J2-FRMR Configuration Register) or if a 0 to 1 transition is detected on RLCV (when UNI is logic one). BPVI is cleared when this register is read.

EXZI

The EXZI bit is set to logic one upon reception of eight-or-more consecutive zeroes. EXZI remains logic zero while UNI is set to logic one in the J2_FRMR Configuration Register. EXZI is cleared when this register is read.

XBITI

The XBITI bit is set to logic one if a change in the debounced (if XBIT_DEB is set to logic one) x-bits (X1, X2, and X3) is detected. XBITI is cleared when this register is read.

X1, X2, X3

The X1, X2, and X3 bits reflect the most recent (debounced if XBIT_DEB is set to logic one) value of bits 785, 786, and 787 respectively of frame three of each multiframe. These bits are the spare or 'x-bits'

Register 34CH: J2-TRAN Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	X3SET	1
Bit 2	R/W	X2SET	1
Bit 1	R/W	X1SET	1
Bit 0	R/W	RLOF	0

RLOF

> The RLOF bit controls the state of the A-bit. When RLOF is a logic one, the A-bit is also set to logic one. When RLOF is a logic zero, the A-bit is set to logic zero. The A-bit in the transmit stream may also be set to logic one if an LOF condition in the J2 FRMR is detected and the RBLEN bit is logic one in the S/UNI-JET Data Link and FERF/RAI Control Register.

X1SET

> The X1SET bit controls the state of the X1 bit (bit 785 in the third frame of a J2 multiframe). When X1SET is a logic one, the X1 bit is set to logic one. When X1SET is a logic zero, the X1 bit is set to logic zero.

X2SET

> The X2SET bit controls the state of the X2 bit (bit 786 in the third frame of a J2 multiframe). When X2SET is a logic one, the X2 bit is set to logic one. When X2SET is a logic zero, the X2 bit is set to logic zero.

X3SET

> The X3SET bit controls the state of the X3 bit (bit 787 in the third frame of a J2 multiframe). When X3SET is a logic one, the X3 bit is set to logic one. When X3SET is a logic zero, the X3 bit is set to logic zero.

Reserved

> The reserved register bits should be set to logic zero for proper operation.

Register 34DH: J2-TRAN Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PLDAIS	0
Bit 4	R/W	PHYAIS	0
Bit 3	R/W	DCRC	0
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBPV	0
Bit 0	R/W	DFERR	0

DFERR

The DFERR bit controls the insertion of framing alignment signal errors. When DFERR is set to logic one, the framing alignment signal is inverted. When DFERR is set to logic zero, the framing alignment signal is not inverted.

DBPV

The DBPV bit controls the insertion of single bipolar violations. When DBPV bit transitions from 0 to 1, a violation is generated by masking the first violation pulse of a B8ZS signature. To generate another violation, this bit must first be written to 0 and then to logic one again. When DBPV is a logic zero, no violation is generated.

DLOS

When set to logic one, the DLOS bit forces the unipolar and bipolar outputs of the J2 TRAN to be all zeros. When DLOS is logic zero, the outputs of the J2 TRAN operate normally.

DCRC

When set to logic one, a the CRC-5 check bits (e_{1-5}) are inverted before transmission. DCRC inverts the e_{1-5} bits even if CDIS of the J2 TRAN Configuration Register is set to logic one.

PHYAIS

When set to logic one, PHYAIS will cause the J2 TRAN to transmit an all 1's AIS (AIS).

PLDAIS

When set to logic one, PLDAIS will cause the J2 TRAN to insert all-ones in the payload data bits. When PLDAIS is a logic zero, data is processed normally through the J2 TRAN.

Register 34EH: J2-TRAN TS97 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS97[1]	1
Bit 6	R/W	TS97[2]	1
Bit 5	R/W	TS97[3]	1
Bit 4	R/W	TS97[4]	1
Bit 3	R/W	TS97[5]	1
Bit 2	R/W	TS97[6]	1
Bit 1	R/W	TS97[7]	1
Bit 0	R/W	TS97[8]	1

TS97[1:8]

The TS97[1:8] bits control what is inserted into the J2 timeslot 97 bits. TS97[1] is the first bit of timeslot 97 transmitted.

S/UNI®-JET Data Sheet
Released

Register 34FH: J2-TRAN TS98 Signaling

Bit	Type	Function	Default
Bit 7	R/W	TS98[1]	1
Bit 6	R/W	TS98[2]	1
Bit 5	R/W	TS98[3]	1
Bit 4	R/W	TS98[4]	1
Bit 3	R/W	TS98[5]	1
Bit 2	R/W	TS98[6]	1
Bit 1	R/W	TS98[7]	1
Bit 0	R/W	TS98[8]	1

TS98[1:8]

The TS98[1:8] bits control what is inserted into the J2 timeslot 98 bits. TS98[1] is the first bit of timeslot 98 transmitted.

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Document ID: PMC-1990267, Issue 3

Register 350H: RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN

The EN bit controls the overall operation of the RDLC. When EN is set to logic one, RDLC is enabled; when set to logic zero, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR

Setting the terminate reception (TR) bit to logic one forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic one to logic zero and back to logic one. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic zero after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic zero.

MEN

Setting the Match Enable (MEN) bit to logic one enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all-ones address. When the MEN bit is logic zero, all packets received are written into the RDLC FIFO.

MM

Setting the Match Mask (MM) bit to logic one ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all-ones address when performing the address comparison.

Reserved

This register bit should be set to logic zero for proper operation.

Register 351H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts. The value of INTC[6:0] = 'b0000000 sets the interrupt FIFO fill level to 128.

INTE

The Interrupt Enable bit (INTE) must set to logic one to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic zero the RDLC will not assert INTB.

The contents of the Interrupt Control Register should only be changed when the EN bit in the RDLC Configuration Register is logic zero. This prevents any erroneous interrupt generation.

Register 352H: RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data Registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-JET Miscellaneous Register (39BH).

INTR

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic one, a RDLC interrupt (INTR is a logic one) will cause INTB to be asserted low. The INTR register bit will be set to logic one when one of the following conditions occurs:

- The number of bytes specified in the RDLC Interrupt Control Register are received on the data link and are written into the FIFO.

- RDLC FIFO buffer overrun is detected.

- The last byte of a packet is written into the RDLC FIFO.

- The last byte of an aborted packet is written into the RDLC FIFO.

- Transition of receiving all-ones to receiving flags is detected.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last

Read from the FIFO as indicated in Table 19:

Table 19   RDLC PBS[2:0] Data Status

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.

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Document ID: PMC-1990267, Issue 3

PBS[2:0]	Data Status
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN

The Packet In (PKIN) bit is logic one when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic zero after the RDLC Status Register is read.

COLS

The Change of Link Status (COLS) bit is set to logic one if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic zero by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic one then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR

The overrun (OVR) bit is set to logic one when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic zero until after the Status Register is read. While the OVR bit is logic one, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic zero.

FE

The FIFO buffer empty (FE) bit is set to logic one when the last RDLC FIFO buffer entry is read. The FE bit goes to logic zero when the FIFO is loaded with new data.

Register 353H: RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data Registers should not occur at rates greater than 1/10 that of the clock selected by the LINESYSCLK bit of the S/UNI-JET Miscellaneous Register (39BH).

RD[7:0]

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.

This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic zero.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 354H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 355H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 358H: TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data Register and reads of the TDPR Interrupt Status/UDR Clear Register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-JET Miscellaneous Register (39BH).

EN

The EN bit enables the TDPR functions. When EN is set to logic one, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data Register. When the EN bit is set to logic zero, the TDPR is disabled and an all-ones Idle sequence is transmitted on the datalink.

CRC

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic one enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic zero, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT

The Abort (ABT) bit controls the sending of the seven consecutive-ones HDLC abort code. Setting the ABT bit to a logic one causes the 01111111 code (the 0 is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic zero. At least one Abort sequence will be sent when the ABT bit transitions from logic zero to logic one.

EOM

The EOM bit indicates that the last byte of data written in the Transmit Data Register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data Register.

Reserved

This bit should be set to logic zero for proper operation.

FIFOCLR

The FIFOCLR bit resets the TDPR FIFO. When set to logic one, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic one, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic zero, then separate closing and opening flags are inserted between successive frames.

Register 359H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 35AH: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic one. LFILLI will cause an interrupt on INTB if LFILLE is set to logic one.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 35BH: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE

The LFILLE enables a transition to logic one on LFILLI to generate an interrupt on INTB. If LFILLE is a logic one, a transition to logic one on LFILLI will generate an interrupt on INTB. If LFILLE is a logic zero, a transition to logic one on LFILLI will not generate an interrupt on INTB.

UDRE

The UDRE enables a transition to logic one on UDRI to generate an interrupt on INTB. If UDRE is a logic one, a transition to logic one on UDRI will generate an interrupt on INTB. If UDRE is a logic zero, a transition to logic one on UDRI will not generate an interrupt on INTB.

OVRE

The OVRE enables a transition to logic one on OVRI to generate an interrupt on INTB. If OVRE is a logic one, a transition to logic one on OVRI will generate an interrupt on INTB. If OVRE is a logic zero, a transition to logic one on OVRI will not generate an interrupt on INTB.

FULLE

The FULLE enables a transition to logic one on FULLI to generate an interrupt on INTB. If FULLE is a logic one, a transition to logic one on FULLI will generate an interrupt on INTB. If FULLE is a logic zero, a transition to logic one on FULLI will not generate an interrupt on INTB.

Reserved

This bit should be set to logic zero for proper operation.

Register 35CH: TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Unused	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data Register and reads of the TDPR Interrupt Status/UDR Clear Register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-JET Miscellaneous Register (39BH).

LFILLI

The LFILLI bit will transition to logic one when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold Register. LFILLI will assert INTB if it is a logic one and LFILLE is programmed to logic one. LFILLI is cleared when this register is read.

UDRI

The UDRI bit will transition to logic one when the TDPR FIFO underruns. That is, the TDPR is in the process of transmitting a packet when it runs out of data to transmit. UDRI will assert INTB if it is a logic one and UDRE is programmed to logic one. UDRI is cleared when this register is read.

OVRI

The OVRI bit will transition to logic one when the TDPR FIFO overruns. That is, the TDPR FIFO is already full when another data byte is written to the TDPR Transmit Data Register. OVRI will assert INTB if it is a logic one and OVRE is programmed to logic one. OVRI is cleared when this register is read.

FULLI

The FULLI bit will transition to logic one when the TDPR FIFO is full. FULLI will assert INTB if it is a logic one and FULLE is programmed to logic one. FULLI is cleared when this register is read.

BLFILL

The BLFILL bit is set to logic one if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic one, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 35DH: TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data Register and reads of the TDPR Interrupt Status/UDR Clear Register should not occur at rates greater than 1/8th that of the clock selected by the LINESYSCLK bit of the S/UNI-JET Miscellaneous Register (39BH).

TD[7:0]

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 360H: RXCP-50 Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	HCSDQDB	0
Bit 0	R/W	DISCOR	0

DISCOR

The DISCOR bit controls the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single-bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

HCSDQDB

The HCSDQDB bit enables HCS checking for either ATM type cells or DQDB type cells. When logic zero, ATM type cells are processed by checking all four octets in the header for HCS validation. When logic one, DQDB cells are processed by checking only three of the header octets (octets 2, 3 and 4) for HCS validation.

HCSADD

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HDSCR

HDSCR enables the self-synchronous $x^{43} + 1$ descrambler to continue running through the bytes which should contain the ATM cell headers. When HDSCR is set to logic zero, the descrambling polynomial will function only over the ATM payload bytes. When HDSCR is set to logic one, the descrambling polynomial will function over all bytes, including the five ATM header bytes. This function is available for use with PPP packets and flags which are scrambled at the source to prevent the generation of "killer" sequences.

DDSCR

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set to logic one, cell payload descrambling is disabled. When DDSCR is set to logic zero, payload descrambling is enabled.

Register 361H: RXCP-50 Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	CCDIS	0
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	IN52	0
Bit 3	R/W	ALIGN[1]	0
Bit 2	R/W	ALIGN[0]	0
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]

The HCS filter bits, HCSFTR[1:0] indicate the number of consecutive error-free cells required, while in detection mode, before reverting back to correction mode. Refer to Table 20.

Table 20   RXCP-50 HCS Filtering Configurations

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell acceptance. This cell is accepted.
01	Two ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.

ALIGN[1:0]

ALIGN[1:0] configures the RXCP-50 to perform cell delineation based on byte, nibble, or bit wide search algorithms when ATM Direct Mapping is used. Cell alignment is relative to overhead bits in the serial input data stream. The ALIGN[1:0] bits are valid only if ATM direct mapping is used. PLCP framing must be disabled. The Recommended settings for DS3, E3, and J2 are shown in Table 21.

Table 21   RXCP-50 Cell Delineation Algorithm Base

ALIGN[1:0]	Cell Delineation Algorithm base
00	Bit
01	Nibble (DS3)
10	Byte (E3,J2, E1, T1)
11	Unused

IN52

The IN52 bit defines the number of bytes contained in incoming cells. When IN52 is a logic zero, incoming cells are 53-bytes in length. When IN52 is a logic one, incoming cells are 52-bytes in length. In order for ATM cell delineation to function properly, incoming cells must be 53-bytes in length including a valid HCS byte. The HCS byte can be stripped off on the Utopia side using the DS27_53 register bit. If the S/UNI QJET is operating in PPP mode, incoming "cells" may be composed of 52 or 53 bytes without an HCS byte. In this case, the CCDIS register bit should be set to disable cell delineation, and the DS27_53 register bit should be set so that it is consistent with IN52.

IDLEPASS

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic zero, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic one, the Idle Cell Header Pattern and Mask Registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

HCSPASS

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the correction mode.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the CCDIS bit in this register is set to logic one.

CCDIS

The CCDIS bit can be used to disable all cell filtering and cell delineation. All payload data read by the RXCP-50 is passed into its FIFO without the requirement of having to find cell delineation first. If PLCP framing is disabled, then alignment of the data read out of the ATM interface with respect to the line overhead is set by the ALIGN[1:0] bits of this register.

Register 362H: RXCP-50 FIFO/UTOPIA Control & Configuration

Bit	Type	Function	Default
Bit 7	R/W	RXPTYP	0
Bit 6		Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and further writes into the FIFO are ignored (no incoming ATM cells will be stored in the FIFO). The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

See section 12.8 on resetting the receive and transmit FIFOs.

RCALEVEL0

The RCALEVEL0 register bit selects the behavior of RCA and DRCA[x] when they de-assert (transition to logic zero if RCAINV is logic zero, or transition to logic one if RCAINV is logic one) as the receive FIFO empties.

When RCALEVEL0 is set to logic one, DRCA[x] and RCA indicates that the receive FIFO is empty. RCA (and DRCA[x]), if polled, will de-assert on the rising RFCLK edge after Payload byte 48 (ATM8=1) or Payload byte 24 (ATM8=0) is output.

When RCALEVEL0 is set to logic zero, DRCA[x] and RCA, if polled, indicates that the receive FIFO is near empty. DRCA[x] and RCA, if polled, will de-assert on the rising RFCLK edge after Payload byte 43 (ATM8=1) or Payload byte 19 (ATM8=0) is output.

RCAINV

The RCAINV bit inverts the polarity of the DRCA[x] and RCA output signal. When RCAINV is a logic one, the polarity of DRCA[x] and RCA is inverted (DRCA[x] and RCA at logic zero means there is a receive cell available to be read). When RCAINV is a logic zero, the polarity of RCA and DRCA[x] is not inverted.

RXPTYP

The RXPTYP bit selects even or odd parity for output RXPRTY. When set to logic one, output RXPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set to logic zero, RXPRTY is the odd parity bit for outputs RDAT[15:0].

Register 363H: RXCP-50 Interrupt Enables and Counter Status

Bit	Type	Function	Default
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5		Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set to logic one, the interrupt is enabled.

FOVRE

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set to logic one, the interrupt is enabled.

HCSE

The HCSE bit enables the generation of an interrupt due to the detection of a corrected or an uncorrected HCS error. When HCSE is set to logic one, the interrupt is enabled.

OOCDE

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set to logic one, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP-50 Count Registers. When XFERE is set to logic one, the interrupt is enabled.

OVR

The OVR bit is the overrun status of the RXCP-50 Performance Monitoring Count Registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP-50 Count Registers have been overwritten. OVR is set to logic zero when this register is read.

XFERI

The XFERI bit indicates that a transfer of RXCP-50 Performance Monitoring Count data has occurred. A logic one in this bit position indicates that the RXCP-50 Count Registers have been updated. This update is initiated by writing to one of the RXCP-50 Count Register locations or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register. XFERI is set to logic zero when this register is read.

Register 364H: RXCP-50 Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI

The FOVRI bit is set to logic one when a FIFO overrun occurs. This bit is reset immediately after a read to this register. No further FIFO overrun indications will occur until the condition which caused the original overrun has cleared. In the case where continuous FIFO overruns are occurring, only a single overrun indication (FOVRI -> '1') will be recorded until the overruns cease.

UHCSI

The UHCSI bit is set high when an uncorrected HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI

The CHCSI bit is set high when a corrected HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI

The OOCDI bit is set high when the RXCP-50 enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP-50 is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV

The LCDV bit gives the Loss of Cell Delineation state. When LCD is logic one, an out of cell delineation (OCD) defect has persisted for the number of cells specified in the LCD Count Threshold Register. When LCD is logic zero, no OCD has persisted for the number of cells specified in the LCD Count Threshold Register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP-50 LCD Count Threshold Register.

OOCDV

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 365H: RXCP-50 LCD Count Threshold (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 366H: RXCP-50 LCD Count Threshold (LSB)

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not de-asserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to the integration periods shown in Table 22.

Table 22 RXCP-50 LCD Integration Periods

Format	Average cell period	Default LCD integration period
DS3 Direct Mapping	9.59 µs	3.45 ms
DS3 PLCP	10.42 µs	3.75 ms
E3 G.751 Direct Mapping	12.46 µs	4.49 ms
E3 G.751 PLCP	13.89 µs	5.00 ms
E3 G.832	12.50 µs	4.50 ms
J2 Direct Mapping	69.01 µs	24.84 ms
DS1 Direct Mapping	276.00 µs	99.40 ms

Format	Average cell period	Default LCD integration period
DS1 PLCP	300.00 us	108.00 ms
E1 Direct Mapping	220.83 µs	79.50 ms
E1 PLCP	237.50 µs	85.50 ms

Register 367H: RXCP-50 Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[3]	0
Bit 2	R/W	PTI[2]	0
Bit 1	R/W	PTI[1]	0
Bit 0	R/W	CLP	1

GFC[3:0]

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note: An all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 368H: RXCP-50 Idle Cell Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[2]	1
Bit 2	R/W	MPTI[1]	1
Bit 1	R/W	MPTI[0]	1
Bit 0	R/W	MCLP	1

MGFC[3:0]

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI[3:0]

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 369H: RXCP-50 Corrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]

The CHCS[7:0] bits indicate the number of corrected HCS error events that occurred during the last accumulation interval. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (Registers 369H – 371H) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H).

Register 36AH: RXCP-50 Uncorrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (Registers 369H – 371H) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H).

Register 36BH: RXCP-50 Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 36CH: RXCP-50 Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 36DH: RXCP-50 Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[18:0]

The RCELL[18:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (Registers 369H – 371H) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H).

Register 36EH: RXCP-50 Idle Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 36FH: RXCP-50 Idle Cell Counter

Bit	Type	Function	Default
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 370H: RXCP-50 Idle Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[18:0]

The ICELL[18:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation. The contents of these registers are valid after 24 RCLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to one of RXCP-50's performance monitor counters (Registers 369H – 371H) or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H).

Register 380H: TXCP-50 Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	HSCR	0
Bit 4	R/W	HCSDQDB	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the FIFO.

See Section 13.9on resetting the receive and transmit FIFOs.

DSCR

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled. In the case where HSCR is logic one, the payload will be scrambled (along with the header) regardless of the setting of the DSCR bit.

HCSADD

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is generated and inserted internally. When the HCSB and DS27_53 register bits are logic one, the HCS octet read from the transmit FIFO is inserted transparently into the transmit cell stream, but the TXCP-50 will still generate and insert the HCS octet for idle cells. If HCSB is logic one and the 26-byte word data structure is selected (DS27_53 is logic zero), then no HCS octet is inserted in the transmit data stream.

HCSDQDB

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic one is written to HCSDQDB, header octets two, three, and four are included in the HCS calculation as required by IEEE-802.6 DQDB specification. When a logic zero is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification and ITU-T Recommendation I.432.

HSCR

The Header Scramble enable bit, HSCR, enables scrambling of the ATM five octet header along with the payload. When set to logic one, the ATM header and payload are both scrambled. When set to logic zero, the header is left unscrambled and payload scrambling is determined by the DSCR bit.

TCALEVEL0

The active high TCA (and DTCA[x]) level 0 bit, TCALEVEL0 determines what output TCA (and DTCA[x]) indicates when it de-asserts (transitions to logic zero if TCAINV is logic zero, or transitions to logic one if TCAINV is logic one).

When TCALEVEL0 is set to logic one, TCA (and DTCA[x]) indicates that the transmit FIFO is full and can accept no more writes. DTCA[x] and TCA, if polled, will de-assert on the rising TFCLK edge when Payload byte 47 (ATM8=1) or Payload word 23 (ATM8=0) is sampled.

When TCALEVEL0 is set to logic zero, TCA (and DTCA[x]) indicates that the transmit FIFO is near full. DTCA[x] and TCA, if polled, will de-assert on the rising TFCLK edge when Payload byte 43 (ATM8=1) or Payload word 19 (ATM8=0) is sampled.

TPTYP

The TPTYP bit selects even or odd parity for input TPRTY. When set to logic one, input TPRTY is the even parity bit for the TDAT input bus. When set to logic zero, input TPRTY is the odd parity bit for the TDAT input bus. When ATM8 is set to logic one, the input bus consists of TDAT[7:0]. When ATM8 is logic zero, the input bus consists of TDAT[15:0].

Register 381H: TXCP-50 Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27-byte word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

DHCS

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-byte word data structure.

FIFODP[1:0]

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA and DTCA[x] de-assert. FIFO depth control may be important in systems where the cell latency through the TXCP-50 must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA (and DTCA[x]) is de-asserted. Note: Regardless of what fill level FIFODP[1:0] is set to, the transmit cell processor can store four complete cells. The selectable FIFO cell depths are shown in Table 23:

Table 23   TXCP-50 FIFO Depth Configurations

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV

The TCAINV bit inverts the polarity of the TCA (and DTCA[x]) output signal. When TCAINV is a logic one, the polarity of TCA (and DTCA[x]) is inverted (TCA (and DTCA[x]) at logic zero means there is transmit cell space available to be written to). When TCAINV is a logic zero, the polarity of TCA (and DTCA[x]) is not inverted.

Register 382H: TXCP-50 Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

These bits should be set to their default values for proper operation

XFERI

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic one in this bit position indicates that the Transmit Cell Count Registers have been updated. This update is initiated by writing to one of the Transmit Cell Count Register locations or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register. XFERI is set to logic zero when this register is read.

OVR

The OVR bit is the overrun status of the Transmit Cell Count Registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count Registers have been overwritten. OVR is set to logic zero when this register is read.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count Registers. When XFERE is set to logic one, the interrupt is enabled.

Register 383H: TXCP-50 Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FOVRI

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register

TPRTYI

The TPRTYI bit indicates if a parity error was detected on the TDAT input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT bus. The active TDAT bus is TDAT[15:0] when ATM8 is tied low and is TDAT[7:0] when ATM8 is tied high. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYPE bit.

TSOCE

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

FOVRE

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INT and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI but are not indicated on output INT.

Register 384H: TXCP-50 Idle Cell Header Control

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO.

PTI[3:0]

The PTI[3:0] bits contains the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP-50 detects that no outstanding cells exist in the transmit FIFO. The all-zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 385H: TXCP-50 Idle Cell Payload Control

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are inserted when the TXCP-50 detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 386H: TXCP-50 Transmit Cell Count (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 387H: TXCP-50 Transmit Cell Count

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 388H: TXCP-50 Transmit Cell Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[18:0]

The TCELL[18:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted.

A write to any one of the TXCP-50 Transmit Cell Counter Registers or to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H) loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter Registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid after 24 TICLK periods containing cell header or payload data (line or PLCP overhead periods do not count) after a transfer is triggered by a write to a TXCP-50 Transmit Cell count Register or the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H).

Register 390H: TTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	Reserved	0

Reserved

The reserved bit should be set to logic zero for proper operation.NOSYNC

The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set low, the TTB synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL

The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5

The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE

The receive trace identifier mismatch interrupt enable (RTIMIE) controls the activation of the interrupt output when comparison between the accepted trace identifier message and the expected trace identifier message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state will activate the interrupt output. When RTIMIE set low, trail trace message match state changes will not affect INTB.

RTIUIE

The receive trace identifier unstable interrupt enable (RTIUIE) control the activation of the interrupt output when the receive trace identifier message changes state from stable to unstable and vice versa. When RTIUIE is set high, changes in the state of the trail trace message unstable indication will activate the interrupt output. When RTIUIE set low, trail trace unstable state changes will not effect INTB.

RRAMACC

The receive RAM access (RRAMACC) control bit is used by the microprocessor to identify that the access from the microprocessor is to the receive trace buffers (addresses 0 - 127) or to the transmit trace buffer (addresses 128 - 191). When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all-zeros path trace message string. When ZEROEN is set high, all-zeros path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all-zeros path trace message strings are ignored.

Register 391H: TTB Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV

The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. RTIMV is set low when the accepted message is equal to the expected message. A mismatch is not declared if the accepted trail trace message string is all-zeros.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

RTIUV

The receive trace identifier unstable value status bit (RTIUV) is set high when eight messages that differ from its immediate predecessor are received. RTIUV is set low and the unstable message count is reset when three or five (depending on PER5 control bit) consecutive identical messages are received.

RTIUI

The receive trace identifier unstable indication status bit (RTIUV) is set high when the stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the trail trace RAM has been completed. BUSY is set high upon writing to the TTB Indirect Address Register, and stays high until the access has completed. At this point, BUSY is set low. This register should be polled to determine when either new data is available in the TTB Indirect Data Register after an indirect read, or when the TTB is ready to accept another write access.

Register 392H: TTB Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[6:0]

The indirect read address bits (A[6:0]) indexes into the trail trace identifier buffers. When RRAMACC is set high, decimal addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive G.832 E3 stream. The receive expected page contains the expected trace identifier message downloaded from the microprocessor. When RRAMACC is set low, decimal addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the TR bytes of the G.832 E3 transmit stream. In this case A[6] is a don't care (for example, address 0 and address 64 are indexes to the same location in the buffer). Note: Only the first 16 addresses need to be written with the trail trace message to be transmitted.

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the trail trace message buffer. Writing to this indirect address register initiates an external microprocessor access to the static page of the trail trace message buffer. When RWB is set high, a read access is initiated. The data read is available upon completion of the access in the TTB Indirect Data Register. When RWB is set low, a write access is initiated. The data in the TTB Indirect Data Register will be written to the addressed location in the static page.

Register 393H: TTB Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]

The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note: The write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

Register 394H: TTB Expected Payload Type Label

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]

The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on Table 24:

Table 24 TTB Payload Type Match Configurations

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

Note

1.   XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Reserved

The reserved bits must be written to logic zero for proper operation.

Register 395H: TTB Payload Type Label Control/Status

Bit	Type	Function	Default
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV

The receive payload type label mismatch status bit (RPLDMV) reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received payload type bits differ from the expected payload type written to the TTB Expected Payload Type Label Register. The PLDMV bit is set low when the received payload type matches the expected payload type.

RPLDMI

The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch status between the received and the expected payload type label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDUV

The receive payload type label unstable status bit (RPLDUV) reports the stable/unstable status of the payload type label bits in the receive stream. RPLDUV is set high when five labels that differ from its immediate predecessor are received. RPLDUV is set low and the unstable label count is reset when five consecutive identical labels are received.

RPLDUI

The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDMIE

The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls the activation of the interrupt output when the comparison between received and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state activates the interrupt output. When RPLDMIE is set low, changes from match to mismatch or mismatch to match will not generate an interrupt.

RPLDUIE

The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of the interrupt output when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state activates the interrupt output. When RPLDUIE is set low, changes in the stable state will not generate and interrupt.

Register 398H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE

The FEACE bit enables the generation of an interrupt when a valid FEAC(FEAC) code is detected. When a logic one is written to FEACE, the interrupt generation is enabled.

AVC

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic zero is written to AVC, a FEAC code is validated when eight out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic one is written to AVC, a FEAC code is validated when four out of the last five received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic one is written to IDLE, the interrupt generation is enabled.

Register 399H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]

The FEAC[5:0] bits contain the received FEAC channel codes. The FEAC[5:0] bits are set to all-ones ("111111") when no code has been validated.

FEACI

The FEACI bit is set to logic one when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic zero when this register is read.

IDLI

The IDLI bit is set to logic one when a validated FEAC code is removed. The FEAC[5:0] bits are set to all-ones when the code is removed. The IDLI bit position is set to logic zero when this register is read.

Register 39AH: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]

FEAC[5:0] contain the six bit code that is transmitted on the FEAC channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of eight ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, .., FEAC5, followed by a zero. The all-ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all ones.

Note: If configured for J2 transmission format (TFRM[1:0] is 10 binary) and any of LCDEN, AISEN, OOFEN, LOSEN are set to logic one in the S/UNI-JET Data Link and FERF/RAI Control, FEAC[5:0] in this register must all be set to logic one for proper RAI transmission upon detection of LCD, PHYAIS, LOF, or LOS by the J2 FRMR. Otherwise, the BOC code configured by the FEAC[5:0] bits of this register will be transmitted instead of the RAI.

Register 39BH: S/UNI-JET Miscellaneous

Bit	Type	Function	Default
Bit 7	R/W	AISOOF	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TPRBS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TCELL	0
Bit 2	R/W	LOC_RESET	0
Bit 1	R/W	FORCELOS	0
Bit 0	R/W	LINESYSCLK	0

LINESYSCLK

LINESYSCLK is used to select the high-speed system clock which the TDPR and RDLC transmit and receive HDLC controllers use as a reference. If LINESYSCLK is set to logic one, then the RDLC uses the receive line clock (RCLK[x]) and the TDPR uses the transmit line clock (TICLK[x]) as its high-speed system reference clock respectively. If LINESYSCLK is set to logic zero, the RDLC uses the receive ATM Utopia interface clock (RFCLK) and the TDPR uses the transmit ATM Utopia interface clock (TFCLK) as its high-speed system reference clock respectively.

The read/write access rate to the RDLC and TDPR are limited by their high-speed reference clock frequency. Data and Configuration settings can be written into the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the TDPR at a maximum rate equal to 1/8 of its high-speed reference clock frequency. Data and status indications can be read from the RDLC at a maximum rate equal to 1/10 of its high-speed reference clock frequency.

Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read and write the TDPR and RDLC Registers.

FORCELOS

FORCELOS is used to force a LOS condition on the transmit unipolar or bipolar data outputs TPOS/TDATO[x] and TNEG[x]. When FORCELOS is logic one, the TPOS/TDATO[x] and TNEG[x] outputs will be forced to logic zero. When FORCELOS is logic zero, the TPOS/TDATO[x] and TNEG[x] outputs will operate normally.

LOC_RESET

LOC_RESET performs a software local reset of the corresponding quadrant of the S/UNI-JET . When LOC_RESET is logic one, the corresponding quadrant of the S/UNI-JET is held in a reset state. When LOC_RESET is logic zero, the quadrant is in normal operational mode.

The LOC_RESET bit for quadrant 1 (Register 09BH) also resets the chip level Utopia bus. While the LOC_RESET for quadrant 1 is set to logic one, the S/UNI-JET's Utopia bus will be held in a reset state, and will not function. In applications where the Utopia bus is required, the LOC_RESET for quadrant 1 should not be permanently set to logic one.

TCELL

When the TCELL bit is a logic one, the TPOHFP/TFPO/TMFPO/TGAPCLK/TCELL pin takes on the TCELL function, and pulses once for every transmitted cell (idle or unassigned).

Reserved

The reserved bit should be set to logic zero for proper operation.

TPRBS

register bit TPRBS is used to insert a pseudo-random binary sequence into the transmit stream in place of other payload data. The exact nature of the PRBS is configurable through the PRGD Registers (xA0H to xAFH).

Reserved

The reserved bit should be set to logic zero for proper operation.

AISOOF

The AISOOF bit allows the receive data output stream on RDATO to be forced to all 1's when the DS3, E3, or J2 FRMR loses frame. When AISOOF is set to logic one, RDATO[x] will be forced to all 1's when frame alignment is lost. When AISOOF is set to logic zero, RDATO will continue to output raw data even when frame alignment is lost.

Note: AISOOF is only valid in framer-only mode (FRMRONLY=1, S/UNI-JET Configuration 1 Register).

Register 39CH: S/UNI-JET FRMR LOF Status.

Bit	Type	Function	Default
Bit 7	R	FRMLOF	X
Bit 6	R/W	FRMLOFE	0
Bit 5	R	FRMLOFI	X
Bit 4	R/W	J2SIGTHRU	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

FRMLOFI

The FRMLOFI bit shows that a transition has occurred on the FRMLOF state. When FRMLOFI is logic one, the FRMLOF state has changed since the last read of this register. The FRMLOFI bit is cleared whenever this register is read.

FRMLOFE

The FRMLOFE bit enables the generation of an interrupt due to a change in the FRMLOF state. When FRMLOFE is a logic one, the interrupt is enabled.

FRMLOF

The FRMLOF bit shows the current state of the E3/T3 LOF or the J2 Extended LOF indication (depending on which mode is enabled). When FRMLOF is logic one, the framer has lost frame synchronization for greater than 1ms, 2ms, or 3ms depending on the setting of the LOFINT[1:0] bits in the S/UNI-JET Receive Configuration Register.

J2SIGTHRU

The J2SIGTHRU bit allows the signaling bits in timeslot 97 and 98 on the TDATI stream to pass transparently through the J2 TRAN. When J2SIGTHRU is logic one, timeslots 97 and 98 are passed transparently through from TDATI. When J2SIGTHRU is logic zero, timeslots 97 and 98 are sourced from the J2 TRAN TS97 Signaling and J2 TRAN TS98 Signaling Registers.

If J2SIGTHRU is set to logic one and TPRBS (S/UNI-JET Miscellaneous Register) is also set to logic one, the transmitted PRBS will continue through timeslots 97 and 98.

J2SIGTHRU is only valid in framer-only mode (FRMRONLY=1, S/UNI-JET Configuration 1 Register).

Reserved

The Reserved bit must be programmed to logic zero for correct operation.

Register 3A0H: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]

The PDR[1:0] bits select the content of the four pattern detector registers (at addresses xACH to xAFH) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in Table 25:

Table 25   PRGD Pattern Detector Register Configuration

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count(MSB)

QRSS

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic one, a one is forced in the TDATO stream when the following 14 bit positions are all zeros. When QRSS is a logic zero, the zero suppression feature is disabled.

PS

The PS bit selects the generated pattern. When PS is a logic one, a repetitive pattern is generated. When PS is a logic zero, a pseudo-random pattern is generated.

The PS bit must be programmed to the desired setting before programming any other PRGD registers, or the transmitted pattern may be corrupted. Any time the setting of the PS bit is changed, the rest of the PRGD registers should be reprogrammed.

TINV

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic one, the data is inverted. When TINV is a logic zero, the data is not inverted

RINV

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic one, the received data is inverted before being processed by the pattern detector. When RINV is a logic zero, the received data is not inverted

AUTOSYNC

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when six or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic one, the auto resync feature is enabled. When AUTO SYNC is a logic zero, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low-to-high transition on MANSYNC initiates the resynchronization.

Register 3A1H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic one, the interrupt is enabled.

BEE

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic one, the interrupt is enabled.

XFERE

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic one, the interrupt is enabled.

SYNCV

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic one the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error-free bit periods). When SYNCV is a logic zero, the pattern detector is out-of-sync (the pattern detector has detected six or more bit errors in a 64 bit period window).

SYNCI

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic one, then the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic zero when this register is read.

BEI

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic one, at least one bit error has been detected. BEI is set to logic zero when this register is read.

XFERI

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic one in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register (006H). XFERI is set to logic zero when this register is read.

OVR

The OVR bit is the overrun status of the pattern detector registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic zero when this register is read.

Register 3A2H: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 3A3H: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 3A4H: PRGD Error Insertion Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT

A low-to-high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in Table 26:

Table 26   PRGD Generated Bit Error Rate Configurations

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 3A8H: Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 3A9H: Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 3AAH: Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 3ABH: Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]

> PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] should be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written.

Register 3ACH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R	PD[7]	0
Bit 6	R	PD[6]	0
Bit 5	R	PD[5]	0
Bit 4	R	PD[4]	0
Bit 3	R	PD[3]	0
Bit 2	R	PD[2]	0
Bit 1	R	PD[1]	0
Bit 0	R	PD[0]	0

Register 3ADH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R	PD[15]	0
Bit 6	R	PD[14]	0
Bit 5	R	PD[13]	0
Bit 4	R	PD[12]	0
Bit 3	R	PD[11]	0
Bit 2	R	PD[10]	0
Bit 1	R	PD[9]	0
Bit 0	R	PD[8]	0

Register 3AEH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R	PD[23]	0
Bit 6	R	PD[22]	0
Bit 5	R	PD[21]	0
Bit 4	R	PD[20]	0
Bit 3	R	PD[19]	0
Bit 2	R	PD[18]	0
Bit 1	R	PD[17]	0
Bit 0	R	PD[16]	0

Register 3AFH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R	PD[31]	0
Bit 6	R	PD[30]	0
Bit 5	R	PD[29]	0
Bit 4	R	PD[28]	0
Bit 3	R	PD[27]	0
Bit 2	R	PD[26]	0
Bit 1	R	PD[25]	0
Bit 0	R	PD[24]	0

PD[31:0]

    PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the control register.

    When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0}. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

    When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note: Bit errors are not accumulated while the pattern detector is out-of-sync.

    When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

    The values of PD[31:0] are updated whenever one of the four PRGD Pattern Detector Registers is written or when Register 006H, the S/UNI-JET Identification, Master Reset, and Global Monitor Update Register is written.

Register 40CH: S/UNI-JET Identification Register

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Device_ID	1
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register provides a device identification to distinguish the S/UNI-JET from a S/UNI-QJET in applications where the S/UNI-QJET is used for prototype purposes.

DEVICE_ID

The DEVICE_ID bit allows software to identify the device as a S/UNI-JET. A logic one identifies the device as a S/UNI-JET, whereas a logic zero identifies the device as a S/UNI-QJET. To access this register, the IOTST bit in the S/UNI-JET Master Test Register must first be set to logic one. The Device_ID bit can now be read. A logic zero must then be written back to the IOTST bit to put the device back into normal mode of operation.

12 Test Features Description

The test mode registers, shown in Table 27, are used for production and board testing.

During production testing, the test mode registers are used to apply test vectors. In this case, the test mode registers (as opposed to the normal mode registers) are selected when A[10] is high.

During board testing, the digital output pins and the data bus are held in a high-impedance state by simultaneously asserting (low) the CSB, RDB, and WRB inputs. All of the TSBs for the S/UNI-JET are placed in test mode 0 so that device inputs may be read and device outputs may be forced through the microprocessor interface. Refer to the section "Test Mode 0" for details.

Note: The S/UNI-JET supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port that can be used for board testing. All digital device inputs may be read and all digital device outputs may be forced through this JTAG test port.

Table 27   Test Mode Register Memory Map

Address	Register
000H-3FFH	Normal Mode Registers
400H	Master Test Register
708H	SPLR Test Register 0
709H	SPLR Test Register 1
70AH	SPLR Test Register 2
70BH	Reserved
70CH	SPLT Test Register 0
70DH	SPLT Test Register 1
70EH	SPLT Test Register 2
70FH	SPLT Test Register 3
710H	PMON Test Register 0
711H	PMON Test Register 1
712H-71FH	Reserved
720H	CPPM Test Register 0
721H	CPPM Test Register 1
722H	CPPM Test Register 2
723H-72FH	Reserved
730H	DS3 FRMR Test Register 0
731H	DS3 FRMR Test Register 1
732H	DS3 FRMR Test Register 2
733H	DS3 FRMR Test Register 3
734H	DS3 TRAN Test Register 0
735H	DS3 TRAN Test Register 1
736H	DS3 TRAN Test Register 2

Address	Register
737H	Reserved
738H	E3 FRMR Test Register 0
739H	E3 FRMR Test Register 1
73AH	E3 FRMR Test Register 2
73BH-73FH	Reserved
740H	E3 TRAN Test Register 0
741H	E3 TRAN Test Register 1
742H	E3 TRAN Test Register 2
743H	Reserved
744H	J2 FRMR Test Register 0
745H	J2 FRMR Test Register 1
746H	J2 FRMR Test Register 2
747H	J2 FRMR Test Register 3
748H-74BH	Reserved
74CH	J2 TRAN Test Register 0
74DH	J2 TRAN Test Register 1
74EH	J2 TRAN Test Register 2
74FH	J2 TRAN Test Register 3
750H	RDLC Test Register 0
751H	RDLC Test Register 1
752H	RDLC Test Register 2
753H	RDLC Test Register 3
754H	RDLC Test Register 4
755H-757H	Reserved
758H	TDPR Test Register 0
759H	TDPR Test Register 1
75AH	TDPR Test Register 2
75BH	TDPR Test Register 3
75CH-75FH	Reserved
760H	RXCP-50 Test Register 0
761H	RXCP-50 Test Register 1
762H	RXCP-50 Test Register 2
763H	RXCP-50 Test Register 3
764H	RXCP-50 Test Register 4
765H	RXCP-50 Test Register 5
766H-77FH	Reserved
780H	TXCP-50 Test Register 0
781H	TXCP-50 Test Register 1
782H	TXCP-50 Test Register 2

Address	Register
783H	TXCP-50 Test Register 3
784H	TXCP-50 Test Register 4
785H	TXCP-50 Test Register 5
786H-78FH	Reserved
790H	TTB Test Register 0
791H	TTB Test Register 1
792H	TTB Test Register 2
793H-797H	Reserved
798H	RBOC Test Register 0
799H	RBOC Test Register 1
79AH	XBOC Test Register 1
79BH	XBOC Test Register 0
79CH-79FH	Reserved
7A0H	PRGD Test Register 0
7A1H	PRGD Test Register 1
7A2H	PRGD Test Register 2
7A3H	PRGD Test Register 3
7A4H-7FFH	Reserved

Notes

1. Although writing values into unused register bits has no effect, it is recommended, to ensure software compatibility with future, feature-enhanced versions of the device, to write unused register bits with logic zero. Reading back unused bits can produce either a logic one or a logic zero; therefore, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

12.1 Test Mode 0 Details

In test mode 0, the S/UNI-JET allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the S/UNI-JET Master Test Register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the S/UNI-JET Master Test Register is set to logic one and the device should be left in its default state after reset unless otherwise noted. All Test Register 1 locations of all blocks must be written with the value 0. Refer to Table 27.

Reading the address locations shown in Table 28 returns the values on the indicated inputs:

Table 28   Test Mode 0 Input Read Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40CH		Device_ID						
430H								

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
436H								
444H								
465H							RENB[3]	
466H	RADR[2][4]	RADR[1][4]	RADR[0][4]					RFCLK
480H				ATM8				
482H	PHY_ADR[2]	TADR[2][1]			TSOC	TENB[2]	TPRTY	TFCLK
483H	PHY_ADR[1]	PHY_ADR[0]			TADR[1][1]	TADR[0][1]		
484H	TDAT[15]	TDAT[14]	TDAT[13]	TDAT[12]	TDAT[11]	TDAT[10]	TDAT[9]	TDAT[8]
485H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
50CH								
50FH								REF8KI
530H								
536H								
544H								
565H								
60CH								
630H								
636H								
644H								
665H							RADR[0][4]	
70CH		TIOHM	TICLK	TPOH	TPOHINS			
730H								RCLK
736H							TOH	TOHINS
744H					RPOS	RNEG		
765H							RADR[1][4]	

Notes

1. Before reading these values, the input must be set to the test state, TENB must be set to logic one, and TFCLK must transition from logic zero to logic one.

2. Before its value will be captured in the test register, TENB must be set to its test state and TFCLK must transition from logic zero to logic one.

3. Before its value will be captured in the test register RENB must be set to its test state and RFCLK must transition from logic zero to logic one.

4. Before reading these values, the input must be set to the test state, RENB must be set to logic one, and RFCLK must transition from logic zero to logic one.

Writing the address locations shown in Table 29 forces the outputs to the value in the corresponding bit position. Note: Zeros should be written to all unused test register locations.

Table 29 Test Mode 0 Output Write Address Locations

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
408H								
40AH								INTB[1]
40CH								
410H								INTB[1]
430H	INTB[1]							
434H								
436H								
432H								
433H								
44CH								
44EH								
450H								INTB[1]
458H								INTB[1]
463H	RDAT[15][2]	RDAT[14][2]	RDAT[13][2]	RDAT[12][2]	RDAT[11][2]	RDAT[10][2]	RDAT[9][2]	RDAT[8][2]
464H	RDAT[7][2]	RDAT[6][2]	RDAT[5][2]	RDAT[4][2]	RDAT[3][2]	RDAT[2][2]	RDAT[1][2]	RDAT[0][2]
465H			RSOC[2]	RPRTY[2]	RCA[3]		INTB[1]	
480H								INTB[1]
490H								INTB[1]
498H		INTB[1]						
4A2H							INTB[1]	
508H								
50AH								INTB[1]
50CH								
510H								INTB[1]
530H	INTB[1]							
534H								
536H								
532H								
533H								
54CH								
54EH								
550H								INTB[1]
558H								INTB[1]
565H			RSOC[2]	RPRTY[2]			INTB[1]	
580H								INTB[1]
590H								INTB[1]
598H		INTB[1]						

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5A2H							INTB[1]	
608H								
60AH								INTB[1]
60CH								
610H								INTB[1]
630H	INTB[1]							
634H								
636H								
632H								
633H								
64CH								
64EH								
650H								INTB[1]
658H								INTB[1]
665H			RSOC[2]	RPRTY[2]			INTB[1]	
680H								INTB[1]
690H								INTB[1]
698H		INTB[1]						
6A2H							INTB[1]	
708H					RPOHCLK	RPOH	REF8KO	
70AH	FRMSTAT							INTB[1]
70CH						TPOHFP	TPOHCLK	
710H								INTB[1]
730H	INTB[1]							
734H								TCLK
736H							TOHFP	TOHCLK
732H			ROH					ROHCL]
733H				ROHFP				
74CH	TPOS							
74EH								TNEG
750H								INTB[1]
758H								INTB[1]
765H		LCD	RSOC[2]	RPRTY[2]		DRCA	INTB[1]	
780H						DTCA		INTB[1]
790H								INTB[1]
798H		INTB[1]						
7A2H							INTB[1]	

Notes

1. All these register bits must be set to logic zero for the INTB output to be tri-stated. If any one of these register bits is a logic one, then INTB will be driven to logic zero.

2. To enable these outputs, after setting the desired state, RADR[0] must be set to logic zero, RENB must be set to logic one, bit 4 of register 09BH must be set to logic one, and RFCLK must transition from logic zero to logic one.

3. To enable this output, after setting the desired state, RADR[2:0] must be set equal to PHY_ADR[2:0], RADR[1:0] must be set equal to binary 00, RFCLK must transition from logic zero to logic one.

4. To enable this output, after setting the desired state, TADR[2:0] must be set equal to PHY_ADR[2:0], TADR[1:0] must be set equal to binary 00, TFCLK must transition from logic zero to logic one.

5. Bit 1 of this register must be logic zero.

12.2   JTAG Test Port

The S/UNI-JET JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. TAP enables the following:

- Reading device input logic levels.

- Forcing device output.

- Identifying the device.

- Bypassing the device scan path.

For more details on the JTAG port, please refer to the **Error! Reference source not found.** section.

Table 30   Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 31   Identification Register

Length	32 bits
Version number	2H
Part Number	7346H
Manufacturer's identification code	0CDH
Device identification	273460CDH

Table 32   Boundary Scan Register

Length - 198 bits

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
TDAT[15][1]	0	IN_CELL	0	TPOHFP	87	OUT_CELL	(0)
TDAT[14]	1	IN_CELL	0	Unconnected	88:90	OUT_CELL	(0)
TDAT[13]	2	IN_CELL	1	LCD	91	OUT_CELL	(0)
TDAT[12]	3	IN_CELL	0	Unconnected	92:94	OUT_CELL	(0)
TDAT[11]	4	IN_CELL	0	RPOH	95	OUT_CELL	(0)
TDAT[10]	5	IN_CELL	1	Unconnected	96:98	OUT_CELL	(0)
TDAT[9]	6	IN_CELL	1	RPOHCLK	99	OUT_CELL	(0)
TDAT[8]	7	IN_CELL	1	Unconnected	100:102	OUT_CELL	(0)
TDAT[7]	8	IN_CELL	0	REF8KO	103	OUT_CELL	(0)
TDAT[6]	9	IN_CELL	0	Unconnected	104:106	OUT_CELL	(0)
TDAT[5]	10	IN_CELL	1	FRMSTAT	107	OUT_CELL	(0)
TDAT[4]	11	IN_CELL	1	Unconnected	108:110	OUT_CELL	(0)
TDAT[3]	12	IN_CELL	0	REF8KI	111	IN_CELL	(0)
TDAT[2]	13	IN_CELL	1	ROHCLK	112	OUT_CELL	(0)
TDAT[1]	14	IN_CELL	0	Unconnected	113;115	OUT_CELL	(0)
TDAT[0]	15	IN_CELL	0	ROHFP	116	OUT_CELL	(0)
TFCLK	16	IN_CELL	0	Unconnected	117:119	OUT_CELL	(0)
Tied to '1'	17	IN_CELL	1	ROH	120	OUT_CELL	(0)
Tied to '1'	18	IN_CELL	1	Unconnected	121:123	OUT_CELL	(0)
TADR[2]	19	IN_CELL	0	TOHFP	124	OUT_CELL	(0)
TADR[1]	20	IN_CELL	0	Unconnected	125:127	OUT_CELL	(0)
TADR[0]	21	IN_CELL	0	TOHCLK	128	OUT_CELL	(0)
TPRTY	22	IN_CELL	0	Unconnected	129:131	OUT_CELL	(0)
TSOC	23	IN_CELL	0	TOHINS	132	IN_CELL	(0)
TENB	24	IN_CELL	1	Tied to '0'	133:135	IN_CELL	(0)
TCA	25	OUT_CELL	1	TOH	136	IN_CELL	(0)
TCA_OEB[2]	26	OUT_CELL	0	Tied to '0'	137:139	IN_CELL	(0)
DTCA	27	OUT_CELL	0	RCLK	140	IN_CELL	(0)
Unconnected	28	OUT_CELL	1	Tied to '0'	141:143	IN_CELL	(0)

Pin/Enable	Register Bit	Cell Type	ID Bit	Pin/Enable	Register Bit	Cell Type	ID Bit
Unconnected	29	OUT_CELL	1	RNEG	144	IN_CELL	(0)
Unconnected	30	OUT_CELL	0	Tied to '0'	145;147	IN_CELL	(0)
PHY_ADR[2]	31	IN_CELL	1	RPOS	148	IN_CELL	(0)
PHY_ADR[1]	32	IN_CELL	(1)	Tied to '0'	149:151	IN_CELL	(0)
PHY_ADR[0]	33	IN_CELL	(1)	TCLK	152	OUT_CELL	(0)
ATM8	34	IN_CELL	(0)	Unconnected	153:155	OUT_CELL	(0)
DRCA	35	OUT_CELL	(0)	TNEG	156	OUT_CELL	(0)
Unconnected	36	OUT_CELL	(0)	Unconnected	157:159	OUT_CELL	(0)
Unconnected	37	OUT_CELL	(0)	TPOS	160	OUT_CELL	(0)
Unconnected	38	OUT_CELL	(0)	Unconnected	161:163	OUT_CELL	(0)
RCA	39	OUT_CELL	(0)	INTB	164	OUT_CELL	(0)
RCA_OEB[3]	40	OUT_CELL	(0)	RSTB	165	IN_CELL	(0)
RSOC	41	OUT_CELL	(0)	WRB	166	IN_CELL	(0)
RENB	42	IN_CELL	(0)	RDB	167	IN_CELL	(0)
RFCLK	43	IN_CELL	(0)	ALE	168	IN_CELL	(0)
Tied to '1'	44	IN_CELL	(0)	CSB	169	IN_CELL	(0)
Tied to '1'	45	IN_CELL	(0)	A[10:0]	170:180	IN_CELL	(0)
RADR[2]	46	IN_CELL	(0)	D[7]	181	IO_CELL	(0)
RADR[1]	47	IN_CELL	(0)	DOENB [7][5]	182	OUT_CELL	(0)
RADR[0]	48	IN_CELL	(0)	D[6]	183	IO_CELL	(0)
RPRTY	49	OUT_CELL	(0)	DOENB[6][5]	184	OUT_CELL	(0)
RDAT[15:0]	50:65	OUT_CELL	(0)	D[5]	185	IO_CELL	(0)
RX_OEB[4]	66	OUT_CELL	(0)	DOENB [5][5]	186	OUT_CELL	(0)
TICLK	67	IN_CELL	(0)	D[4]	187	IO_CELL	(0)
Tied to '0'	68:70	IN_CELL	(0)	DOENB [4][5]	188	OUT_CELL	(0)
TIOHM	71	IN_CELL	(0)	D[3]	189	IO_CELL	(0)
Tied to '0'	72:73	IN_CELL	(0)	DOENB [3][5]	190	OUT_CELL	(0)
Tied to '1'	74	IN_CELL	(0)	D[2]	191	IO_CELL	(0)
TPOH	75	IN_CELL	(0)	DOENB [2][5]	192	OUT_CELL	(0)
Tied to '0'	76:78	IN_CELL	(0)	D[1]	193	IO_CELL	(0)
TPOHINS	79	IN_CELL	(0)	DOENB [1][5]	194	OUT_CELL	(0)
Tied to '0'	80:82	IN_CELL	(0)	D[0]	195	IO_CELL	(0)
TPOHCLK	83	OUT_CELL	(0)	DOENB [0][5]	196	OUT_CELL	(0)
Unconnected	84:86	OUT_CELL	(0)	HIZ[6]	197	OUT_CELL	(0)

Notes

1. TDAT[15] is the first bit of the boundary scan chain.

2. TCA_OEB will set TCA to tri-state when set to logic one. When set to logic zero, TCA will be driven.

3. RCA_OEB will set RCA to tri-state when set to logic one. When set to logic zero, RCA will be driven.

4. RX_OEB will set RDAT[15:0], RPRTY, and RSOC to tri-state when set to logic one. When set to logic zero, RDAT[15:0], RPRTY, and RSOC will be driven.

5. The DOENB signals will set the corresponding bidirectional signal (the one preceding the DOENB in the boundary scan chain — see note 1 also) to an output when set to logic zero. When set to logic one, the bidirectional signal will be tri-stated.

6. HIZ will set all outputs not controlled by TCA_OEB, RCA_OEB, RX_OEB, and DOENB to tri-state when set to logic one. When set to logic zero, those outputs will be driven.

13 Operation

13.1 Software Initialization Sequence

Using the following software initialization sequence puts the S/UNI-JET in a normal power consumption state. PMC-Sierra™ strongly recommends using this reset sequence to guarantee the device's long term reliability.

Note: After a reset, the S/UNI-JET may start using more power than is required. While the device's normal operations are not altered, the excessive power consumption can cause the device to give off high levels of heat, which in turn, could lead to future problems with the device.

To initialize the device:

- Reset the S/UNI-JET.

- Set IOTST (bit 2) in the Master Test Register (datasheet pg. 291) to '1' (by writing 00000100 to register 400H).

- Put the S/UNI-JET Receive Cell Processor (RXCP) into test mode by writing:
  - ° 00000101 to test register 461H
  - ° 00000101 to test register 561H
  - ° 00000101 to test register 661H
  - ° 00000101 to test register 761H

- Set the S/UNI-JET Receive Cell Processor block built in set test (BIST) controls signals by writing:
  - ° 01000000 to test register 462H
  - ° 01000000 to test register 562H
  - ° 01000000 to test register 662H
  - ° 01000000 to test register 762H
  - ° 10101010 to test register 463H
  - ° 10101010 to test register 563H
  - ° 10101010 to test register 663H
  - ° 10101010 to test register 763H

- Put the S/UNI-JET Transmit Cell Processor (TXCP) into test mode by writing:
  - ° 00000011 to test register 481H
  - ° 00000011 to test register 581H
  - ° 00000011 to test register 681H
  - ° 00000011 to test register 781H

- Set the S/UNI-JET Transmit Cell Processor block built in set test (BIST) controls signals by writing:
  - ° 10000000 to test register 480H
  - ° 10000000 to test register 580H
  - ° 10000000 to test register 680H
  - ° 10000000 to test register 780H
  - ° 10101010 to test register 482H
  - ° 10101010 to test register 582H
  - ° 10101010 to test register 682H
  - ° 10101010 to test register 782H

- Toggle REF8KI (pin T3, datasheet page 29) signal several times. This provides the clock to the RAM. REF8KI is the test clock used by the TXCP and RXCP blocks when in test mode.

- Set IOTST (bit 2) in the Master Test Register (datasheet pg. 291) to '0' (by writing 00000000 to Register 400H).

- Resume normal device programming.

13.2 Register Settings for Basic Configurations

Table 33   Register Settings for Basic Configurations

Mode of Operation	S/UNI-JET Registers (values in Hexadecimal)																	
	300	302	303	304	308	30C	330	334	338	339	340	341	344	34C	360	361	380	39B
T3 C-bit ADM	C0	00	00	F8	00	00	83	01	--	--	--	--	--	--	04	04	04	00
T3 M23 ADM	C0	00	00	F8	00	00	82	00	--	--	--	--	--	--	04	04	04	00
T3 C-bit PLCP	40	00	00	F8	04	04	83	01	--	--	--	--	--	--	04	00	04	00
T3 M23 PLCP	40	00	00	F8	04	04	82	00	--	--	--	--	--	--	04	00	04	00
T3 C-bit framer only[1]	50	00	00	78	00	00	83	01	--	--	--	--	--	--	--	--	--	01
T3 M23 framer only[1]	50	00	00	78	00	00	82	00	--	--	--	--	--	--	--	--	--	01
E3 G.832 ADM	C0	40	40	F8	00	00	--	--	04	00	01	01	--	--	04	08	04	00
E3 G.832 framer only[1]	50	40	40	78	00	00	--	--	04	00	01	01	--	--	--	--	--	01
E3 G.751 ADM	C0	40	40	F8	00	44	--	--	00	00	00	41	--	--	04	08	04	00
E3 G.751 PLCP	40	40	40	F8	44	44	--	--	00	04	00	41	--	--	04	00	04	00
E3 G.751 framer only[1]	50	40	40	78	00	00	--	--	00	00	00	01	--	--	--	--	--	01
J2 ADM	C0	80	80	F8	00	00	--	--	--	--	--		03	0E	04	08	04	00
J2 framer only[1]	50	80	80	78	00	00	--	--	--	--	--		03	0E	--		--	01
E1 PLCP	40	C0	C0	--	C4	C4	--	--	--	--	--		--	--	04	00	04	00
E1 ADM	40	C0	C0	--	C0	C0	--	--	--	--	--		--	--	04	00	04	00

Mode of Operation	S/UNI-JET Registers (values in Hexadecimal)																	
	300	302	303	304	308	30C	330	334	338	339	340	341	344	34C	360	361	380	39B
T1 PLCP	40	C0	C0	--	84	84	--	--	--	--	--		--	--	04	00	04	00
T1 ADM	40	C0	C0	--	80	80	--	--	--	--	--		--	--	04	00	04	00
External Framer ADM[2]	40	C0	C0	--	01	01	--	--	--	--	--	--	--		04	00[4]	04	00

Notes

1. In framer only modes, TGAPCLK and RGAPCLK are enabled by programming Register 301H to 30CH.

2. Byte, nibble, or bit alignment of the ATM Cell bytes to the line overhead is configured using the TOCTA bit in Register 300H, and the FORM[1:0] bits in Register 30CH.

3. Unipolar mode is selected for DS3, E3, and J2 modes by setting the TUNI bit to logic one in Register 302H and the UNI bit in 330H, 338H, and 344H respectively. When the DS3, E3, or J2 framers are bypassed, unipolar mode is selected by default.

4. Bit, Nibble, and Byte alignment of the ATM cell octets to the arbitrary external frame overhead is set using the ALIGN[1:0] bits of Register 361H.

5. ATM cells are configured to have the Coset Polynomial added to the HCS byte and payload scrambling/descrambling is enabled.

6. ATM Idle cell header octets H1, H2, H3, and H4 are configured to be 00H 00H 00H 01H respectively.

13.3   PLCP Frame Formats

The S/UNI-JET supports four different PLCP frame formats:

- DS3 PLCP.

- DS1.

- G.751 E3.

- E1.

The structure of each of these formats is quite similar, and is illustrated in Figure 8 through Figure 11.

Figure 8   DS3 PLCP Frame Format

A1	A2	P11	Z6	ATM Cell		
A1	A2	P10	Z5	ATM Cell		
A1	A2	P9	Z4	ATM Cell		
A1	A2	P8	Z3	ATM Cell		
A1	A2	P7	Z2	ATM Cell		
A1	A2	P6	Z1	ATM Cell		**PLCP**
A1	A2	P5	F1	ATM Cell		**Frame Rate**
A1	A2	P4	B1	ATM Cell		**125 µs**
A1	A2	P3	G1	ATM Cell		
A1	A2	P2	M2	ATM Cell		
A1	A2	P1	M1	ATM Cell		
A1	A2	P0	C1	ATM Cell		Trailer
Framing (3 octets)		**POH**		**53 octets**		**13 or 14 nibbles**

The DS3 PLCP frame provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the DS3 frame; however, there is no relationship between the start of the PLCP frame and the start of the DS3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) is varied continuously such that the resulting PLCP frame rate can be locked to an 8 kHz reference.

Figure 9   DS1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell		
A1	A2	P8	Z3	ATM Cell		
A1	A2	P7	Z2	ATM Cell		
A1	A2	P6	Z1	ATM Cell		**PLCP**
A1	A2	P5	F1	ATM Cell		**Frame Rate**
A1	A2	P4	B1	ATM Cell		**3 ms**
A1	A2	P3	G1	ATM Cell		
A1	A2	P2	M2	ATM Cell		
A1	A2	P1	M1	ATM Cell		
A1	A2	P0	C1	ATM Cell		Trailer
Framing (3 octets)		**POH**		**53 octets**		**6 octets**

The DS1 PLCP frame provides the transmission of 10 ATM cells every 3 ms. The PLCP frame is octet aligned to the framing bit in the DS1 frame; there is no relationship between the start of the PLCP frame, and the start of the DS1 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is always six, and cannot be varied.

Figure 10   G.751 E3 PLCP Frame Format

A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	PLCP Frame Rate 125 µs
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer

Framing (3 octets)	POH	53 octets	17,18,19,20, or 21 octets

The G.751 E3 PLCP frame provides the transmission of 9 ATM cells every 125 µs. The PLCP frame is octet aligned to the 16 overhead bits in the ITU-T Recommendation G.751 E3 frame; there is no relationship between the start of the PLCP frame, and the start of the E3 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is nominally 18, 19, or 20, and is based on the number of E3 overhead octets (4, 5, or 6) that have been inserted during the PLCP frame period. The nominal octet stuffing can be varied by ±1 octet to allow the E3 PLCP frame to be locked to an external 8 kHz reference. Thus the trailer can be 17, 18, 19, 20, or 21 octets in length.

Figure 11   E1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell
A1	A2	P8	Z3	ATM Cell
A1	A2	P7	Z2	ATM Cell
A1	A2	P6	Z1	ATM Cell
A1	A2	P5	F1	ATM Cell
A1	A2	P4	B1	ATM Cell
A1	A2	P3	G1	ATM Cell
A1	A2	P2	M2	ATM Cell
A1	A2	P1	M1	ATM Cell
A1	A2	P0	C1	ATM Cell

PLCP Frame Rate 2.375 ms

Framing (3 octets)   **POH**   **53 octets**

The E1 PLCP frame provides the transmission of 10 ATM cells every 2.375 ms. Thirty of the thirty-two available E1 channels are used for transporting the PLCP frame. The remaining two channels are reserved for E1 framing and signaling functions. The PLCP frame is octet aligned to the channel boundaries in the E1 frame. The PLCP frame is aligned to the 125 μs E1 frame (the A1 octet of the first row of the PLCP frame is inserted in timeslot 1 of the E1 frame).

13.3.1   PLCP Path Overhead Octet Processing

Table 34   PLCP Overhead Processing

Overhead Field	Transmit Operation	Receive Operation
A1, A2: Frame Alignment Pattern	Inserts the PLCP frame alignment pattern (F628H)	Searches the receive stream for the PLCP frame alignment pattern. When the pattern has been detected for two consecutive rows, along with two valid, and sequential path overhead identifier octets, the S/UNI-JET declares in-frame. Note: The ATM cell boundaries are implicitly known when the PLCP frame is located, thus cell delineation is accomplished by locating the PLCP frame. When errors are detected in both octets in a single row, or when errors are detected in two consecutive path overhead identifier octets, the S/UNI-JET declares an OOF defect. The LOF defect is an integrated version of the OOF defect state.
PO-P11: Path Overhead Identifier	Inserts the path overhead identifier codes in accordance with the PLCP frame alignment. See Table 35.	Identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.
Z1-Z6:	These octets are unused and are	These octets are ignored and are extracted on

Overhead Field	Transmit Operation	Receive Operation
Growth:	nominally programmed with all zeros. Access to these octets is provided by the PLCP transmit overhead access port.	the RPOH pin.
F1: User Channel	This octet is unused and the value inserted in this octet is controlled by an internal register or by TPOH pin.	This octet is ignored and is extracted on the RPOH pin.
B1: Bit Interleaved Parity	This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A, Pn octets and the trailer). The B1 value is calculated based on even parity and the value inserted in the current frame is the BIP result calculated for the previous frame.	The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted and compared against the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are accumulated in a counter in the CPPM block.
G1: Path Status	The first four bit positions provide a PLCP FEBE function and indicates the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000b-1000b) indicating between zero and eight B1 errors. The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal insertion is controlled by the internal registers or by TPOH pin.	The G1 byte provides the PLCP FEBE function and is accumulated in an a counter in the CPPM block. PLCP yellow alarm is detected or removed when the yellow bit is set to logic one or zero for ten consecutive frames. The yellow alarm state and the link status signal state are contained in the SPLR Status Register.
M1, M2: Control Information	These octets carry the DQDB layer management information. Internal register controls the nominal value inserted in these octets. These octets are unused in ATM Forum T3 UNI 3.0 specification.	These octets are ignored and are extracted on the RPOH pin.
C1: Cycle/Stuff Counter	The coding of this octet depends on the PLCP frame format. For DS1 and E3 PLCP formats, this octet is programmed with all zeros. For the DS3 PLCP format, this octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles. The stuffing may be varied by a nibble so that the PLCP frame rate can be locked to an external 8 kHz	Interprets the trailer length according to the selected PLCP frame format and the received C1 code.

Overhead Field	Transmit Operation	Receive Operation
	timing reference from REF8KI, a looptimed 8 kHz reference, or fixed stuffing via the FIXSTUFF bit in the SPLT Configuration Register. See Table 36.	
	For the G.751 E3 PLCP format, this octet indicates the number of stuff octets (17 to 21) at the end of the PLCP frame. Depending on the alignment of the G.751 E3 frame to the E3 PLCP frame, 18, 19 or 20 octets are nominally stuffed. The stuffing may be varied by ±1 octet so that the PLCP frame rate can be locked to an external 8 kHz timing reference from REF8KI. The S/UNI-JET also supports fixed timing using the FIXSTUFF bit in the SPLT Configuration Register. See Table 37.	

Table 35   PLCP Path Overhead Identifier Codes

POI	POI Code (Hex)
P11	2C
P10	29
P9	25
P8	20
P7	1C
P6	19
P5	15
P4	10
P3	0D
P2	08
P1	04
P0	01

Table 36   DS3 PLCP Trailer Length

C1(Hex)	Frame/Trailer Length
FF	1 (13 Nibbles)
00	2 (14 Nibbles)
66	3 (13 Nibbles)
99	3 (14 Nibbles)

Table 37   E3 PLCP Trailer Length

C1(Hex)	Trailer Length
3B	17 octets
4F	18 octets
75	19 octets
9D	20 octets
A7	21 octets

13.4   DS3 Frame Format

The S/UNI-JET supports both M23 and C-bit parity DS3 framing formats. This format can be extended to support direct byte mapping or PLCP mapping of ATM cells. An overview of the DS3 frame format is shown in Figure 12.

Figure 12   DS3 Frame Structure
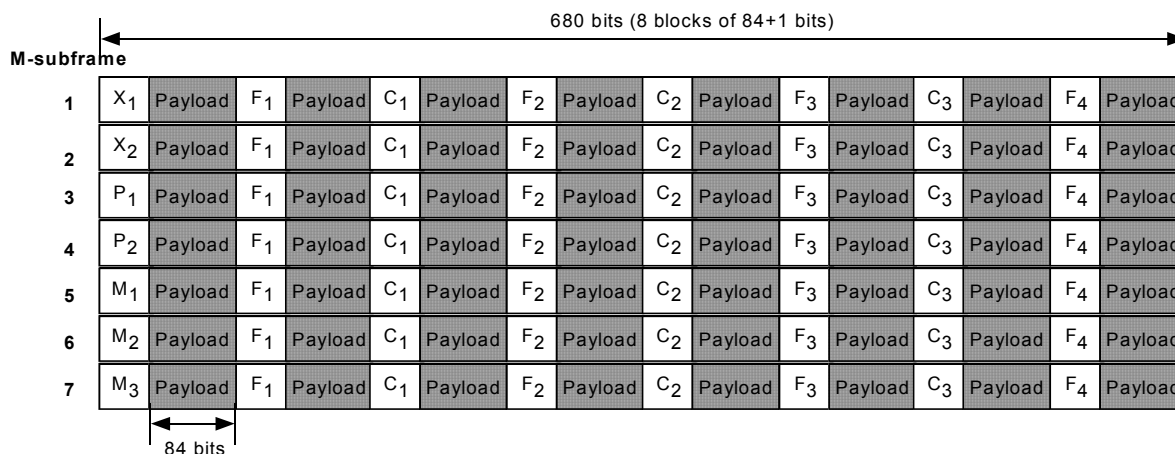
The DS3 receiver decodes a B3ZS-encoded signal and provides indications of LCVs. The B3ZS decoding algorithm and the LCV definition are software selectable.

While in-frame, the DS3 receiver continuously checks for LCV, M-bit or F-bit framing bit errors, and P-bit parity errors. When C-bit parity mode is selected, both C-bit parity errors and FEBEs are accumulated.

When the C-bit parity framing format is detected, both the FEAC channel and the PMDL are extracted. HDLC messages in the PMDL are received by an internal data link receiver.

The DS3 transmitter allows for the insertion of the overhead bits into a DS3 bit stream and produces a B3ZS-encoded signal. Status signals such as FERF, AIS, and idle signal can be inserted when the transmission of these signals is enabled

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The processing of the overhead bits in the DS3 frame is described in Table 38. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFP, and TOHCLK signals. In the receive direction, most of the overhead bits our brought out serially on the ROH data stream.

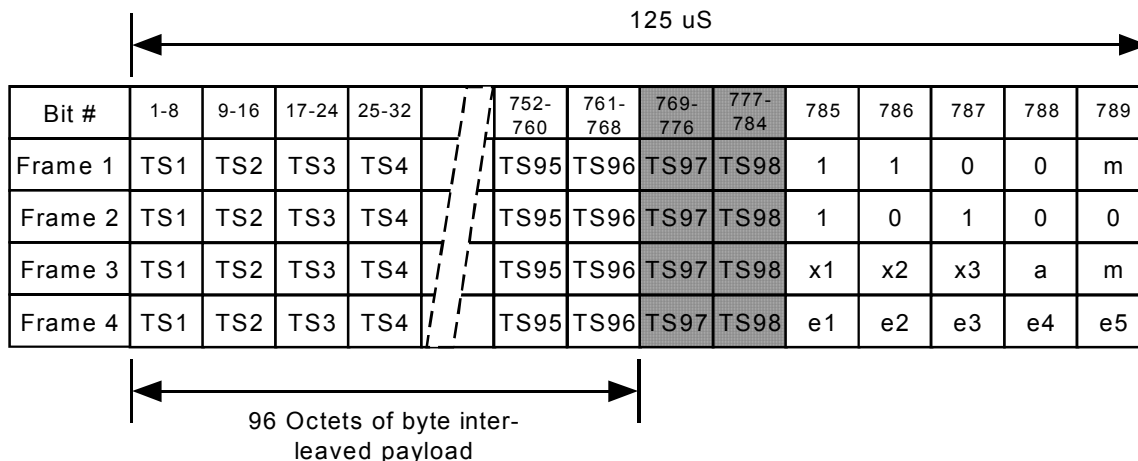**Table 38   DS3 Frame Overhead Operation**

Control Bit	Transmit Operation	Receive Operation
Xx: X-Bit Channel	Inserts the FERF signal on the X-bits.	Monitors and detects changes in the state of the FERF signal on the X-bits.
Px: P-Bit Channel	Calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.	Calculates the parity for the received payload. Errors are accumulated in internal registers.
Mx: M-Frame Alignment Signal	Generates the M-frame alignment signal (M1=0, M2=1, M3=0).	Finds the M-frame alignment by searching for the F-bits and the M-bits. OOF is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Fx: M-subframe Alignment Signal	Generates the M-subframe signal (F1=1, F2=0, F3=0, F4=1).	Finds M-frame alignment by searching for the F-bits and the M-bits. OOF is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits.
Cx: C-Bit Channels	M23 Operation: The C bits are passed through transparently in M23 framer only mode except for the C-bit Parity ID bit which toggles every M-frame. In M23 ATM applications, the C bits other than the Parity ID bit are forced to logic one. C-bit Parity Operation: The C-bit Parity ID bit is forced to logic one. The second C-bit in M-subframe 1 is set to logic one. The third C-bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC channel is sourced by the XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. The 3 C-bits in M-subframe 5 contain the 28.2 Kbit/s path maintenance datalink. The remaining C-bits are unused and set to logic one.	The state of the C-bit parity ID bit is stored in a register. This bit indicates whether an M23 or C-bit parity format is received. C-bit Parity Operation: The FEAC channel on the third C-bit in M-subframe 1 is detected by the RBOC block. Path parity errors and FEBEs on the C-bits in M-subframes 3 and 4 are accumulated in counters. The path maintenance datalink signal is extracted by the receive HDLC controller.

13.5 G.751 E3 Frame Format

The S/UNI-JET provides support for the G.751 E3 frame format, shown in Figure 13. This format can be extended to allow for direct byte mapping or PLCP mapping of ATM cells.

Figure 13   G.751 E3 Frame Structure
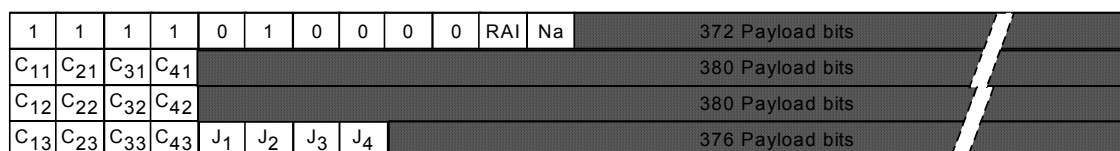
The processing of the overhead bits in the G.751 E3 frame is described in Table 39. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFP, and TOHCLK signals. In the receive direction, most of the overhead bits are brought out serially on the ROH data stream.

When used to transport ATM cells in either ATM direct mapping mode or with PLCP framing, bits 13, 14, 15, and 16 of the E3 frame (directly following the RAI and Na bits) are set to 1, 1, 0 and 0.

Table 39   G.751 E3 Frame Overhead Operation

Control Bit	Transmit Operation	Receive Operation
Frame Alignment Signal	Inserts the frame alignment signal 1111010000b.	Finds frame alignment by searching for the frame alignment signal. When the pattern has been detected for three consecutive frames, an in-frame condition is declared. When errors are detected in four consecutive frames, an OOF condition is declared.
RAI: RAI	Optionally asserts the RAI signal under a register control or when LOS, OOF, AIS and LCD conditions are detected.	Extracts the RAI signal and outputs it on the ROH output pin. The state of the RAI signal is also written to a register bit.
Na: National Use Bit	Asserts the National Use bit under a register control or from the internal HDLC controller.	Extracts the National Use bit and stores the value in a register bit.
Cjk: Justification Service Bits	When the device is configured as an E3 G.751 framer device, the Justification Service Bits can be inserted on the TDATI input pin the same way as normal payload data. When the device is configured for ATM application, the Justification Service Bits are used as payload bits.	Extracts the Justification Service Bits on the ROH output pin when the Cjk bits are configured as overhead.

Control Bit	Transmit Operation	Receive Operation
Jk: Tributary Justification Bits	When the device is configured as a E3 G.751 framer, the Tributary Justification Bits can be inserted on the TDATI input pin the same way as normal payload data. When the device is configured for ATM application, the Tributary Justification Bits are used a payload bits.	Extracts the Tributary Justification Bits on the ROH output pin when the Jk bits are configured as overhead.

13.6 G.832 E3 Frame Format

The S/UNI-JET provides support for the G.832 E3 frame format. This format can be extended to allow for direct byte mapping of ATM cells. The G.832 E3 frame format is shown in Figure 14.

Figure 14   G.832 E3 Frame Structure
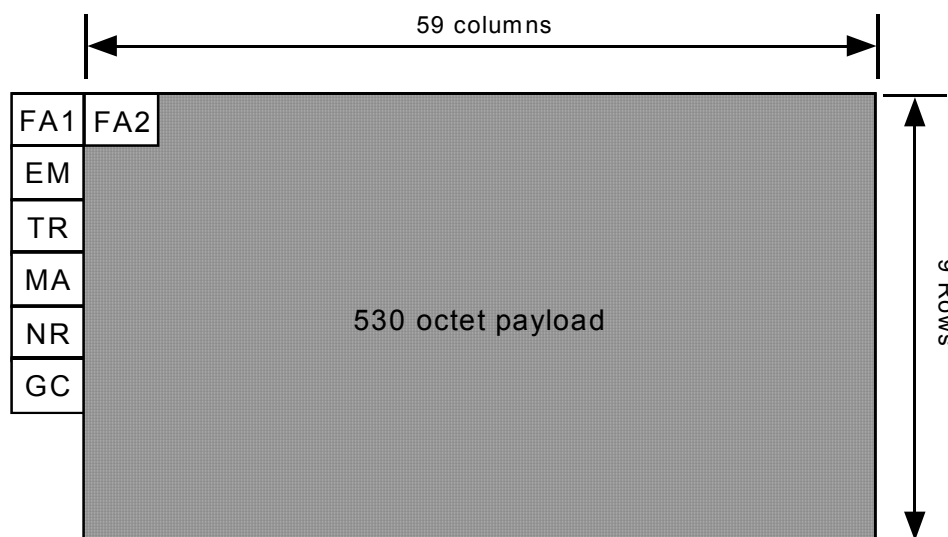
The processing of the overhead bits in the G.832 E3 frame is described in Table 40. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data stream using the TOH, TOHINS, TOHFP, and TOHCLK signals. In the receive direction, the overhead bits are brought out serially on the ROH data stream.

Table 40   G.832 E3 Frame Overhead Operation

Control	Transmit Operation	Receive Operation
FA1, FA2: Frame Alignment Pattern	Inserts the G.832 E3 frame alignment pattern (F628H).	Searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern is detected for two consecutive frames, an in-frame condition is declared. Note: There is no

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Control	Transmit Operation	Receive Operation
		ATM cell alignment with the G.832 E3 frame. Therefore cell delineation must be performed to locate the ATM cell boundaries.
EM: Error Monitor, BIP-8	Inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits of the previous 125 µs frame.	Computes the incoming BIP-8 value over one 125 µs frame. The result is held and compared against the value in the EM byte of the subsequent frame.
TR: Trail Trace	Inserts the 16 byte trail access point identifier specified in internal registers.	Extracts the repetitive trail access point identifier and verifies that the same pattern is received. Compares the received pattern to the expected pattern programmed in a register.
MA: Maintenance and Adaptation Byte	Inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multiframe Indicator bits and the Timing Marker bit as programmed in a register or as indicated by detection of receive OOF or BIP-8 errors.	Extracts and reports the FERF bit value when it has been the same for 3 or five consecutive frames. S/UNI-JET also extracts and accumulates FEBE occurrences and extracts the Payload Type, Tributary Unit Multiframe, and Timing Market indicator bits and reports them through microprocessor accessible registers.
NR: Network Operator Byte	Inserts the Network Operator byte from the TOH overhead stream or optionally from the TDPR. All 8 bits of the Network Operator byte are inserted from TOH or from the TDPR.	Extracts the Network Operator byte and outputs it on ROH or optionally terminates it in the RDLC. All 8 bits of the Network Operator byte are extracted and presented on ROH or to the RDLC.
GC: General Purpose Communication Channel	Inserts the GC byte from the TOH overhead stream or optionally from the TDPR block.	Extracts the GC byte and outputs it on ROH or optionally terminates it in the RDLC block.

13.7 J2 Frame Format

The S/UNI-JET provides support for the G.704 and NTT J2 frame format. This format can be extended to allow for direct byte mapping of ATM cells as specified in G.804. The J2 frame format consists of 789 bits frames each 125 us long, consisting of 96 bytes of payload, two reserved bytes, and five F-bits. The frames are grouped into five frame multiframes as shown in Figure 15.

Figure 15   J2 Frame Structure

Bit #	1-8	9-16	17-24	25-32		752-760	761-768	769-776	777-784	785	786	787	788	789
Frame 1	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	1	1	0	0	m
Frame 2	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	1	0	1	0	0
Frame 3	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	x1	x2	x3	a	m
Frame 4	TS1	TS2	TS3	TS4		TS95	TS96	TS97	TS98	e1	e2	e3	e4	e5

125 uS

96 Octets of byte inter-leaved payload

The J2 framer decodes a unipolar or B8ZS encoded signal and frames to the resulting 6,312 Kbit/s J2 bit stream. Once in frame, the J2 framer provides indications of frame and multiframe boundaries and marks overhead bits, x-bits, m-bits and reserved channels (TS97 and TS98). Indications of LOS, bipolar violations, excessive zeroes, change of frame alignment, framing errors, and CRC errors are provided and accumulated in internal counters.

The J2 transmitter inserts the overhead bits into a J2 bit stream and produces a B8ZS-encoded signal. The J2 transmitter adheres to the framing format specified in G.704 and NTT Technical Reference for High Speed Digital Leased Circuit Services.

The processing of the overhead bits in the J2 frame is described in Table 41. In the transmit direction, the overhead bits can be inserted on a bit-by-bit basis from a user supplied data using the TOH, TOHINS, TOHFP, and TOHCLK signals. In the receive direction, the overhead bits are brought out serially on the ROH data stream.

Table 41   J2 Frame Overhead Operation

Control	Transmit Operation	Receive Operation
TS1-TS96: Byte Interleaved Payload	Inserts the ATM cells into TS1 to TS96 octets.	Extracts the ATM cell octet payload and performs cell delineation.
TS97-TS98: Signaling channels	Inserts the signaling bytes from either register bits or from the TOH and TOHINS inputs. These bits can be optionally inserted via TDATI input when in framer only mode.	Extracts signaling bytes on the ROH output.
Frame Alignment Signal	Inserts the frame alignment signal automatically.	Finds J2 frame alignment by searching for the frame alignment signal.
M-bits: 4kHz Data Link	Inserts the 4 KHz data link signal from the internal HDLC controller or from the bit oriented code generator.	Extracts the 4 KHz data link signal for the internal HDLC controller.

Control	Transmit Operation	Receive Operation
X-bits: Spare Bits	Inserts the spare bits via register bits or via TOH and TOHINS input pins.	Extracts and presents the x-bits on register bits. The X-bit states can be debounced and presented on the ROH output pin. An interrupt change can be generated to signal a change in the X-bit state.
A-bit: Remote LOF Indication	Inserts the A-bit via register bit. The A-bit can be optionally be asserted when the J2 framer is in LOF condition.	Extracts and presents the A-bit on a register bit. The A-bit state can be debounced and presented on the ROH output pin. An interrupt can be generated to signal a change in the A-bit state.
E1-E5: CRC-5 Check Sequence	Automatically calculates and inserts the CRC-5 check sequence.	Calculates the CRC-5 check sequence for the received data stream. Discrepancies with the received CRC-5 code can be configured to generate an interrupt. CRC-5 errors are accumulated in an internal counter.

13.8   S/UNI-JET Cell Data Structure

ATM cells may be passed to and from the S/UNI-JET using a 26-word or 27-word data structure and a 52-byte or 53-byte word data structure. These data structures are shown in Figure 16, Figure 17, Figure 18, and Figure 19.

Figure 16   16-bit Wide, 26-byte Word Structure
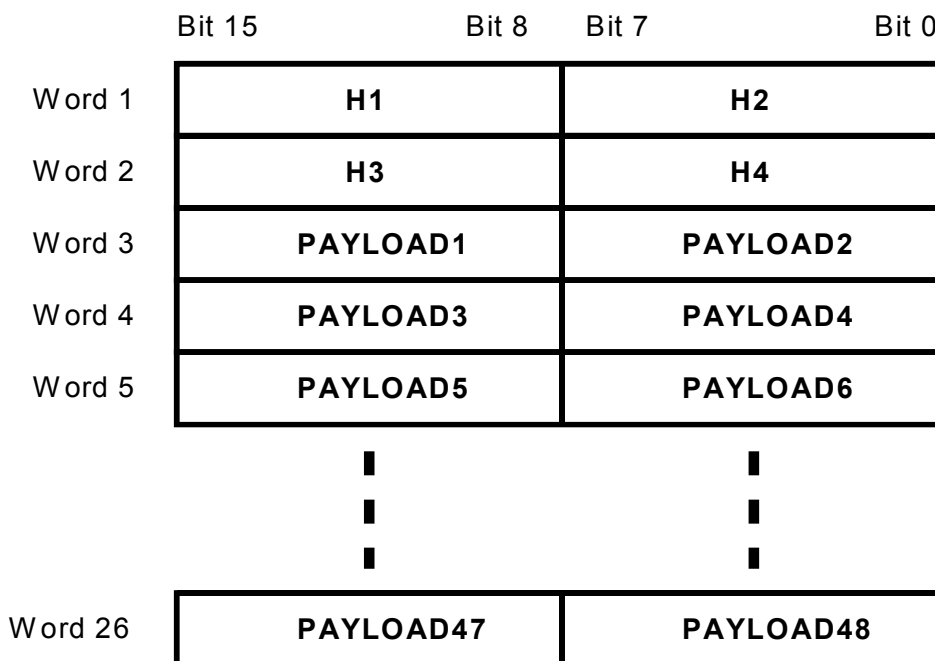
Figure 17   16-bit Wide, 27-byte Word Structure

	Bit 15	Bit 8	Bit 7	Bit 0
Word 1	**H1**		**H2**	
Word 2	**H3**		**H4**	
Word 3	**H5**		**HCS STATUS/CONTROL**	
Word 4	**PAYLOAD1**		**PAYLOAD2**	
Word 5	**PAYLOAD3**		**PAYLOAD4**	
Word 6	**PAYLOAD5**		**PAYLOAD6**	
Word 27	**PAYLOAD47**		**PAYLOAD48**	
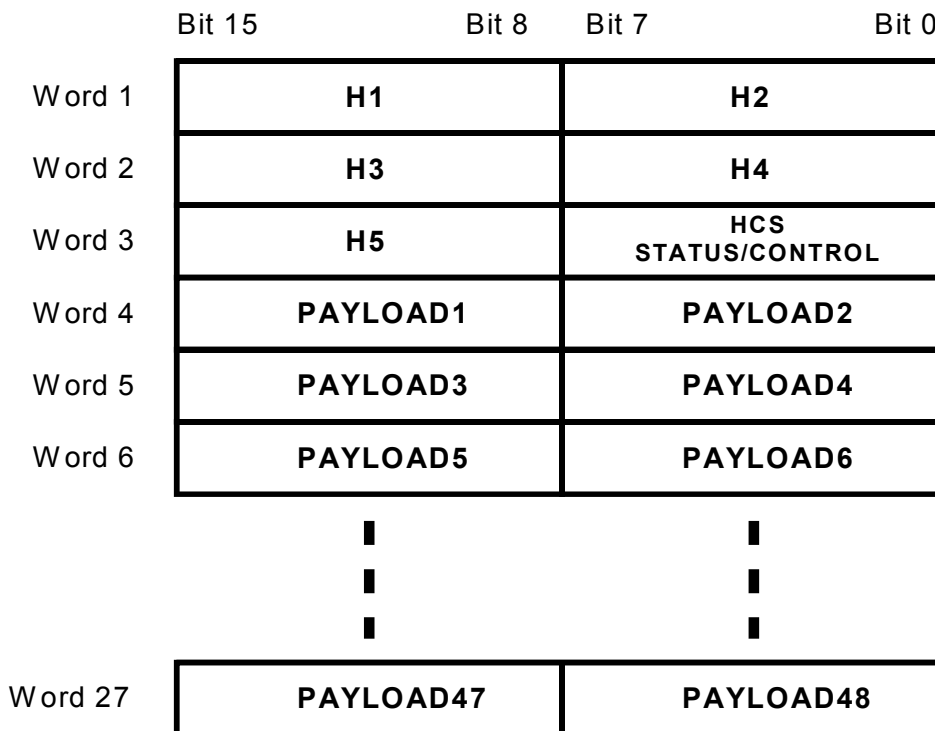
The 16-bit SCI-PHY^{TM} compliant data structure is selected when the ATM8 input is tied low. Bit 15 of each word is the most significant bit, which corresponds to the first bit transmitted or received. Selection between the 26-byte and 27-byte word structure is done with the DS27_53 register bit in the S/UNI-JET Configuration 1 Register. The 26-byte word structure is chosen when DS27_53 is set to logic zero. The 27-byte word structure is chosen when DS27_53 is set to logic one. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). The HCS octet is only passed through the 27-byte word structure. Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction with the 27-byte word structure, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error. (If the HCSPASS bit in the RXCP-50 Configuration 2 Register is set to logic zero, the all-ones pattern will never be passed in this structure.) An alternating ones and zeros pattern (xxAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, with the 27-byte word structure, the HCSB bit in the TXCP-50 Configuration 1 Register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position. (For example a logic one in bit 7 causes the most significant bit of the HCS to be inverted.)

With the 26-byte word structure, if the HCSB bit in the TXCP-50 is logic one, then no HCS byte is inserted on the data read from the Utopia interface or on the Idle cells. In such a configuration, the RXCP-50 should be configured to pass the 26-word output without requiring cell delineation by setting the CCDIS bit to logic one. This setting is useful for passing arbitrary payload through the transmit and receive Utopia interfaces.

Figure 18   8-bit Wide, 52-byte Word Structure
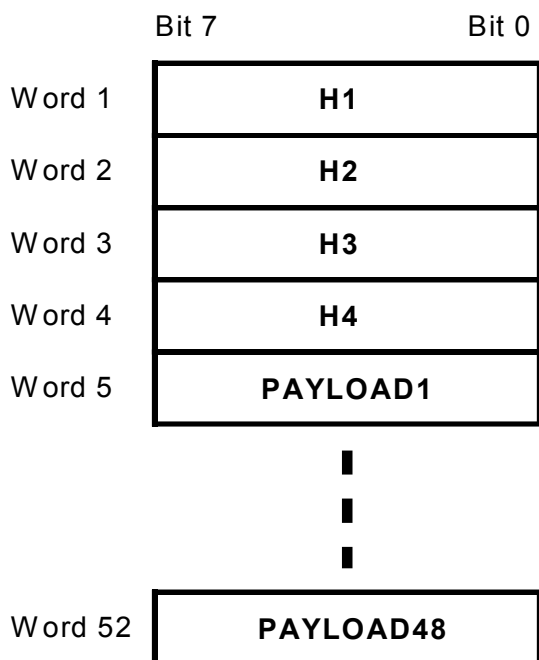
Figure 19   8-bit Wide, 53-byte Word Structure
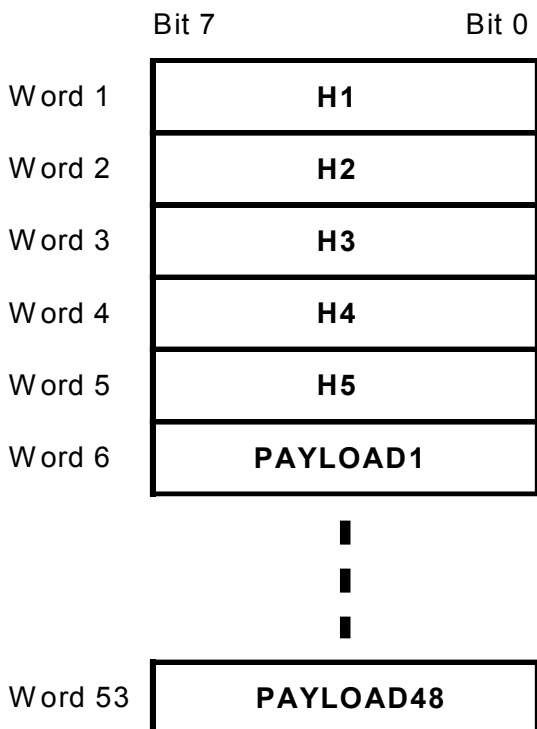
The 8-bit SCI-PHY™ compliant data structure is selected when the ATM8 input is tied high. Bit 7 of each word is the most significant bit, which corresponds to the first bit transmitted or received. Selection between the 52-byte and 53-byte word data structures is done by the DS27_53 register bit in the S/UNI-JET Configuration 1 Register. The 52-byte word structure is chosen when DS27_53 is set to logic zero. The 53-byte word structure is chosen when DS27_53 is set to logic one. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). The header check sequence octet (HCS) is passed through the 53-byte word structure. Word 5 of this structure contains the HCS octet.

In the receive direction, cells containing "detected and uncorrected" header errors are dropped when the HCSPASS bit in the RXCP-50 Configuration 2 Register is set to logic zero. No HCS status information is passed within this data structure. Cells with error free headers and "detected and corrected" headers are passed when HCSPASS and DISCOR are logic zero. Cells containing uncorrectable HCS errors are dropped while the HCSPASS bit is set to logic zero. Error free headers, "detected and corrected" headers, and "detected and uncorrected" headers are passed when HCSPASS is a logic one.

In the receive direction, idle cells are dropped when the IDLEPASS bit in the RXCP-50 Configuration 2 Register is set to a logic zero. No cells are passed when the S/UNI-JET is in the PLCP LOF defect state (for PLCP based transmission), or when the S/UNI-JET is in the out of cell delineation defect state (for non-PLCP based transmission).

In the transmit direction, the HCSB bit in the TXCP-50 Configuration 1 Register determines whether the HCS is calculated internally or is inserted directly from Word 5. For the 52-byte word structure, if the HCSB bit in the TXCP-50 is logic one, then no HCS byte is inserted and the TXCP-50 will only transmit the data present on the 52 words. In such a configuration, the RXCP-50 should be configured to pass the 52-byte word output without requiring cell delineation by setting the CCDIS bit to logic one. This setting is useful for passing arbitrary payload through the transmit and receive Utopia interfaces.

13.9   Resetting the RXFF and TXFF FIFOs

Resetting the receive and transmit FIFOs can be accomplished using the FIFORST bits (RXCP-50 FIFO/UTOPIA Control & Configuration, TXCP-50 Configuration 1 Registers). When resetting, the FIFORST bit should be written with a logic one, and held for two or more clock cycles (the longer of two Utopia clock cycles or 16 line clock cycles). After de-asserting FIFORST, data can be safely written to the TXFF after two or more clock cycles have passed.

13.10   Servicing Interrupts

The S/UNI-JET will assert INTB to logic zero when a condition that is configured to produce an interrupt occurs. To determine the condition that caused this interrupt to occur, follow the procedure below:

- Read the INT bits of the S/UNI-JET Clock Activity Monitor and Interrupt Identification Register (307H).

- Read the S/UNI-JET Interrupt Status Register (005H, 105H, 205H, and 305H) to identify which block produced the interrupt. For example, a logic one on the TDPRI register bit in register 305H indicates that the TDPR block of the S/UNI-JET produced the interrupt.

- Service the interrupt.

- If the INTB pin is still logic zero, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.11   Using the Performance Monitoring Features

The PMON and CPPM blocks are provided for performance monitoring purposes. The RXCP-50 and TXCP-50 also contain performance monitor registers. The PMON block is used to monitor DS3, E3, and J2 performance primitives while the CPPM is used to monitor PLCP and idle-cell-based primitives. The RXCP-50 is used to monitor received cell primitives, and the TXCP-50 is used to monitor transmit cell primitives. The counters in the PMON block have been sized as not to saturate if polled every second. The counters in the CPPM blocks have been sized as not to saturate if polled every 1/2 second at line rates up to 44.736 MHz. The counters in the RXCP-50 and TXCP-50 have been sized to not saturate if polled every second at line rates up to 44.736 MHz.

The DS3, E3, and J2 primitives can be accumulated independently of the PLCP and cell-based primitives. An accumulation interval is initiated by writing to one of the PMON event counter register addresses. After writing to a PMON count register, a number of RCLK clock periods (three for J2 mode, 255 for DS3 mode, 500 for G.832 E3 mode, and three for G.751 E3 mode) must be allowed to elapse to permit the PMON counter values to be properly transferred. The PMON registers may then be read.

PLCP and cell-based primitives can be accumulated independent of the DS3, E3, or J2 primitives. An accumulation interval is initiated by writing to one of the CPPM event counter register addresses. After writing to a CPPM count register, a maximum of 67 RCLK clock periods must be allowed to elapse to permit all the CPPM values to be properly transferred. The CPPM registers may then be read.

The RXCP-50 and TXCP-50 accumulate cell-based primitives such as received cells, corrected cell headers, uncorrected cell headers, and transmitted cells. An accumulation interval in each block is initiated by writing to one of the RXCP-50 or TXCP-50 event counter register addresses. After writing to a count register, a maximum of 67 RCLK or TICLK clock periods must be allowed to elapse to permit all the RXCP-50 or TXCP-50 values to be properly transferred. The RXCP-50 or TXCP-50 count registers may then be read.

Writing to the S/UNI-JET Identification, Master Reset, and Global Monitor Update Registers causes the PMON, CPPM, RXCP-50, and TXCP-50 performance event counters to latch and a new accumulation period to start in all four quadrants of the S/UNI-JET. A maximum of 67 RCLK clock periods must be allowed to elapse to permit all the event count registers to be properly transferred.

13.12 Using the Internal PMDL Transmitter

Note: The access rate to the TDPR Registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-JET Miscellaneous Register (39BH). Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data Registers should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR Registers.

Upon reset of the S/UNI-JET , the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic zero (default value). An HDLC all-ones idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic one. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic one. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable Register to logic one. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold Registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic one. If no message is sent after the EN bit is set to logic one, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status Register to determine when to write to the TDPR Transmit Data Register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the S/UNI-JET Clock Activity Monitor and Interrupt Identification Register, and the S/UNI-JET Interrupt Status Register to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data Register.

13.12.1   Interrupt Driven Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold.

The CRC bit can be set to logic one so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic one so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun.

Use the following procedure to transmit HDLC packets:

- Wait for data to be transmitted. Once data is available to be transmitted, then go to step 2.

- Write the data byte to the TDPR Transmit Data Register.

- If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration Register to logic one. Go to step 1.

- If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 3, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine, described in the following section, should be immediately followed.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold Register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

13.12.2   TDPR Interrupt Routine

Upon assertion of INTB, the source of the interrupt must first be identified by reading the S/UNI-JET Clock Activity Monitor and Interrupt Identification Register (007H) and the S/UNI-JET Interrupt Status Registers (005H, 105H, 205H, 305H). Once the source of the interrupt has been identified as TDPR, do the following procedure:

- Read the TDPR Interrupt Status Register.

- If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic one, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To reenable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear Register should be written with any value.

- If OVRI=1, then the FIFO has overflowed. The packet which the last byte written into the FIFO belongs to has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data Register occurs. This write contains the first byte of the next packet to be transmitted.

If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data Register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic one so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic zero since packet transmission is set to work with a periodic polling procedure.

To transmit HDLC packets:

- Wait until data is available to be transmitted, then go to step 2.

- Read the TDPR Interrupt Status Register.

- If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status Register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

- If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data Register. Go to step 6.

- If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data Register. Go to step 6.

- If more data bytes are to be transmitted in the packet, then go to step 2.

- If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration Register to logic one. Go to step 1.

13.13 Using the Internal Data Link Receiver

Note: The access rate to the RDLC Registers is limited by the rate of the internal high-speed system clock selected by the LINESYSCLK register bit of the S/UNI-JET Miscellaneous Registers (09BH, 19BH, 29BH, 39BH). Consecutive accesses to the RDLC Status and RDLC Data Registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC Registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic zero (default state). The RDLC Interrupt Control Register should then be initialized to enable the INT output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic one, the RDLC Status Register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control Register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration Register to logic one. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer, which provides alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO, which provides alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status Register for a change in the link status. If the COLS bit is set to logic one, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits are used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status Register is being read the PKIN bit will be logic one. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status Register is read, the PKIN bit is cleared to logic zero. If this register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic one and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status Register to determine when to read the RDLC Data Register. In the interrupt driven mode, the processor controlling the RDLC uses the S/UNI-JET INTB output, the S/UNI-JET Clock Activity Monitor and Interrupt Identification Register, and the S/UNI-JET Interrupt Status Registers to determine when to read the RDLC Data Register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the S/UNI-JET is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the S/UNI-JET Clock Activity Monitor and Interrupt Identification Register, and the S/UNI-JET Interrupt Status Registers. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

- Reads the RDLC Status Register. The INTR bit should be logic one.
  - ° If OVR = 1, then discards last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.
  - ° If COLS = 1, then sets the EMPTY FIFO software flag.
  - ° If PKIN = 1, increments the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

- Reads the RDLC Data Register.

- Reads the RDLC Status Register.

- ° If OVR = 1, then discards last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.
- ° If COLS = 1, then sets the EMPTY FIFO software flag.
- ° If PKIN = 1, increments the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

- Starts the processing of FIFO data. Uses the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.
  - ° If PBS[2:0] = 001, discards data byte read in step 3 and sets the LINK ACTIVE software flag.
  - ° If PBS[2:0] = 010, discards the data byte read in step 3 and clears the LINK ACTIVE software flag.
  - ° If PBS[2:0] = 1XX, stores the last byte of the packet, decrements the PACKET COUNT, and checks the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.
  - ° If PBS[2:0] = 000, stores the packet data.
  - ° If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, goes to step 3 or else clears the EMPTY FIFO software flag and leaves this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all-ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 20   Typical Data Frame
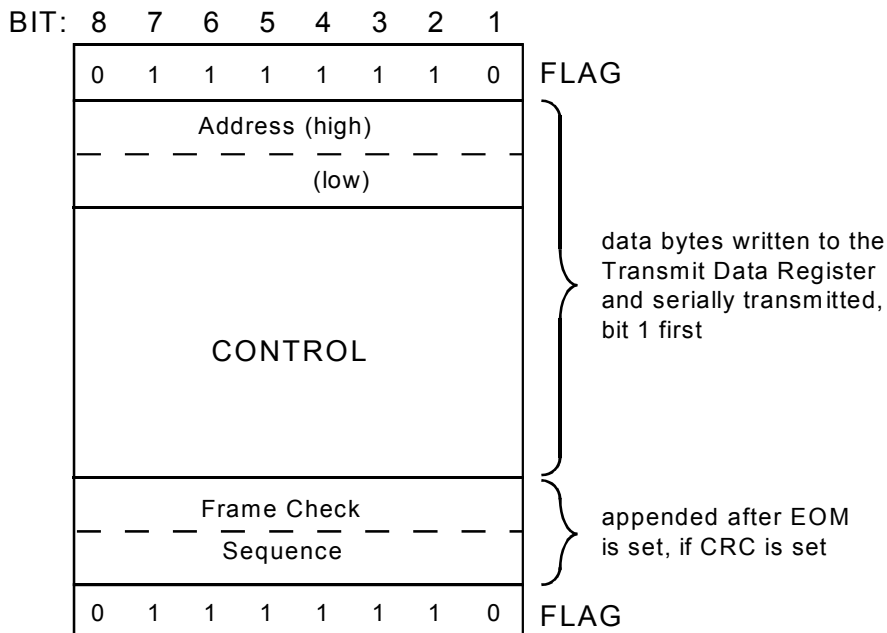
Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 21 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs.

Figure 21   Example Multi-Packet Operational Sequence
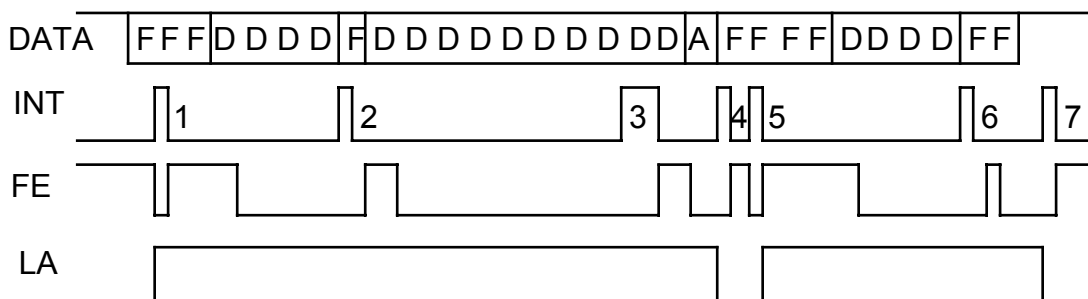
Notes

1.   F is the flag sequence (01111110).

2.   A is the abort sequence (01111111).

3.   D is the packet data bytes.

4.   INT is the active high interrupt output.

5.   FE is the internal FIFO empty status.

6.   LA is the state of the LINK ACTIVE software flag.

At points 1 and 5 the first flag after all-ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes high. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic one.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status Register is read since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

13.14   PRGD Pattern Generation

A pseudo-random or repetitive pattern can be inserted or extracted in the PLCP payload (if PLCP framing is enabled) or in the DS3, E3, J2, or Arbitrary framing format payload (if PLCP framing is disabled). It cannot be inserted into the ATM cell payload.

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 22:

Figure 22   PRGD Pattern Generator
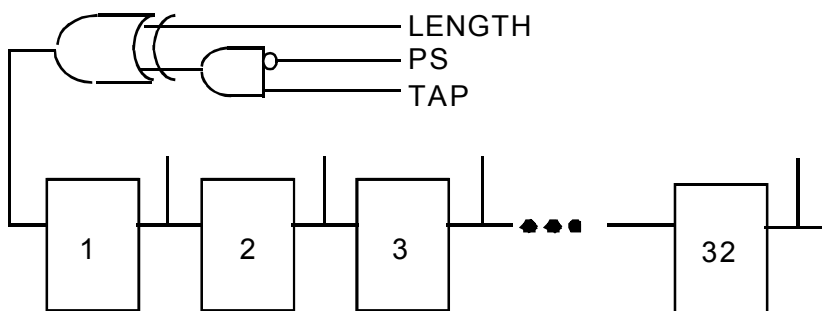
The pattern generator consists of a 32-bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

13.14.1 Generating and detecting repetitive patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic one. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion Registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48-bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences.

Note: The PRGD does *not* look for the pattern loaded into the Pattern Insertion Registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control Register, and reading the Pattern Detector Registers, which will then contain the 32 bits detected immediately prior to the strobe.

13.14.2 Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in the Table 42 and Table 43.

Table 42   Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^3 -1	00	02	FF	FF	FF	FF	0	0
2^4 -1	00	03	FF	FF	FF	FF	0	0
2^5 -1	01	04	FF	FF	FF	FF	0	0
2^6 -1	04	05	FF	FF	FF	FF	0	0
2^7 -1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0

$2^7 -1$ (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
$2^9 -1$ (O.153)	04	08	FF	FF	FF	FF	0	0
$2^{10} -1$	02	09	FF	FF	FF	FF	0	0
$2^{11} -1$ (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
$2^{15} -1$ (O.151)	0D	0E	FF	FF	FF	FF	1	1
$2^{17} -1$	02	10	FF	FF	FF	FF	0	0
$2^{18} -1$	06	11	FF	FF	FF	FF	0	0
$2^{20} -1$ (O.153)	02	13	FF	FF	FF	FF	0	0
$2^{20} -1$ (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
$2^{21} -1$	01	14	FF	FF	FF	FF	0	0
$2^{22} -1$	00	15	FF	FF	FF	FF	0	0
$2^{23} -1$ (O.151)	11	16	FF	FF	FF	FF	1	1
$2^{25} -1$	02	18	FF	FF	FF	FF	0	0
$2^{28} -1$	02	1B	FF	FF	FF	FF	0	0
$2^{29} -1$	01	1C	FF	FF	FF	FF	0	0
$2^{31} -1$	02	1E	FF	FF	FF	FF	0	0

Table 43   Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

Notes (For the Pseudo Random and Repetitive Pattern Generation Tables)

1. The PS bit and the QRSS bit are contained in the PRGD Control Register

2. TR is the PRGD Tap Register

3. LR is the PRGD Length Register

4. IR#1 is the PRGD Pattern Insertion #1 Register

5. IR#2 is the PRGD Pattern Insertion #2 Register

6. IR#3 is the PRGD Pattern Insertion #3 Register

7. IR#4 is the PRGD Pattern Insertion #4 Register

8. The TINV bit and the RINV bit are contained in the PRGD Control Register

13.15   JTAG Support

The S/UNI-JET supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The TAP consists of the five standard pins (TRSTB, TCK, TMS, TDI, and TDO) used to control the TAP controller and the boundary scan registers.

The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 23.

Figure 23   Boundary Scan Architecture
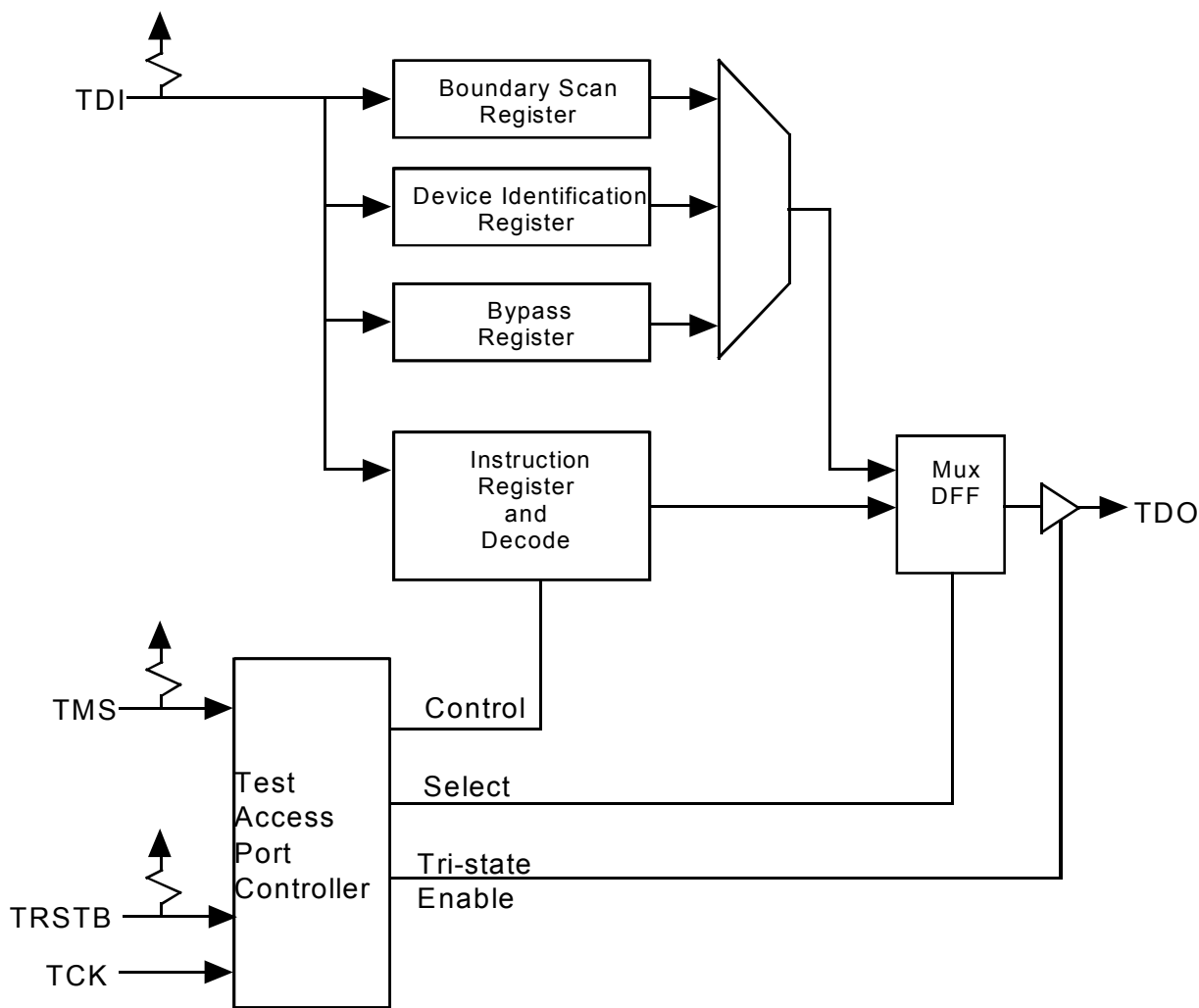
The boundary scan architecture consists of:

- A TAP controller.

- An instruction register with instruction decode.

- A bypass register

- A device identification register

- A boundary scan register.

The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.15.1   TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 24   TAP Controller Finite State Machine

All transitions dependent on input TMS
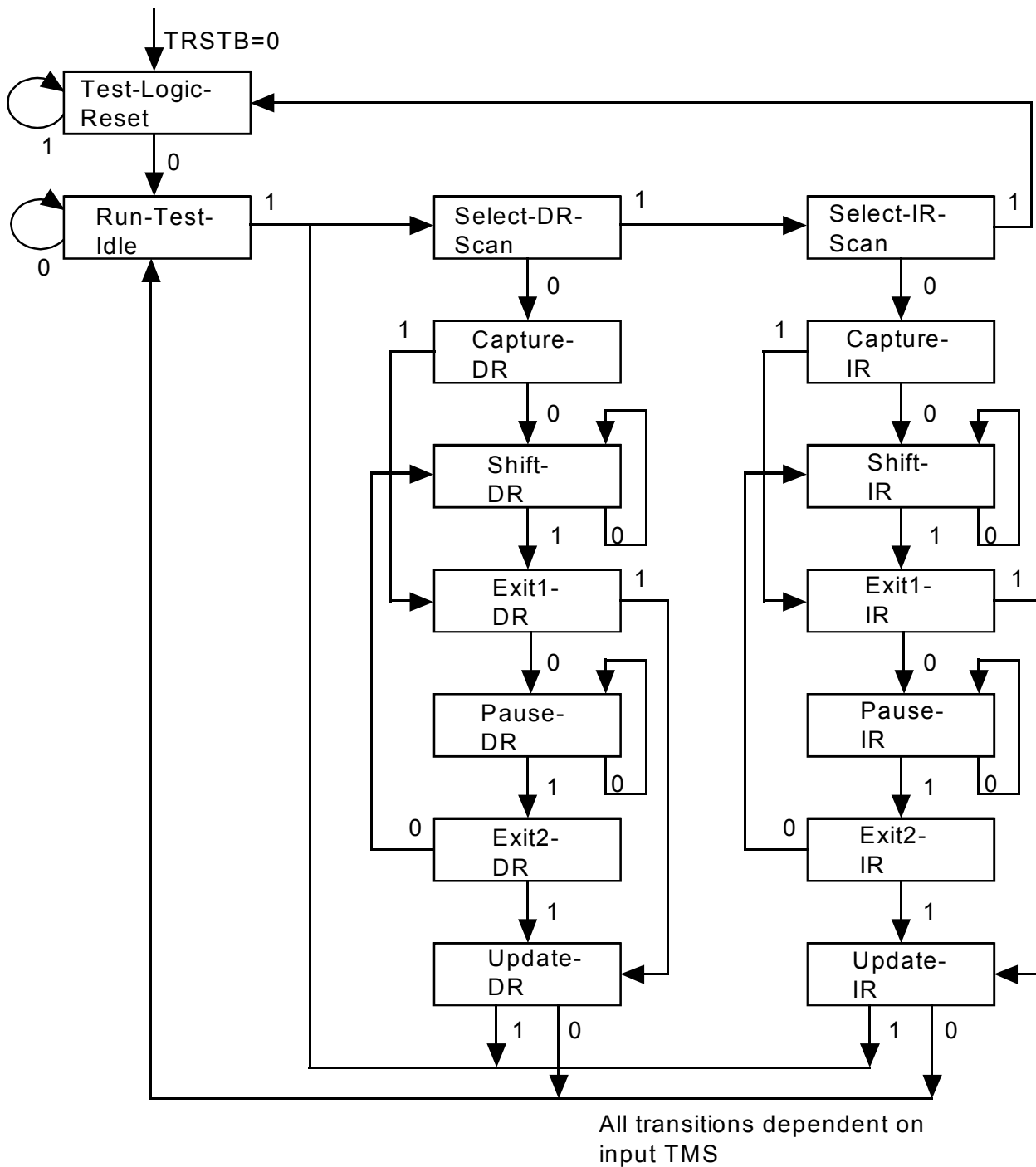
Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

Boundary Scan Cell Description

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located in the TEST FEATURES DESCRIPTION - JTAG Test Port section.

Figure 25 Input Observation Cell (IN_CELL)
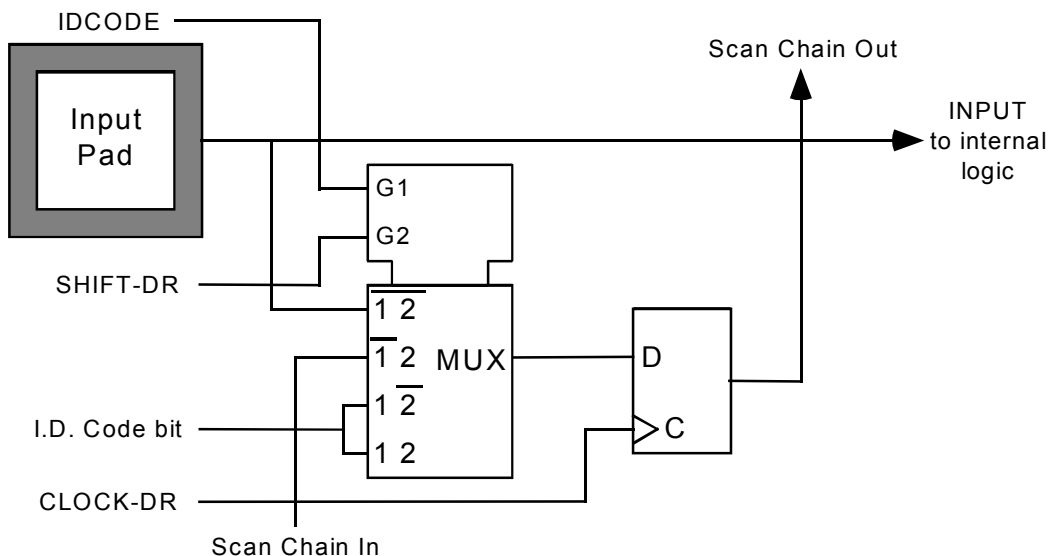
Figure 26 Output Cell (OUT_CELL)
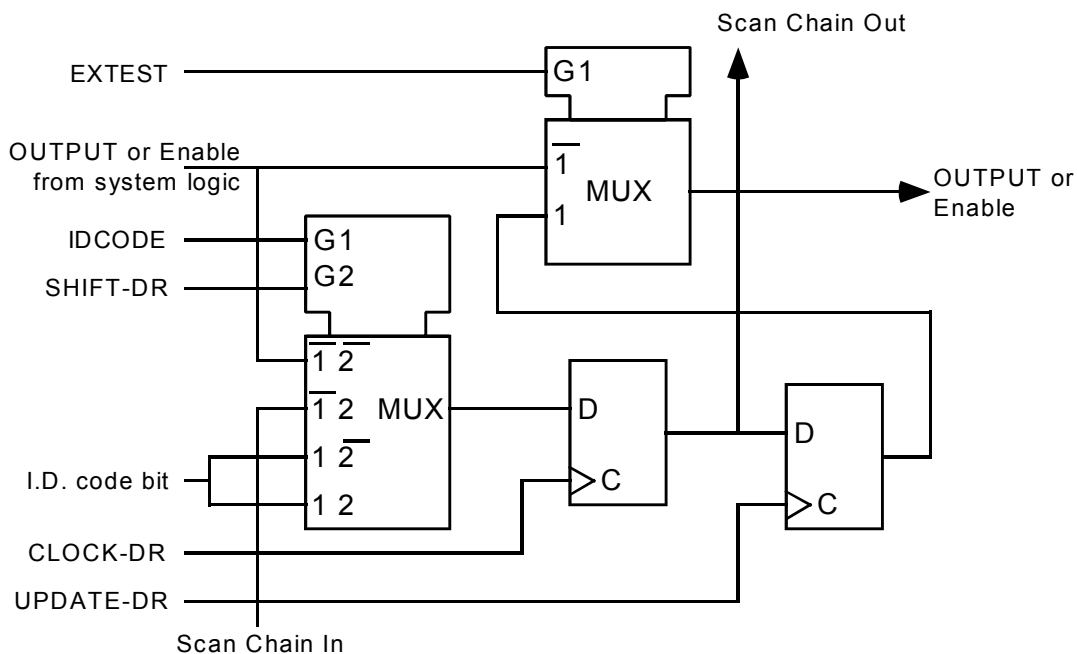
Figure 27 Bi-directional Cell (IO_CELL)
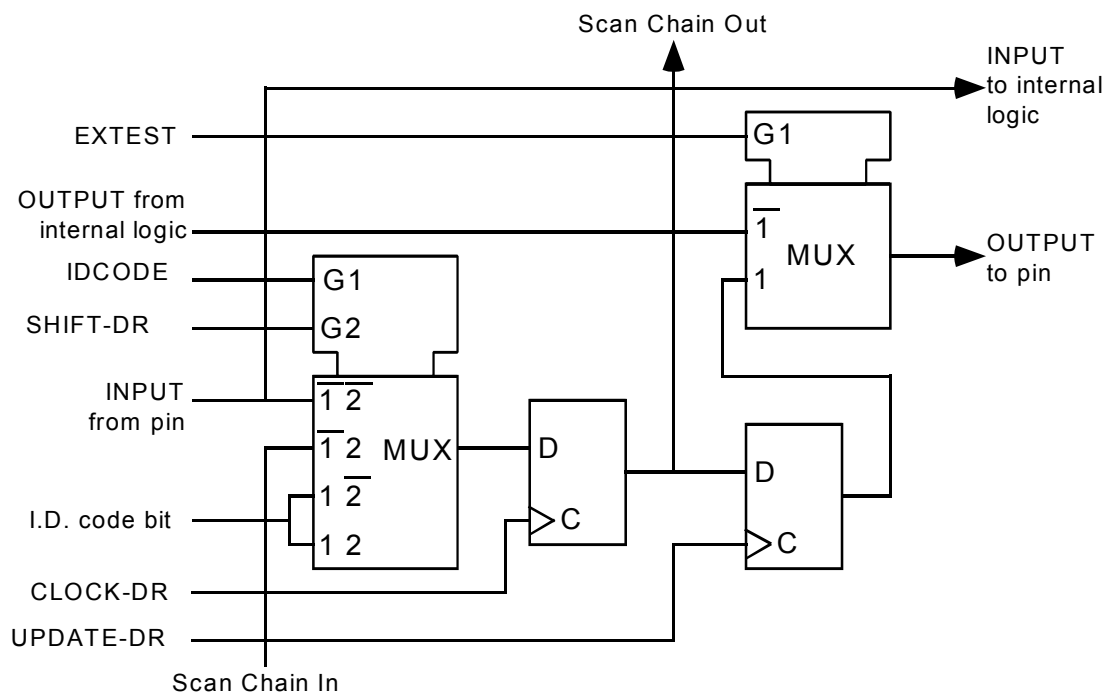
Figure 28 Layout of Output Enable and Bi-directional Cells
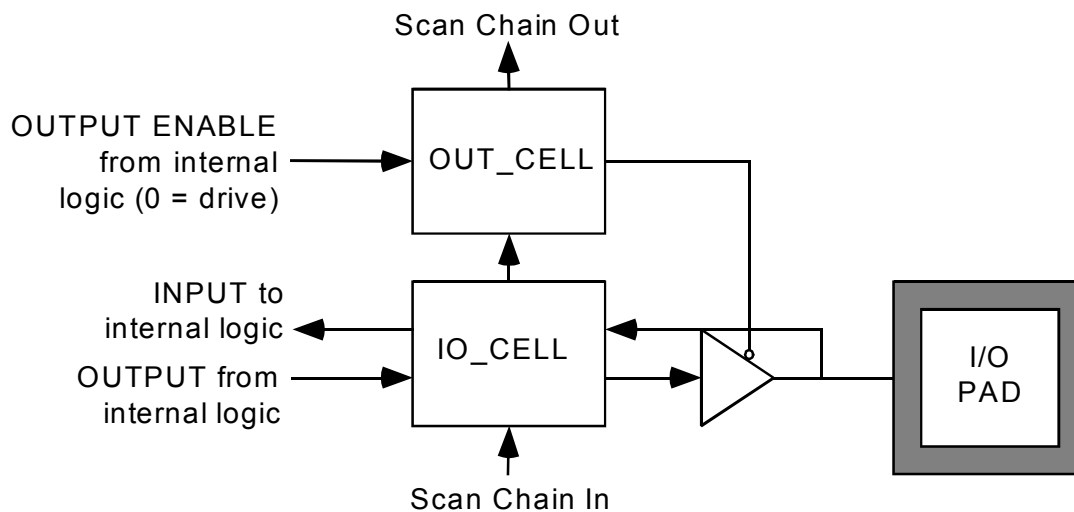
14 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-JET registers are set to their default states).

Figure 29   Receive DS1 Stream
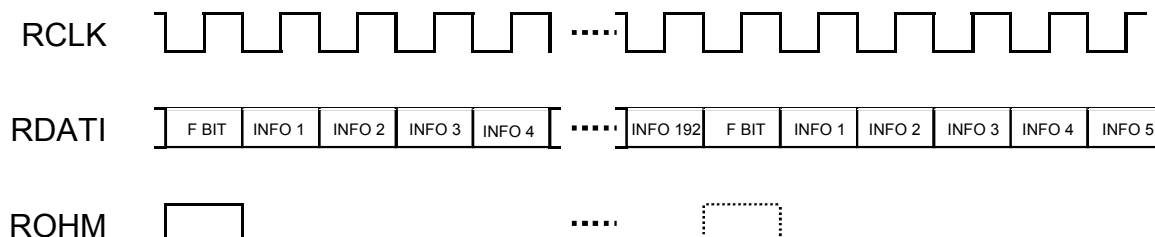
The Receive DS1 Stream diagram (Figure 29) shows the expected DS1 overhead indicators on ROHM when the S/UNI-JET is configured for DS1 PLCP or DS1 direct-mapped frame formats. Frame pulses on ROHM are not required to be present. Once internally synchronized by a pulse on ROHM, the S/UNI-JET can use its internal timeslot counter for DS1 overhead bit identification. The ATM cell stream is contained in RDATI, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to identify the DS1 framing bit position.

Figure 30   Receive E1 Stream
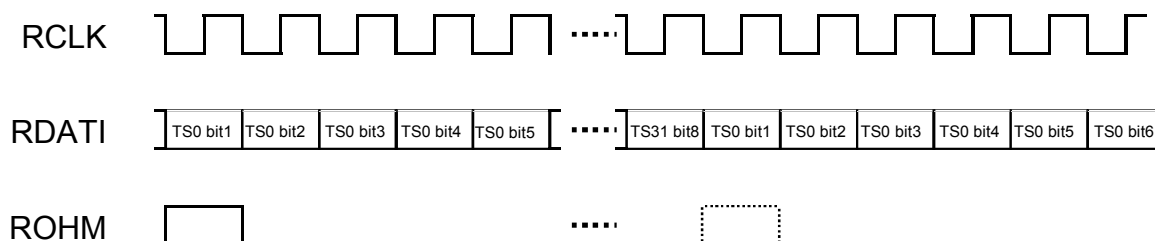
The expected Receive E1 Stream for direct-mapped or PLCP applications is shown in Figure 30. Frame pulses on ROHM are not required to be present every frame. Once internally synchronized by a pulse on ROHM, the S/UNI-JET can use its internal timeslot counter for E1 overhead bit identification. The ATM cell stream is contained in RDATI, along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to identify the E1 framing bit position.

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Document ID: PMC-1990267, Issue 3

**Figure 31   Receive Bipolar DS3 Stream**
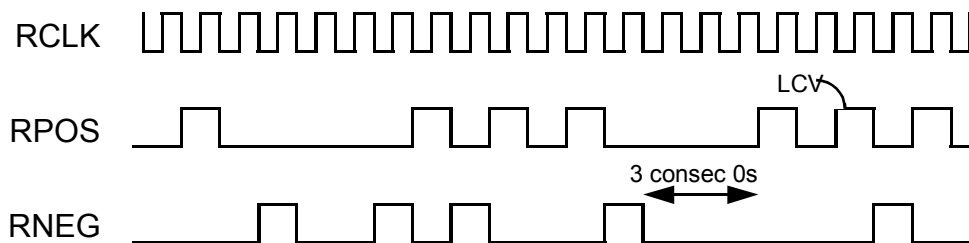
The Receive Bipolar DS3 Stream diagram (Figure 31) shows the operation of the S/UNI-JET while processing a B3ZS encoded DS3 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B3ZS signature. A LCV is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 32   Receive Unipolar DS3 Stream
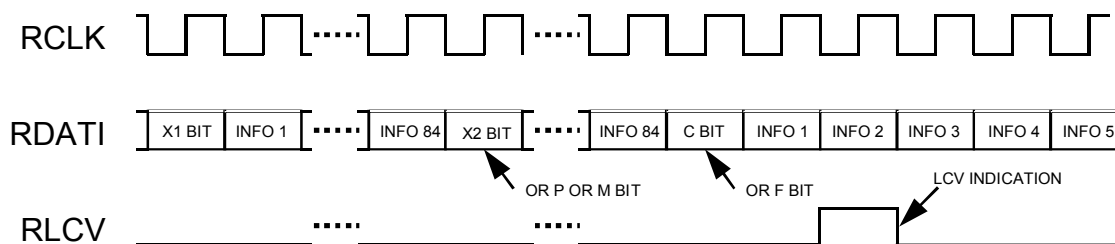
The Receive Unipolar DS3 Stream diagram (Figure 32) shows the complete DS3 receive signal on the RDATI input. LCV indications, detected by an upstream B3ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV.

Figure 33   Receive Bipolar E3 Stream
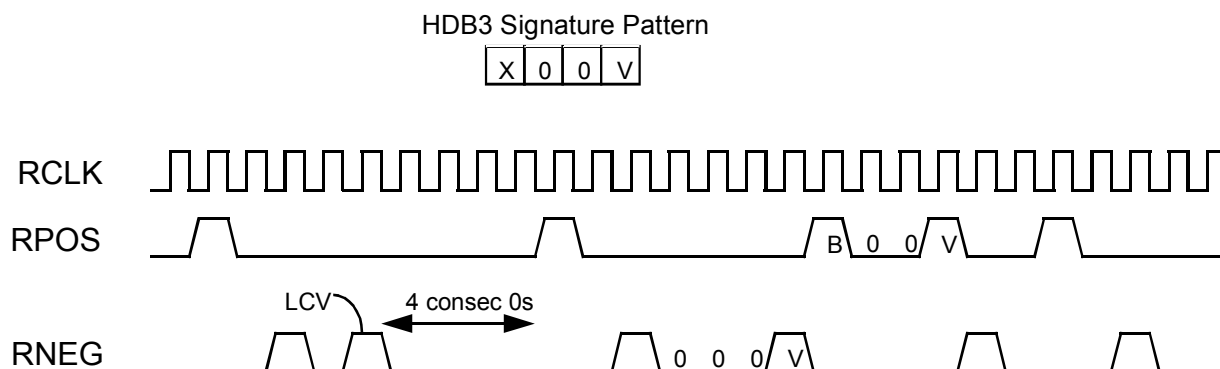
The Receive Bipolar E3 Stream diagram (Figure 33) shows the operation of the S/UNI-JET while processing an HDB3-encoded E3 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid HDB3 signature. A LCV is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid HDB3 signature.

Figure 34   Receive Unipolar E3 Stream
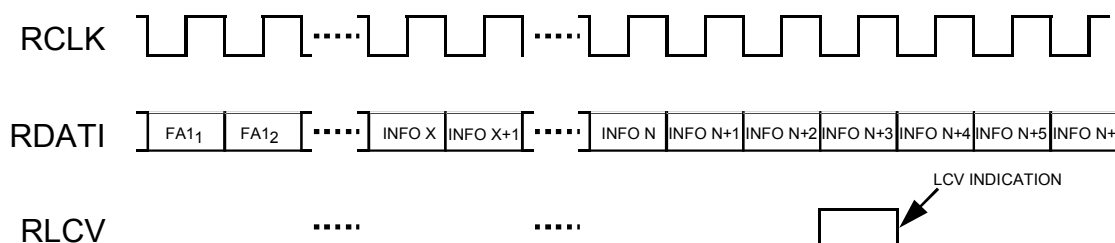
The Receive Unipolar E3 Stream diagram (Figure 34) shows the unipolar E3 receive signal on the RDATI input. LCV indications, detected by an upstream HDB3 decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV.

Figure 35   Receive Bipolar J2 Stream
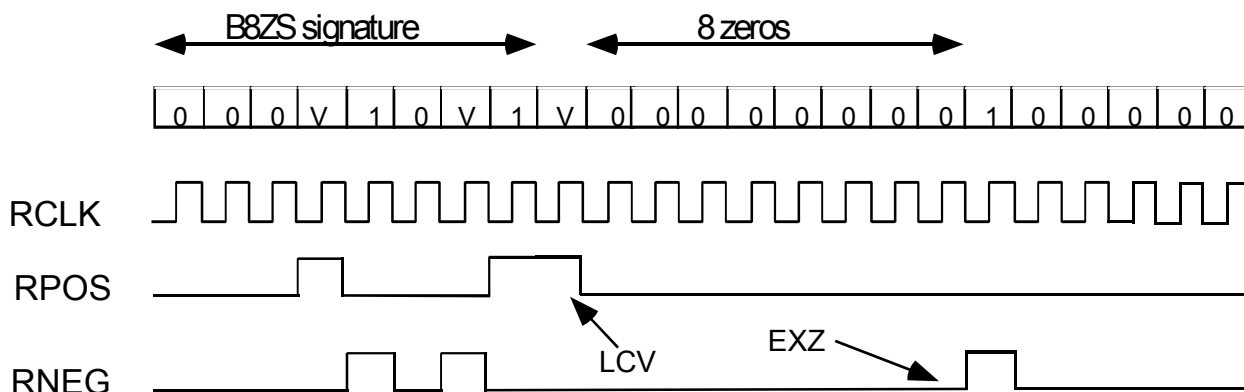
The Receive Bipolar J2 Stream diagram (Figure 35) shows the operation of the S/UNI-JET while processing a B8ZS-encoded J2 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B8ZS signature. A LCV is declared upon detection of a bipolar violation which is not part of a valid B8ZS signature. An excessive zeros indication is given when 8 or more consecutive zeros are detected.

Figure 36   Receive Unipolar J2 Stream
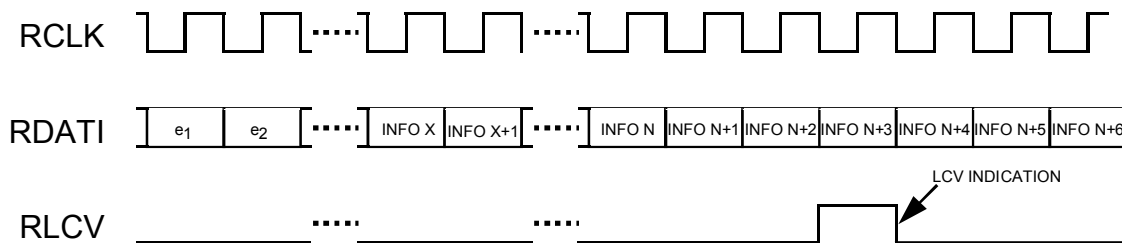
The Receive Unipolar J2 Stream diagram (Figure 36) shows the unipolar J2 receive signal on the RDATI input. LCV indications, detected by an upstream B8ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON LCV Event Counter is incremented each time a logic one is sampled on RLCV.

Figure 37   Generic Receive Stream
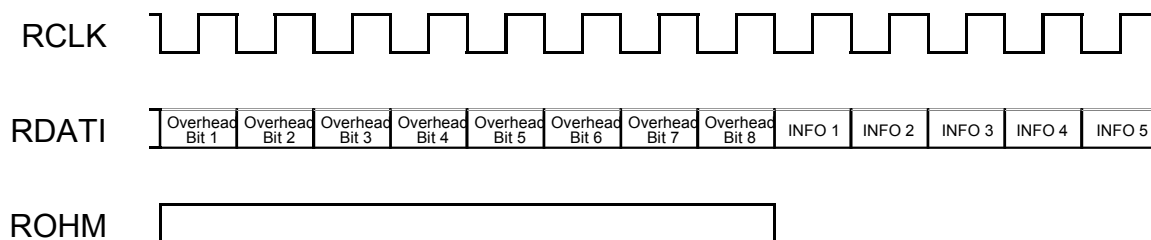
The generic receive stream diagram (Figure 37) illustrates how ROHM is used to mark the location of the transmission system overhead bits in the RDATI stream. RDATI and ROHM are both sampled on the rising edge of RCLK.

Figure 38   Receive DS3 Overhead
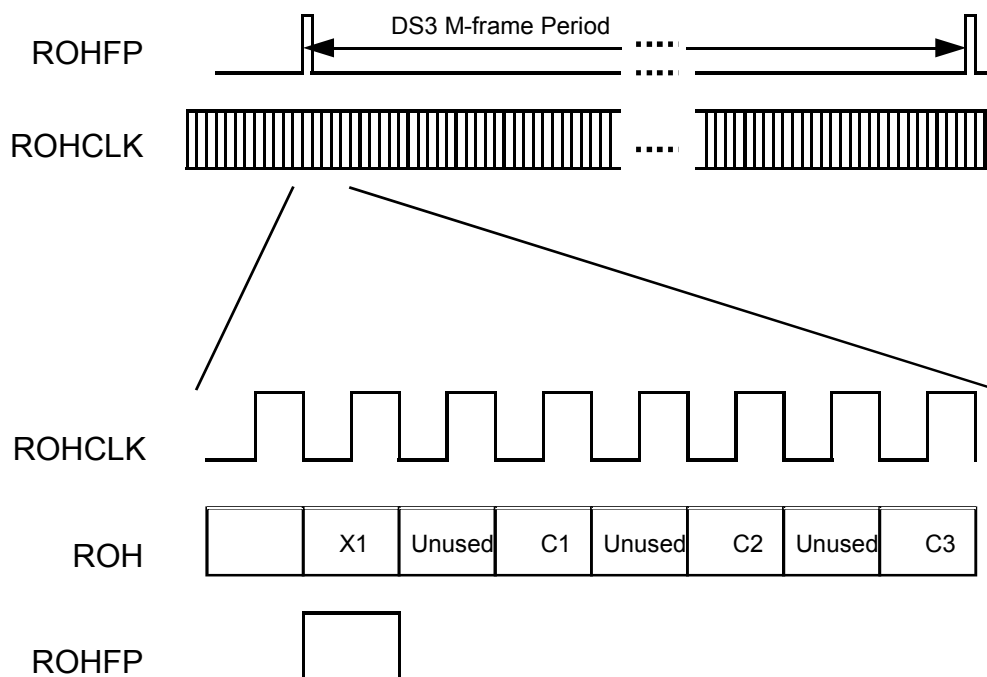
The Receive DS3 Overhead diagram (Figure 38) shows the extraction of the DS3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and

M-frame position indicator (ROHFP). The DS3 M-frame can be divided into seven M-subframes, with each subframe containing eight overhead bits. The table below illustrates the overhead bit order on ROH:

Table 44   DS3 Receive Overhead Bits

M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

The DS3 framing bits (F-bits) are not extracted on the overhead port. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table. The ROH stream is invalid when the DS3 frame alignment is lost.

Figure 39   Receive G.832 E3 Overhead

The Receive G.832 E3 Overhead diagram (Figure 39) shows the extraction of the G.832 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP).

Figure 40   Receive G.751 E3 Overhead

The Receive G.751 E3 Overhead diagram (Figure 40) shows the extraction of the G.751 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). The justification indication bits (C_{jk}) along with the justification opportunity bits (J_1-J_4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic zero).

Figure 41   Receive J2 Overhead
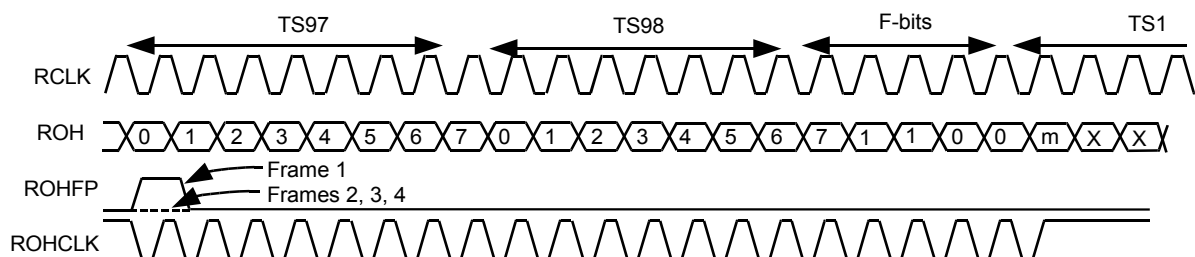
The Receive J2 Overhead diagram (Figure 41) shows the extraction of the J2 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). ROHCLK is a gapped clock with a maximum instantaneous rate equal to the RCLK frequency. ROHFP pulses on the first bit of TS97 in the first frame of each J2 multiframe.

Figure 42   Receive PLCP Overhead
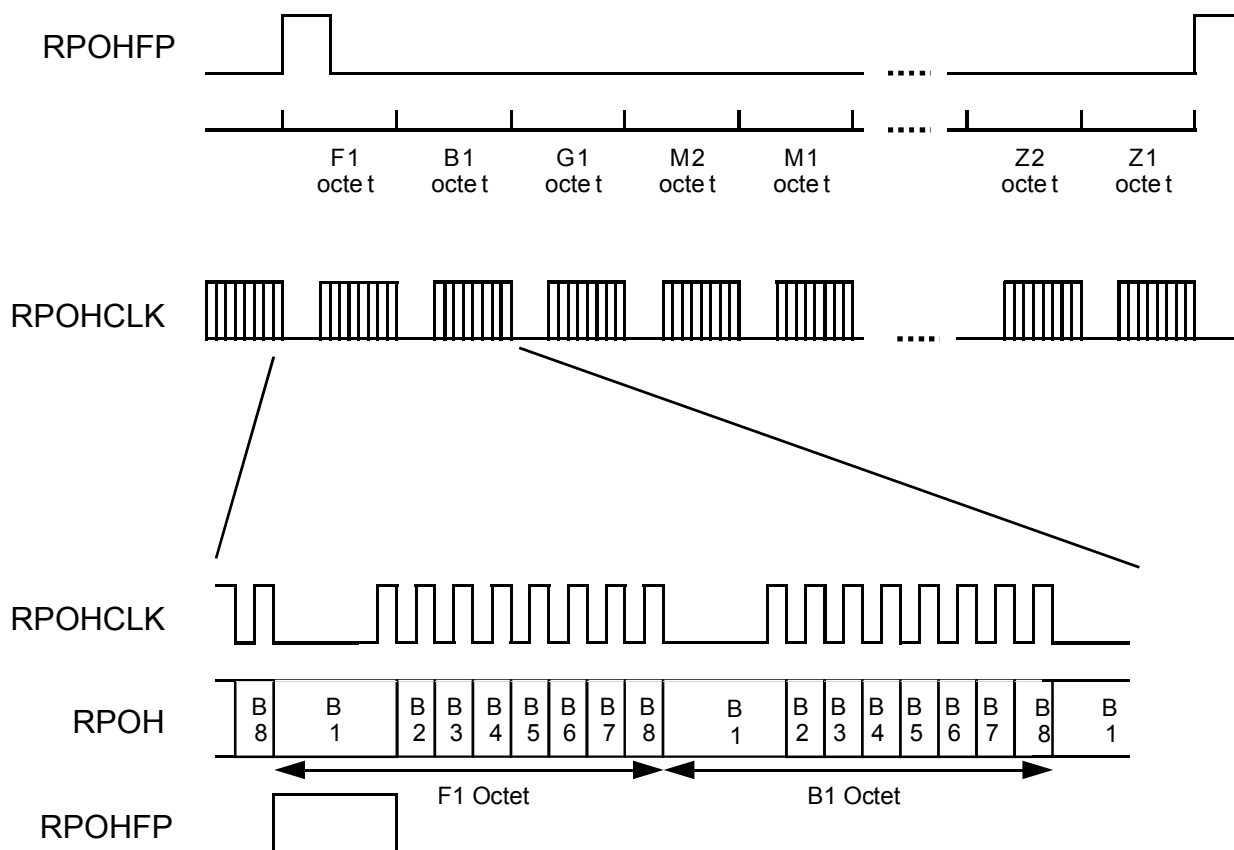
The Receive PLCP Overhead diagram (Figure 42) shows the extraction of the PLCP path overhead bits on the RPOH output, along with overhead clock (RPOHCLK), and PLCP frame position indicator (RPOHFP). The path overhead octets are shifted out in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (RPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the 8 kHz receive PLCP frame timing.

Figure 43   Transmit DS1 Stream
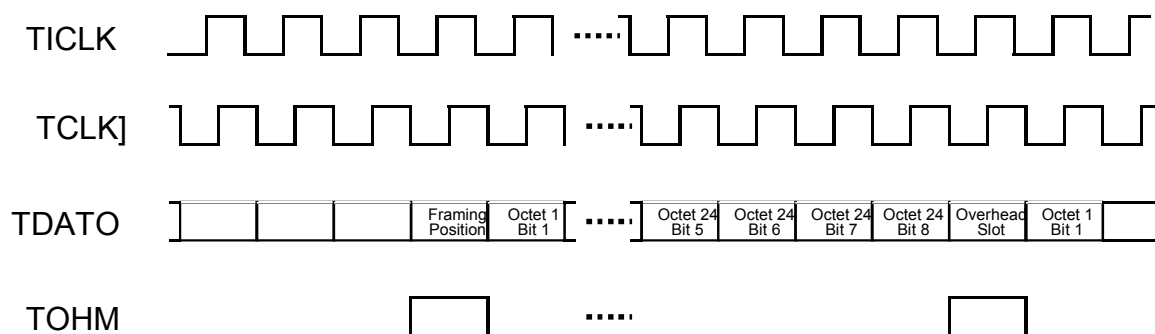
The Transmit DS1 Stream diagram (Figure 43) illustrates the generation of DS1 overhead indicators on TOHM when the S/UNI-JET is configured for DS1 PLCP or non-PLCP frame formats. The S/UNI-JET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC or PM4344 TQUAD) must be used to insert the appropriate DS1 framing pattern. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 44   Transmit E1 Stream
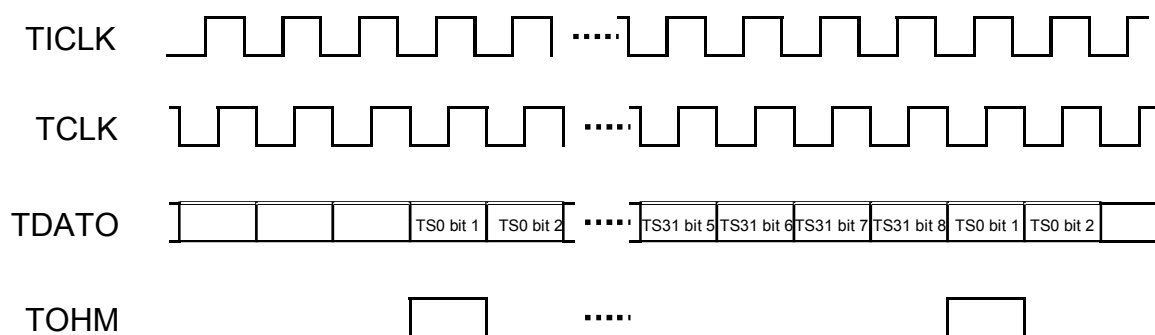
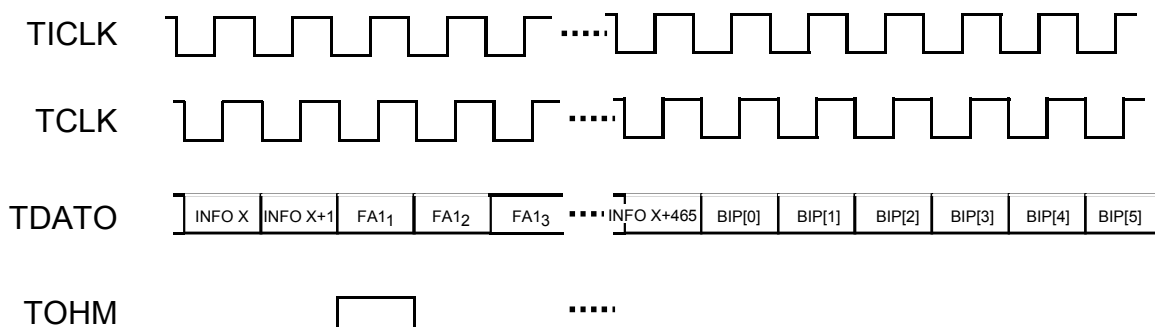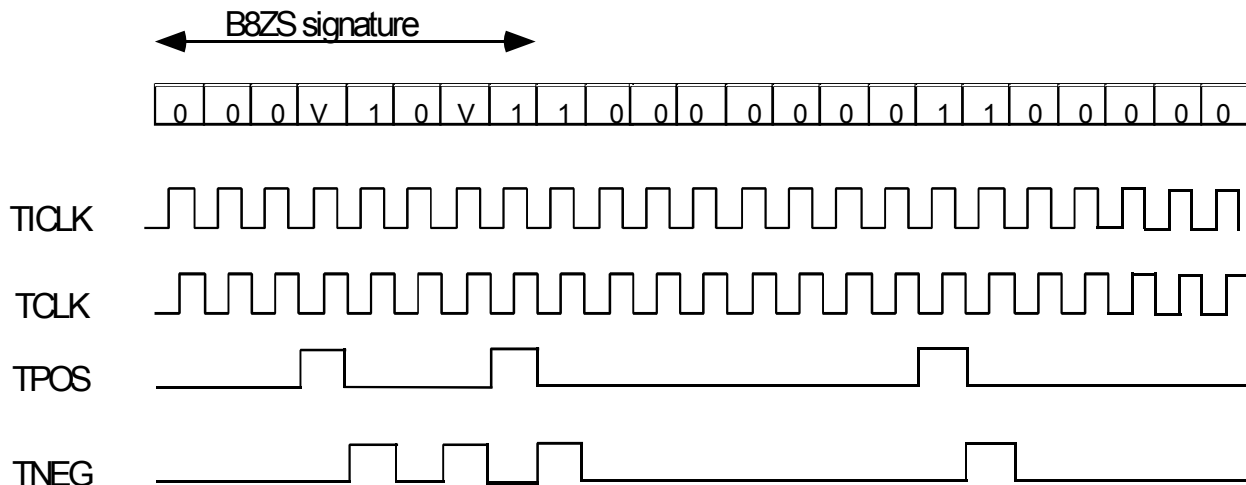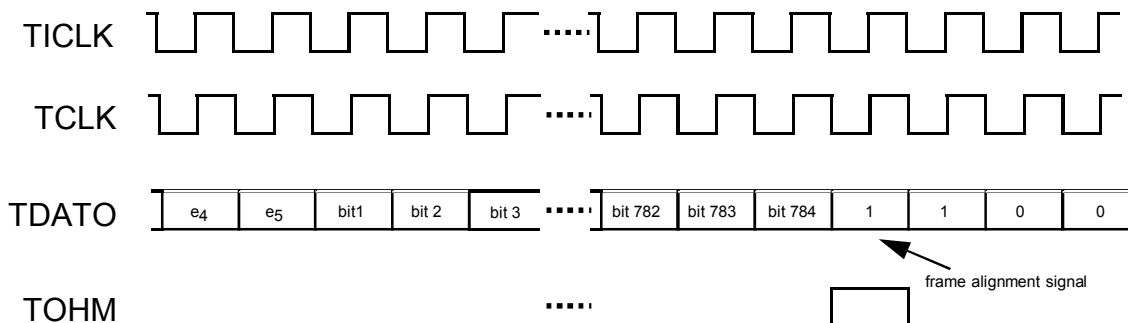The Transmit E1 Stream diagram (Figure 44) illustrates the generation of E1 frame alignment indicators on TOHM when the S/UNI-JET is configured for E1 PLCP or non-PLCP frame formats. The S/UNI-JET flywheels using its internal timeslot counter to generate TOHM. The ATM cell stream is inserted in TDATO, along with a framing bit placeholder every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC or PM6344 EQUAD) must be used to insert the appropriate E1 framing pattern. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 45   Transmit Bipolar DS3 Stream
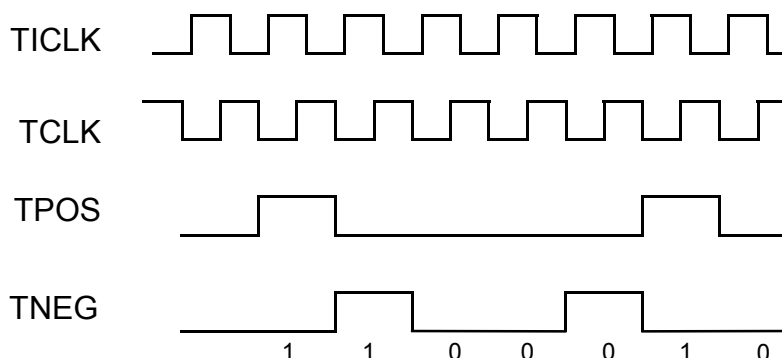
The Transmit Bipolar DS3 Stream diagram (Figure 45) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 46   Transmit Unipolar DS3 Stream
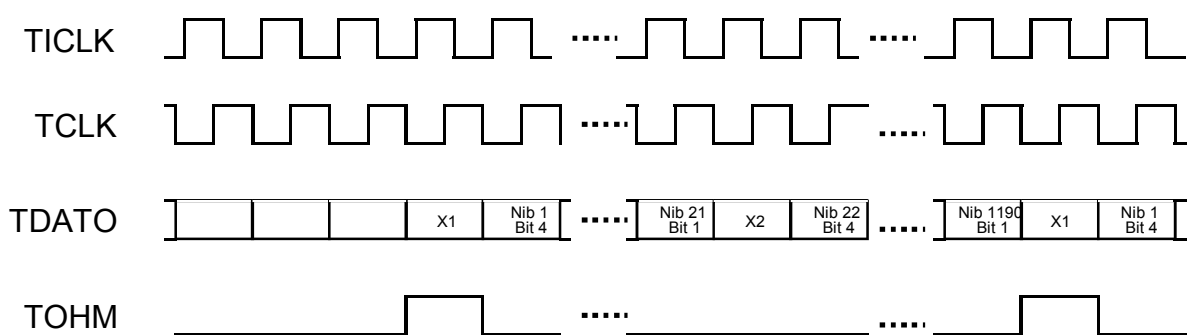
The Transmit Unipolar DS3 Stream diagram (Figure 46) illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TDATO. The TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

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Figure 47 Transmit Bipolar E3 Stream
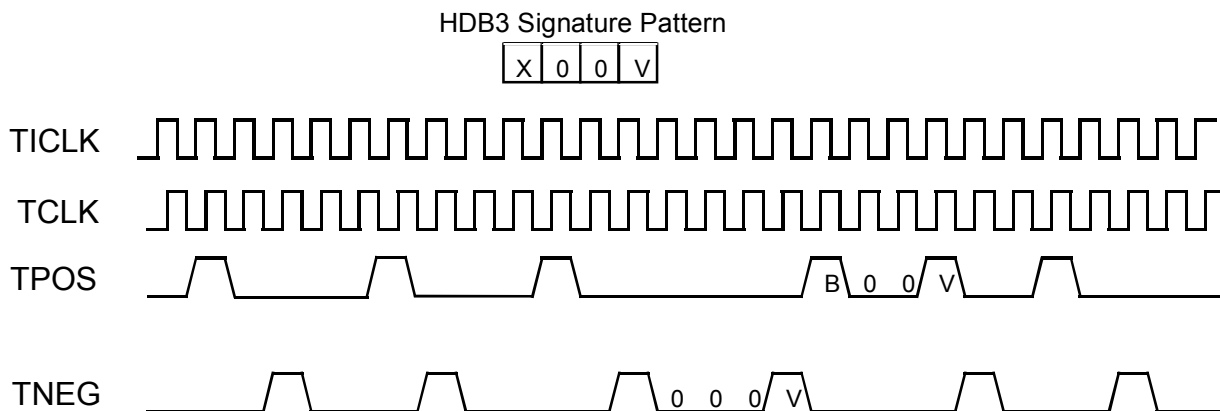
The Transmit Bipolar E3 Stream diagram (Figure 47) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a E3 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 48 Transmit Unipolar E3 Stream

The Transmit Unipolar E3 Stream diagram (Figure 48) illustrates the unipolar E3 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TDATO. The TOHM output shown marks the G.832 frame boundary (the first bit of the FA1 frame alignment byte) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 49   Transmit Bipolar J2 Stream

The Transmit Bipolar J2 Stream diagram (Figure 49) illustrates the generation of a bipolar J2 stream. The B8ZS encoded J2 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a J2 line interface unit. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 50   Transmit Unipolar J2 Stream

The Transmit Unipolar J2 Stream diagram (Figure 50) illustrates the unipolar J2 stream generation. The ATM cell stream, along with valid J2 overhead bits is contained in TDATO. The TOHM output shown marks the J2 multi-frame boundary (the first frame-alignment bit of each J2 multi-frame) in the transmit stream. Note: TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 51   Generic Transmit Stream

TICLK bit logic 0:
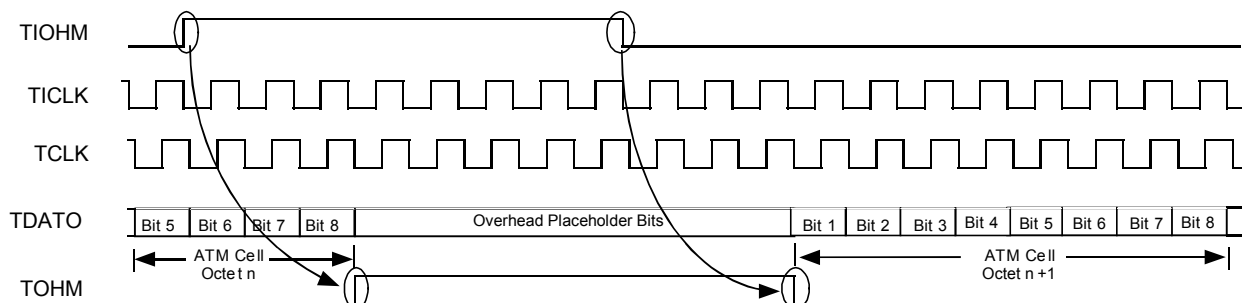
TICLK bit logic 1:
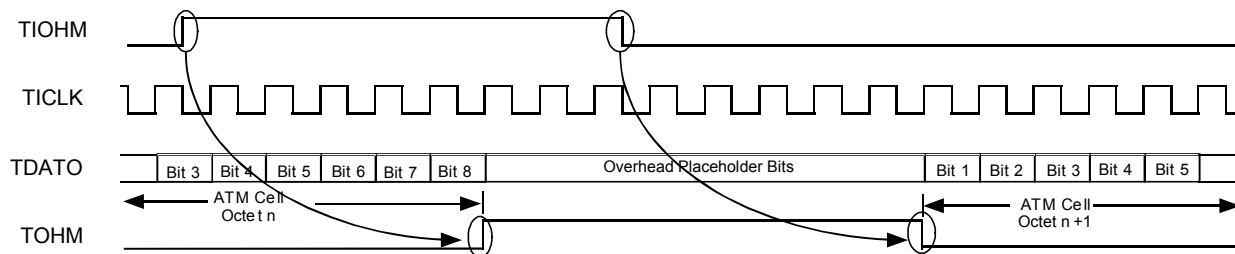
The Generic Transmit Stream diagram (Figure 51) illustrates overhead indication positions when interfacing to a non-PLCP based transmission system not supported by the SUNI-QJET. The overhead bit placeholder positions are indicated using the TIOHM input. The ATM cells presented in the TDATO transmit stream are held off to include the overhead placeholders. The location of these placeholder positions is indicated by TOHM. A downstream framer inserts the correct overhead information in the placeholder positions.

The delay between TIOHM and TOHM is dependent on the state of the TICLK bit of the S/UNI-JET Transmit Configuration Register. If the TICLK bit is a logic zero, TOHM is updated on the falling TCLK edge. TCLK is a flow-through version of TICLK and the propagation delay between TICLK and TCLK may vary depending on specific configurations. If the TICLK bit is a logic one, TOHM is presented on the fifth rising edge of TICLK after the rising edge which samples TIOHM.

Figure 52   Transmit DS3 Overhead
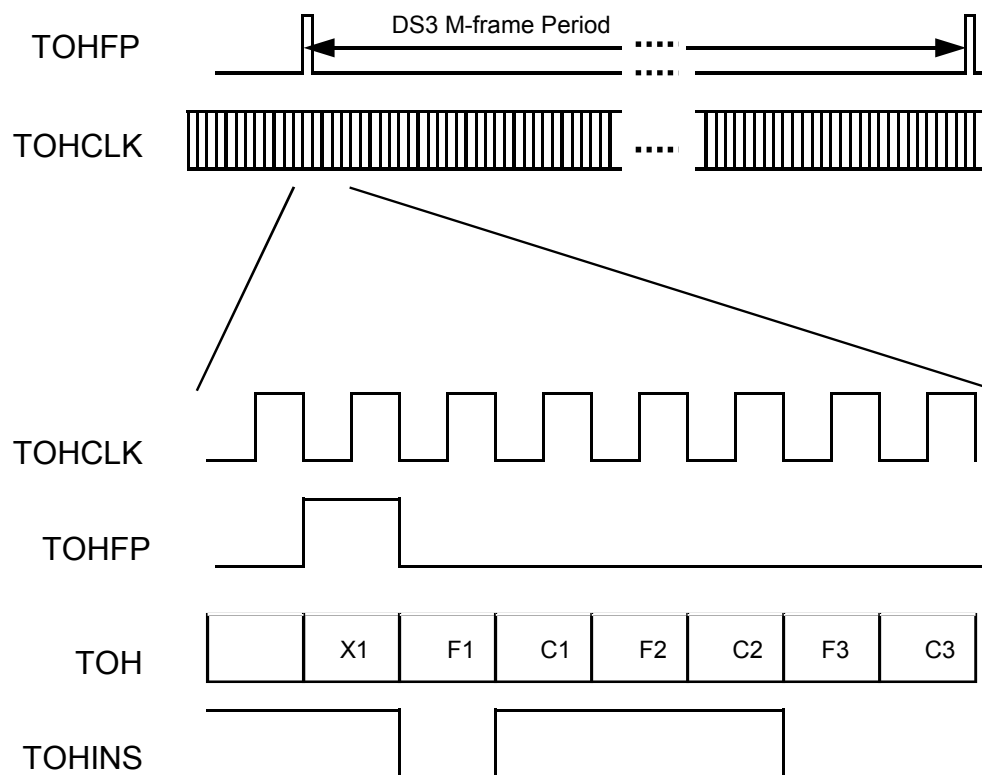
The Transmit DS3 Overhead diagram (Figure 52) shows the insertion of DS3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per DS3 M-frame period (during the X1 bit position). In Figure 52, the data sampled on TOH during the X1, C1, F2, and C2 bit positions is inserted into the DS3 overhead bits in the transmit stream. The F1, F3, and C3 overhead bits are internally generated by the S/UNI-JET . Table 45 illustrates the overhead bit order on TOH:

Table 45   DS3 Transmit Overhead Bits

| M-subframe	DS3 Overhead Bits							
	1	2	3	4	5	6	7	8
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

Figure 53   Transmit G.832 E3 Overhead
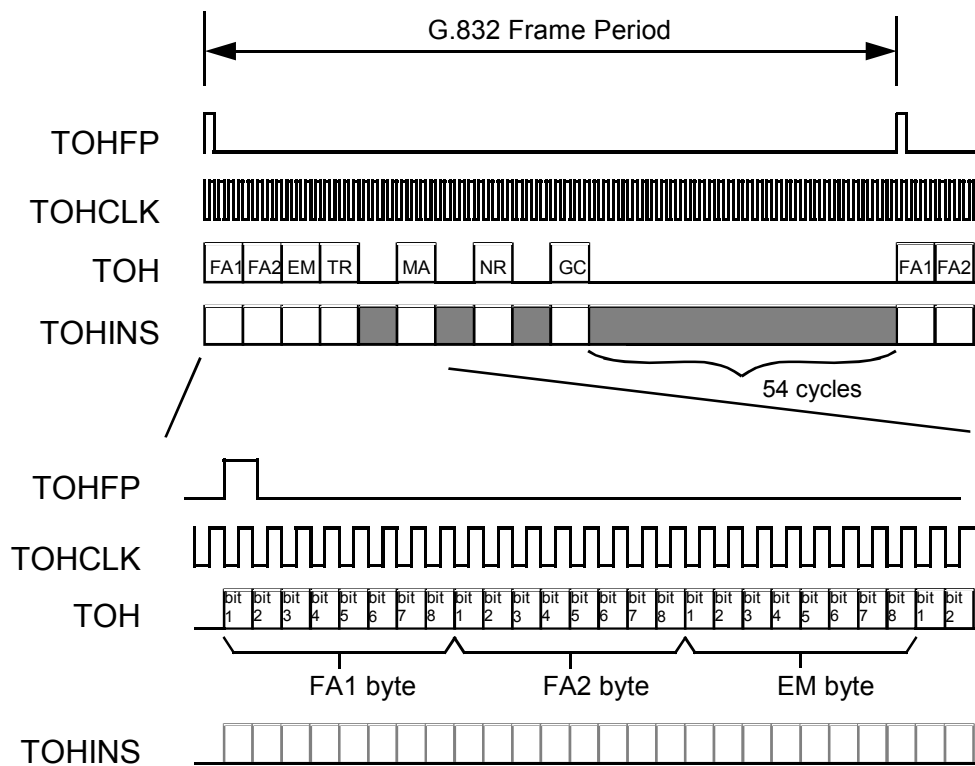
The Transmit G.832 E3 Overhead diagram (Figure 53) shows the insertion of G.832 E3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per G.832 frame period (during the first bit position of the FA1 byte). In Figure 53, the bit data sampled on TOH during each byte position while TOHINS is logic one is inserted into the G.832 E3 overhead bits in the transmit stream. Note: If an entire byte is to be replaced with data from the TOH stream, TOHINS must be held logic one for the duration of that byte position. Also Note: The EM byte behaves as an error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead. Asserting TOHINS during the "gaps" in the TOH stream has no effect.

Figure 54   Transmit G.751 E3 Overhead
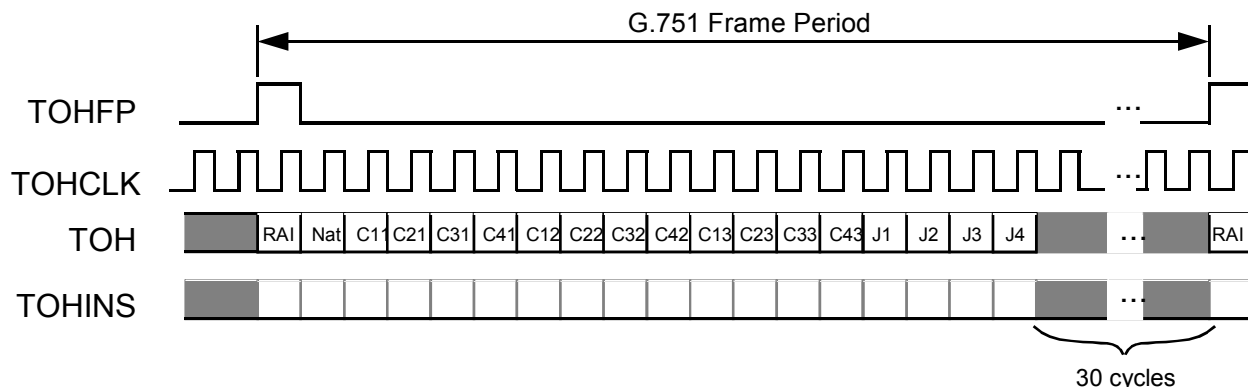
The Transmit G.751 E3 Overhead diagram (Figure 54) shows the insertion of G.751 overhead bits RAI, the National Use Bit, and the stuff indication and opportunity bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic one once per G.751 E3 frame period (during the RAI bit position). In Figure 54, the data sampled on TOH during the RAI, National Use, or stuff bit positions while TOHINS is logic one is inserted into the G.751 E3 overhead bits in the transmit stream.

The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options Register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

Figure 55   Transmit J2 Overhead
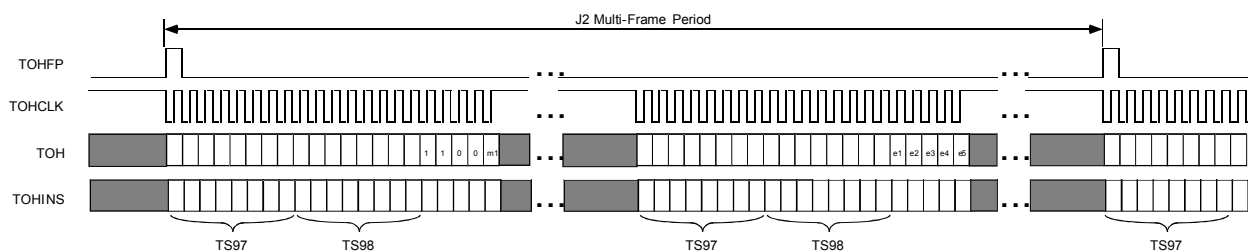
The Transmit J2 Overhead diagram (Figure 55) shows the insertion of J2 overhead bits using the TOH and TOHINS inputs. The TOHFP output is set to logic one once per J2 multiframe (for the first bit of TS97 in the first frame of the J2 multiframe). TOHCLK is a gapped clock which will pulse at a maximum instantaneous rate equal to the TICLK frequency. When TOHINS is a logic one, the TOH input pin state replaces that generated within the J2 TRAN block. TOH and TOHINS are sampled on the rising TOHCLK clock edge.

Figure 56   Transmit PLCP Overhead
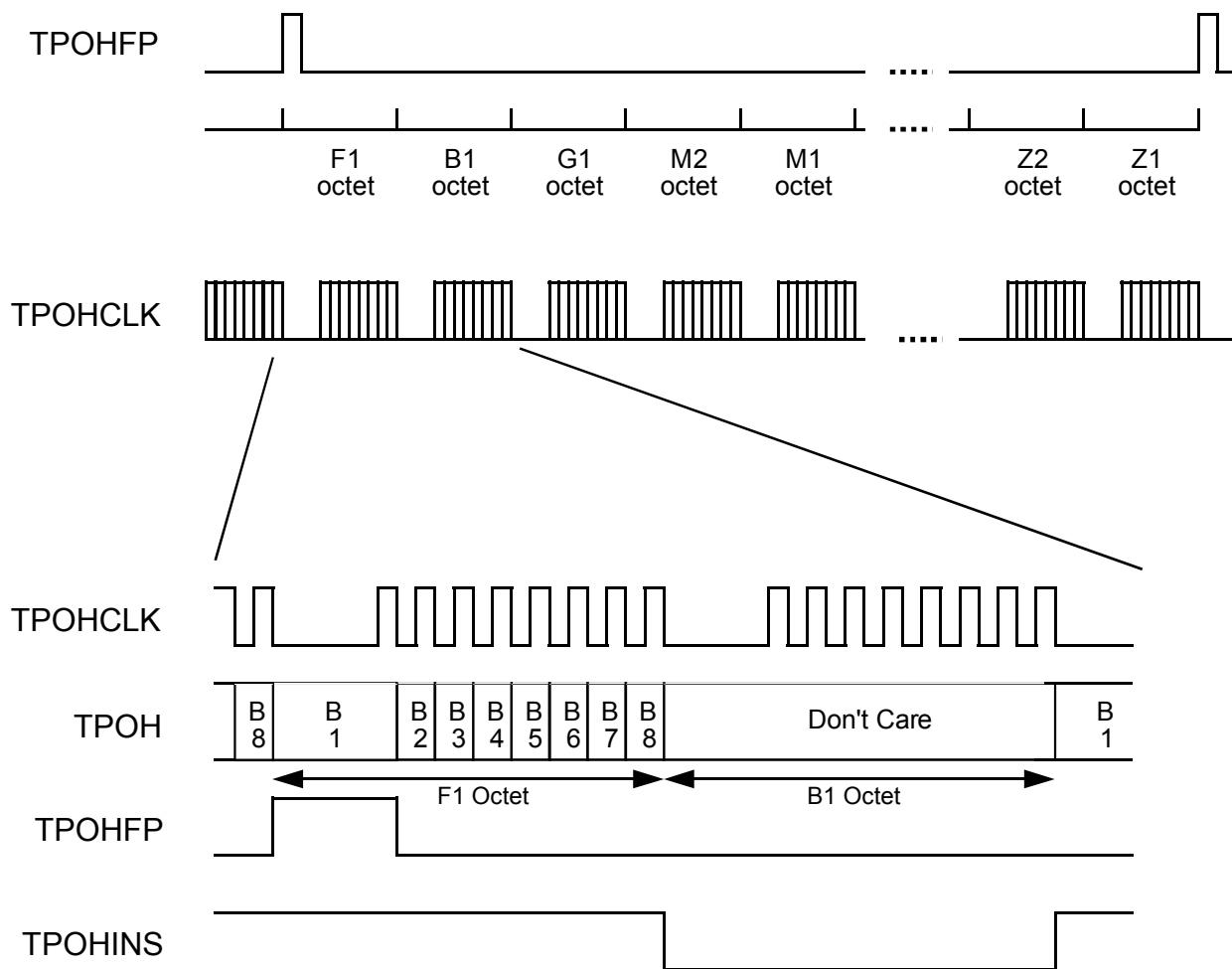
The Transmit PLCP Overhead diagram (Figure 56) shows the insertion of the PLCP path overhead bits using the TPOH input, along with overhead clock (TPOHCLK), and PLCP frame position indicator (TPOHFP). The path overhead octets are shifted in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (TPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the transmit PLCP frame timing. TPOH and TPOHINS are sampled using the rising edge of TPOHCLK. The bit presented on TPOH is only inserted into the path overhead if TPOHINS is asserted during the bit in question, or if the appropriate bit is set in the SPLT Control Register. the timing diagram above assumes that the SRCB1 bit in the SPLT Control Register is programmed to logic zero, thereby selecting internal insertion of that octet.

Figure 57   Framer Mode DS3 Transmit Input Stream
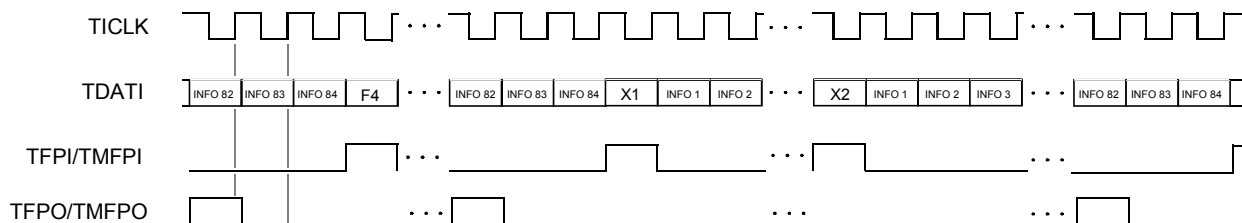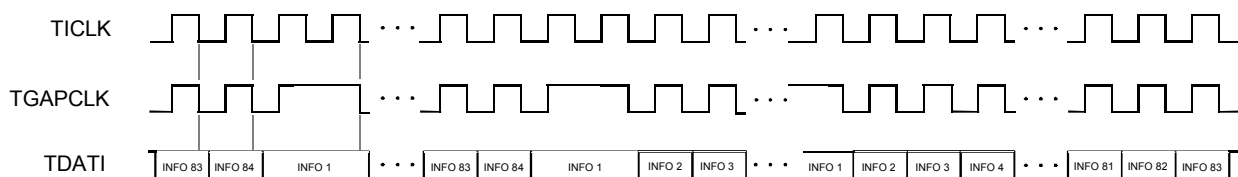

Figure 58   Framer Mode DS3 Transmit Input Stream With TGAPCLK

The Framer Mode DS3 Transmit Input Stream diagrams (Figure 57 and Figure 58) show the expected format of the inputs TDATI and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set, and the S/UNI-JET is configured for the DS3 transmit format. If the TXMFPI register bit is logic zero, then TFPI is valid, and the S/UNI-JET will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI. If the TXMFPI register bit is logic one, then TMFPI is valid, and the S/UNI-JET will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI. If the TXMFPO register bit is logic zero, then TFPO is valid, and the S/UNI-JET will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse. If the TXMFPO register bit is logic one, then TMFPO is valid and the S/UNI-JET will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one, as in Figure 58. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

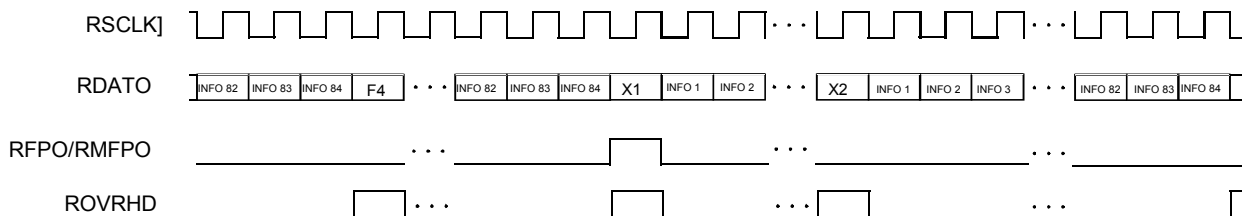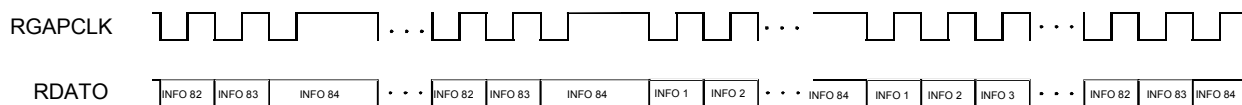**Figure 59   Framer Mode DS3 Receive Output Stream**

Figure 60   Framer Mode DS3 Receive Output Stream with RGAPCLK

The Framer Mode DS3 Receive Output Stream diagrams (Figure 59 and Figure 60) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set. Figure 59 shows the data streams when the S/UNI-JET is configured for the DS3 receive format. If the RXMFPO and 8KREFO register bits are logic zero, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic one (as shown in Figure 59) and the 8KREFO register bit is logic zero, RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. As shown in Figure 60 the RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one. RGAPCLK remains high during the overhead bit positions and RDATO does not change.

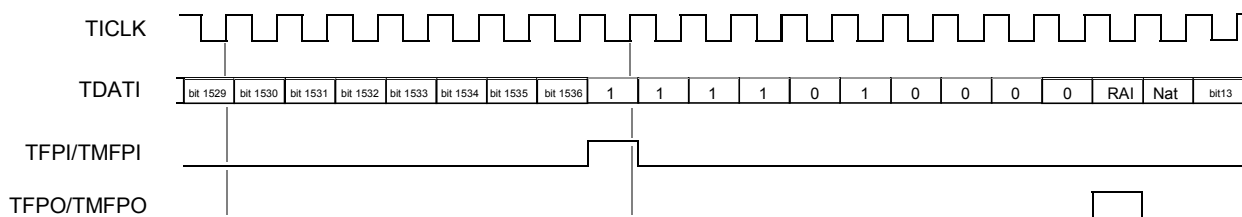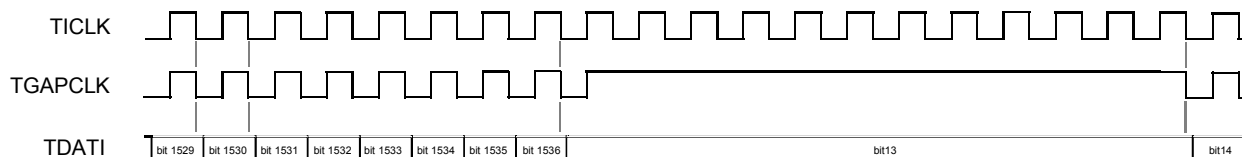**Figure 61   Framer Mode G.751 E3 Transmit Input Stream**

Figure 62   Framer Mode G.751 E3 Transmit Input Stream With TGAPCLK

The Framer Mode G.751 E3 Transmit Input Stream diagrams (Figure 61 and Figure 62) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set, and the S/UNI-JET is configured for the E3 G.751 transmit format. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the frame alignment signal in the G.751 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 1536 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one, as in Figure 62. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

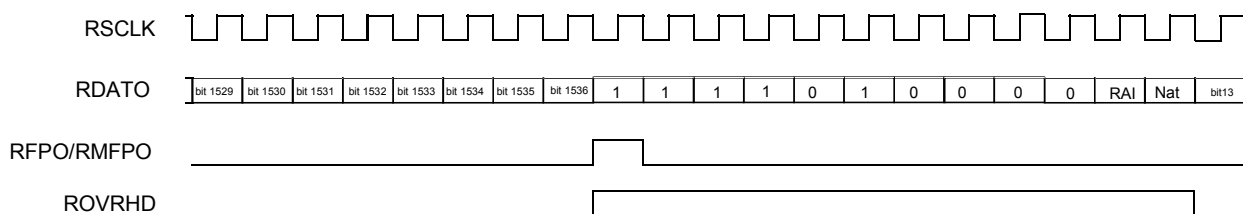**Figure 63   Framer Mode G.751 E3 Receive Output Stream**

Figure 64   Framer Mode G.751 E3 Receive Output Stream with RGAPCLK

The Framer Mode G.751 E3 Receive Output Stream diagrams (Figure 63 and Figure 64) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY and the 8KREFO bits in the S/UNI-JET Configuration 1 Register are set to logic one and logic zero respectively. Figure 63 shows the data streams when the S/UNI-JET is configured for the E3 G.751 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the framing alignment signal in the G.751 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. If the PYLD&JUST register bit in the E3 FRMR Maintenance Options Register is set to logic zero, the C_{jk} and P_k bits in the RDATO stream will be marked as overhead bits. If the PYLD&JUST register bit is set to logic one, the C_{jk} and P_k bits in the RDATO stream will be marked as payload. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 64.

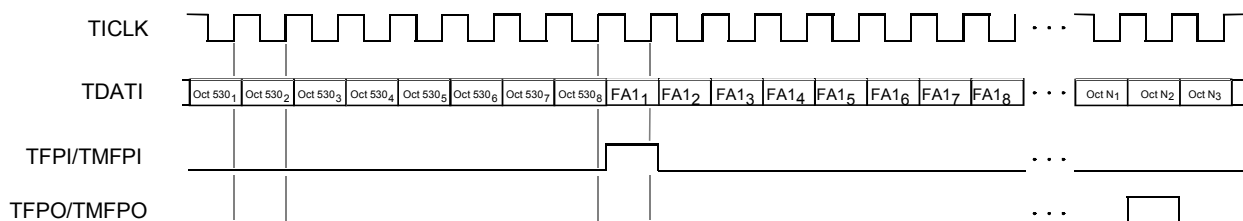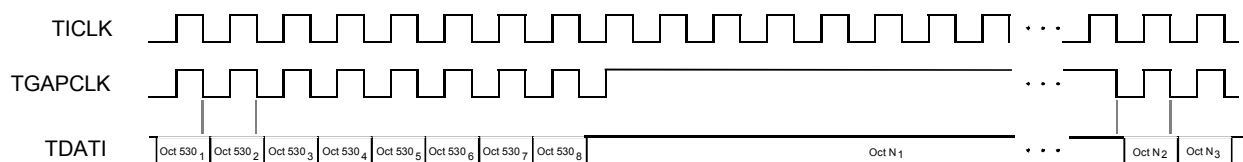**Figure 65   Framer Mode G.832 E3 Transmit Input Stream**

Figure 66   Framer Mode G.832 E3 Transmit Input Stream With TGAPCLK

The Framer Mode G.832 E3 Transmit Input Stream diagrams (Figure 65 and Figure 66) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set, and the S/UNI-JET is configured for the E3 G.832 transmit format. TFPI or TMFPI pulses high for one TICLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 input data stream on TDATI. TFPO or TMFPO will pulse high for one out of every 4296 TICLK cycles, providing upstream equipment with a reference frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one, as in Figure 66. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.
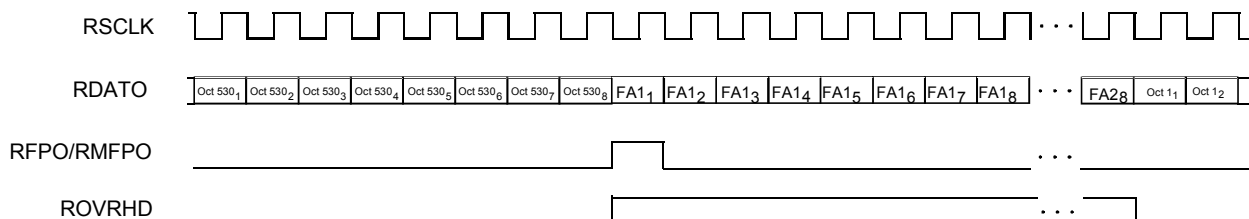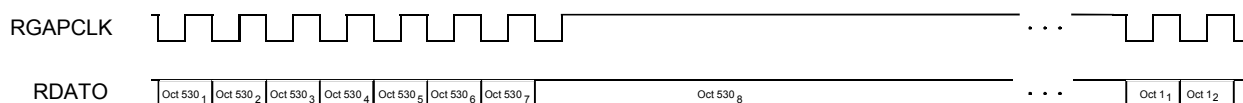
Figure 67   Framer Mode G.832 E3 Receive Output Stream

**Figure 68   Framer Mode G.832 E3 Receive Output Stream with RGAPCLK**

The Framer Mode G.832 E3 Receive Output Stream diagrams (Figure 67 and Figure 68) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set. Figure 67 shows the data streams when the S/UNI-JET is configured for the E3 G.832 receive format. RFPO or RMFPO pulses high for one RSCLK cycle and is aligned to the first bit of the FA1 byte in the G.832 E3 output data stream on RDATO. ROVRHD will be high for every overhead bit position on the RDATO data stream. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 68.

Figure 69   Framer Mode J2 Transmit Input Stream

Figure 70   Framer Mode J2 Transmit Input Stream With TGAPCLK
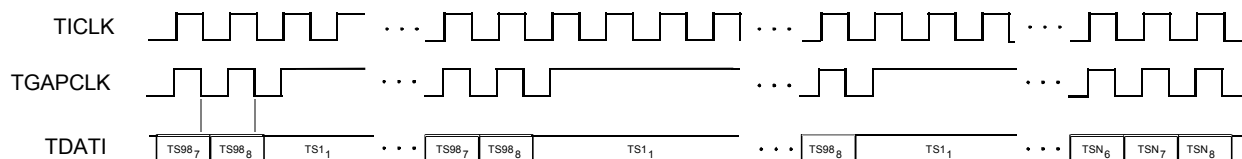
The Framer Mode J2 Transmit Input Stream diagrams (Figure 69 and Figure 70) show the expected format of the inputs TDATI, TFPI/TMFPI, and TICLK and the output TFPO/TMFPO (and TGAPCLK) when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set, and the S/UNI-JET is configured for the J2 transmit format. If the TXMFPI register bit is logic zero, then TFPI is valid (as shown in Figure 69). The S/UNI-JET will expect TFPI to pulse once every J2 frame with alignment to the first frame alignment bit on TDATI. If the TXMFPI register bit is logic one, then TMFPI is valid. The S/UNI-JET will expect TMFPI to pulse once every J2 multi-frame with alignment to the first frame alignment bit on TDATI. If the TXMFPO register bit is logic zero, then TFPO is valid. The S/UNI-JET will pulse TFPO once every 789 TICLK cycles, providing upstream equipment with a reference frame pulse. If the TXMFPO register bit is logic one, then TMFPO is valid and the S/UNI-JET will pulse TMFPO once every 3156 TICLK cycles, providing upstream equipment with a reference multi-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one, as in Figure 70. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the falling edge of TGAPCLK.

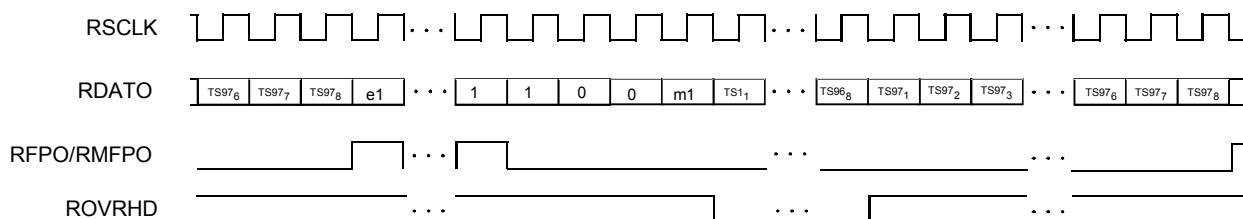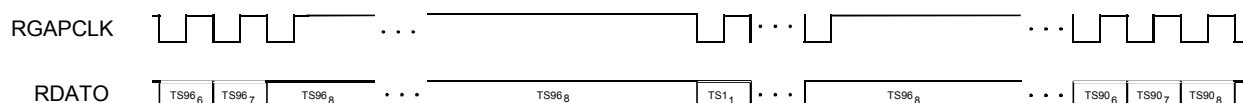### Figure 71   Framer Mode J2 Receive Output Stream

Figure 72   Framer Mode J2 Receive Output Stream with RGAPCLK

The Framer Mode J2 Receive Output Stream diagrams (Figure 71 and Figure 72) show the format of the outputs RDATO, RFPO/RMFPO, RSCLK (and RGAPCLK), and ROVRHD when the FRMRONLY bit in the S/UNI-JET Configuration 1 Register is set. Figure 71 shows the data streams when the S/UNI-JET is configured for the J2 receive format. If the RXMFPO register bit is a logic zero, RFPO is valid and will pulse high for one RSCLK cycle once each J2 frame with alignment to the first frame alignment bit on the RDATO data stream (as shown in Figure 71). If the RXMFPO register bit is a logic one, RMFPO is valid and will pulse high once each J2 multi-frame aligned to the first frame alignment bit on the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. The RGAPCLK output is available in place of RSCLK when the RXGAPEN bit in the S/UNI-JET Configuration 2 Register is set to logic one. RGAPCLK remains high during the overhead bit positions as shown in Figure 72.

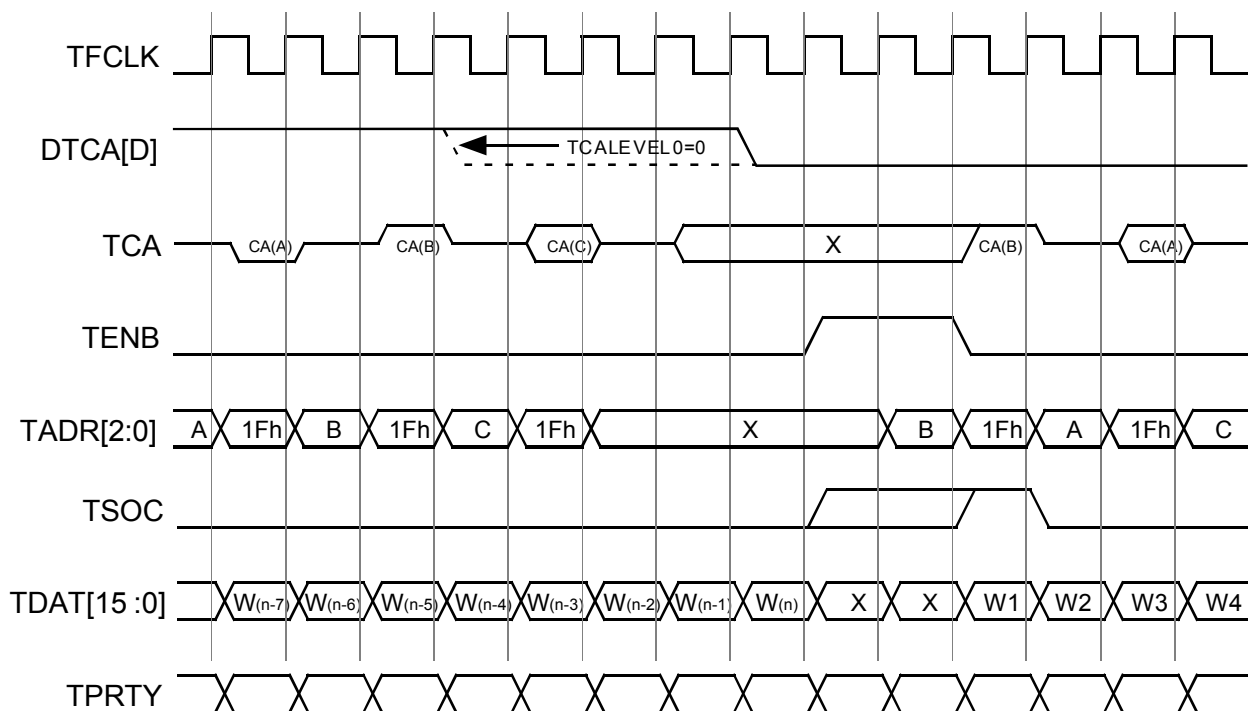**Figure 73   Multi-PHY Polling and Addressing Transmit Cell Interface**

Figure 73 is an example of the multi-PHY polling and selection sequence supported by the S/UNI-JET . "A", "B", "C", and "D" represent any arbitrary address values of PHY devices which may be occupied by the S/UNI-JET . The ATM Layer device is not restricted in its polling order. Initially PHY "D" is accepting a cell and the direct TCA for that PHY is shown as DTCA[D]. The effect of TCALEVEL0 is indicated with a dashed line in the figure. The PHY associated with address "A" indicates it cannot accept a cell, but PHY "B" indicates it is willing to accept a cell. As a result, the ATM Layer places address "B" on TADR[2:0] the cycle before TENB is asserted to select PHY "B" as the next cell destination. In this example, the PHY "C" status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted. The data on TDATI (W1, W2, ..) may be 8-bit or 16-bits wide, depending on the setting of the ATM8 input.

During multi-PHY operation, several PHY layer devices share the TCA signal. As a result, this signals must be tri-stated in all PHY devices which have not been selected for polling by the ATM Layer. The value of TADR[2:0] selects the PHY being polled for the TCA signal, and all devices not corresponding to this address must tri-state its TCA output. This multi-PHY operation is directly supported by the S/UNI-JET .

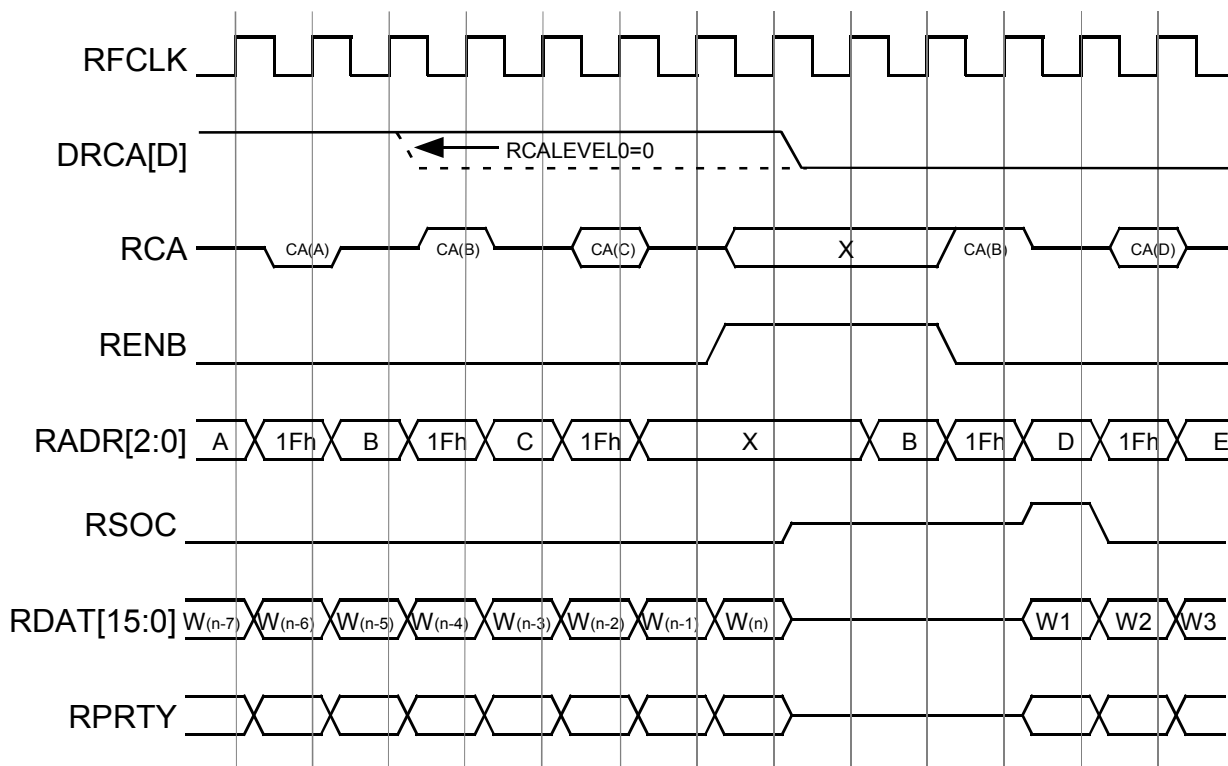**Figure 74 Multi-PHY Polling and Addressing Receive Cell Interface**

Figure 74 shows an example of the multi-PHY polling and selection sequence supported by the S/UNI-JET . "A", "B", "C", "D", and "E" represent any arbitrary address values which may be occupied by the S/UNI-JET . Initially cell data is being received from PHY "D," and the DRCA[D] signal shows how the DRCA[x] signals behave based on the value of the RCALEVEL0 register bit(s). The ATM Layer device is not restricted in its polling order. The PHY associated with address "A" indicates it does not have a cell available, but PHY "B" indicates that it does. As a result, the ATM Layer places address "B" on RADR[2:0] the cycle before RENB is asserted to select PHY "B" as the next cell source. In this example, PHY "C"s status is ignored. The ATM Layer device is not constrained to select the latest PHY polled. As soon as the cell transfer is started, the polling process may be restarted. The data on RDAT (W1, W2, ..) may be 8-bit or 16-bits wide, depending on the setting of the ATM8 input.

During multi-PHY operation, several PHY layer devices share the RDAT[15:0], RSOC, RPRTY, and RCA signals. As a result, these signals must be tri-stated in all PHY devices which have not been selected for reading or polling by the ATM Layer. Selection of which PHY layer device is being read is made by the value on RADR[2:0] the cycle before RENB is asserted and affects the RDAT[15:0], RSOC, and RPRTY signals. The value of RADR[2:0] selects the PHY being polled for the RCA signal, and all devices not corresponding to this address must tri-state its RCA output. These multi-PHY operations are directly supported by the S/UNI-JET.

15   Absolute Maximum Ratings

Table 46   Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Supply VDD with respect to GND	-0.3 V to 4.6 V
Voltage on BIAS with respect to GND	VDD - 0.3 V to 5.5 V
Voltage on Any Pin	-0.3 V to BIAS +0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. Characteristics

T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DD} < BIAS < 5.5 V

(Typical Conditions: T_A = 25°C, V_{DD} = 3.3 V, V_{BIAS} = 5 V)

Table 47   DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5 V Tolerant Bias	VDD	5.0	5.5	Volts	
I_{BIAS}	Current into 5 V Bias		6.0		µA	V_{BIAS} = 5.5 V
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0		BIAS	Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.23	0.4	Volts	Guaranteed output Low voltage at VDD=2.97 V and I_{OL}=maximum rated for pad. [4, 5, 6]
V_{OH}	Output or Bi-directional High Voltage	2.4	2.93		Volts	Guaranteed output High voltage at VDD=2.97 V and I_{OH}=maximum rated current for pad. [4, 5, 6]
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB, TRSTB, TICLK[4:1], RCLK[4:1], TFCLK, RFCLK, TCK, TDI, TMS, and REF8KI.
I_{ILPU}	Input Low Current	-100	-60	-10	µA	V_{IL} = GND. [1, 3]
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = VDD. [1, 3]
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. [2, 3]
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = VDD. [2, 3]
C_{IN}	Input Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		6		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		6		pF	t_A=25°C, f = 1 MHz
IDDOP1	Operating Current			165	mA	VDD = 3.63 V, Outputs Unloaded (DS3/PLCP mode)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
IDDOP2	Operating Current			20	mA	VDD = 3.63 V, Outputs Unloaded (T1/E1 PLCP mode)
IDDOP3	Operating Current			170	mA	VDD = 3.63 V, Outputs Unloaded (DS3 ATM mode)
I_{DDOP4}	Operating Current			150	mA	V_{DD} = 3.63 V, Outputs Unloaded (E3 ATM mode)
I_{DDOP5}	Operating Current			40	mA	V_{DD} = 3.63 V, Outputs Unloaded (J2 ATM mode)
I_{DDOP6}	Operating Current			150	mA	V_{DD} = 3.63 V, Outputs Unloaded (52 Mbit/s arbitrary framing format with ATM direct mapping)
I_{DDOP7}	Operating Current			230	mA	V_{DD} = 3.63 V, Outputs Unloaded (DS3 framer only)
I_{DDOP8}	Operating Current			120	mA	V_{DD} = 3.63 V, Outputs Unloaded (E3 framer only)
I_{DDOP9}	Operating Current			30	mA	V_{DD} = 3.63 V, Outputs Unloaded (J2 framer only)

Notes

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. The Utopia interface outputs, RDAT[15:0], RPRTY, RCA, DRCA, RSOC, TCA, and DTCA, have 12 mA drive capability.

5. The outputs TCLK, TPOS/TDATO, TNEG/TOHM, TPOHFP/TFPO/TMFPO/TGAPCLK, LCD/RDATO, RPOH/ROVRHD, RPOHCLK/RSCLK/RGAPCLK, and REF8KO/RPOHFP/RFPO/RMFPO have 6 mA drive capability.

6. The data bus outputs, D[7:0], and all outputs not specified above have 3 mA drive capability.

17 Microprocessor Interface Timing Characteristics

(T_A = -40°C to +85°C, V_{DD} = 3.3 V ±10%)

Table 48   Microprocessor Interface Read Access (Figure 75)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

**Figure 75   Microprocessor Interface Read Timing**
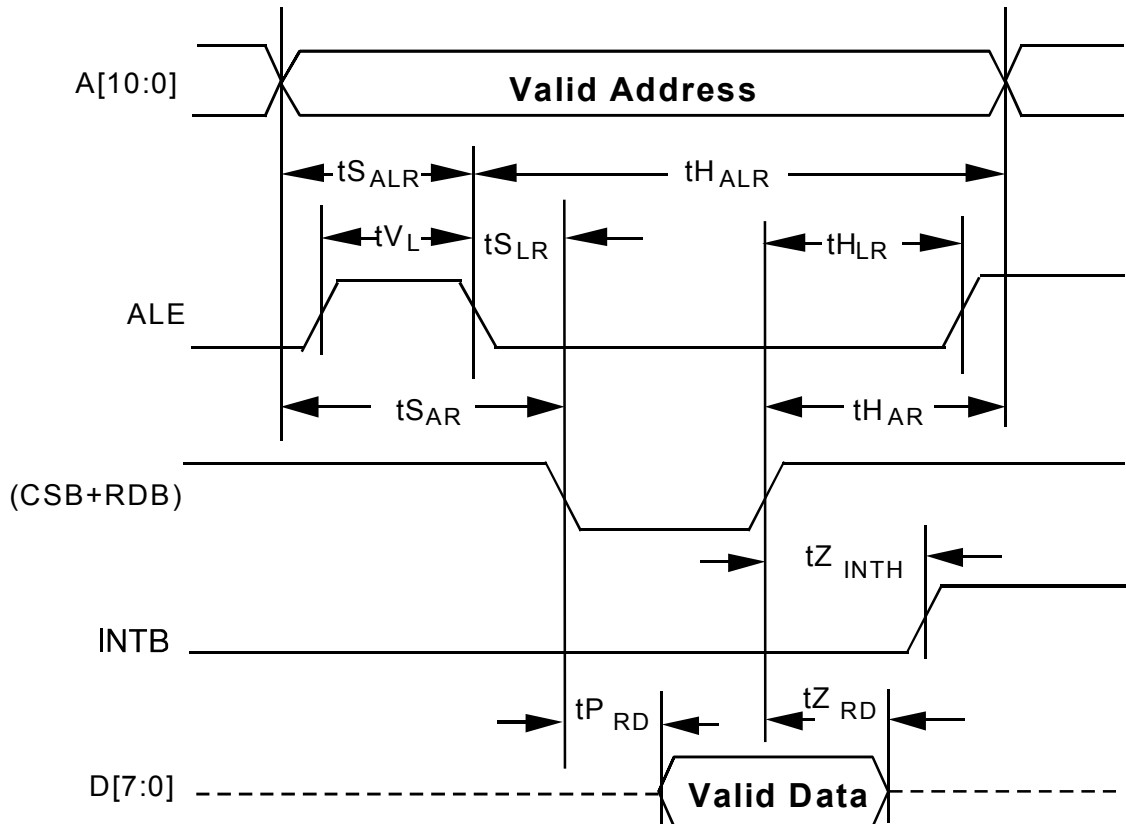
Notes

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 49   Microprocessor Interface Write Access (Figure 76)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 76 Microprocessor Interface Write Timing
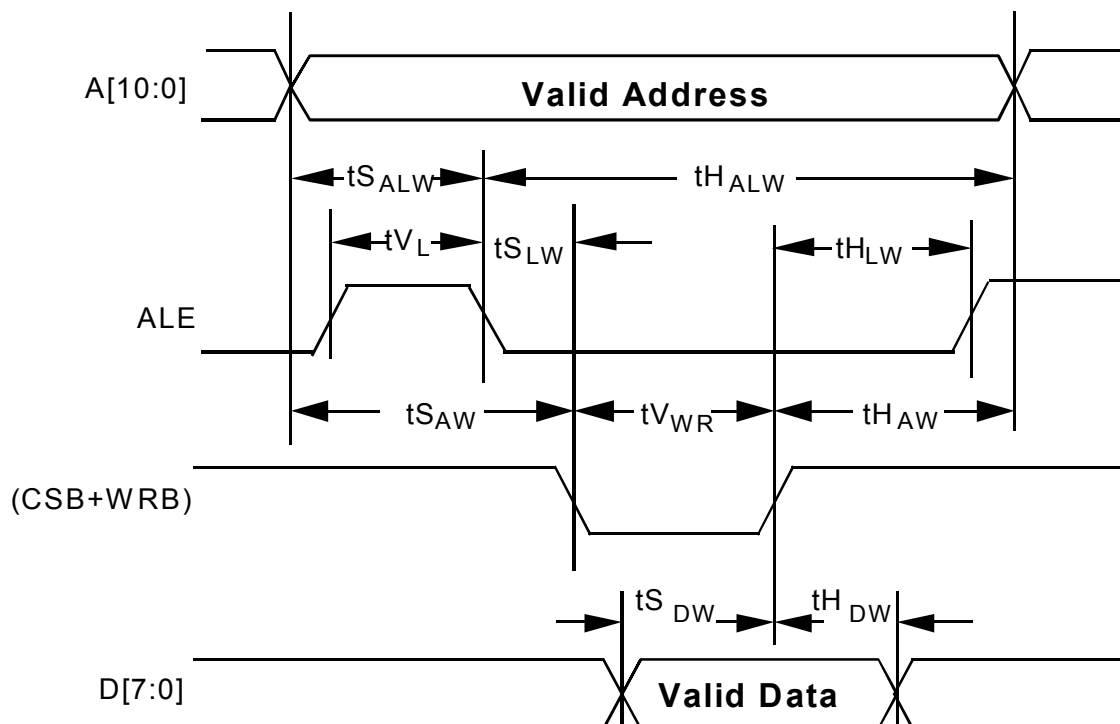
Notes

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

3. Parameter tH_{AW} is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18   A.C. Timing Characteristics

$(T_A = -40°C$ to $+85°C$, $V_{DD} = 3.3V \pm 10\%)$

Table 50   RSTB Timing (Figure 77)

Symbol	Description	Min	Typical	Max	Units
tV$_{RSTB}$	RSTB Pulse Width[4]		100		ns

Figure 77   RSTB Timing
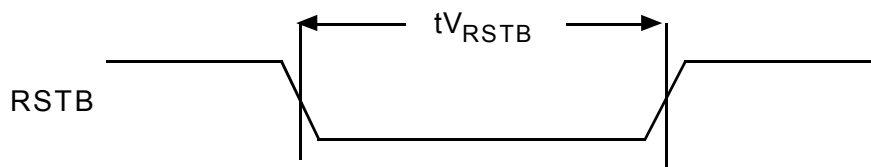
Table 51   Transmit ATM Cell Interface Timing (Figure 78)

Symbol	Description	Min	Max	Units
f$_{TFCLK}$	TFCLK Frequency		52	MHz
D$_{TFCLK}$	TFCLK Duty Cycle	40	60	%
tS$_{TFCLK}$	TENB, TADR[2:0], TDATI[15:0], TPRTY, and TSOC Set-up time to TFCLK	3		ns
tH$_{TFCLK}$	TENB, TADR[2:0], TDATI[15:0], TPRTY, and TSOC Hold time to TFCLK	1		ns
tP$_{TCA}$	TFCLK High to DTCA and TCA Valid	1	12	ns
tZ$_{TCA}$	TFCLK High to TCA Tri-state	1	10	ns
tZB$_{TCA}$	TFCLK High to TCA Driven	1		ns

Figure 78   Transmit ATM Cell Interface Timing
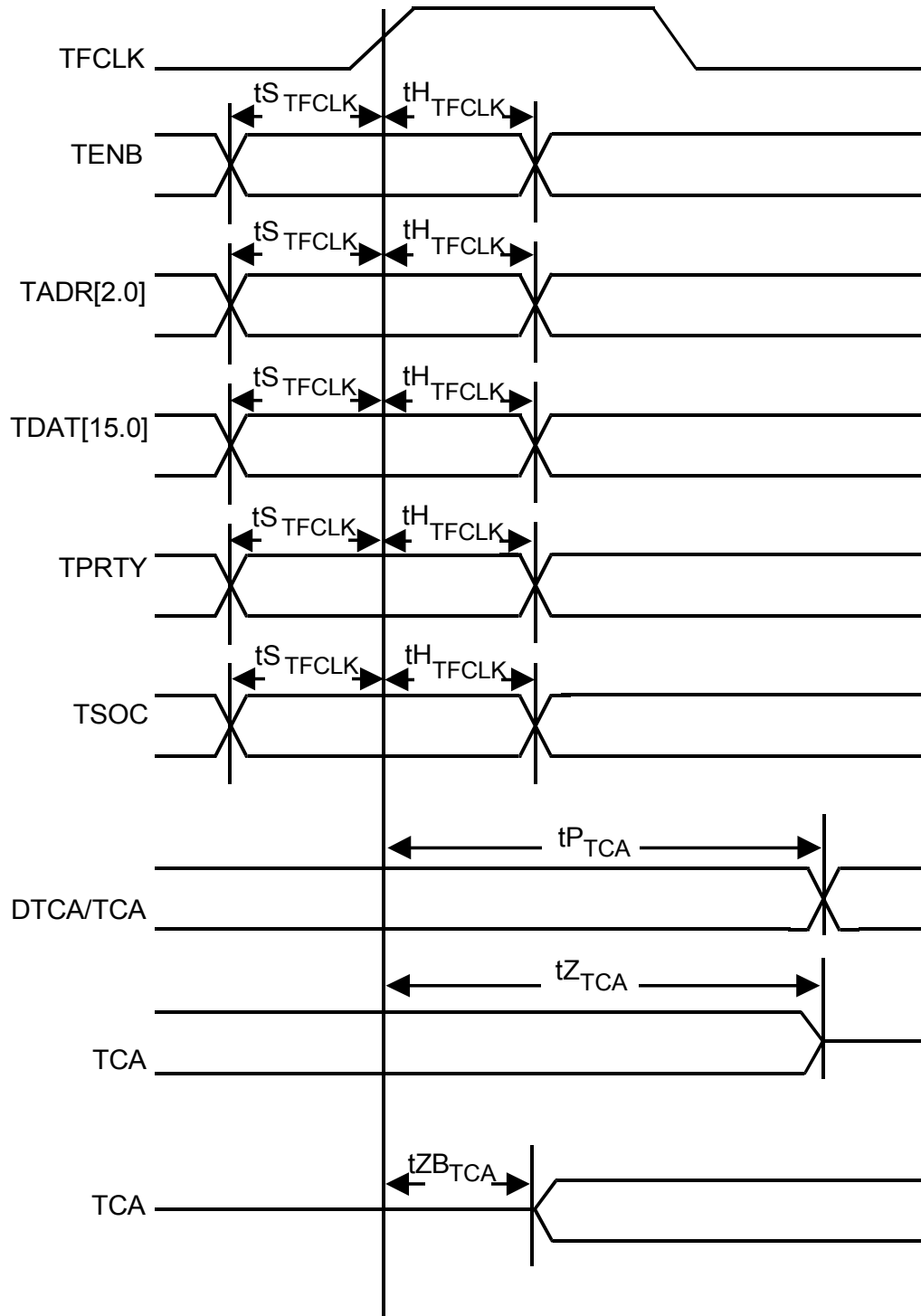
Table 52   Receive ATM Cell Interface Timing (Figure 79)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency		52	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
tS_{RFCLK}	RENB and RADR[2:0] Set-up time to RFCLK	3		ns
tH_{RFCLK}	RENB and RADR[2:0] Hold time to RFCLK	1		ns
tP_{RFCLK}	RFCLK High to Output Valid	1	12	ns
tZ_{RFCLK}	RFCLK High to Output Tri-state	1	12	ns
tZB_{RFCLK}	RFCLK High to Output Driven	1		ns

Figure 79 Receive ATM Cell Interface Timing
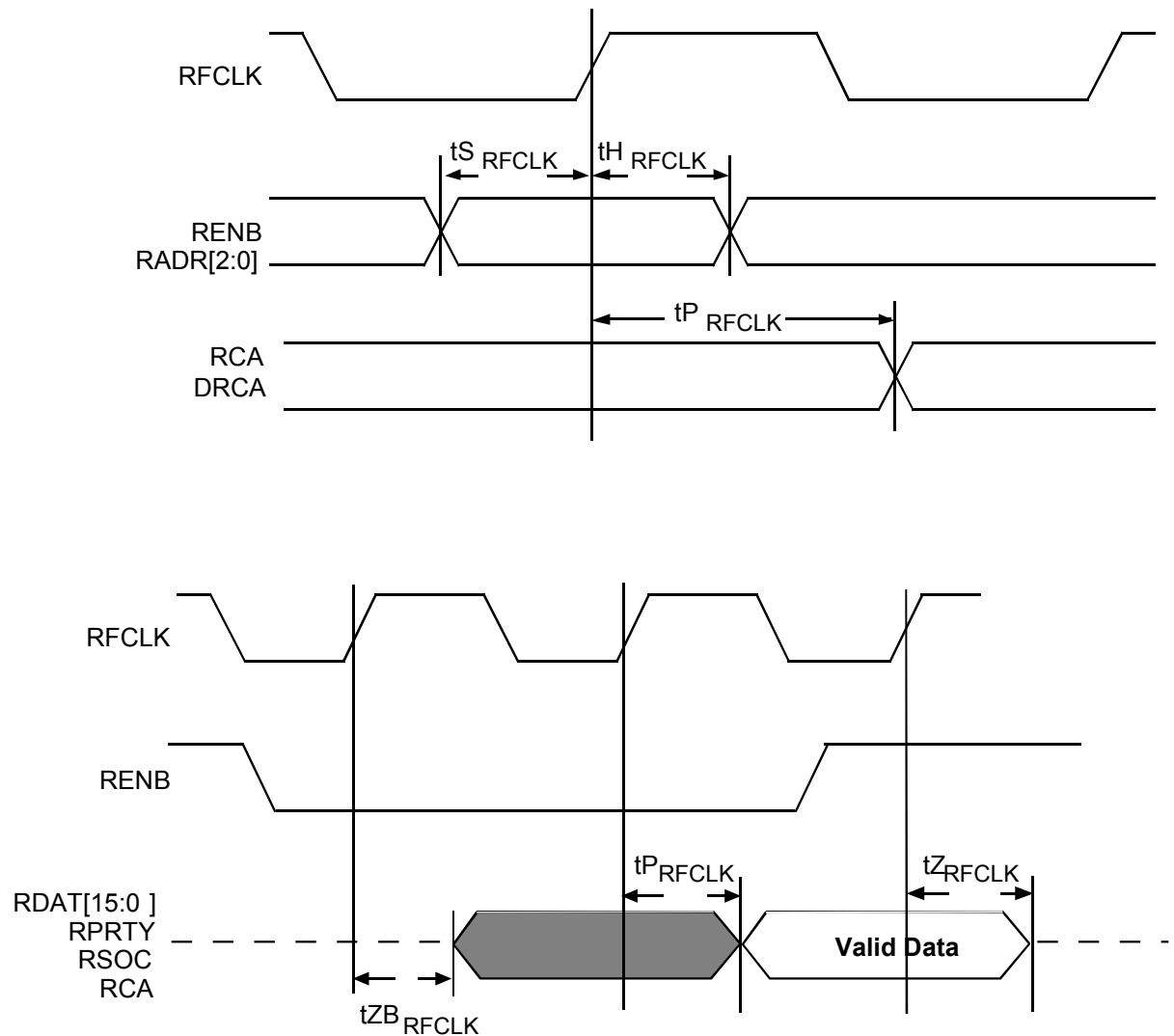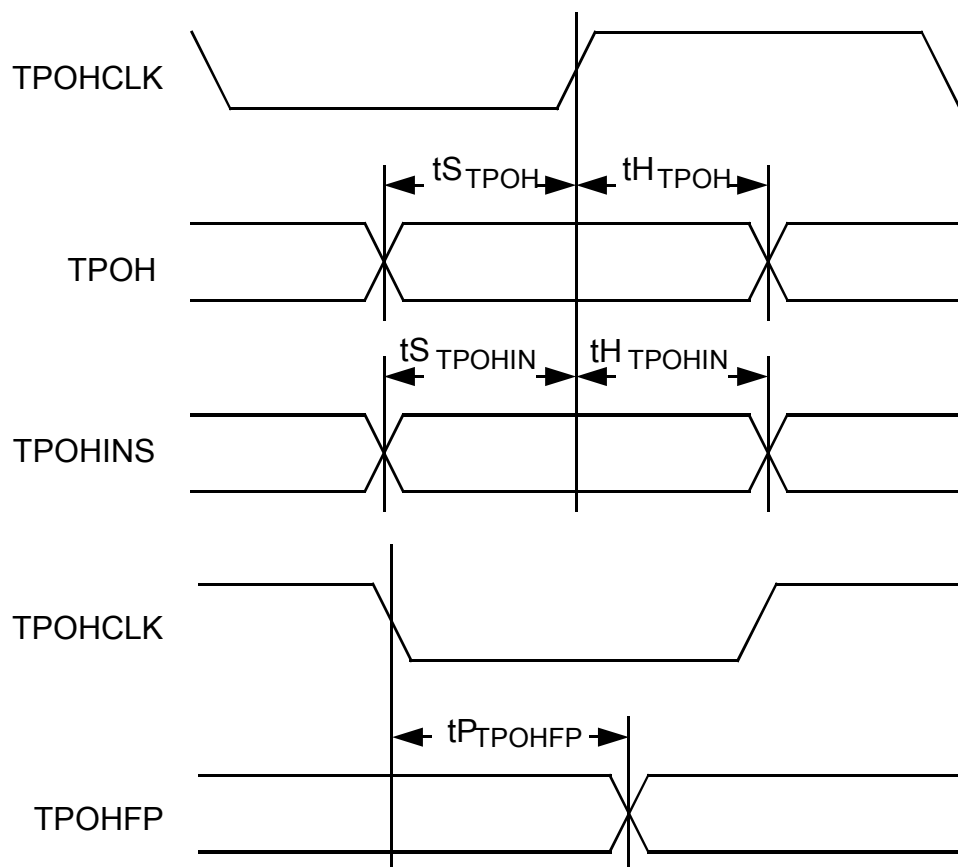
Table 53   Transmit Interface Timing (Figure 80)

Symbol	Description	Min	Typ	Max	Units
f_{TICLK}	TICLK Frequency: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)			52 35 7 52	MHz
$t0_{TICLK}$	TICLK minimum pulse width low: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
$t1_{TICLK}$	TICLK minimum pulse width high: DS3 Framer (TFRM[1:0] = 00) E3 Framer (TFRM[1:0] = 01) J2 Framer (TFRM[1:0] = 10) framer bypass (TFRM[1:0] = 11)	 7.7 11 57 7.7			ns
tS_{TIOHM}	TIOHM/TFPI/TMFPI to TICLK Set-up Time	5			ns
tH_{TIOHM}	TIOHM/TFPI/TMFPI to TICLK Hold Time	1			ns
tS_{TDATI}	TDATI to TICLK Set-up Time	5			ns
tH_{TDATI}	TDATI to TICLK Hold Time	1			ns
tS_{LTIOHM}	TIOHM/TFPI/TMFPI to RCLK Set-up Time (LOOPT=1)	5			ns
tH_{LTIOHM}	TIOHM/TFPI/TMFPI to RCLK Hold Time (LOOPT=1)	1			ns
tS_{LTDATI}	TDATI to RCLK Set-up Time (LOOPT=1)	5			ns
tH_{LTDATI}	TDATI to RCLK Hold Time (LOOPT=1)	1			ns
tP_{TFPO}	TICLK to TFPO/TMFPO[x] Prop Delay, or RCLK to TFPO/TMFPO Prop Delay when loop timing is used.	2		16	ns
tS_{TGAP}	TDATI to TGAPCLK Set-up Time	3			ns
tH_{TGAP}	TDATI to TGAPCLK Hold Time	2			ns
tW_{REF8KI}	REF8KI pulse width[4]		15		ns
tS_{TOH}	TOH to TOHCLK Set-Up Time	20			ns
tH_{TOH}	TOH to TOHCLK Hold Time	20			ns
tS_{TOHINS}	TOHINS to TOHCLK Set-Up Time	20			ns
tH_{TOHINS}	TOHINS to TOHCLK Hold Time	20			ns
tP_{TOHFP}	TOHCLK to TOHFP Prop Delay	-15		20	ns

Symbol	Description	Min	Typ	Max	Units
tS$_{TPOH}$	TPOH to TPOHCLK Set-Up Time	20			ns
tH$_{TPOH}$	TPOH to TPOHCLK Hold Time	20			ns
tS$_{TPOHIN}$	TPOHINS to TPOHCLK Set-Up Time	20			ns
tH$_{TPOHIN}$	TPOHINS to TPOHCLK Hold Time	20			ns
tP$_{TPOHFP}$	TPOHCLK to TPOHFP Prop Delay	-15		20	ns
tP$_{TPOS}$	TCLK Edge to TPOS/TDATO Prop Delay	-1		4.5	ns
tP$_{TNEG}$	TCLK Edge to TNEG/TOHM Prop Delay	-1		4.5	ns
tP$_{TPOS2}$	TICLK High to TPOS/TDATO Prop Delay	2		13	ns
TP$_{TNEG2}$	TICLK High to TNEG/TOHM Prop Delay	2		13	ns

Figure 80   Transmit Interface Timing

TPOHCLK

tS_{TPOH} tH_{TPOH}

TPOH

tS_{TPOHIN} tH_{TPOHIN}

TPOHINS

TPOHCLK

tP_{TPOHFP}

TPOHFP

TICLK=0, TCLKINV=0

TICLK=0, TCLKINV=1

TICL K

TCL K

tP_{TPOS}

TPOS /TD ATO

tP_{TNEG}

TNE G/T OHM

TICL K

TCL K

tP_{TPOS}

TPOS /TD ATO

tP_{TNEG}

TNE G/T OHM

TICLK=1, TCLKINV=X

TICL K

TCL K

tP_{TPOS2}

TPOS /TD ATO

tP_{TNEG2}

TNE G/T OHM
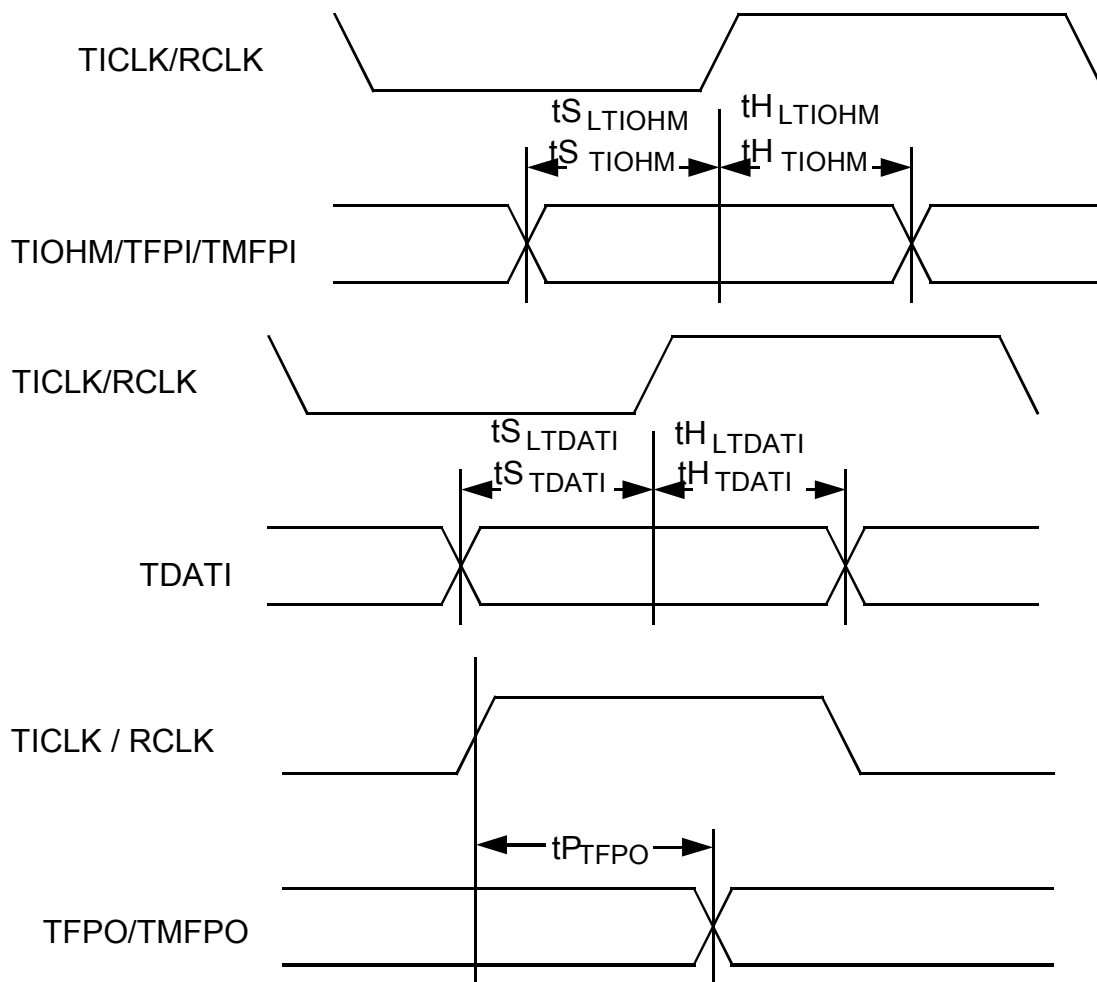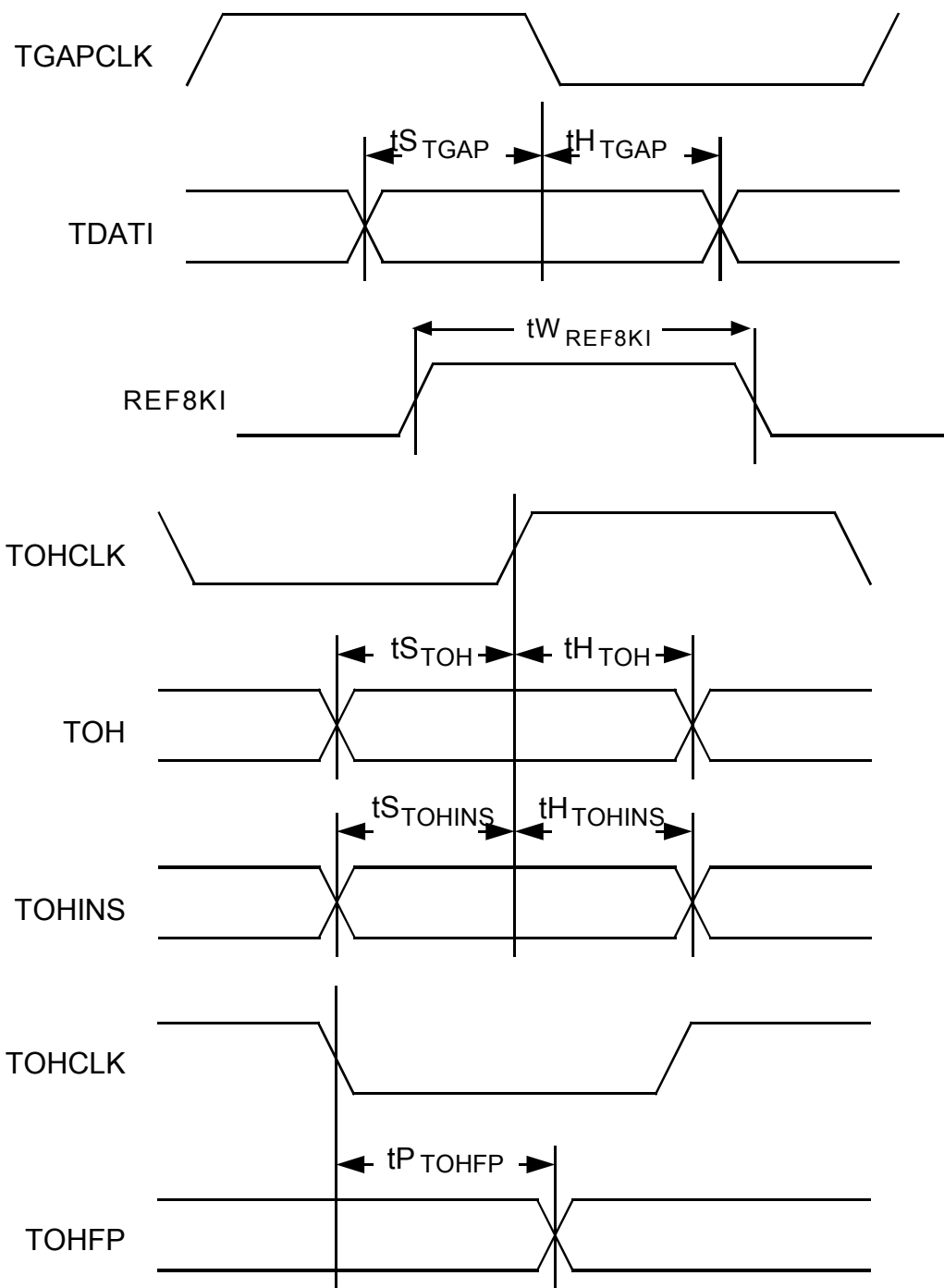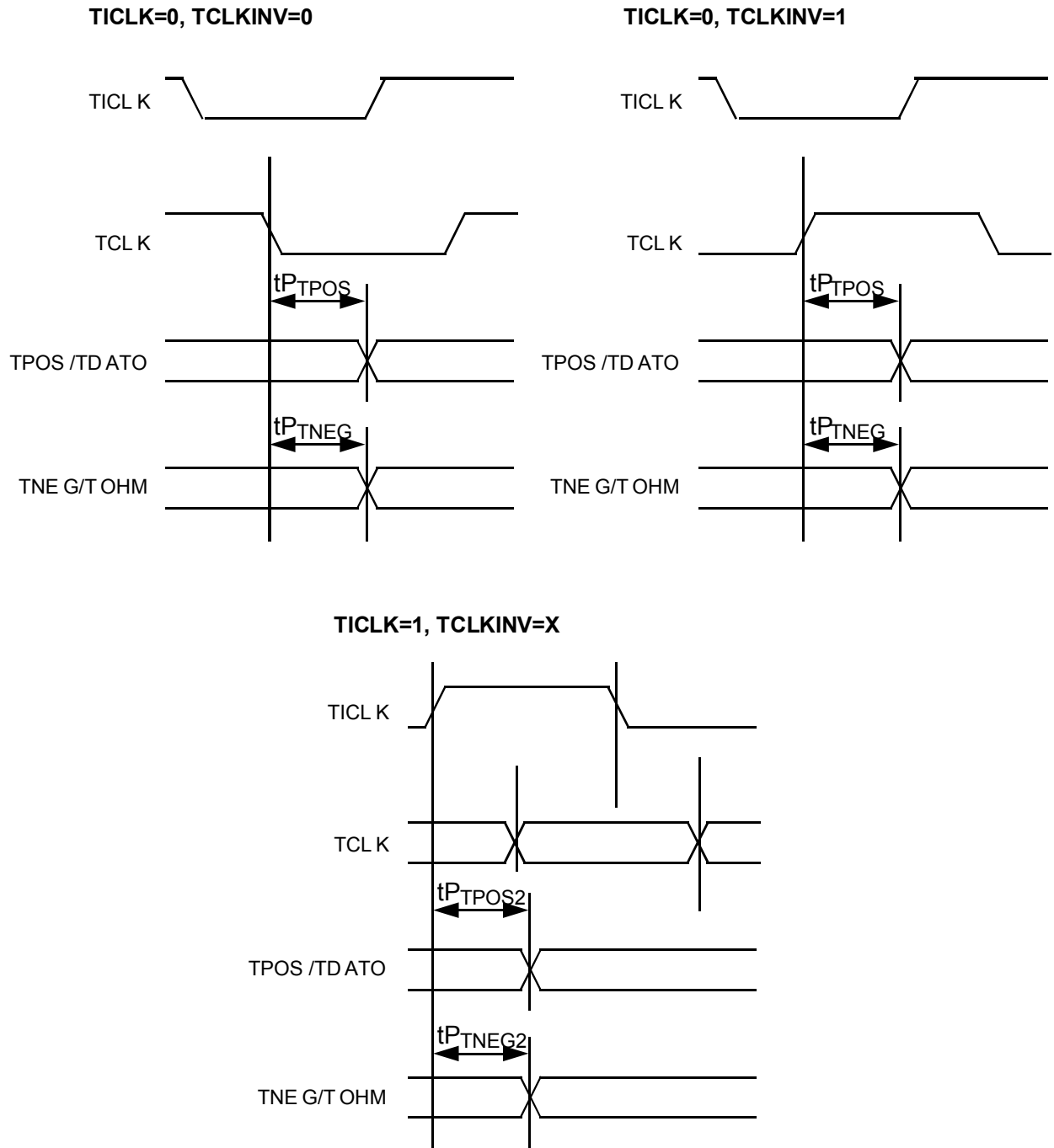
Table 54   Receive Interface Timing (Figure 81)

Symbol	Description	Min	Max	Units
F_{RCLK}	RCLK Frequency: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)		52 35 7 52	MHz MHz
$t0_{RCLK}$	RCLK minimum pulse width low: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)	 7.7 11 57 7.7		ns
$t1_{RCLK}$	RCLK minimum pulse width high: DS3 Framer (RFRM[1:0] = 00) E3 Framer (RFRM[1:0] = 01) J2 Framer (RFRM[1:0] = 10) framer bypass (RFRM[1:0] = 11)	 7.7 11 57 7.7		ns
tS_{RPOS}	RPOS/RDATI Set-up Time	4		ns
tH_{RPOS}	RPOS/RDATI Hold Time	1		ns
tS_{RNEG}	RNEG/ROHM Set-Up Time	4		ns
tH_{RNEG}	RNEG/ROHM Hold Time	1		ns
tP_{RRDATO}	RSCLK/RGAPCLK rising edge to RDATO Prop Delay	2	13	ns
tP_{RRFPO}	RSCLK rising edge to RFPO/RMFPO Prop Delay	1	13	ns
$tP_{RROVRHD}$	RSCLK rising edge to ROVRHD Prop Delay	1	13	ns
tP_{FRDATO}	RSCLK/RGAPCLK falling edge to RDATO Prop Delay	-2	10	ns
tP_{FRFPO}	RSCLK falling edge to RFPO/RMFPO Prop Delay	-2	10	ns
$tP_{FROVRHD}$	RSCLK falling edge to ROVRHD Prop Delay	-2	10	ns
tP_{ROH}	ROHCLK Low to ROH Prop Delay	-15	20	ns
tP_{ROHFP}	ROHCLK Low to ROHFP Prop Delay	-15	20	ns
tP_{RPOH}	RPOHCLK Low to RPOH Prop Delay	-15	20	ns
tP_{RPOHFP}	RPOHCLK Low to RPOHFP Prop Delay	-15	20	ns

Figure 81 Receive Interface Timing
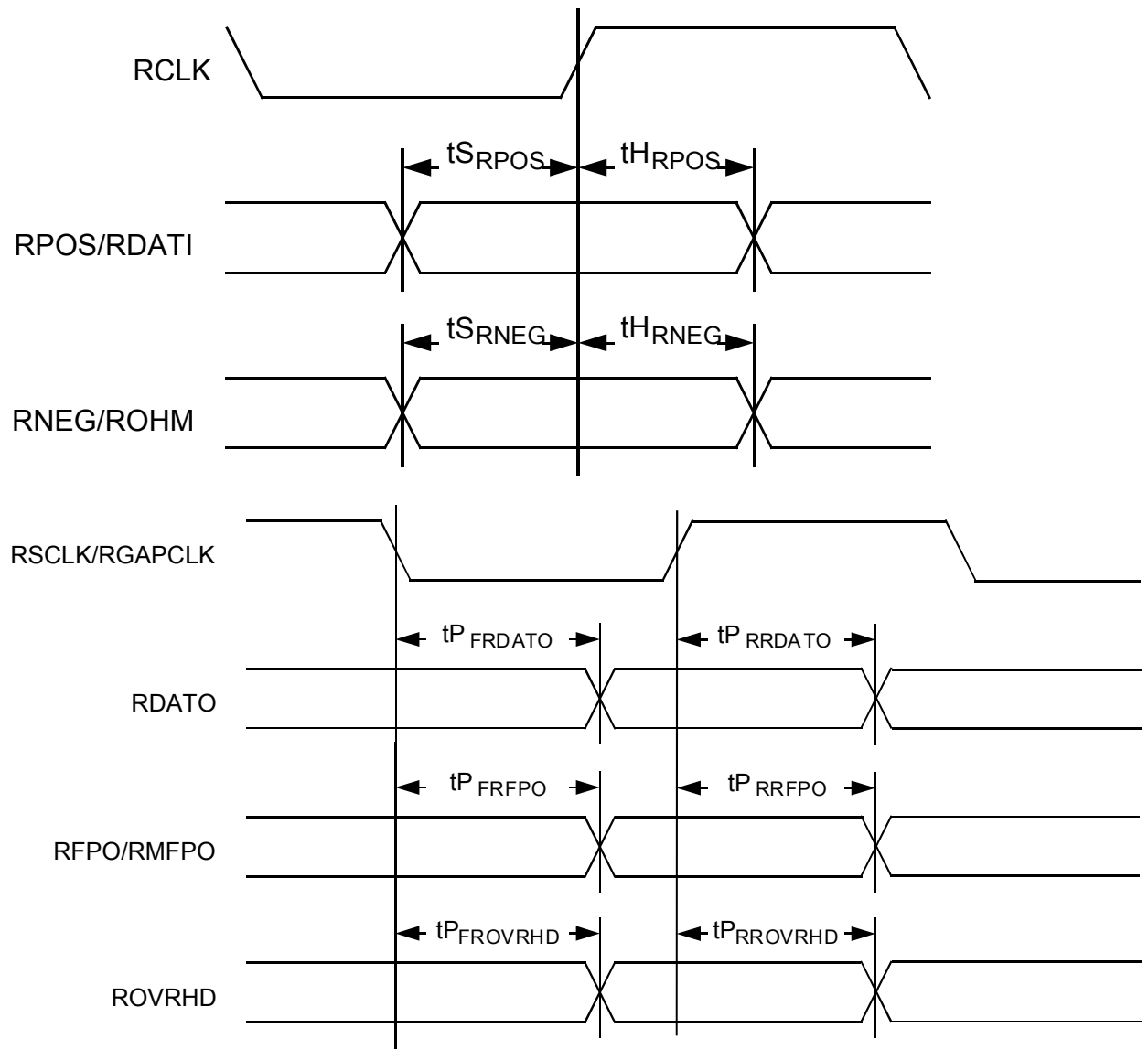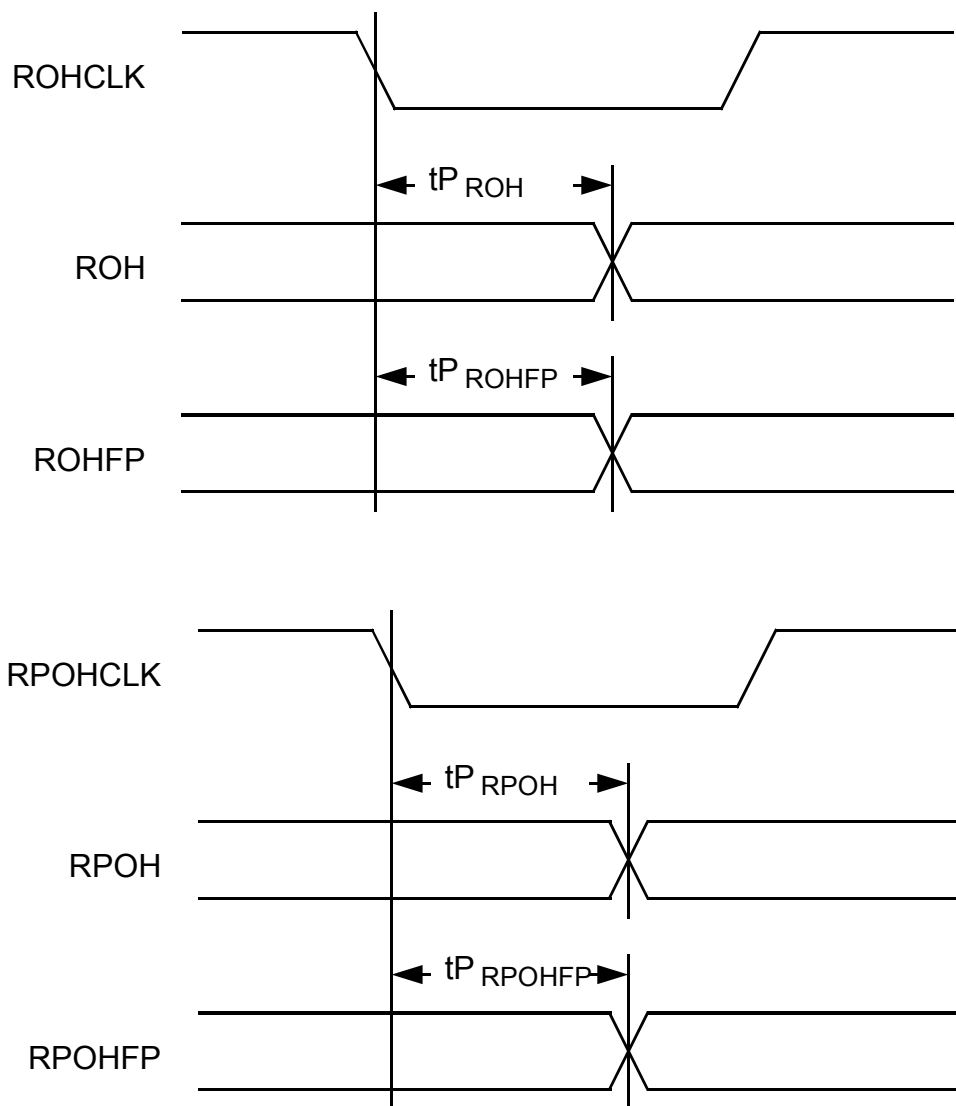
Table 55   JTAG Port Interface (Refer to Figure 82)

Symbol	Description	Min	Typical	Max	Units
$t1_{TCK}$	TCK high pulse width[5]				ns
$t0_{TCK}$	TCK low pulse width[5]	100			ns
tS_{TMS}, tS_{TDI}	TMS and TDI Set-up time to TCK[1]	50			ns
TH_{TMS}, TH_{TDI}	TMS and TDI Hold time to TCK[2]	50			ns
TP_{TDO}	TCK Low to TDO Valid[6,7]	2		50	ns
TV_{TRSTB}	TRSTB minimum pulse width[4,5]		100		ns

Figure 82   JTAG Port Interface Timing
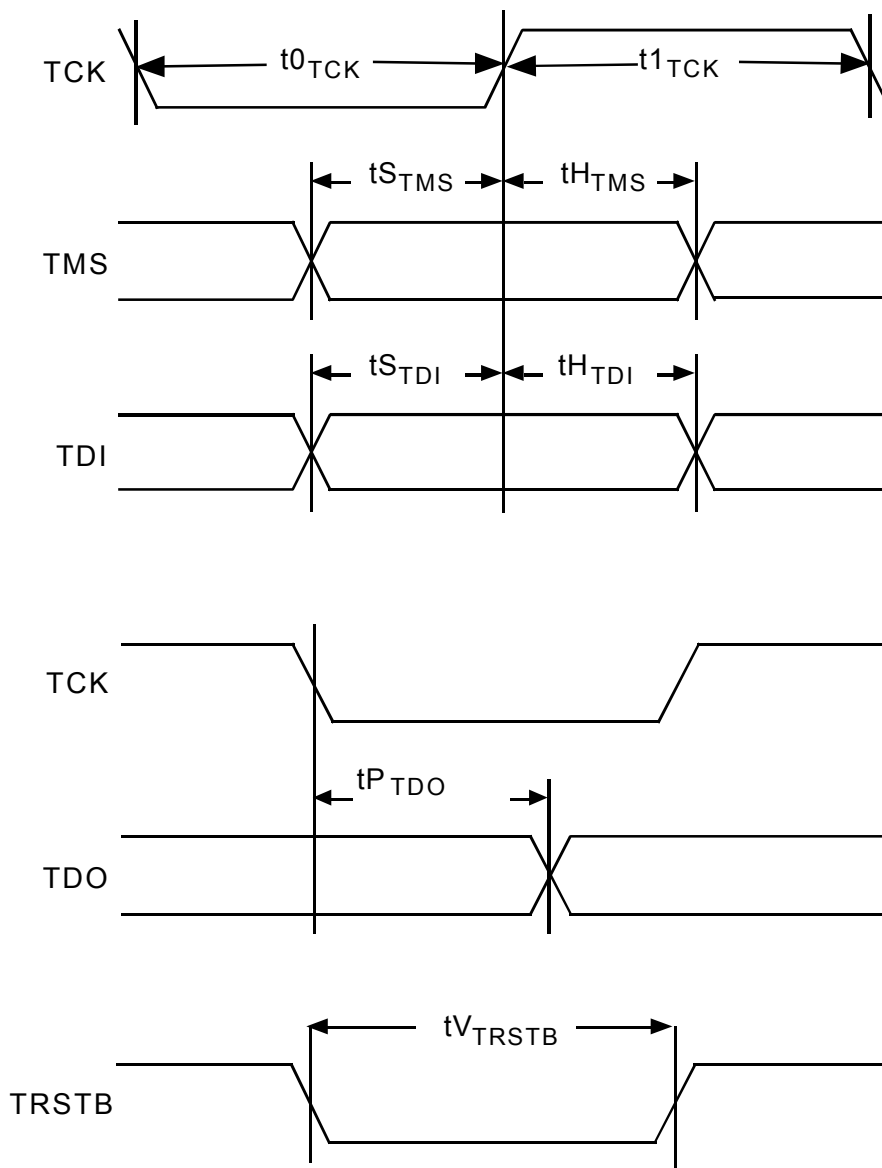
Notes (on Input Timing)

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. It is recommended that the load on TGAPCLK[x] be kept less than 50pF. A larger load on these pins may result in functional failures.

4. This parameter is guaranteed by design. No production tests are done on this parameter.

5. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

Notes (on Output Timing)

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 50 pF load on the outputs.
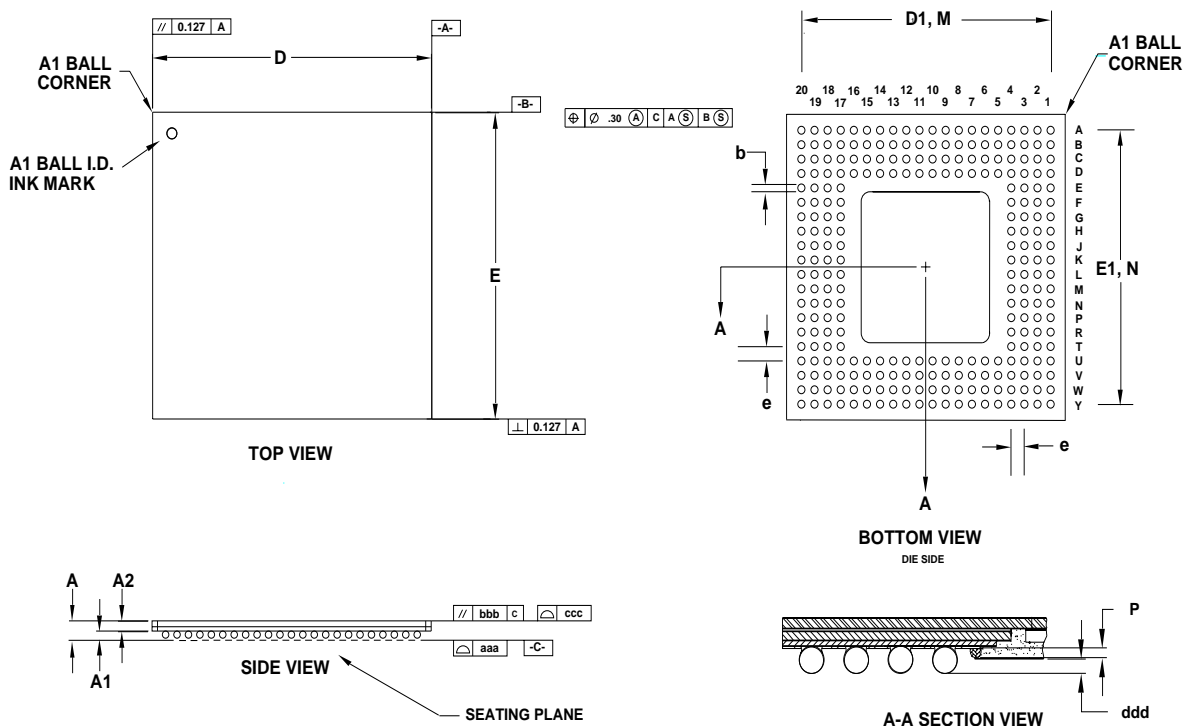
19 Ordering and Thermal Information

Table 56 Packaging Information

Part No.	Description
PM7347-BI	256-pin Ball Grid Array (SBGA)

Table 57 Thermal Information

Part No.	Ambient Temperature	Theta Ja	Theta Jc
PM7347-BI	-40°C to 85°C	19 °C/W	5 °C/W

20 Mechanical Information

Notes: 1) ALL DIMENSIONS IN MILLIMETER.

2) DIMENSION aaa DENOTES COPLANARITY

3) DIMENSION bbb DENOTES PARALLEL

4) DIMENSION ccc DENOTES FLATNESS

PACKAGE TYPE: 256 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 27 x 27 x 1.45 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
Min.	1.32	0.56	0.76	26.90	24.03	26.90	24.03			0.60				0.15	0.20
Nom.	1.45	0.63	0.82	27.00	24.13	27.00	24.13	20x20	1.27	0.75				0.33	0.30
Max.	1.58	0.70	0.88	27.10	24.23	27.10	24.23			0.90	0.15	0.15	0.20	0.50	0.35

Notes