

### FEATURES

- Outstanding Gain Linearity
- Ultra High Gain ..... 5000V/mV Min
- Low  $V_{OS}$  Over Temperature ..... 60 $\mu$ V Max
- Excellent  $TCV_{OS}$  ..... 0.3 $\mu$ V/ $^{\circ}$ C Max
- High PSRR ..... 3 $\mu$ V/V Max
- Low Power Consumption ..... 60mW Max
- Fits OP-07, 725, 108A/308A, 741 Sockets
- Available in Die Form

### ORDERING INFORMATION †

TO-99	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	
OP77AJ*	OP77AZ*	-	-	MIL
OP77EJ	OP77EZ	-	-	IND
-	-	OP77EP	-	COM
OP77BJ*	OP77BZ*	-	OP77BRC/883	MIL
OP77FJ	OP77FZ	-	-	IND
-	-	OP77FP	-	COM
-	-	OP77GP	-	COM
-	-	OP77GS††	-	COM
-	-	OP77HP	-	XIND
-	-	OP77HS††	-	XIND

\* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

### GENERAL DESCRIPTION

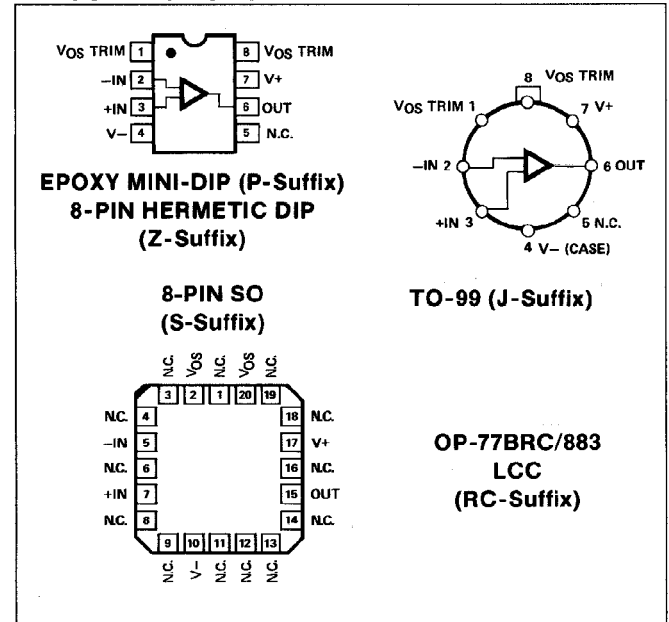
The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full  $\pm 10$ V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides

superior performance in high closed-loop-gain applications. Low initial  $V_{OS}$  drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional  $TCV_{OS}$  of 0.3 $\mu$ V/ $^{\circ}$ C maximum and the low  $V_{OS}$  of 25 $\mu$ V maximum, eliminates the need for  $V_{OS}$  adjustment and increases system accuracy over temperature.

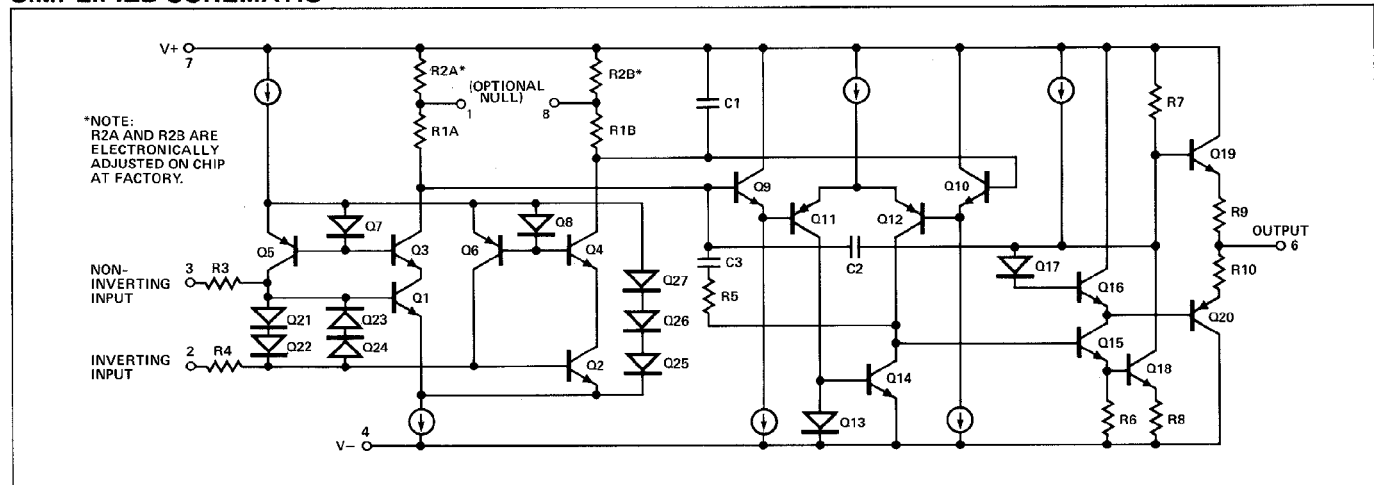
PSRR of 3 $\mu$ V/V (110dB) and CMRR of 1.0 $\mu$ V/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems.

*Continued*

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC



# OP77

This product is available in six standard grades and five standard packages: the TO-99 can, the 8-pin mini-DIP in ceramic, SO or epoxy, and the 20-contact LCC.

The OP-77 is a direct or upgrade replacement for the OP-07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the  $V_{OS}$  adjust pot. For higher precision performance refer to OP-177.

## ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage .....	$\pm 22V$
Differential Input Voltage .....	$\pm 30V$
Input Voltage (Note 1) .....	$\pm 22V$
Output Short-Circuit Duration .....	Indefinite
Storage Temperature Range	
J, Z, and RC Packages .....	$-65^{\circ}C$ to $+150^{\circ}C$
P Package .....	$-65^{\circ}C$ to $+125^{\circ}C$
Operating Temperature Range	
OP-77A, OP-77B (J, Z, RC) .....	$-55^{\circ}C$ to $+125^{\circ}C$
OP-77E, OP-77F (J, Z) .....	$-25^{\circ}C$ to $+85^{\circ}C$

OP-77E, OP-77F, OP-77G (P, S) .....	$0^{\circ}C$ to $70^{\circ}C$
OP-77H (P, S) .....	$-40^{\circ}C$ to $+85^{\circ}C$
Junction Temperature ( $T_J$ ) .....	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 60 sec.) .....	$+300^{\circ}C$

PACKAGE TYPE	$\theta_{JA}$ (Note 3)	$\theta_{JC}$	UNITS
TO-99 (J)	150	18	$^{\circ}C/W$
8-Pin Hermetic DIP (Z)	148	16	$^{\circ}C/W$
8-Pin Plastic DIP (P)	103	43	$^{\circ}C/W$
20-Contact LCC (RC, TC)	98	38	$^{\circ}C/W$
8-Pin SO (S)	158	43	$^{\circ}C/W$

### NOTES:

- For supply voltages less than  $\pm 22V$ , the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = +25^{\circ}C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		-	10	25	-	20	60	$\mu V$
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Note 1)	-	0.2	-	-	0.2	-	$\mu V/Mo$
Input Offset Current	$I_{OS}$		-	0.3	1.5	-	0.3	2.8	nA
Input Bias Current	$I_B$		-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz (Note 2)	-	0.35	0.6	-	0.35	0.6	$\mu Vp-p$
Input Noise Voltage Density	$e_n$	$f_o = 10Hz$ (Note 2)	-	10.3	18.0	-	10.3	18.0	$V/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 2)	-	10.0	13.0	-	10.0	13.0	
		$f_o = 1000Hz$ (Note 2)	-	9.6	11.0	-	9.6	11.0	
Input Noise Current	$i_{np-p}$	0.1Hz to 10Hz (Note 2)	-	14	30	-	14	30	$pAp-p$
Input Noise Current Density	$i_n$	$f_o = 10Hz$ (Note 2)	-	0.32	0.80	-	0.32	0.80	$pA/\sqrt{Hz}$
		$f_o = 100Hz$ (Note 2)	-	0.14	0.23	-	0.14	0.23	
		$f_o = 1000Hz$ (Note 2)	-	0.12	0.17	-	0.12	0.17	
Input Resistance – Differential-Mode	$R_{IN}$	(Note 3)	26	45	-	18.5	45	-	M $\Omega$
Input Resistance – Common-Mode	$R_{INCM}$		-	200	-	-	200	-	G $\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$	-	$\pm 13$	$\pm 14$	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	-	0.1	1.0	-	0.1	1.0	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	-	0.7	3	-	0.7	3	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	5000	12000	-	2000	8000	-	V/mV
		$R_L \geq 10k\Omega$	$\pm 13.5$	$\pm 14.0$	-	$\pm 13.5$	$\pm 14.0$	-	V
		$R_L \geq 2k\Omega$	$\pm 12.5$	$\pm 13.0$	-	$\pm 12.5$	$\pm 13.0$	-	
		$R_L \geq 1k\Omega$	$\pm 12.0$	$\pm 12.5$	-	$\pm 12.0$	$\pm 12.5$	-	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	-	0.1	0.3	-	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	-	0.4	0.6	-	MHz
Open-Loop Output Resistance	$R_O$		-	60	-	-	60	-	$\Omega$
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	-	50	60	-	50	60	mW
		$V_S = \pm 3V$ , No Load	-	3.5	4.5	-	3.5	4.5	
Offset Adjustment Range		$R_p = 20k\Omega$	-	$\pm 3$	-	-	$\pm 3$	-	mV

### NOTES:

- Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$ .

- Sample tested.
- Guaranteed by design.

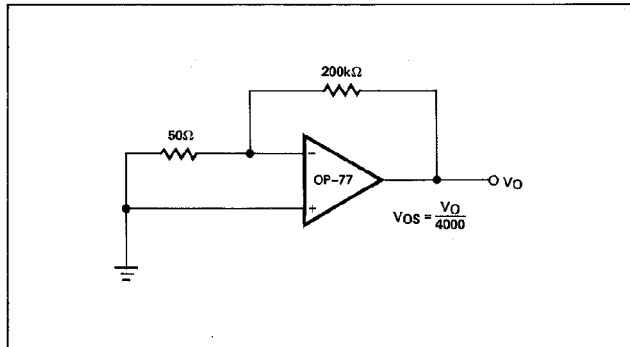
## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	25	60	—	45	120	$\mu V$
Average Input Offset Voltage Drift	$TCV_{OS}$	(Note 1)	—	0.1	0.3	—	0.2	0.6	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$		—	0.5	2.2	—	0.5	4.5	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	1.5	25	—	1.5	50	$\mu A/^\circ C$
Input Bias Current	$I_B$		-0.2	2.4	4	-0.2	2.4	6	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	8	25	—	15	35	$\mu A/^\circ C$
Input Voltage Range	IVR		$\pm 13$	$\pm 13.5$	—	$\pm 13$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1	3	—	1	5	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13.0$	—	$\pm 12$	$\pm 13.0$	—	V
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	—	60	75	—	60	75	mW

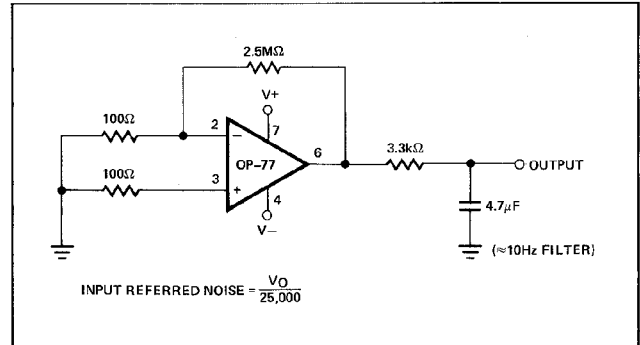
### NOTES:

- OP-77A:  $TCV_{OS}$  is 100% tested.
- Guaranteed by end-point limits.

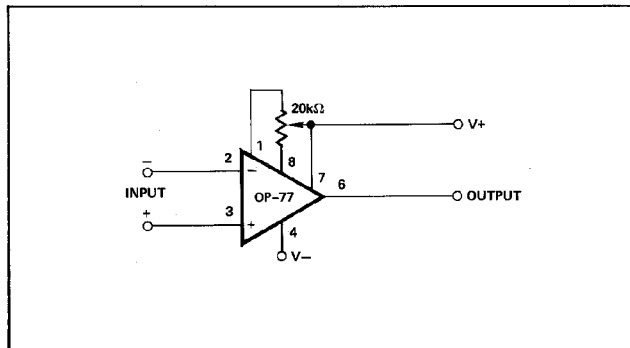
### TYPICAL OFFSET VOLTAGE TEST CIRCUIT



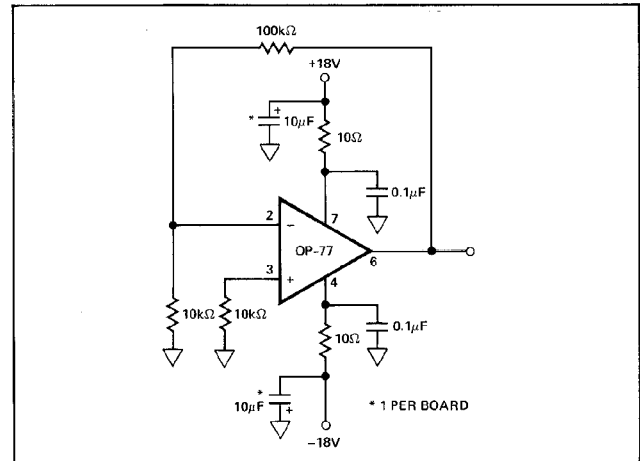
### TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



### OPTIONAL OFFSET NULLING CIRCUIT



### BURN-IN CIRCUIT



# OP77

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F			OP-77G/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	10	25	—	20	60	—	50	100	$\mu V$
Long-Term $V_{OS}$ Stability	$V_{OS}/\text{Time}$	(Note 1)	—	0.3	—	—	0.4	—	—	0.4	—	$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$		—	0.3	1.5	—	0.3	2.8	—	0.3	2.8	nA
Input Bias Current	$I_B$		-0.2	1.2	2.0	-0.2	1.2	2.8	-0.2	1.2	2.8	nA
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	$i_{np-p}$	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	$pA_{p-p}$
Input Noise Current Density	$i_n$	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	26	45	—	18.5	45	—	18.5	45	—	M $\Omega$
Input Resistance — Common-Mode	$R_{INCM}$		—	200	—	—	200	—	—	200	—	G $\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	—	0.1	1.6	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3.0	—	0.7	3.0	—	0.7	3.0	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	5000	12000	—	2000	6000	—	2000	6000	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	$\pm 13.5$	$\pm 14.0$	—	$\pm 13.5$	$\pm 14.0$	—	$\pm 13.5$	$\pm 14.0$	—	V
		$R_L \geq 2k\Omega$	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.5$	$\pm 13.0$	—	
		$R_L \geq 1k\Omega$	$\pm 12.0$	$\pm 12.5$	—	$\pm 12.0$	$\pm 12.5$	—	$\pm 12.0$	$\pm 12.5$	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	$R_O$		—	60	—	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	—	50	60	—	50	60	—	50	60	mW
		$V_S = \pm 3V$ , No Load	—	3.5	4.5	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_P = 20k\Omega$	—	$\pm 3$	—	—	$\pm 3$	—	—	$\pm 3$	—	mV

## NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$ .
2. Sample tested.
3. Guaranteed by design.

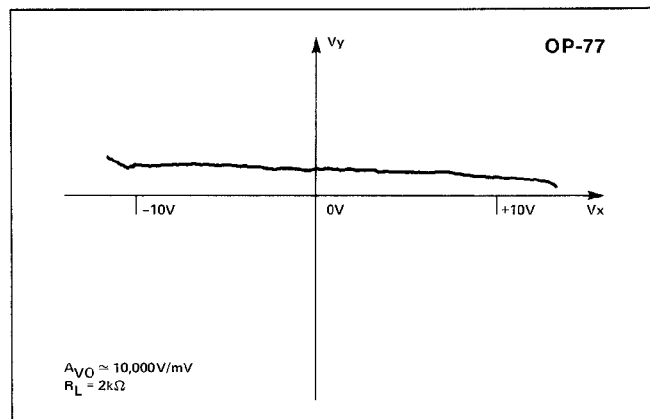
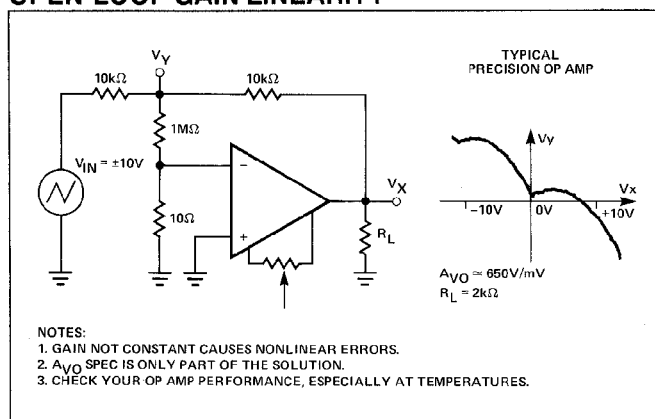
**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-25^\circ C \leq T_A \leq +85^\circ C$  for OP-77E/FJ and OP-77E/FZ,  $0^\circ C \leq T_A \leq +70^\circ C$  for OP-77E/F/GP/GS,  $-40^\circ C \leq T_A \leq +85^\circ C$  for OP-77HP/HS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F			OP-77G/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	J, Z Packages P Package	-	10	45	-	20	100	-	-	-	$\mu V$
Average Input Offset Voltage Drift	$TCV_{OS}$	J, Z Packages P Package (Note 1)	-	0.1	0.3	-	0.2	0.6	-	-	-	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$		-	0.5	2.2	-	0.5	4.5	-	0.5	4.5	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	-	1.5	40	-	1.5	85	-	1.5	85	$\mu A/^\circ C$
Input Bias Current	$I_B$	E, F, G Grades H Grade	-0.2	2.4	4.0	-0.2	2.4	6.0	-0.2	2.4	6.0	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	-	8	40	-	15	60	-	15	60	$\mu A/^\circ C$
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	-	$\pm 13.0$	$\pm 13.5$	-	$\pm 13.0$	$\pm 13.5$	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	-	0.1	1.0	-	0.1	3.0	-	0.1	3.0	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	-	1.0	3.0	-	1.0	5.0	-	1.0	5.0	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	2000	6000	-	1000	4000	-	1000	4000	-	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13.0$	-	$\pm 12$	$\pm 13.0$	-	$\pm 12$	$\pm 13.0$	-	V
Power Consumption	$P_d$	$V_S = \pm 15V$ , No Load	-	60	75	-	60	75	-	60	75	mW

**NOTES:**

1. OP-77E:  $TCV_{OS}$  is 100% tested on J and Z packages.
2. Guaranteed by end-point limits.

**OPEN-LOOP GAIN LINEARITY**

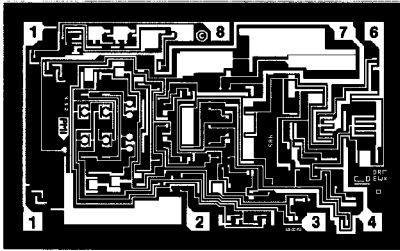


Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use end-point testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Since this is so difficult for manufacturers to test, you should make your own evaluation. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

This is the output gain linearity trace for the new OP-77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive – approximately 10,000,000.

# OP77

## DICE CHARACTERISTICS



1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V<sub>-</sub>
6. OUTPUT
7. V<sub>+</sub>
8. BALANCE

DIE SIZE 0.093 × 0.057 inch, 5301 sq. mils  
(2.36 × 1.45 mm, 3.42 sq. mm)

### WAFER TEST LIMITS at V<sub>S</sub> = ±15V, T<sub>A</sub> = 25°C for OP-77N/G devices.

PARAMETER	SYMBOL	CONDITIONS	OP-77N LIMIT	OP-77G LIMIT	UNITS
Input Offset Voltage	V <sub>OS</sub>		40	75	μV MAX
Input Offset Current	I <sub>OS</sub>		2.0	2.8	nA MAX
Input Bias Current	I <sub>B</sub>		±2	±2.8	nA MAX
Input Resistance Differential-Mode	R <sub>IN</sub>	(Note 1)	26	17	MΩ MIN
Input Voltage Range	IVR		±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = ±13V	1	1.6	μV/V MAX
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = ±3V to ±18V	3	3	μV/V MAX
Output Voltage Swing	V <sub>O</sub>	R <sub>L</sub> = 10kΩ R <sub>L</sub> = 2kΩ R <sub>L</sub> = 1kΩ	±13.5 ±12.5 ±12.0	±13.5 ±12.5 ±12.0	V MIN
Large-Signal Voltage Gain	A <sub>VO</sub>	R <sub>L</sub> = 2kΩ V <sub>O</sub> = ±10V	2000	1000	V/mV MIN
Differential Input Voltage			±30	±30	V MAX
Power Consumption	P <sub>d</sub>	V <sub>OUT</sub> = 0V	60	60	mW MAX

#### NOTES:

1. Guaranteed by design.

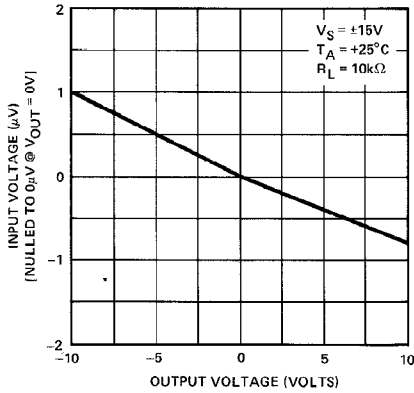
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

### TYPICAL ELECTRICAL CHARACTERISTICS at V<sub>S</sub> = ±15V, T<sub>A</sub> = +25°C, unless otherwise noted.

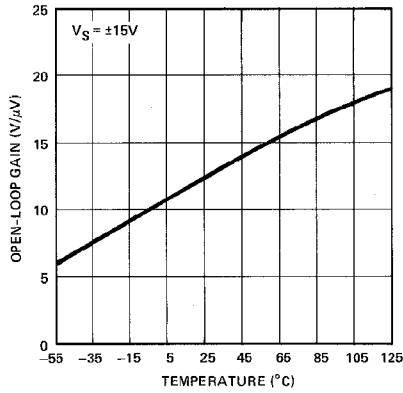
PARAMETER	SYMBOL	CONDITIONS	OP-77N TYPICAL	OP-77G TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV <sub>OS</sub>	R <sub>S</sub> = 50Ω	0.1	0.2	μV/°C
Nullified Input Offset Voltage Drift	TCV <sub>OSn</sub>	R <sub>S</sub> = 50Ω, R <sub>P</sub> = 20kΩ	0.1	0.2	μV/°C
Average Input Offset Current Drift	TCI <sub>OS</sub>		0.5	0.5	pA/°C
Slew Rate	SR	R <sub>L</sub> ≥ 2kΩ	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	A <sub>VCL</sub> = +1	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

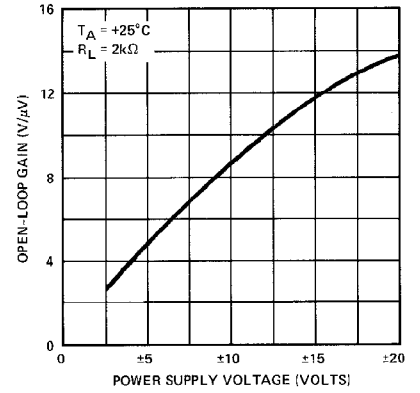
GAIN LINEARITY (INPUT VOLTAGE vs OUTPUT VOLTAGE)



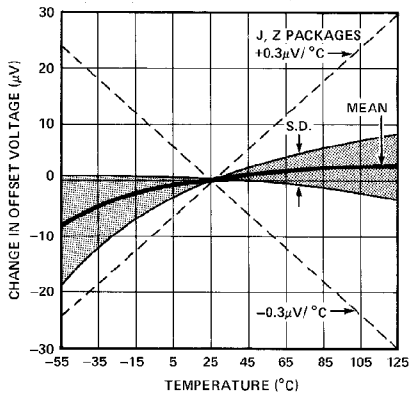
OPEN-LOOP GAIN vs TEMPERATURE



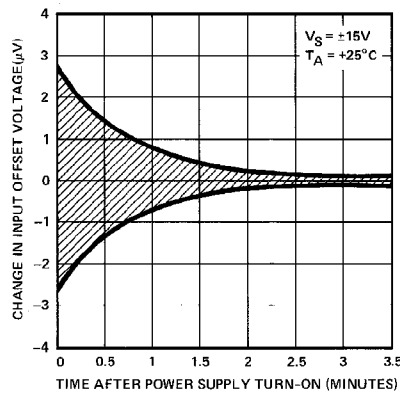
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



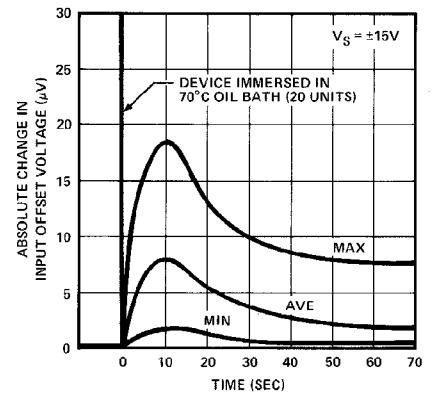
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



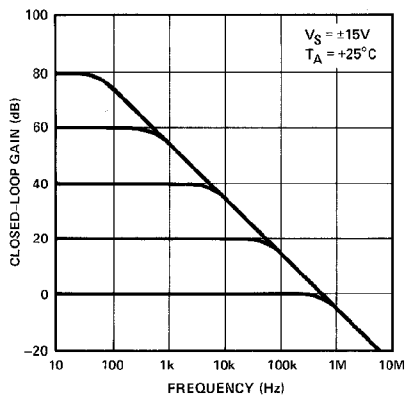
WARM-UP DRIFT



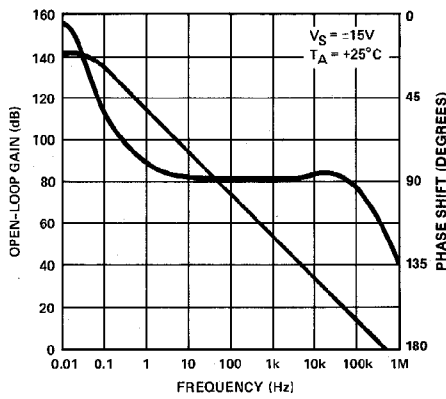
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



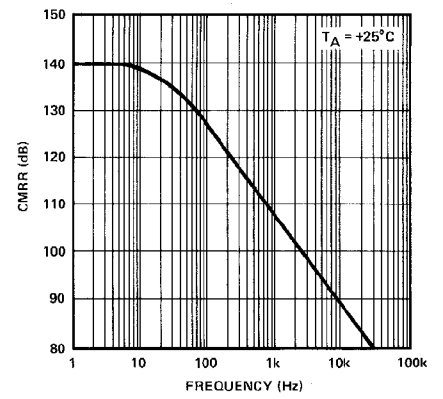
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



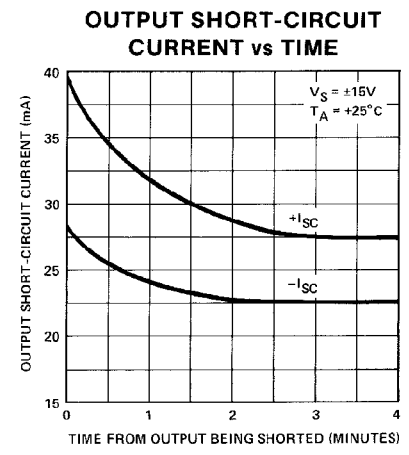
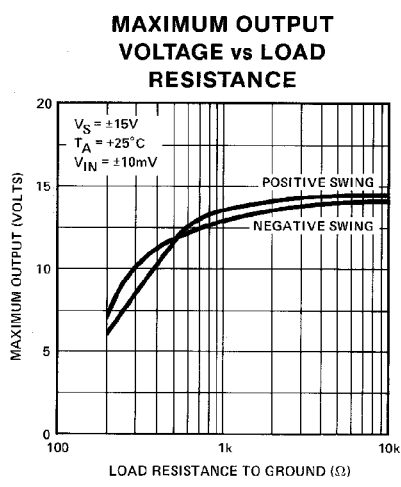
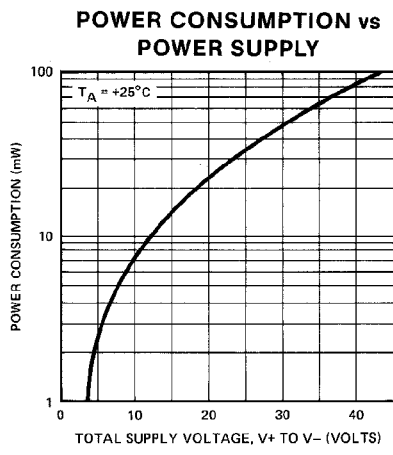
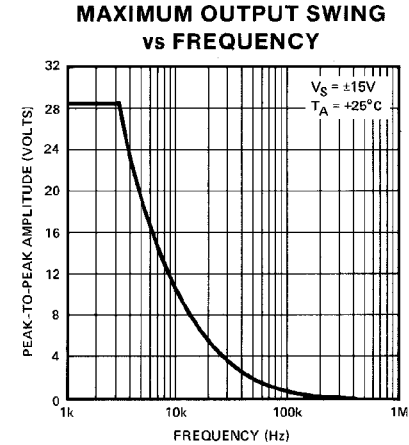
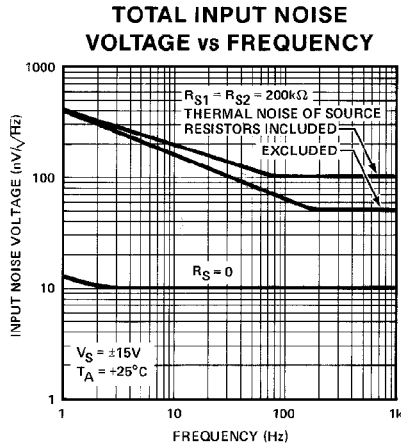
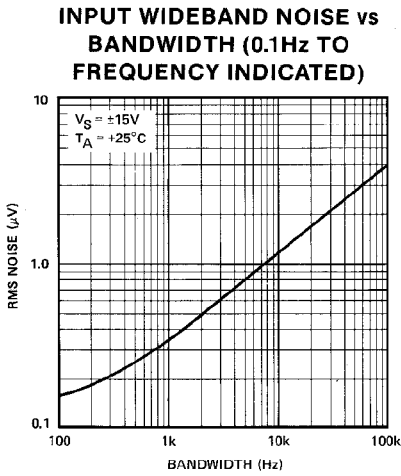
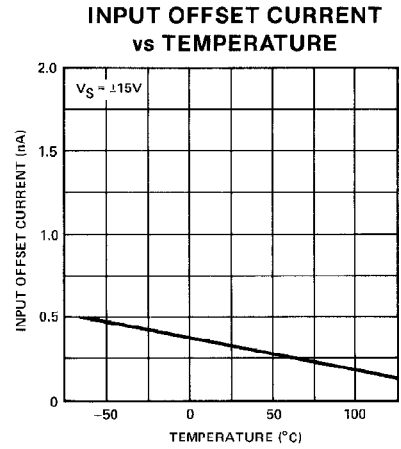
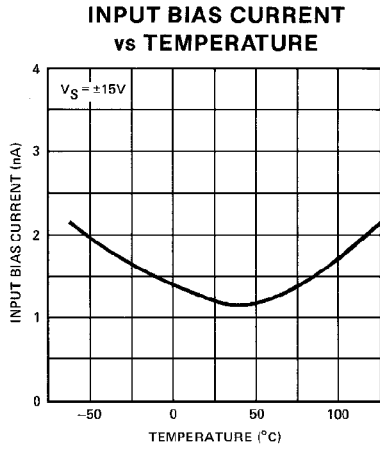
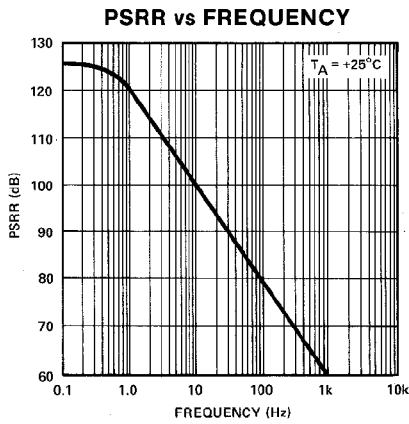
OPEN-LOOP GAIN/PHASE RESPONSE



CMRR vs FREQUENCY



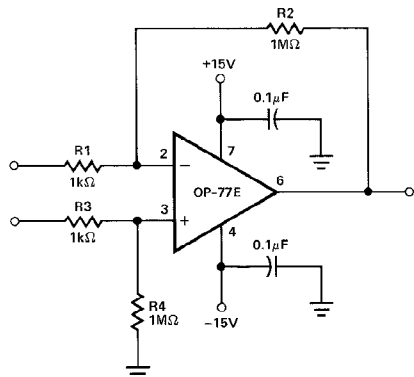
## TYPICAL PERFORMANCE CHARACTERISTICS





## APPLICATIONS INFORMATION

### PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER



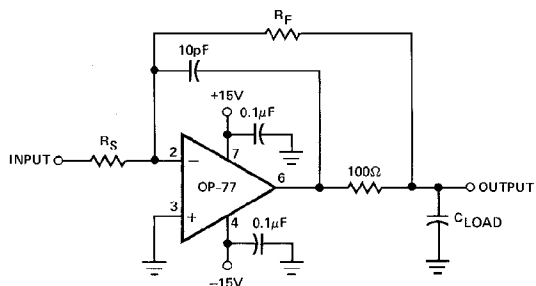
The high gain, gain linearity, CMRR, and low  $TCV_{OS}$  of the OP-77 make it possible to obtain performance not previously available in single stage very high-gain amplifier applications.

For best CMR,  $\frac{R1}{R2}$  must equal  $\frac{R3}{R4}$ . In this example,

with a 10mV differential signal, the maximum errors are as listed.

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.01%/V
GAIN LINEARITY, WORST CASE	0.02%
$TCV_{OS}$	0.003%/°C
$TCI_{OS}$	0.008%/°C

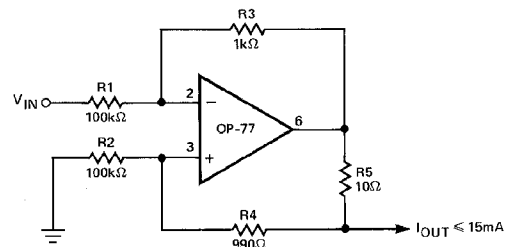
### ISOLATING LARGE CAPACITIVE LOADS



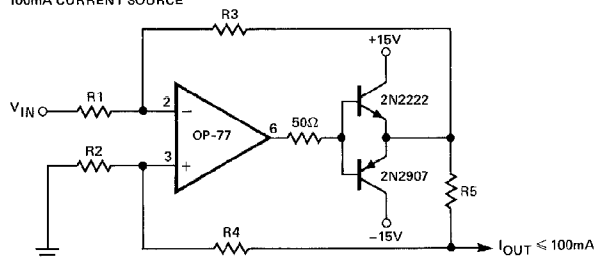
This circuit reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP-77.

### BILATERAL CURRENT SOURCE

#### BASIC CURRENT SOURCE



#### 100mA CURRENT SOURCE



$$I_{OUT} = V_{IN} \frac{R3}{R1 \cdot R5}$$

GIVEN  $R3 = R4 + R5, R1 = R2$

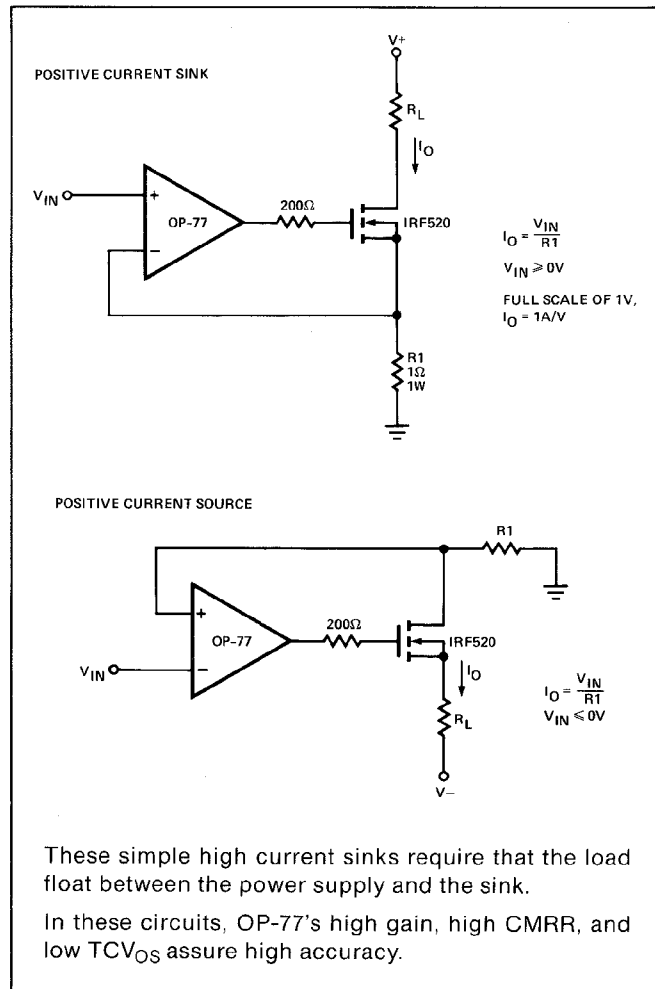
These current sources will supply both positive and negative current into a grounded load.

Note that  $Z_O = \frac{R5 \left( \frac{R4}{R2} + 1 \right)}{R5 + R4 - \frac{R3}{R1}}$

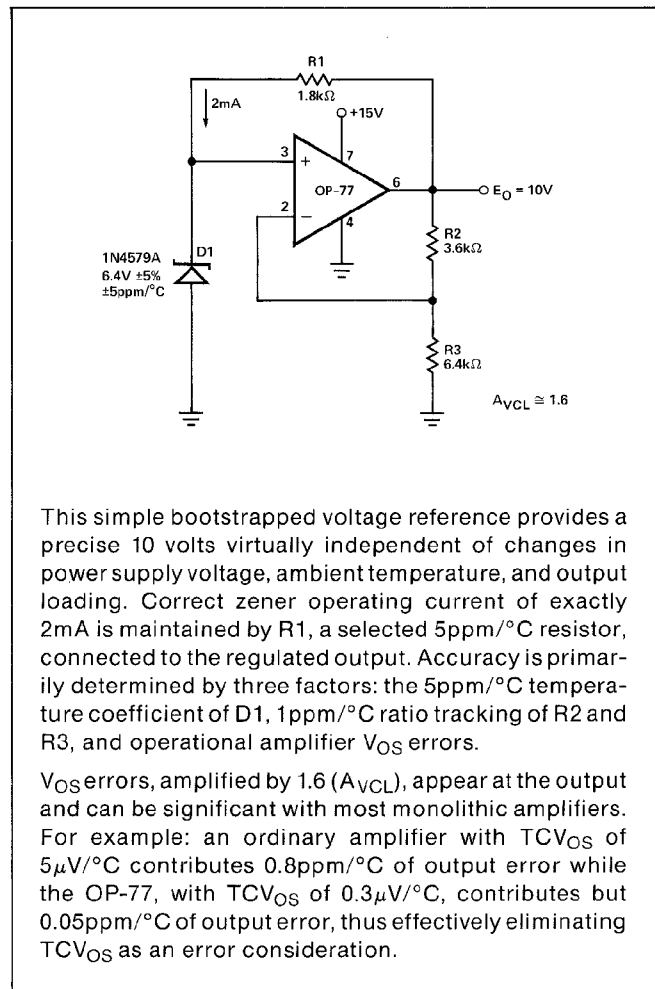
and that for  $Z_O$  to be infinite,

$$\frac{R5 + R4}{R2} \text{ must} = \frac{R3}{R1}$$

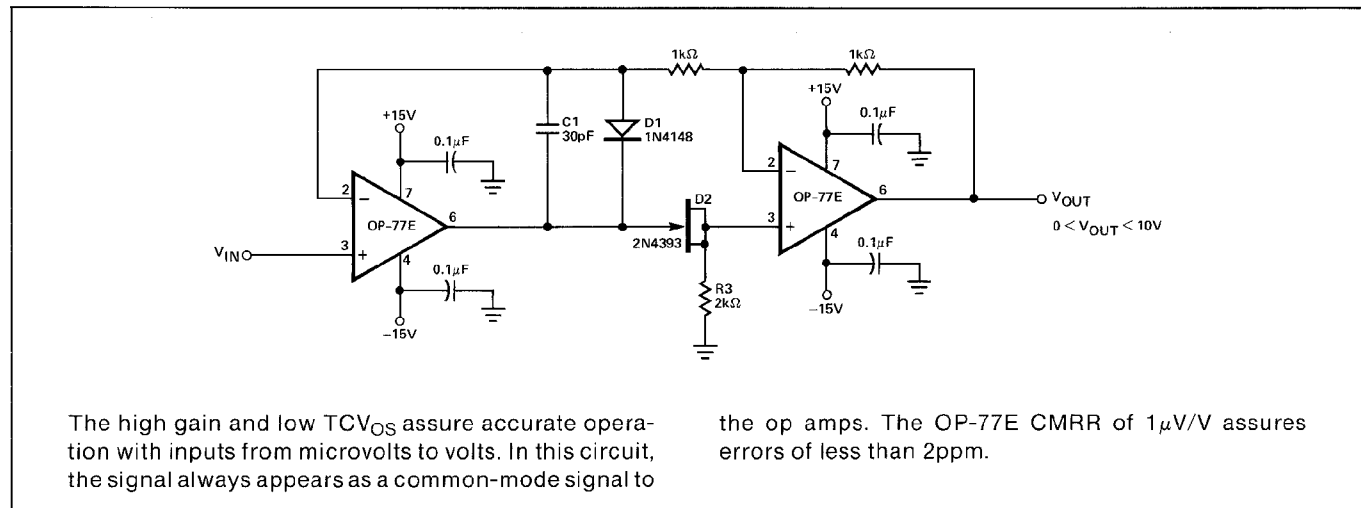
## PRECISION CURRENT SINKS



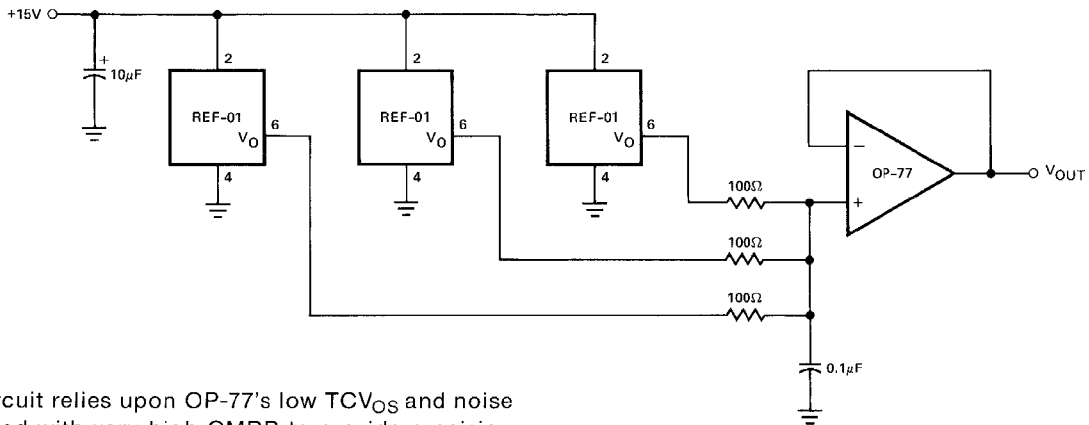
## HIGH STABILITY VOLTAGE REFERENCE



## PRECISION ABSOLUTE VALUE AMPLIFIER

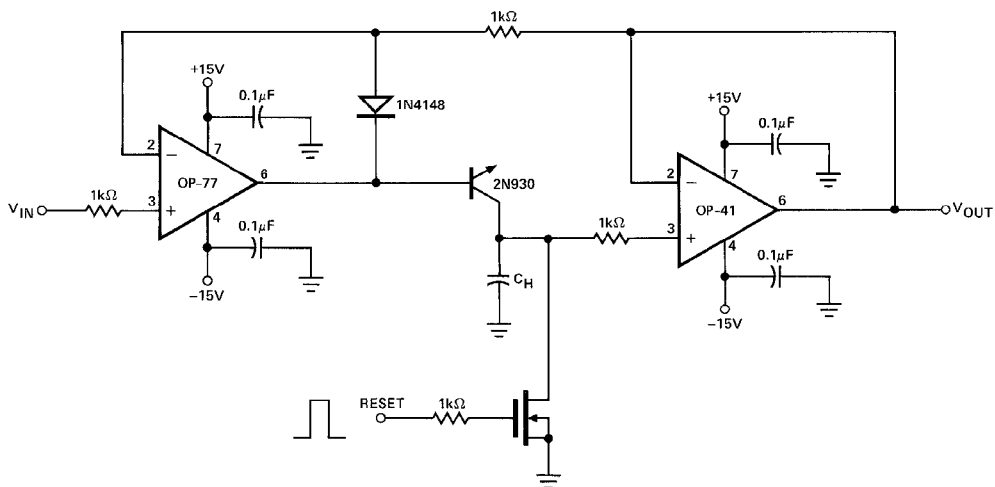


**LOW NOISE PRECISION REFERENCE**



This circuit relies upon OP-77's low  $TCV_{OS}$  and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

**PRECISION POSITIVE PEAK DETECTOR**



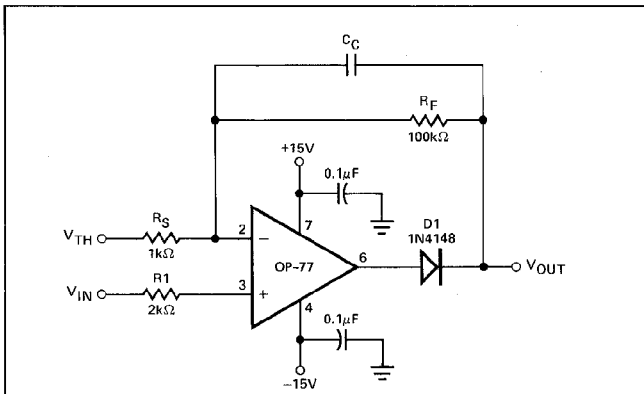
$C_H$  must be of polystyrene, Teflon\*, or polyethylene to minimize dielectric absorption and leakage. The droop

rate is determined by the size of  $C_H$  and the bias current of the OP-41.

\*Teflon is a registered trademark of the Dupont Company.

# OP77

## PRECISION THRESHOLD DETECTOR/ AMPLIFIER

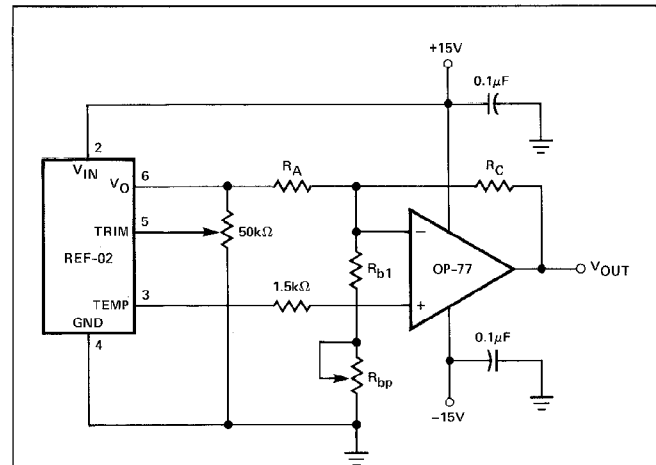


When  $V_{IN} < V_{TH}$ , amplifier output swings negative, reverse biasing diode D1.  $V_{OUT} = V_{TH}$  if  $R_L = \infty$ .  
When  $V_{IN} \geq V_{TH}$ , the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left( 1 + \frac{R_F}{R_S} \right)$$

$C_C$  is selected to smooth the response of the loop.

## PRECISION TEMPERATURE SENSOR



### RESISTOR VALUES

TCV <sub>OUT</sub> SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	-55°C to +125°C	-55°C to +125°C	-67°F to +257°C
OUTPUT VOLTAGE RANGE	-0.55V to +1.25V	-5.5V to +12.5V	-0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
$R_a$ ( $\pm 1\%$ Resistor)	9.09kΩ	15kΩ	7.5kΩ
$R_{b1}$ ( $\pm 1\%$ Resistor)	1.5kΩ	1.82kΩ	1.21kΩ
$R_{bp}$ (Potentiometer)	200Ω	500Ω	200Ω
$R_c$ ( $\pm 1\%$ Resistor)	5.11kΩ	84.5kΩ	8.25kΩ