PM5355

S/UNI-622™

S/UNI-622

SATURN USER NETWORK INTERFACE (622-MBIT/S) STANDARD PRODUCT

DATA SHEET

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PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
3	June 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R3 data sheet from PMC-930527, R8.
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1	October 1994	Creation of Document

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1 FEATURES

- Monolithic Saturn User Network Interface that implements the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432 and the ATM Forum BISDN Inter Carrier Interface (B-ICI) Specification.
- Supports a 77.76 Mbyte/s STS-12c (STM-4c), a 19.44 Mbyte/s STS-3c (STM-1), a 6.48 Mbyte/s STS-1, or a 51.84 Mbit/s STS-1 line side interface.
- Provides four-cell deep FIFO buffers in both the transmit and receive paths.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a generic parallel output port and a generic parallel input port to control and monitor front end line devices.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low-power, +5 Volt, CMOS technology.
- 208-pin high-performance plastic quad flat pack (PQFP) package.

1.1 The receiver section:

- Frames to and descrambles the received STS-12c/3c/1 (STM-4c/1, AU-3) stream.
- Filters and captures the automatic protection switch channel (APS) bytes in readable registers and detects APS byte failure.
- Interprets the received payload pointer (H1, H2) and extracts the STS-12c/3c/1 (STM-4c/1, AU-3) synchronous payload envelope and path overhead.
- Extracts ATM cells from the received STS-12c/3c/1 (STM-4c/1, AU-3) synchronous payload envelope using ATM cell delineation and provides optional ATM cell payload descrambling, header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.
- Provides a generic 16-bit wide datapath interface to read extracted cells from an internal four-cell FIFO buffer.

- Extracts all transport overhead bytes and serializes them in four 5.184 Mbit/s streams for optional external processing.

- Extracts the section user channel (F1) and the order wire channels (E1, E2) and serializes them into three independent 64 kbit/s streams for optional external processing.

- Extracts the data communication channels (D1-D3, D4-D12) and serializes them at 192 kbit/s (D1-D3) and 576 kbit/s (D4-D12) for optional external processing.

- Extracts all path overhead bytes and serializes them at 576 kbit/s for optional external processing.

- Extracts the 16- or 64-byte section trace (C1) sequence and the 16- or 64-byte path trace (J1) sequence into internal register banks.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (AIS), line remote defect indication (LRDI), loss of pointer (LOP), path alarm indication signal (AIS), path remote defect indication signal (RDI-P) and loss of cell delineation (LCD).

- Counts received section BIP-8 (B1) errors, received line BIP-96/24/8 (B2) errors, line far end block errors (line FEBEs), received path BIP-8 (B3) errors and path far end block errors (path FEBEs) for performance monitoring purposes.

- Counts received cells written into the receive FIFO, received HCS errored cells that are discarded, and received HCS errored cells that are corrected and passed on.

- Extracts and serializes the GFC field from all received cells (including idle/unassigned cells) for external processing.

1.2 The transmitter section:

- Provides an internal four-cell FIFO into which cells are written using a generic 16-bit wide datapath interface.

- Inserts the generic flow control (GFC) bits via a simple serial interface.

- Counts transmit cells read from the transmit FIFO.

- Provides idle/unassigned cell insertion, HCS generation/insertion, and ATM cell payload scrambling.
- Inserts ATM cells into the transmitted STS-12c/3c/1 (STM-4c/1, AU-3) synchronous payload envelope.
- Inserts a register programmable path signal label.
- Generates the transmit payload pointer (H1, H2) and inserts the path overhead.
- Optionally inserts the 16- or 64-byte section trace (C1) sequence and the 16- or 64-byte path trace (J1) sequence from internal register banks.
- Optionally inserts externally generated path overhead bytes received via a 576 kbit/s serial interface.
- Optionally inserts externally generated data communication channels (D1-D3, D4-D12) via a 192 kbit/s (D1-D3) serial stream and a 576 kbit/s (D4-D12) serial stream.
- Optionally inserts externally generated section user channel (F1) and externally generated order wire channels (E1, E2) via three 64 kbit/s serial interfaces.
- Optionally inserts externally generated transport overhead bytes received via four 5.184 Mbit/s serial interfaces.
- Scrambles the transmitted STS-12c/3c/1 (STM-4c/1, AU-3) stream and inserts the framing bytes (A1, A2) and the identity byte (C1).
- Optionally inserts path alarm indication signal (AIS), path remote defect indication (RDI-P), line alarm indication signal (AIS) and line remote defect indication (LRDI) indication.
- Optionally inserts register programmable APS bytes.
- Inserts path BIP-8 codes (B3), path far end block error (FEBE) indications, line BIP-96/24/8 codes (B2), line far end block error (FEBE) indications, and section BIP-8 codes (B1) to allow performance monitoring at the far end.
- Allows forced insertion of all-zeros data (after scrambling), the corruption of the framing bytes or the corruption of the section, line, or path BIP-8 codes for diagnostic purposes.

2 APPLICATIONS

- Workstations
- LAN Switches and Hubs
- Routers
- Video Servers
- Backbones
- Broadband Switching Systems

3 REFERENCES

1. ITU-T Recommendation G.709 - "Synchronous Multiplexing Structure," Helsinki, March 1993.

2. ITU-T Recommendation I.432 - "B-ISDN User-Network Interface-Physical Interface Specification," Helsinki, March 1993.

3. Bell Communications Research - "SONET Transport Systems Common Generic Criteria", GR-253-CORE, Issue 1, December 1994.

4. Bell Communications Research - "Generic Requirements for Operations of Broadband Switching Systems", TA-NWT-00001248, Issue 2, October 1993.

5. ATM Forum - "622 Mbps Physical Layer Specification", af-phy-0046.000, January 1996.

6. ANSI T1.105-1991, Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET)

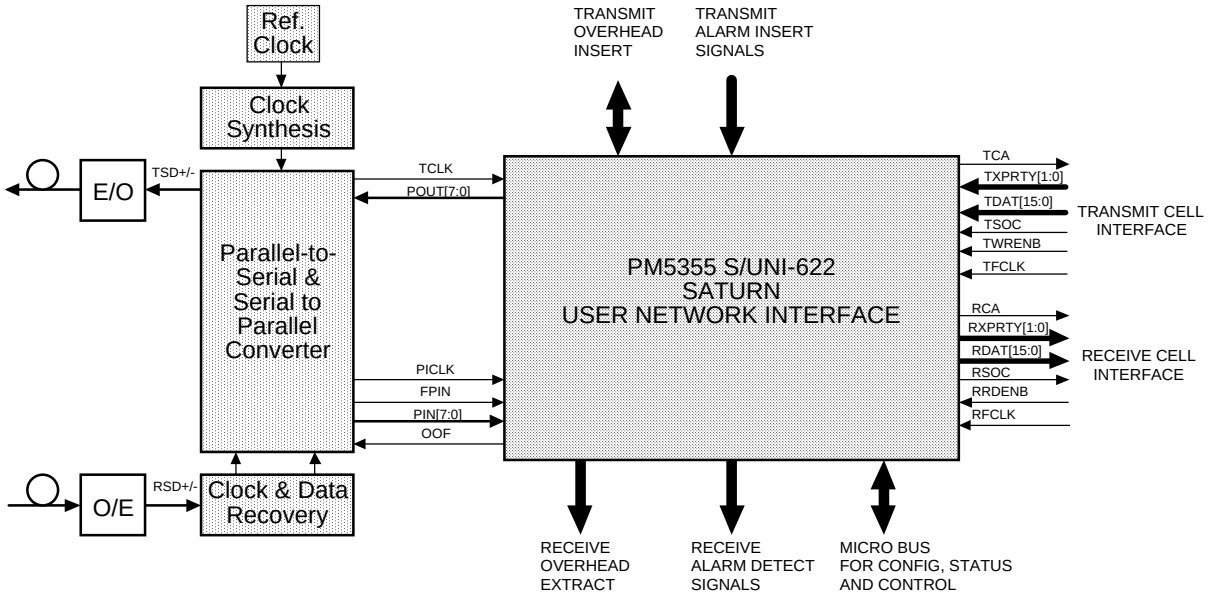
7. IEEE 1149.1 - "Standard Test Access Port and Boundary Scan Architecture", May 21, 1990.

8. PMC-940212, ATM_SCI_PHY, "SATURN Compliant Interfaces For ATM Devices," October 1995, Issue 3.

4 APPLICATION EXAMPLES

The S/UNI-622 is typically used to implement the core of an ATM User Network Interface by which an ATM terminal is linked to an ATM switching system using SONET/SDH-compatible transport. The S/UNI-622 may find application at either end of terminal-to-switch links or switch-to-switch links, both in private network (LAN) and public network (WAN) situations. In a typical STS-3c (STM-1) or STS-12c (STM-4c) application, the S/UNI-622 requires a clock and data recovery/serial-to-parallel converter device in the receive direction and a serial-to-parallel converter/clock synthesis device in the transmit direction on the line side. The clock synthesis function is not required if the transmit side is looptimed to the receive clock. The initial configuration and ongoing control and monitoring of the S/UNI-622 are normally provided via a generic microprocessor interface. The S/UNI-622 supports a "hardware-only" operating mode for STS-12c (STM-4c) where an external microprocessor is not required. This application is shown in Figure 1.

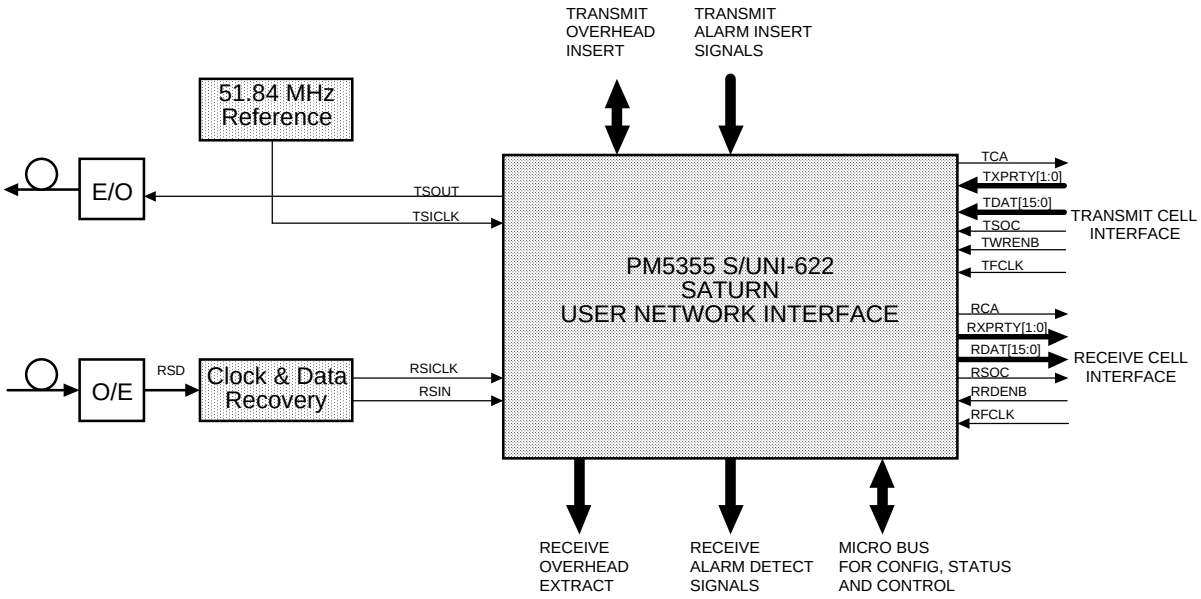
Figure 1 - Typical STS-12c/3c ATM Interface



In a typical STS-1 application, the S/UNI-622 requires a clock and data recovery device in the receive direction and a clock source in the transmit direction on the line side. The initial configuration and ongoing control and monitoring of the S/UNI-622 are normally provided via a generic microprocessor interface. A typical STS-1 ATM Interface is shown in Figure 2. On the receive side, an

external clock and data recovery device is used. On the transmit side, the S/UNI-622 is configured for looptime operation where the receive clock, RSICLK, is used as the transmit clock source.

Figure 2 - Typical STS-1 ATM Interface



5 BLOCK DIAGRAM

Figure 3 - Normal Operating Mode

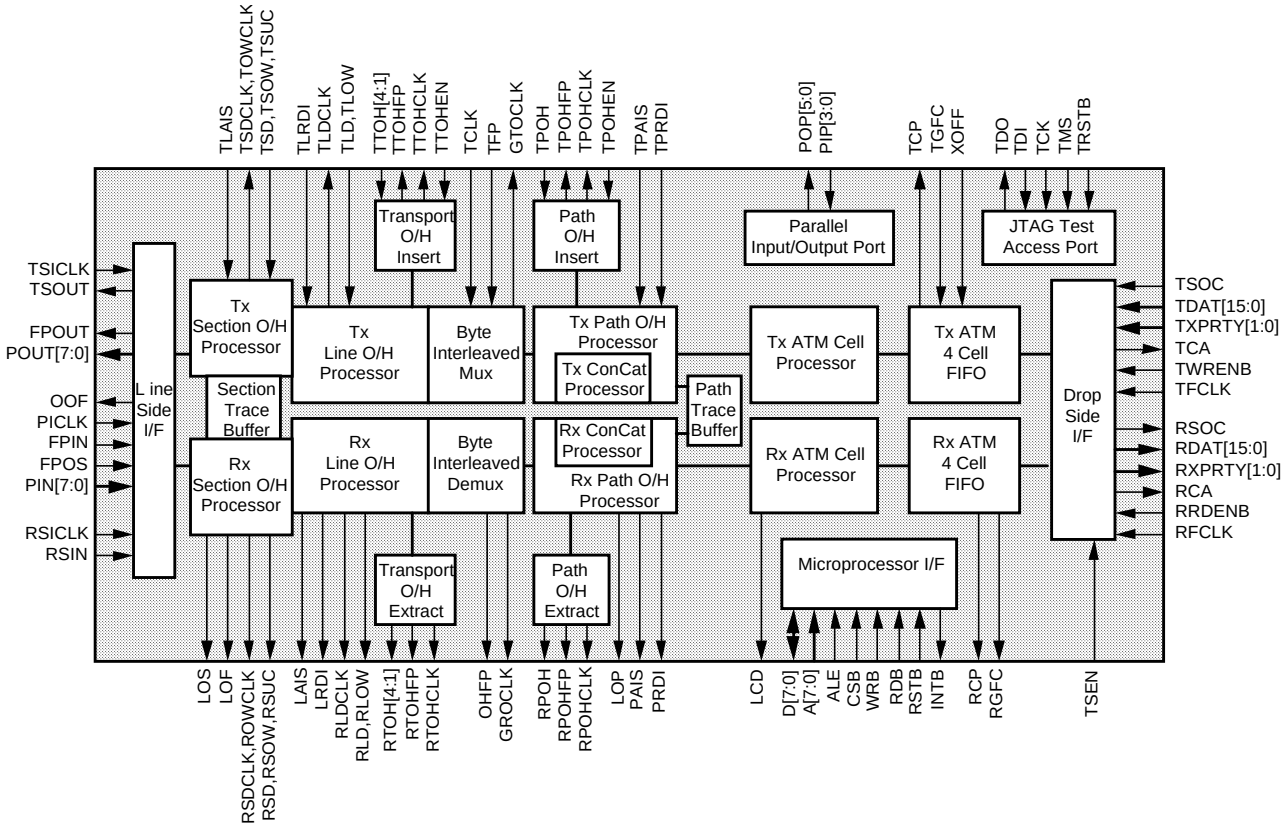
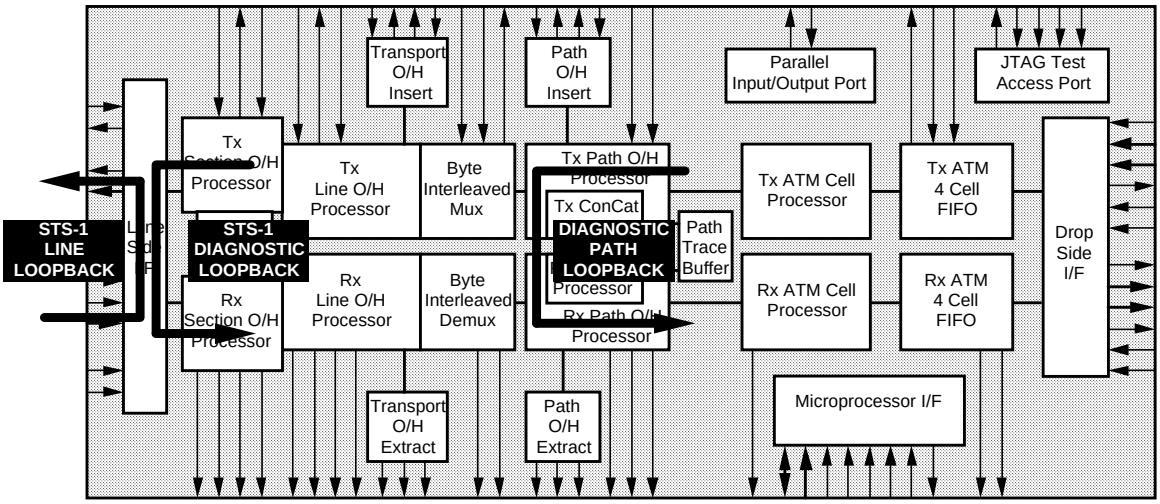


Figure 4 - Loopback Modes



6 DESCRIPTION

The PM5355 S/UNI-622 SATURN User Network Interface is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 622-Mbit/s ATM User Network Interface.

The S/UNI-622 receives SONET/SDH frames via a byte-serial interface (or bit-serial interface for STS-1), and processes section, line, and path overhead. It performs framing (A1, A2), performs descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1) are also accumulated. The S/UNI-622 interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload. In addition to basic processing of the received SONET/SDH overhead, the S/UNI-622 provides convenient access to all overhead bytes, which are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The S/UNI-622 frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four-cell FIFO buffer. The received cells are read from the FIFO using a generic 16-bit wide datapath interface. Counts of errored received ATM cell headers that are uncorrectable and those that are correctable are accumulated independently for performance monitoring purposes.

The S/UNI-622 transmits SONET/SDH frames via a byte-serial interface (or bit-serial interface for STS-1) and formats section, line, and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted. The S/UNI-622 generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. In addition to the basic formatting of the transmitted SONET/SDH overhead, the S/UNI-622 provides convenient access to all overhead bytes, which are optionally inserted from lower rate serial interfaces, allowing external sourcing of overhead, if desired. The S/UNI-622 also supports the insertion of a large variety of errors into the transmit stream,

such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

ATM cells are written to an internal four-cell FIFO using a generic 16-bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. Generic flow control (GFC) bits may be inserted downstream of the FIFO via a serial link so that all FIFO latency may be bypassed. The S/UNI-622 provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

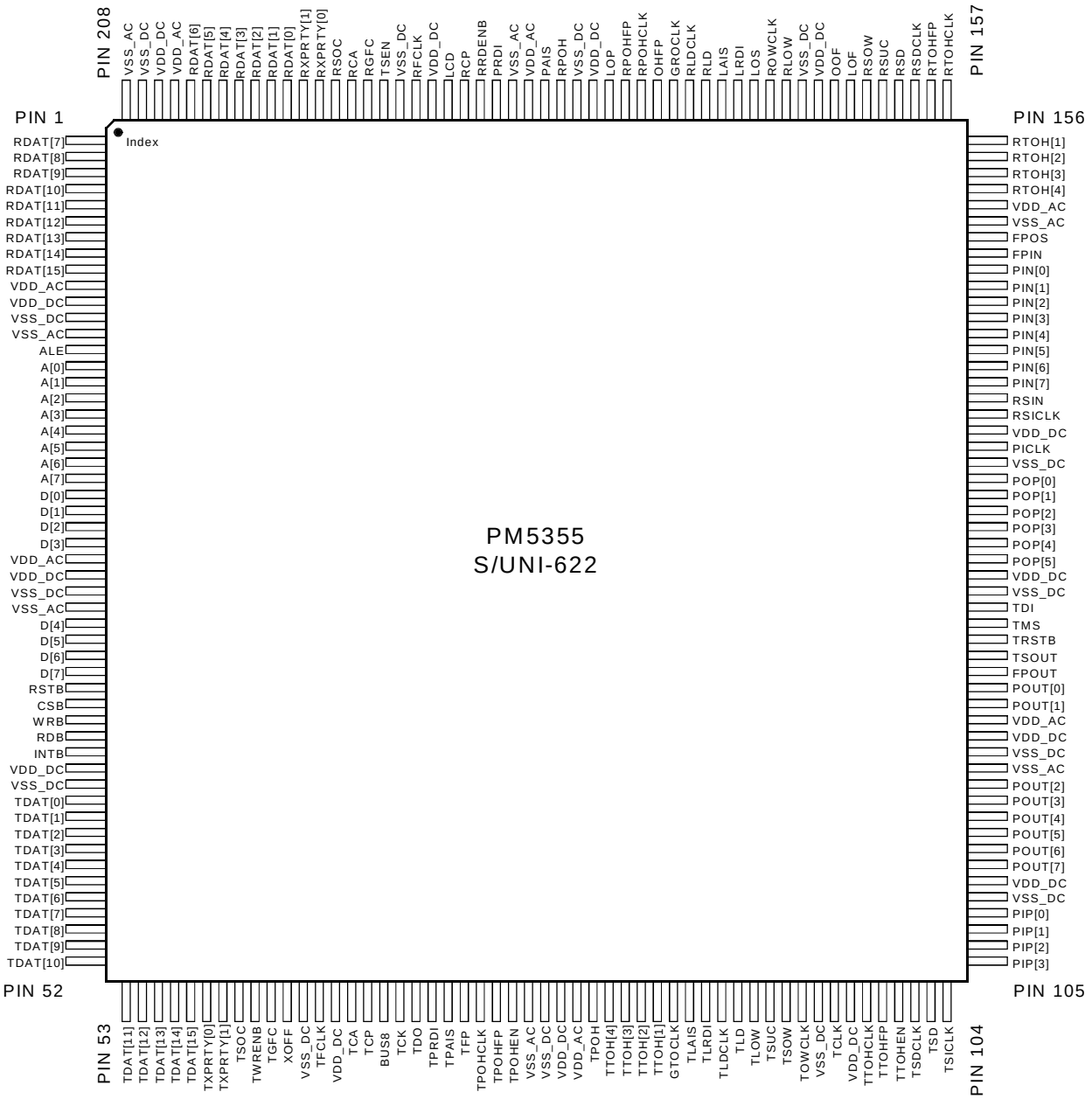
No auxiliary clocks are required directly by the S/UNI-622 since it operates from two line clocks. The S/UNI-622 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-622 also provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-622 is implemented in low-power, +5 Volt, CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 208-pin PQFP package.

7 PIN DIAGRAM

The S/UNI-622 is packaged in a 208-pin slugged plastic QFP package having a body size of 28 mm by 28 mm and a pin pitch of 0.5 mm.

Figure 5 -



8 PIN DESCRIPTION

Table 1 -

Pin Name	Type	Pin No.	Function
PICLK RX_VCLK	Input	137	The parallel input clock (PICLK) provides timing for S/UNI-622 receive function operation. PICLK is a 6.48 MHz (STS-1), 19.44 MHz (STS-3c/STM-1), or 77.76 MHz (STS-12c/STM-4c), nominally 50% duty cycle clock, depending on the selected operating mode. PIN[7:0] and FPIN are sampled on the rising edge of PICLK. The test vector clock (RX_VCLK) signal is used during S/UNI-622 production testing to verify internal functionality.
PIN[0] PIN[1] PIN[2] PIN[3] PIN[4] PIN[5] PIN[6] PIN[7]	Input	148 147 146 145 144 143 142 141	The data input (PIN[7:0]) bus carries the byte-serial STS-12c/3c/1 stream. PIN[7:0] is sampled on the rising edge of PICLK. PIN[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). PIN[0] is the least significant bit (corresponding to bit 8 of each word, the last bit received).
FPIN	Input	149	The active-high framing position input (FPIN) signal indicates the SONET frame position on the PIN[7:0] bus. The byte position indicated by FPIN is selected by the FPOS input as described below. FPIN is sampled on the rising edge of PICLK.
FPOS	Input	150	The frame position input (FPOS) selects the frame byte position in the SONET frame indicated by the FPIN input. When FPOS is tied high and STS-3c or STS-12c mode is selected, a pulse on FPIN marks the third A2 framing byte position on the PIN[7:0] bus. When FPOS is tied low and STS-3c or STS-12c mode is selected, a pulse on FPIN marks the first synchronous payload envelope byte position after the C1 bytes on PIN[7:0]. When configured for STS-1 mode, a pulse on FPIN always marks the first synchronous payload envelope byte position after the C1 byte on PIN[7:0].
RSICLK	Input	139	The receive serial incoming clock (RSICLK) provides timing for processing the bit-serial STS-1 receive stream, RSIN. RSICLK is nominally a 51.84 MHz, 50% duty cycle clock. RSIN is sampled on the rising edge of RSICLK. RSICLK is divided by eight to produce GROCLK when the bit-serial STS-1 mode is selected. RSICLK should be disabled when the bit-serial STS-1 interface is not used.
RSIN	Input	140	The receive incoming serial stream (RSIN) carries the scrambled STS-1 stream in bit-serial format. RSIN is sampled on the rising edge of RSICLK.

Pin Name	Type	Pin No.	Function
OOF	Output	164	The out of frame (OOF) signal is high while the S/UNI-622 is out of frame. OOF is low while the S/UNI-622 is in-frame. An out of frame declaration occurs when four consecutive errored framing patterns (A1 and A2 bytes) have been received. OOF is intended to be used to enable an upstream framing pattern detector to search for the framing pattern. This alarm indication is also available via register access. OOF is updated on the rising edge of PICLK.
GROCLK	Output	174	The generated receive outgoing clock (GROCLK) is nominally a 6.48 MHz or 19.44 MHz, 50% duty cycle clock. When configured for STS-1 bit-serial mode, GROCLK is the RSICLK clock input divided down by eight. For this mode, GROCLK is updated on the rising edge of RSICLK and is expected to be used to drive input PICLK. When configured for STS-1 or STS-3c byte-serial mode, GROCLK is a flowed through version of PICLK. When configured for STS-12c byte-serial mode, GROCLK is the PICLK clock input divided by four. For this mode, GROCLK is updated on the rising edge of PICLK.
TCLK TX_VCLK	Input	97	The transmit clock (TCLK) provides timing for S/UNI-622 transmit function operation. TCLK should be a 6.48 MHz (STS-1), 19.44 MHz (STS-3c/STM-1), or 77.76 MHz (STS-12c/STM-4c), nominally 50% duty cycle clock, depending on the selected operating mode. The test vector clock (TX_VCLK) signal is used during S/UNI-622 production testing to verify internal functionality.
TFP	Input	74	The active high transmit frame pulse (TFP) signal is used to align the SONET/SDH transport frame generated by the S/UNI-622 device to a system reference. TFP should be brought high for a single GTOCLK period every 810 (STS-1), 2430 (STS-3c), 2430 (STS-12c) GTOCLK cycles, or a multiple thereof. TFP may be tied low if such synchronization is not required. The offset between a pulse applied to the TFP input and the resultant FPOUT pulse is 18 TCLK periods in STS-1 mode, 26 TCLK periods in STS-3c mode and 81 TCLK periods in STS-12c mode. TFP is sampled on the rising edge of GTOCLK.
POUT[0] POUT[1] POUT[2] POUT[3] POUT[4] POUT[5] POUT[6] POUT[7]	Output	122 121 116 115 114 113 112 111	The parallel outgoing stream, (POUT[7:0]), carries the scrambled STS-12/3c/1 stream in byte-serial format. POUT[7:0] is updated on the rising edge of TCLK. POUT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). POUT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted).

Pin Name	Type	Pin No.	Function
FPOUT	Output	123	The active-high framing position output (FPOUT) signal marks the frame alignment on the POUT[7:0] bus. FPOUT goes high for a single TCLK period during the first synchronous payload envelope byte after the twelve C1 bytes. FPOUT is updated on the rising edge of TCLK.
TSICLK	Input	104	The transmit serial incoming clock (TSICLK) provides timing for updating the bit-serial outgoing stream when bit-serial STS-1 mode is selected. TSICLK is nominally a 51.84 MHz, 50% duty cycle clock. TSOUT is updated on the rising edge of TSICLK. TSICLK should be disabled when the bit-serial STS-1 interface is not used.
TSOUT	Output	124	The transmit serial outgoing stream, (TSOUT), carries the scrambled stream in bit-serial format when STS-1 bit-serial mode is selected. TSOUT is updated on the rising edge of TSICLK. In STS-1 bit-serial mode with line loopback or loop time modes enabled, TSOUT is updated on the rising edge of RSICLK.
GTOCLK	Output	87	The generated transmit output clock (GTOCLK) is nominally a 6.48 MHz or 19.44 MHz, 50% duty cycle clock. When configured for STS-1 bit-serial mode, GTOCLK is the TSICLK clock input divided down by eight. For this mode, GTOCLK is updated on the rising edge of TSICLK and is expected to be used to drive input TCLK. In STS-1 bit-serial mode with line loopback or loop time modes enabled, GTOCLK is the RSICLK clock input divided down by eight and is updated on the rising edge of RSICLK. When configured for STS-1 or STS-3c byte-serial mode, GTOCLK is a flowed through version of TCLK. When configured for STS-12c byte-serial mode, GTOCLK is the TCLK clock input divided by four. For this mode, GTOCLK is updated on the rising edge of TCLK.
LOS	Output	169	The loss of signal (LOS) signal is set high when loss of signal is declared. This occurs when a violating period (20 ± 3 µs) of consecutive all-zeros bytes is detected on the incoming STS-12c/3c/1 signal (before descrambling). LOS is removed when two valid framing words (A1, A2) are detected and during the intervening time, no violating period of consecutive all zeros patterns is detected. This alarm indication is also available via register access. LOS is updated on the rising edge of PICLK.
LOF	Output	163	The loss of frame (LOF) signal is set high when loss of frame is declared. This occurs when an out-of-frame condition (as indicated by a high level on the OOF output) persists for a period of 3 ms. LOF is removed when an in-frame condition (as indicated by a low level on the OOF output) persists for a period of 3 ms. This alarm indication is also available via register access. LOF is updated on the rising edge of PICLK.

Pin Name	Type	Pin No.	Function
LAIS	Output	171	The line alarm indication signal (LAIS) is set high when line AIS is declared. This occurs when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. LAIS is removed when any pattern other than 111 is detected in bits 6, 7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. This alarm indication is also available via register access. LAIS is updated on the rising edge of PICLK.
LRDI	Output	170	The line remote defect indication (LRDI) signal is set high when line RDI is declared. This occurs when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. LRDI is removed when any pattern other than 110 is detected in bits 6, 7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. This alarm indication is also available via register access. LRDI is updated on the rising edge of PICLK.
LOP	Output	178	The loss of pointer (LOP) signal is set high when loss of pointer is declared. This occurs when a valid pointer (H1, H2) is not found in eight consecutive frames, or if eight consecutive new data flags are detected. LOP is removed when the same valid and normal pointer with a normal new data flag is detected in three consecutive frames. The loss of pointer state is not entered if the incoming stream contains path AIS. This alarm indication is also available via register access. LOP is updated on the falling edge of GROCLK.
PAIS	Output	182	The path AIS (PAIS) signal is set high when STS-path AIS is declared. This occurs when an all-ones pattern is observed in the pointer bytes (H1, H2) for three consecutive frames. Path AIS is removed when the same valid and normal pointer is detected for three consecutive frames or a legal pointer with an active NDF is received. This alarm indication is also available via register access. PAIS is updated on the falling edge of GROCLK.
PRDI	Output	185	The path remote defect indication (PRDI) signal is set high when a path remote defect indication is detected. This occurs when bit 5 of the path status byte (G1) is set high for five (or ten) consecutive frames. Path remote defect is removed when bit 5 of the G1 byte is set low for five (or ten) consecutive frames. This indication is also available via register access. PRDI is updated on the falling edge of GROCLK.
LCD	Output	188	The loss of cell delineation (LCD) signal indicates when cell delineation can not be found. LCD transitions high when an out of cell delineation (OCD) anomaly has persisted for 4 ms. Once asserted, LCD remains high until no OCD anomaly has been detected for 4 ms at which time, LCD is set low. The OCD state is entered when the cell delineation state machine is not in the SYNC state. Please refer to the Functional Description section for an explanation of the cell delineation state machine. This alarm indication is also available via register access. LCD is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
TLAIS	Input	88	The active-high transmit line alarm indication (TLAIS) signal controls the insertion of line AIS. Line AIS is inserted by overwriting the SONET/SDH frame contents with all ones (before scrambling). The section overhead is not overwritten. This function can also be performed via register access. Line AIS insertion is internally synchronized to frame boundaries. The TLAIS input take precedence over the TTOH and TTOHEN inputs. TLAIS is sampled on the rising edge of TCLK.
TLRDI	Input	89	The active-high transmit line remote defect indication (TLRDI) signal controls the insertion of line RDI. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6,7, and 8 of the K2 byte. This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of signal, or loss of frame. The TLRDI input takes precedence over the TTOH and TTOHEN inputs. TLRDI is sampled on the rising edge of TCLK.
TPAIS	Input	73	The active-high transmit path alarm indication (TPAIS) signal controls the insertion of STS-path AIS. A high level on TPAIS forces the insertion of an all ones pattern into the complete synchronous payload envelope, and the payload pointer bytes (H1, H2). Path AIS insertion is internally synchronized to SPE frame boundaries. This function can also be performed via register access. TPAIS is sampled on the rising edge of GTOCLK.
TPRDI	Input	72	The transmit path remote defect indication (TPRDI) signal controls the insertion of the path remote defect indication signal. A high level on TPRDI forces a logic one to be inserted in the path remote defect indication bit position in the path status byte (G1). This function can also be performed via register access, or be enabled to occur automatically upon detection of receive line AIS, loss of frame, loss of signal, loss of pointer or path AIS. The TPOH and TPOHEN inputs take precedence over the TPRDI input. TPRDI is sampled on the rising edge of GTOCLK.
RFCLK	Input	190	The receive FIFO clock (RFCLK) is used to read words from the synchronous FIFO interface. RFCLK must cycle at a 52 MHz or lower rate, but at a high enough rate to avoid FIFO overflow. RRDENB is sampled using the rising edge of RFCLK. RSOC, RCA, RXPRTY[1:0] and RDAT[15:0] are updated on the rising edge of RFCLK.
RRDENB	Input	186	The active-low receive read enable input (RRDENB) is used to initiate reads from the receive FIFO. When sampled low using the rising edge of RFCLK, a word is read from the internal synchronous FIFO and output on bus RDAT[15:0]. When sampled high using the rising edge of RFCLK, no read is performed and outputs RDAT[15:0], RXPRTY[1:0] and RSOC are tristated if the TSEN input is high. RRDENB must operate in conjunction with RFCLK to access the FIFO at an instantaneous rate high enough to avoid FIFO overflows.

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Tristate	198 199 200 201 202 203 204 1 2 3 4 5 6 7 8 9	The receive cell data (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive FIFO. RDAT[15:0] is updated on the rising edge of RFCLK. When the S/UNI-622 is configured for tristate operation using the TSEN input, tristating of output bus RDAT[15:0] is controlled by input RRDENB.
RXPRTY[0] RXPRTY[1]	Tristate	196 197	The receive parity (RXPRTY[1:0]) signals indicate the parity of the RDAT[15:0] bus. In word parity mode, RXPRTY[1] is the parity calculation over the RDAT[15:0] bus and RXPRTY[0] is unused. In byte parity mode, RXPRTY[1] is the parity calculation over the RDAT[15:8] bus and RXPRTY[0] is the parity calculation over the RDAT[7:0] bus. Selection between word parity mode and byte parity mode is made using a register bit. Odd or even parity selection is made using a register bit. RXPRTY[1:0] is updated on the rising edge of RFCLK. When the S/UNI-622 is configured for tristate operation using the TSEN input, tristating of output bus RXPRTY[1:0] is control by input RRDENB.
RSOC	Tristate	195	The receive start of cell (RSOC) signal marks the start of cell on the RDAT[15:0] bus. When RSOC is high, the first word of the cell structure is present on the RDAT bus. RSOC is updated on the rising edge of RFCLK. When the S/UNI-622 is configured for tristate operation using the TSEN input, tristating of output RSOC is control by input RRDENB.
RCA	Output	194	The receive cell available (RCA) signal indicates when a cell is available in the receive FIFO. When high, RCA indicates that the receive FIFO has at least one cell available to be read. When RCA goes low, the receive FIFO contains only four words or is empty. Selection is made using a bit in the RACP Interrupt Enable/Control register. RCA is updated on the rising edge of RFCLK. The active polarity of TCA is programmable and defaults to active-high.

Pin Name	Type	Pin No.	Function
TSEN	Input	192	The tristate enable (TSEN) signal allows tristate control over outputs RDAT[15:0], RXPRTY[1:0] and RSOC. When TSEN is high, the active-low receive read enable input, RRBENB, controls when outputs RDAT[15:0], RXPRTY[1:0] and RSOC are driven. When TSEN is low, outputs RDAT[15:0], RXPRTY[1:0] and RSOC are always driven.
TFCLK	Input	65	The transmit FIFO clock (TFCLK) is used to write words to the synchronous FIFO interface. TFCLK must cycle at a 52 MHz or lower rate. TWRENB, TSOC, TXPRTY[1:0] and TDAT[15:0] are sampled on the rising edge of TFCLK. In addition, TCA is updated on the rising edge of TFCLK.
TWRENB	Input	61	The active-low transmit write enable input (TWRENB) is used to initiate writes to the transmit FIFO. When sampled low using the rising edge of TFCLK, the 16-bit word on TDAT[15:0] is written into the transmit FIFO. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53-octet cell must be written to the FIFO before it is inserted into the STS-12c/3c/1 SPE. Idle/unassigned cells are inserted when a complete cell is not available from the FIFO.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8]	Input	42 43 44 45 46 47 48 49 50	The transmit cell data (TDAT[15:0]) bus carries the ATM cell octets that are written to the transmit FIFO. TDAT[15:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.
TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]		51 52 53 54 55 56 57	

Pin Name	Type	Pin No.	Function
TXPRTY[0] TXPRTY[1]	Input	58 59	The transmit parity (TXPRTY[1:0]) signals indicate the parity of the TDAT[15:0] bus. In word parity mode, TXPRTY[1] is expected to be the parity calculation over the TDAT[15:0] bus and TXPRTY[0] is ignored. In byte parity mode, TXPRTY[1] is expected to be the parity calculation over the TDAT[15:8] bus and TXPRTY[0] is expected to be the parity calculation over the TDAT[7:0] bus. Selection between word parity mode and byte parity mode is made using a register bit. Odd or even parity selection is made using a register bit. TXPRTY[1:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.
TSOC	Input	60	The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[15:0] bus. When TSOC is high, the first word of the cell structure is present on the TDAT[15:0] stream. It is not necessary for TSOC to be present for each cell. An interrupt may be generated if TSOC is high during any word other than the first word of the cell structure. TSOC is sampled on the rising edge of TFCLK and is considered valid only when TWRENB is simultaneously asserted.
TCA	Output	67	The transmit cell available (TCA) signal indicates when a cell is available in the transmit FIFO. When high, TCA indicates that the transmit FIFO is not full. When TCA goes low, it indicates that either the transmit FIFO is near full and can accept no more than four writes or that the transmit FIFO is full. Selection is made using a register bit. In addition, to reduce FIFO latency, the FIFO full level can be programmed using bits in the FIFO register. TCA is updated on the rising edge of TFCLK. The active polarity of TCA is programmable and defaults to active-high. The TCA output is asserted (set high) when the S/UNI-622 is reset.
XOFF	Input	63	The XOFF pin should not be used, and must be forced low.
RTOH[1] RTOH[2] RTOH[3] RTOH[4]	Output	156 155 154 153	The receive transport overhead bus (RTOH[4:1]) contains the receive transport overhead bytes (A1, A2, C1, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1, Z2, and E2) extracted from the incoming stream. When STS-12c (STM-4c) mode is selected, RTOH[1] contains the transport overhead from STS-3 (STM-1) #1, RTOH[2] contains the transport overhead for STS-3 (STM-1) #2, RTOH[3] contains the transport overhead for STS-3 (STM-1) #3, and RTOH[4] contains the transport overhead for STS-3 (STM-1) #4. When STS-3c (STM-1) or STS-1 mode is selected, RTOH[1] contains all the transport overhead bytes. RTOH[4:2] are not used. RTOH[4:1] is updated on the falling edge of RTOHCLK.
RTOHCLK	Output	157	The receive transport overhead clock (RTOHCLK) is nominally a 5.184 MHz clock (STS-12c/STS-3c) or a 1.728 MHz clock (STS-1) which provides timing to process the extracted receive transport overhead. When STS-12c (STM-4c) or STS-3c (STM-1) mode is selected, RTOHCLK is a gapped 6.48 MHz clock. When STS-1 mode is selected, RTOHCLK is a gapped 2.16 MHz clock. RTOHCLK is updated on the falling edge of GROCLK.

Pin Name	Type	Pin No.	Function
RTOHFP	Output	158	The receive transport overhead frame position (RTOHFP) signal is used to locate the individual receive transport overhead bits in the transport overhead bus, RTOH[4:1]. RTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH[4:1] stream. RTOHFP is updated on the falling edge of RTOHCLK.
RPOH	Output	181	The receive path overhead data (RPOH) signal contains the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4 and Z5) extracted from the received STS-12c/3c/1 frame. RPOH is updated on the falling edge of RPOHCLK.
RPOHCLK	Output	176	The receive path overhead clock (RPOHCLK) is nominally a 576 kHz clock which provides timing to process the extracted receive path overhead. RPOHCLK is a gapped 648 KHz clock. RPOHCLK is updated on the falling edge of GROCLK.
RPOHFP	Output	177	The receive path overhead frame position (RPOHFP) signal may be used to locate the individual receive path overhead bits in the path overhead data stream, RPOH. RPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK.
RSDCLK	Output	159	The receive section DCC clock (RSDCLK) is a 192 kHz clock used to update the RSD output. RSDCLK is generated by gapping a 216 kHz clock.
RSD	Output	160	The receive section DCC (RSD) signal contains the serial section data communications channel (D1, D2 D3) extracted from the incoming stream. RSD is updated on the falling edge of RSDCLK.
RLDCLK	Output	173	The receive line DCC clock (RLDCLK) is a 576 kHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.
RLD	Output	172	The receive line DCC (RLD) signal contains the serial line data communications channel (D4 - D12) extracted from the incoming stream. RLD is updated on the falling edge of RLDCLK.
ROWCLK	Output	168	The receive order wire clock (ROWCLK) is a 64 kHz clock used to update the RSOW, RSUC, and RLOW outputs. ROWCLK is generated by gapping a 72 kHz clock.
RSOW	Output	162	The receive section order wire (RSOW) signal contains the section order wire channel (E1) extracted from the incoming stream. RSOW is updated on the falling edge of ROWCLK.
RSUC	Output	161	The receive section user channel (RSUC) signal contains the section user channel (F1) extracted from the incoming stream. RSUC is updated on the falling edge of ROWCLK.
RLOW	Output	167	The receive line order wire (RLOW) signal contains the line order wire channel (E2) extracted from the incoming stream. RLOW is updated on the falling edge of ROWCLK.

Pin Name	Type	Pin No.	Function
OHFP	Output	175	The overhead frame pulse (OHFP) signal identifies the start of a byte on outputs RSOW, RSUC and RLOW. If required, OHFP is one GROCLK clock cycle wide and can be used as a reset pulse for an external counter. Please refer to the functional timing diagrams for details.
TTOH[4] TTOH[3] TTOH[2] TTOH[1]	Input	83 84 85 86	The transmit transport overhead bus (TTOH[4:1]) contains the transport overhead bytes (A1, A2, C1, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1, Z2 and E2) and error masks (H1, H2, B1 and B2) which may be inserted or used to insert bit interleaved parity errors or payload pointer bit errors into the overhead byte positions in the outgoing stream. Insertion is controlled by the TTOHEN input. When STS-12c (STM-4c) mode is selected, TTOH[1] contains the transport overhead for STS-3 (STM-1) #1. TTOH[2] contains the transport overhead for STS-3 (STM-1) #2. TTOH[3] contains the transport overhead for STS-3 (STM-1) #3. TTOH[4] contains the transport overhead for STS-3 (STM-1) #4. When STS-3c (STM-1) or STS-1 mode is selected, TTOH[1] contains all the transport overhead bytes. TTOH[4:2] are not used. The TTOH[4:1] inputs are sampled on the rising edge of TTOHCLK.
TTOHEN	Input	101	The transmit transport overhead insert enable (TTOHEN) signal, together with internal register bits, controls the source of the transport overhead data which is transmitted. While TTOHEN is high, values sampled on the TTOH[4:1] input bus are inserted into the corresponding transport overhead bit position (for the A1, A2, C1, E1, F1, D1-D3, K1, K2, H3, D4-D12, Z1, Z2 and E2 bytes). While TTOHEN is low, default values are inserted into these transport overhead bit positions. A high level on TTOHEN during the B1, B2 or H1-H2 bit positions enables an error mask. While an error mask is enabled, a high level on input TTOH causes the corresponding B1, B2 or H1-H2 bit position to be inverted. A low level on TTOH allows the corresponding bit position to pass through the S/UNI-622 uncorrupted. TTOHEN is sampled on the rising edge of TTOHCLK.
TTOHCLK	Output	99	The transmit transport overhead clock (TTOHCLK) is nominally a 5.184 MHz clock (STS-12c/STS-3c) or a 1.728 MHz clock (STS-1) clock which provides timing for upstream circuitry that sources the transport overhead stream, TTOH[4:1]. When STS-12c (STM-4c) or STS-3c (STM-1) mode is selected, TTOHCLK is a gapped 6.48 MHz clock. When STS-1 mode is selected, TTOHCLK is a gapped 2.16 MHz clock. TTOHCLK is updated in the rising edge of TCLK.
TTOHFP	Output	100	The transmit transport overhead frame position (TTOHFP) signal is used to locate the individual transport overhead bits in the transport overhead bus, TTOH[4:1]. TTOHFP is set high while bit 1 (the most significant bit) of the first framing byte (A1) is expected in the incoming stream. TTOHFP is updated on the falling edge of TTOHCLK.

Pin Name	Type	Pin No.	Function
TPOH	Input	82	The transmit path overhead data (TPOH) signal contains the path overhead bytes (J1, C2, G1, F2, Z3, Z4 and Z5) and error masks (B3 and H4) which may be inserted or used to insert path BIP-8 or multiframe bit errors into the path overhead byte positions in the STS-12c/3c/1 stream. Insertion is controlled by the TPOHEN input, or by bits in internal registers. TPOH is sampled on the rising edge of TPOHCLK.
TPOHEN	Input	77	The transmit path overhead insert enable (TPOHEN) signal, together with internal register bits, controls the source of the path overhead data which is inserted in the POUT[7:0] stream. While TPOHEN is high, values sampled on the TPOH input are inserted into the corresponding path overhead bit position (for the J1, C2, G1, F2, Z3, Z4 and Z5 bytes). While TPOHEN is low, values obtained from internal registers are inserted into these path overhead bit positions. A high level on TPOHEN during the H4 or B3 bit positions enables an error mask. While an error mask is enabled, a high level on input TPOH causes the corresponding B3 or H4 bit position to be inverted. A low level on TPOH allows the corresponding bit position to pass through the S/UNI-622 uncorrupted. TPOHEN is sampled on the rising edge of TPOHCLK.
TPOHCLK	Output	75	The transmit path overhead clock (TPOHCLK) is nominally a 576 kHz clock which provides timing for upstream circuitry that sources the path overhead stream, TPOH. TPOHCLK is a gapped 810 kHz clock. TPOHCLK is updated in the falling edge of GROCLK.
TPOHFP	Output	76	The transmit path overhead frame position (TPOHFP) signal may be used to locate the individual path overhead bits in the path overhead data stream, TPOH. TPOHFP is logic one while bit 1 (the most significant bit) of the path trace byte (J1) is expected in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
TOWCLK	Output	95	The transmit order wire clock (TOWCLK) is a 64 kHz clock used to sample the TSOW, TSUC, and TLOW inputs. TOWCLK is generated by gapping a 72 kHz clock.
TSOW	Input	94	The transmit section order wire (TSOW) signal contains the section order wire channel (E1) inserted into the outgoing stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH[1] and TTOHEN takes precedence over overhead sourced using TSOW. TSOW is sampled on the rising edge of TOWCLK.
TSUC	Input	93	The transmit section user channel (TSUC) signal contains the section user channel (F1) inserted into the outgoing stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH[1] and TTOHEN takes precedence over overhead sourced using TSUC. TSUC is sampled on the rising edge of TOWCLK.

Pin Name	Type	Pin No.	Function
TLOW	Input	92	The transmit line order wire (TLOW) signal contains the line order wire channel (E2) inserted into the outgoing stream. When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH[1] and TTOHEN takes precedence over overhead sourced using TLOW. TLOW is updated on the rising edge of TOWCLK.
TSDCLK	Output	102	The transmit section DCC clock (TSDCLK) is a 192 kHz clock used to sample the TSD input. TSDCLK is generated by gapping a 216 kHz clock.
TSD	Input	103	The transmit section DCC (TSD) signal contains the serial section data communications channel (D1, D2 D3). When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH[1] and TTOHEN takes precedence over overhead sourced using TSD. TSD is sampled on the rising edge of TSDCLK.
TLDCLK	Output	90	The transmit line DCC clock (TLDCLK) is a 576 kHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
TLD	Input	91	The transmit line DCC (TLD) signal contains the serial line data communications channel (D4 - D12). When not used, this input should be connected to logic zero. Overhead sourced using inputs TTOH[1] and TTOHEN takes precedence over overhead sourced using TLD. TLD is sampled on the rising edge of TLDCLK.
RCP	Output	187	The receive cell pulse (RCP) signal marks the most significant bit (MSB) of a cell header's GFC field on output, RGFC. RCP is updated on the falling edge of GROCLK.
RGFC	Output	193	The receive generic flow control (RGFC) signal contains the serialized GFC field extracted from receive cells. The GFC field is output MSB first. The RCP output identifies the MSB of every GFC field. The GFC Control register can be used to gate off individual GFC bits. When the S/UNI-622 is in the OCD state, RGFC is forced low. RGFC is updated on the falling edge of GROCLK.
TCP	Output	68	The transmit cell pulse (TCP) signal is provided to locate the most significant GFC bit (GFC[3]) of a cell's GFC field sourced on input TGFC. TCP pulses high for one GTOCLK period to identify the GTOCLK cycle before the cycle the GFC[3] bit is output on TGFC. TCP is updated on the falling edge of GTOCLK.
TGFC	Input	62	The transmit generic flow control (TGFC) input contains GFC bits that can be inserted into the GFC fields of transmitted cells (including idle/unassigned cells). Insertion is controlled using bits in the TACP Fixed Stuff/GFC register. TGFC is sampled on the rising edge of GTOCLK.

Pin Name	Type	Pin No.	Function
POP[5] POP[4] POP[3] POP[2] POP[1] POP[0]	Output	130 131 132 133 134 135	The parallel output port (POP[5:0]) is used to control the operation of front end line devices. The signal levels on this parallel output port correspond to the bit values contained in the S/UNI-622 Parallel Output Port Register.
PIP[3] PIP[2] PIP[1] PIP[0]	Input	105 106 107 108	The parallel input port (PIP[3:0]) is used to monitor the operation of front end line devices. An interrupt may be generated when state changes are detected on the monitored signals. State changes and the real-time signal levels on this port are available via the S/UNI-622 Parallel Input Port register.
CSB	Input	36	The active-low chip select (CSB) signal is low during S/UNI-622 register accesses. Note that when not being used, CSB must be tied high. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	38	The active-low read enable (RDB) signal is low during S/UNI-622 register read accesses. The S/UNI-622 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	37	The active-low write strobe (WRB) signal is low during a S/UNI-622 register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	23 24 25 26 31 32 33 34	The bidirectional data bus D[7:0] is used during S/UNI-622 register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6]	Input	15 16 17 18 19 20 21	The address bus A[7:0] selects specific registers during S/UNI-622 register accesses.

Pin Name	Type	Pin No.	Function
A[7]/TRS		22	The test register select (TRS) signal selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
RSTB	Input	35	The active-low reset (RSTB) signal provides an asynchronous S/UNI-622 reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
ALE	Input	14	The address latch enable (ALE) is active-high and latches the address bus A[7:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-622 to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	OD Output	39	The active-low interrupt (INTB) signal goes low when a S/UNI-622 interrupt source is active and that source is unmasked. The S/UNI-622 may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication detect and others. INTB is tristated when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
TCK	Input	70	The test clock (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	126	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	127	The test data input (TDI) signal carries test data into the S/UNI-622 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	71	The test data output (TDO) signal carries test data out of the S/UNI-622 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.
TRSTB	Input	125	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-622 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB must be connected to the RSTB input.
BUS8	Input	69	This pin must be connected to GND for proper operation of the S/UNI-622

Pin Name	Type	Pin No.	Function
VDD_AC1	Power	10	The AC power (VDD_AC1 - VDD_AC7) pins should be connected to a well-decoupled +5 V DC supply in common with VDD_DC.
VDD_AC2		27	
VDD_AC3		81	
VDD_AC4		120	
VDD_AC5		152	
VDD_AC6		183	
VDD_AC7		205	
VSS_AC1	Ground	13	The AC ground (VSS_AC1 - VSS_AC7) pins should be connected to GND in common with VSS_DC.
VSS_AC2		30	
VSS_AC3		78	
VSS_AC4		117	
VSS_AC5		151	
VSS_AC6		184	
VSS_AC7		208	
VDD_DC1	Power	11	The DC power (VDD_DC1 - VDD_DC14) pins should be connected to a well-decoupled +5 V DC supply in common with VDD_AC.
VDD_DC2		28	
VDD_DC3		40	
VDD_DC4		66	
VDD_DC5		80	
VDD_DC6		98	
VDD_DC7		110	
VDD_DC8		119	
VDD_DC9		129	
VDD_DC10		138	
VDD_DC11		165	
VDD_DC12		179	
VDD_DC13		189	
VDD_DC14		206	

Pin Name	Type	Pin No.	Function
VSS_DC1	Ground	12	The DC ground (VSS_DC1 - VSS_DC14) pins should be connected to GND in common with VSS_AC.
VSS_DC2		29	
VSS_DC3		41	
VSS_DC4		64	
VSS_DC5		79	
VSS_DC6		96	
VSS_DC7		109	
VSS_DC8		118	
VSS_DC9		128	
VSS_DC10		136	
VSS_DC11		166	
VSS_DC12		180	
VSS_DC13		191	
VSS_DC14		207	

Notes on Pin Description:

1. All S/UNI-622 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

2. All S/UNI-622 outputs and bidirectionals have at least 2 mA drive capability. The data bus outputs, D[7:0], have 4 mA drive capability. The FIFO interface outputs, RDAT[15:0], RXPRTY[1:0], RCA, RSOC, and TCA, have 4 mA drive capability. Outputs POUT[7:0], FPOUT, TSOUT, GTOCLK and GROCLK also have 4 mA drive capability

3. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.

4. The VSS_DC and VSS_AC ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-622.

5. The VDD_DC and VDD_AC power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-622.

9 FUNCTIONAL DESCRIPTION

9.1 Receive Section Overhead Processor

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. In addition, it extracts the section orderwire channel, the section user channel, the section data communication channel from the section overhead and provides them serially on outputs RSOW, RSUC and RSD, respectively. The RSOP is intended to operate with an upstream device which performs clock and data recovery, deserialization and preframing (to the A1 and A2 framing bytes).

9.1.1 Framer

The Framer Block determines the in-frame/out-of-frame status of the STS-12c/3c/1 data stream. Output OOF reflects this status, and is updated with timing aligned to PICLK.

While out of frame, upstream circuitry monitors the bit-serial STS-12c/3c/1 data stream for an occurrence of the framing pattern (A1, A2). The upstream circuitry is expected to pulse input FPIN when a framing pattern has been detected to reinitializes the channel counter to the new alignment. The Framer block declares frame alignment when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the first A2 byte are seen error-free depending upon the selected framing algorithm. The first algorithm examines 24, 6 or 2 bytes depending on the mode, while the second algorithm examines only the first occurrence of A1 and the first four bits of the first occurrence of A2 in the sequence regardless of the mode. Once in frame, the Framer block monitors the framing pattern sequence and declares OOF when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes are examined for bit errors each frame, or only the first A1 byte and the first four bits of the first A2 byte are examined for bit errors each frame.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment, the performance of each algorithm is dominated by the alignment algorithm used by the upstream circuitry. Once in frame alignment, the Framer block continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} bit error rate (BER), the first algorithm provides a mean time between OOF occurrences of 4 minutes for STS-1 mode, 14 seconds for STS-3c (STM-1) mode and 0.13 seconds for

STS-12c (STM-4c) mode. The second algorithm provides a mean time between OOF occurrences of 103 minutes independent of operating mode.

9.1.2 Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the received byte-serial stream. The generating polynomial is $1 + x^6 + x^7$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the identity bytes (C1) are not descrambled. A register bit is provided to disable the descrambling operation.

9.1.3 Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-12c/3c/1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without losing any events. It is intended that this counter be polled at least once per second so that bit error events are not missed.

9.1.4 Loss of Signal

The Loss of Signal Block monitors the scrambled data of the complete STS-12c/3c/1 stream for the absence of ones. When 20 ± 3 µs of all zeros patterns is detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. LOS is updated with timing aligned to PICLK.

9.1.5 Loss of Frame

The Loss of Frame Block monitors the in-frame/out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. To provide for intermittent out-of-frame conditions, the 3 ms

timer is not reset to zero until an in-frame condition persists for 3 ms. The loss of frame is cleared when an in-frame condition persists for a period of 3 ms. LOF indication is updated with timing aligned to PICLK.

9.2 Receive Line Overhead Processor

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring. In addition, it extracts the line orderwire channel and the line data communication channel from the line overhead and provides them serially on outputs RLOW and RLD respectively.

9.2.1 Line RDI Detect

The LRDI Detect Block detects the presence of line remote defect indications in the STS-12c/3c/1 stream. Output LRDI is asserted when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames. LRDI is updated with timing aligned to PICLK.

9.2.2 Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (AIS) in the STS-12c/3c/1 stream. Output LAIS is asserted when a 111 binary pattern is detected in bits 6, 7 8 of the K2 byte for five consecutive frames. LAIS is removed when any pattern other than 111 is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames. LAIS is updated with timing aligned to PICLK.

9.2.3 Automatic Protection Switch Control Block

The Automatic Protection Switch Control (APSC) Block filters and captures the receive automatic protection switch channel bytes (K1 and K2) and allows them to be read via the S/UNI-622 Receive K1 Register and the S/UNI-622 Receive K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received in which no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the S/UNI-622 Receive K1 Register and the S/UNI-622 Receive K2 Register.

9.2.4 Error Monitor

The Error Monitor Block calculates the received line BIP error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-12c/3c/1 stream. The line BIP code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP code extracted from the STS-12c/3c/1 of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 768000 (12 x 8 x 8000) bit errors can be detected per second.

The Error Monitor Block accumulates these line layer bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note that this counter should be polled at least once per second to avoid saturation which in turn may result in missed bit error events.

The Error Monitor Block also accumulates line far end block error indications (contained in the Z2 byte).

9.3 Byte Interleaved Demultiplexer

The Byte Interleaved Demultiplexer block (BIDX) is only active when STS-12c (STM-4c) mode is selected. It performs a 1:4 byte-serial to word- (four byte) serial demultiplexing function on the incoming byte-serial STS-12c data stream. The demultiplexed streams with a divide-by-four clock are made available to downstream blocks for lower rate processing.

9.4 Transport Overhead Extract Port

The Transport Overhead Extract Port (also known as the Receive Transport Overhead Access Port, RTOP) extracts the entire receive transport overhead on the RTOH[4:1] bus for optional external processing. Output RTOHFP is provided to identify the most significant bit of the A1 framing bytes on RTOH[4:1]. The transport overhead clock, RTOHCLK is nominally a 5.184 MHz (STS-12c, STS-3c modes) or a 1.728 MHz (STS-1 mode) clock. RTOH[4:1] and RTOHFP are updated with timing aligned to RTOHCLK.

9.5 Receive Path Overhead Processor

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, and path level alarm indication. In conjunction with the Receive Concatenation Processor (RCOP) sub block, the RPOP also

identifies the synchronous payload envelope and monitors the performance of the STS-12c/3c/1 line.

9.5.1 Pointer Interpreter

The Pointer Interpreter Block interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-12c/3c/1 stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown in Figure 6:

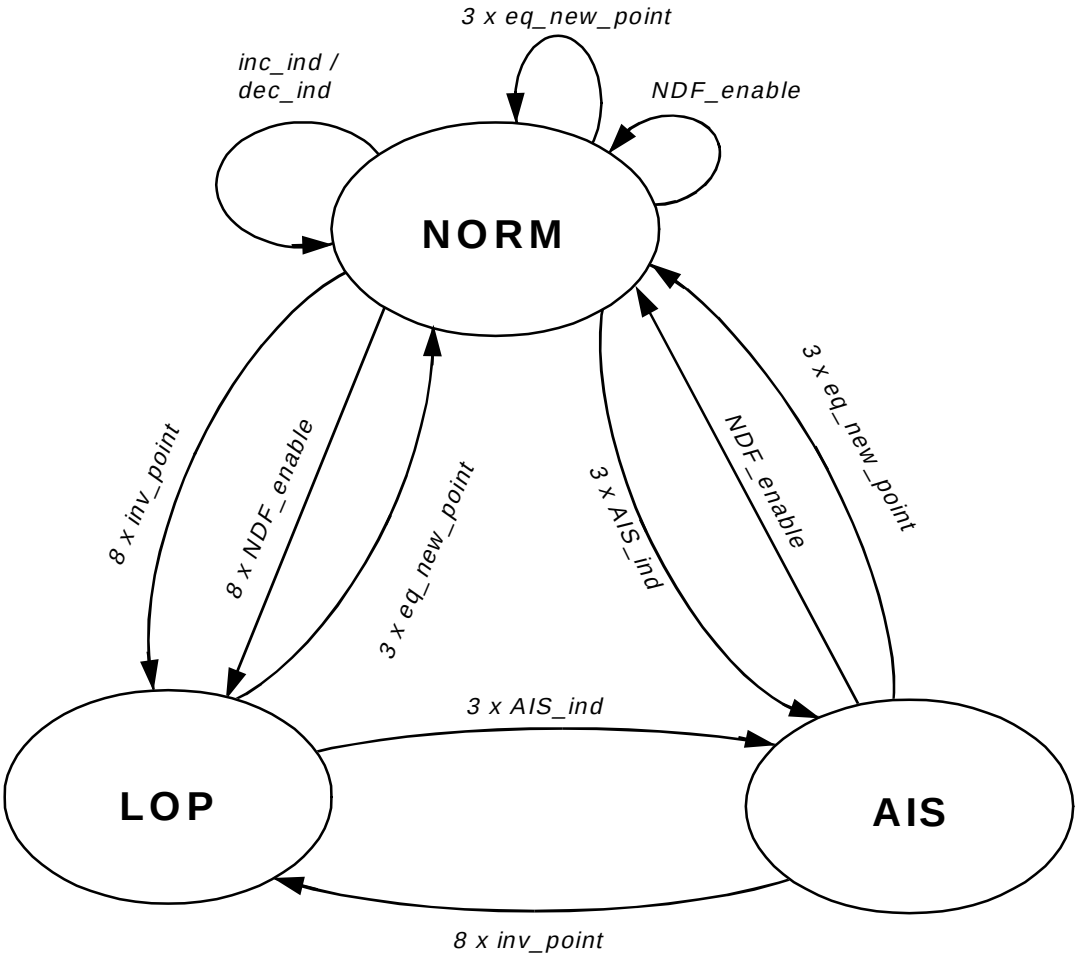
NORM_state (NORM)

AIS_state (AIS)

LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behaviour is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 6 - Pointer Interpretation State Diagram



The following events (indications) are defined

norm_point:	disabled NDF + ss + offset value equal to active offset
NDF_enable:	enabled NDF + ss + offset value in range of 0 to 782
AIS_ind:	H1 = 'hFF, H2 = 'hFF
inc_ind:	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago

dec_ind:	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
inv_point:	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point:	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset.
Note 1.-	active offset is defined as the accepted current phase of the SPE in the NORM_state and is undefined in the other states.
Note 2 -	enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.
Note 3 -	disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.
Note 4 -	the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_point indication.
Note 5 -	ss bits are unspecified in SONET and has bit pattern 10 in SDH
Note 6 -	the use of ss bits in definition of indications may be optionally disabled.
Note 7 -	the requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
Note 8 -	new_point is also an inv_point.

The transitions indicated in the state diagram are defined as follows:

inc_ind/dec_ind:	offset adjustment (increment or decrement indication)
3 x eq_new_point:	three consecutive equal new_point indications
NDF_enable:	single NDF_enable indication
3 x AIS_ind:	three consecutive AIS indications

8 x inv_point:	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications
Note 1 -	the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
Note 2 -	3 x new_point takes precedence over 8 x inv_point.
Note 3 -	all three offset values received in 3 x eq_new_point must be identical.
Note 4 -	"consecutive event counters" are reset to zero on a change of state.

The Pointer Interpreter Block detects loss of pointer (LOP) in the incoming STS-12c/3c/1 stream. LOP is declared (LOP output set high) on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. LOP is removed (LOP output set low) when the same valid pointer with normal NDF is detected for three consecutive frames. Incoming STS Path AIS (pointer bytes set to all ones) does not cause entry into the LOP state.

The Pointer Interpreter Block detects path AIS in the incoming STS-12c/3c/1 stream. PAIS is declared (PAIS output set high) on entry to the AIS_state after three consecutive AIS indications. PAIS is removed (PAIS set low) when the same valid pointer with normal NDF is detected for three consecutive frames or when a valid pointer with NDF enabled is detected.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The pointer value is used to extract the path overhead from the incoming stream. The current pointer value can be read from an internal register.

The ATM Forum 622.08 Mbps Physical Layer Specification states that the receiving equipment supporting the private/public UNI or the private NNI shall check for the concatenation indication when interpreting the pointer as specified in ANSI T1.105 and ITU G.709. T1.105 requires that one monitor the concatenation indication bytes H1* and H2* but does not specify any action when an error occurs. Hence the S/UNI-622 is compatible with the ANSI T1.105 concatenation indication specification. ITU G.709 refers one to ITU G.783. The G.783 document defines, in Annex B, a state diagram, illustrated below, for the interpretation of the concatenation pointers H1* and H2*. This functionality is not contained in the S/UNI-622 but can be realized externally as illustrated in Figure 8.

Figure 7 - ITU G.783 Concatenation Indicator State Diagram

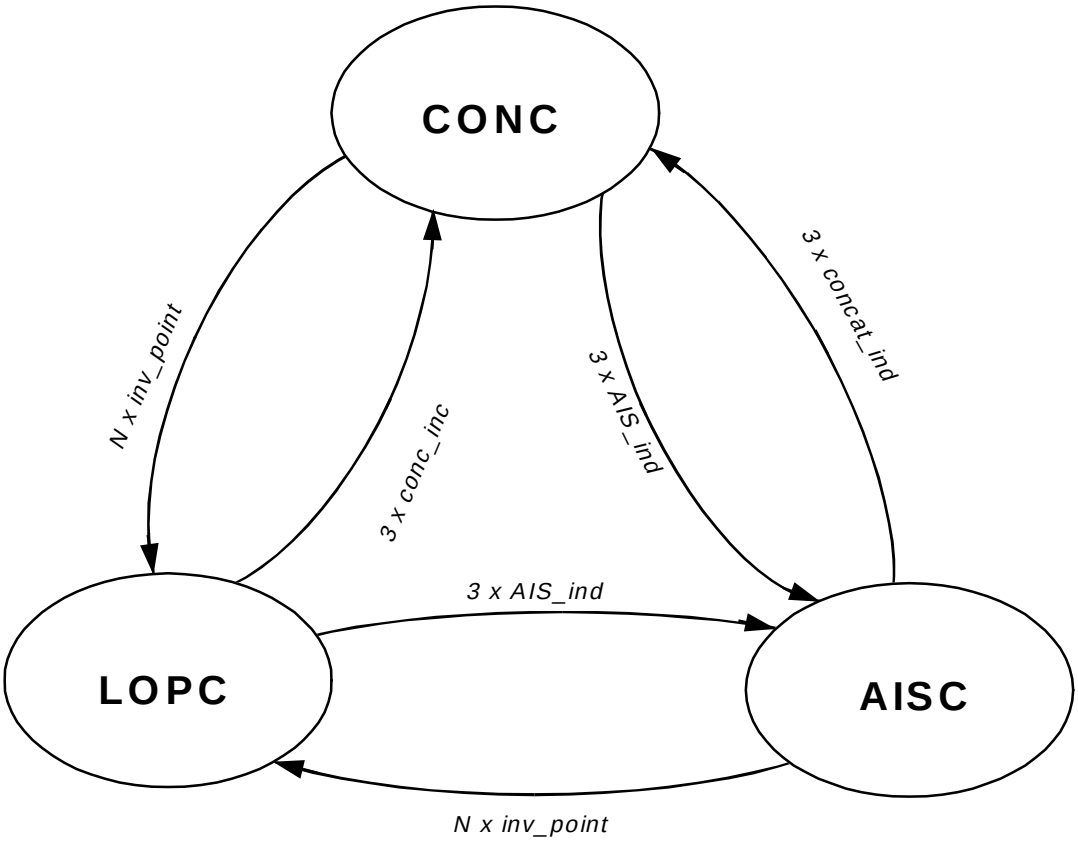
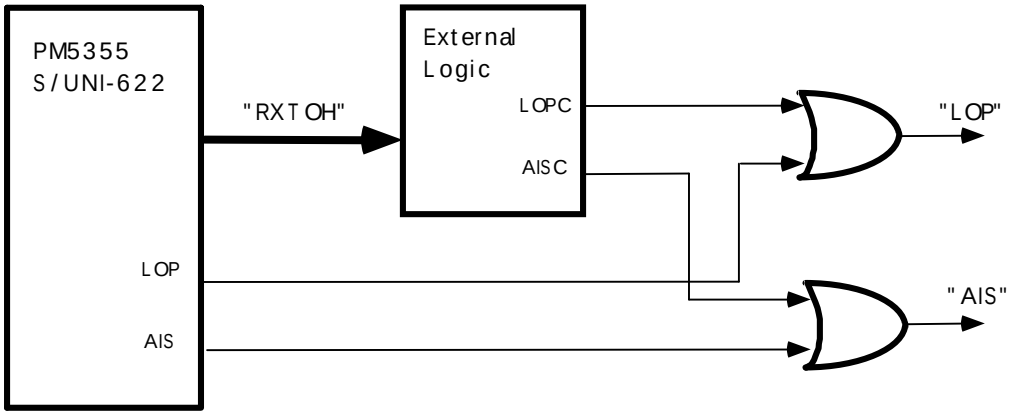


Figure 8 - ITU G.783 Concatenation Indicator Implementation



9.5.2 SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free-running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell payload.

9.5.3 Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBEs). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame. The RPOP block performs the BIP-8 calculation over the STS-3c #1 portion of the SPE while the RCOP sub block performs the calculation over the remaining STS-3c #2, #3 and #4 portions of the SPE. The two calculations are combined by the RPOP to form the final BIP-8 code.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0 (0000B) and 8 (1000B), representing zero to eight errors. Any other value is interpreted as zero errors.

The path remote defect indication is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five (or ten) consecutive frames. PRDI is set low when bit 5 is low for five (or ten) consecutive frames. PRDI is updated with timing aligned to GROCLK.

9.6 Path Overhead Extract

The Path Overhead Extract Block uses timing information from the SPE Timing block to extract, serialize and output the Path Overhead bytes on output RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) on RPOH. The path overhead clock, RPOHCLK is nominally a 576 kHz clock. RPOH and RPOHFP are updated with timing aligned to RPOHCLK.

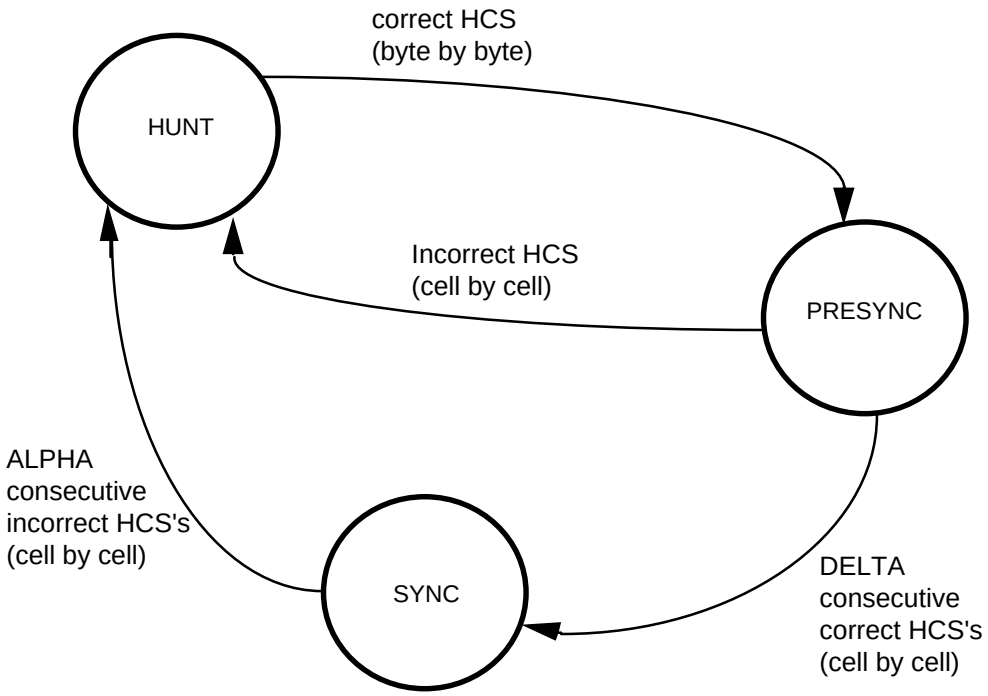
9.7 Receive ATM Cell Processor

The Receive ATM Cell Processor (RACP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RACP also provides a four-cell deep receive FIFO. This FIFO is used to separate the STS-12c/3c/1 line timing from the higher layer ATM system timing. The cells are passed in a twenty-seven word cell structure where a word is sixteen bits.

9.7.1 Cell Delineation

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells must be byte aligned before insertion in the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates one by one to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks onto the particular cell boundary and enters the PRESYNC state. This state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which point a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 9.

Figure 9 - Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is 7, and DELTA is 6. These values result in a maximum average time to delineate of 8 µs.

9.7.2 Descrambler

The self synchronous descrambler operates on the 48-byte cell payload only. The circuitry descrambles the information field using the polynomial $x^{43} + 1$. The descrambler is disabled for the duration of the header and HCS fields, and may optionally be disabled.

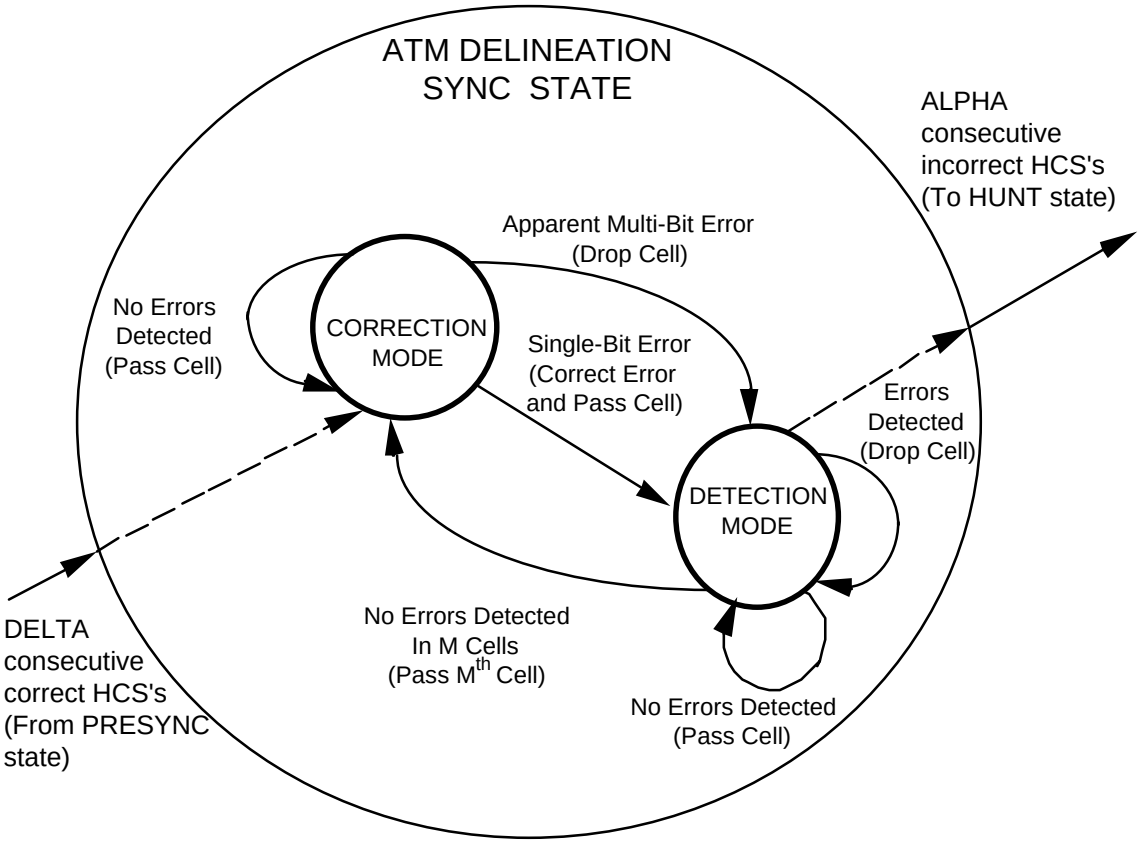
9.7.3 Cell Filter and HCS Verification

Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RACP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the

corrected header contents match the pattern contained in the RACP Match Header Pattern and RACP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RACP Match Header Pattern and RACP Match Header Mask registers. Idle/Unassigned cells are assumed to contain the all-zeros pattern in the VCI and VPI fields. The RACP Match Header Pattern and RACP Match Header Mask registers allow filtering control over the contents of the GFC, PTI and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RACP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine (described above) is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 10:

Figure 10 - HCS Verification State Diagram



In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single- bit error or a multi-bit error, the state machine transitions to the 'Detection Mode' state. In this state, programmable HCS error filtering is provided. The detection of any HCS error causes the corresponding cell to be dropped. The state machine transitions back to the 'Correction Mode' state when M (where M = 1, 2, 4, 8) cells are received with correct HCSs. The M^{th} cell is not discarded.

9.7.4 Performance Monitor

The Performance Monitor consists of two 12-bit saturating HCS error event counters. One of the counters accumulates correctable HCS errors which are single-bit HCS errors detected while the HCS Verification state machine is in the 'Correction Mode' state described above. The second counter accumulates uncorrectable HCS errors which are HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or multiple bit HCS errors detected while the state machine is in the 'Correction Mode' state as described above.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without the loss of any events. It is intended that the counter be polled at least once per second so as not to miss HCS error events.

9.7.5 GFC Extraction Port

The GFC Extraction Port outputs the received GFC bits in a serial stream. The four GFC bits are presented for each received cell, with the RCP output indicating the position of the most significant bit. Individual GFC bits may be masked through an internal register from appearing on the RGFC output. The serial output is forced low when an uncorrected cell is received or if cell delineation is lost.

9.7.6 Receive FIFO

The Receive FIFO provides FIFO management and the asynchronous interface between the S/UNI-622 device and the external environment. The receive FIFO can accommodate four cells. The receive FIFO provides for the separation of the STS-12c/3c/1 line or physical layer timing from the ATM layer timing.

The FIFO supports a data structure consists of twenty-seven 16-bit words consisting of the 5-octet cell header and the 48-octet payload (the HCS byte, along with the header status octet, is passed in this structure). Note that depending on the selected cell filtering options, the header status may be an 1) error-free header, 2) errored and corrected header, or 3) errored and uncorrectable header.

Management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions. Upon detection of an overrun, the FIFO is automatically reset. Up to four cells may be lost during the FIFO reset operation. Upon detection of an underrun, the offending read is ignored. FIFO overruns are indicated through a maskable interrupt and register bits. The FIFO interface provided to the system is a synchronous interface emulating commercial synchronous FIFOs. All receive FIFO signals, RSOC, RRDENB, RCA, RXPRTY[1:0] and RDAT[15:0] are either sampled or updated on the rising edge of the RFCLK clock input.

9.8 Transmit Section Overhead Processor

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion. It presents a STS-12c/3c/1 data stream in byte-serial format at 77.76-Mbyte/s to an off-chip serializer for transmission at the bit-serial rate.

9.8.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame, except for the section overhead, being set to one before scrambling. The Line AIS Insert Block substitutes all ones when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation and deactivation of line AIS insertion is synchronized to frame boundaries.

9.8.2 BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the unscrambled STS-12c/3c/1 stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-12c/3c/1 frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. Details are provided in the

references. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.8.3 Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and identity bytes (C1) into the STS-12c/3c/1 frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

9.8.4 Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit serial stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $1 + x^6 + x^7$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled.

The POUT[7:0] outputs are provided by the Scrambler Block and are updated with timing aligned to TCLK. It also provides the FPOUT signal. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

9.9 Transmit Line Overhead Processor

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion and line BIP-96/24/8 insertion (B2).

9.9.1 APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into STS-1 #1 of the STS-12c/3c/1 stream when enabled by an internal register.

9.9.2 Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-96/24/8 error detection code (B2) based on the line overhead and synchronous payload envelope of the STS-12c/3c/1 stream. The line BIP-96/24/8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-96/24/8 code is inserted into the B2 byte positions of the following frame. BIP-96/24/8 errors may be continuously inserted under register control for diagnostic purposes.

9.9.3 Line RDI Insert

The Line RDI Insert Block multiplexes the line overhead bytes into the STS-12c/3c/1 output stream and optionally inserts line RDI. Line RDI is inserted by this block when enabled via the TLRDI input or through register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7 and 8 of the K2 byte contained in the STS-12c/3c/1 stream.

9.9.4 Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-96/24/8 errors (Z2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

9.10 Byte Interleaved Multiplexer

The Byte Interleaved Multiplexer block (BIMX) is only active when STS-12c (STM-4c) mode is selected. It performs a 4:1 (32-bit word to byte) multiplexing function on the incoming word serial stream from the Transmit Path Overhead Processor (TPOP) block. The resulting multiplexed byte-serial stream is passed to the Transmit Line Overhead Processor from which the line overhead (multiplexer section) is added to the stream.

A generated transmit clock (GTOCLK) is provided for general use. GTOCLK is the supplied transmit clock, TCLK, divided down by four.

9.11 Transport Overhead Insert Port

The Transport Overhead Insert Port (also known as the Transmit Transport Overhead Access Port, TTOP) allows the complete transport overhead to be inserted using the TTOH[4:1] bus, along with the transport overhead clock, TTOHCLK, and the transport overhead frame position, TTOHFP. The transport overhead clock, TTOHCLK, is nominally a 5.184 MHz (STS-12c and STS-3c modes) or a 1.728 MHz (STS-1 mode) clock. The transport overhead enable signal, TTOHEN, controls the insertion of transport overhead from the TTOH[4:1] bus. When configured for STS-3c (STM-1) or STS-1 mode, only TTOH[1] is required.

The state of the TTOHEN input determines whether the data sampled on TTOH[4:1], or the default overhead byte values (shown in Figure 8) are inserted in the STS-12c/3c/1 stream. For example, when configured for STS-12c (STM-4c) mode, a high level on TTOHEN during the section user channel (F1) bit positions causes the eight values shifted in on each of the TTOH inputs to be

inserted into the four F1 byte position in the STS-12c stream. A low level on TTOHEN during the section user channel bit positions causes the default value (00H) to be inserted in the STS-12c stream. Other combinations are also possible.

During the H1, H2, B1 and B2 byte positions in the TTOH[4:1] streams, a high level on TTOHEN enables an error insertion mask. While an error mask is enabled, a high level on inputs TTOH[4:1] causes the corresponding bits in the H1, H2, B1 or B2 byte to be inverted. A low level on inputs TTOH[4:1] causes the corresponding bits in the B1 or B2 byte to pass through the S/UNI-622 unmodified.

Figure 11 - STS-12c (STM-4c) Default Transport Overhead Values

A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A1 (F6)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	A2 (28)	C1 (*)	C1 (02)	C1 (03)	C1 (04)	C1 (05)	C1 (06)	C1 (07)	C1 (08)	C1 (09)	C1 (0A)	C1 (0B)	C1 (0C)
B1 (*)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	E1 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	F1 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
D1 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D2 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D3 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
H1 (62)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H1 (93)	H2 (08)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H2 (FF)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)	H3 (00)
B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	B2 (**)	K1 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	K2 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
D4 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D5 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D6 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
D7 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D8 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D9 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
D10 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D11 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	D12 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)
Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z1 (00)	Z2 (***)	Z2 (00)	Z2 (***)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	Z2 (00)	E2 (00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)

* : C1 value defaults to 01 but can be programmed to to be the 16 or 64 byte section trace message.
** : B1, B2 values depend on payload contents
***: Z2 value depends on incoming line bit errors. When not configured for STS-1, the first Z2 byte has a default value of 00.

9.12 Transmit Path Overhead Processor

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals. In conjunction with the Transmit Concatenation Processor (TCOP), the TPOP also provides for insertion of the synchronous payload envelope and path BIP-8 (B3) insertion.

9.12.1 Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2). The block contains a free-running timeslot counter that locates the start of the synchronous payload envelope based on the generated pointer value and the SONET/SDH frame alignment.

The Pointer Generator Block generates the outgoing pointer as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second through twelfth pointer bytes. Rules 1 - 4 apply to the first pointer bytes of the STS-12c/3c/1 stream:

1. A "normal pointer value" locates the start of the SPE. Note: $0 \leq$ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

2. Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

3. Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

4. Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position, the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the incoming stream. The current pointer value may be read via internal registers.

9.12.2 BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the STS-3c #1 portion of the outgoing STS-12c/3c/1 SPE stream. The TCOP sub block performs the calculation over the remaining STS-3c #2, #3 and #4 portions of the SPE. The resulting parity bytes are combined and inserted into the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

9.12.3 FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. The asynchronous nature of these signals implies that more than eight FEBE events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining FEBEs are transmitted at the next opportunity. Far end block errors may be inserted under register control for diagnostic purposes.

9.12.4 SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the STS-12c/3c/1 stream.

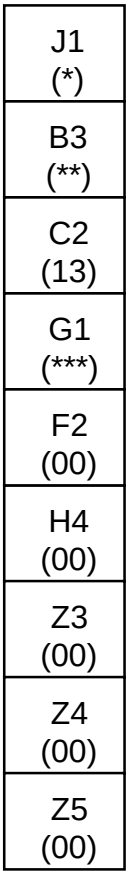
9.13 Path Overhead Insert

The Path Overhead Insert Block provides a bit-serial path overhead interface to the TPOP. Any, or all, of the path overhead bytes may be sourced from, or modified by, the bit-serial path overhead stream, TPOH. The individual bits of each path overhead byte are shifted in using the TPOHCLK output. The TPOHFP output is provided to identify when the most significant bit of the Path Trace byte is expected on TPOH. The state of the TPOHEN input, together with an internal register, determines whether the data sampled on TPOH, or the default path overhead byte values (shown in the table below) are inserted in the STS-12c/3c/1 stream. For example, a high level on TPOHEN during the path signal label (C2) bit positions causes the eight values shifted in on TPOH to be inserted in the C2 byte position in the STS-12c/3c/1 stream. A low level on TPOHEN during the path trace bit positions causes the default value (00H) to be inserted in the STS-12c/3c/1 stream. Other combinations are also possible.

Note, for the J1 byte, insertion can also be sourced from the SPTB block. J1 byte insertion via the TPOHEN input takes precedence over insertion via the SPTB block, which in turn takes precedence over insertion via the internal register source.

During the B3 and H4 byte positions in the TPOH stream, a high level on TPOHEN enables an error insertion mask. While the error mask is enabled, a high level on input TPOH causes the corresponding bit in the B3 or H4 byte to be inverted. A low level on TPOH causes the corresponding bit in the B3 or H4 byte to pass through the TPOP unmodified.

Figure 12 - Default Path Overhead Values



* J1 value defaults to 00H but can be programmed to be the 16 or 64 byte path trace message.
** B3 value depend on payload contents.
*** G1 value depends on incoming path bit errors.

9.14 Transmit ATM Cell Processor

The Transmit ATM Cell Processor (TACP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TACP contains a four-cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

9.14.1 Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

9.14.2 Scrambler

The Scrambler scrambles the 48-octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler described in the references. The cell headers are transmitted unscrambled, and the scrambler may optionally be completely disabled.

9.14.3 HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1 is used. The coset polynomial, $x^6+x^4+x^2+1$ is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

9.14.4 GFC Insertion Port

The GFC Insertion Port provides the ability to insert the GFC value downstream of the FIFO. The four GFC bits are received on a serial stream that is synchronized to the transmit cell by a framing pulse. The GFC enable register bits control the insertion of each serial bit. If the enable is cleared, the default GFC value is inserted. For idle/unassigned cells, the default is the contents of the TACP Idle/Unassigned Cell Header Control register. For assigned cells, the default is the value written with the cell into the transmit FIFO.

9.14.5 Transmit FIFO

The Transmit FIFO provides FIFO management and the asynchronous interface between the S/UNI-622 device and the external environment. The transmit FIFO can accommodate four cells. It provides for the separation of the STS-12c/3c/1 line or physical layer timing from the ATM layer timing.

The FIFO supports a data structure consists of twenty-seven 16-bit words consisting of the 5-octet cell header and the 48-octet payload (the HCS byte, along with the header error insertion control, is passed in this structure). Note that the header error insertion control allows the programmable insertion of one or more bit errors in the HCS octet.

Management functions include filling the transmit FIFO, indicating when cells are available to be written to the transmit FIFO, maintaining the transmit FIFO read and write pointers, and detecting a FIFO overrun condition. The FIFO depth can be programmed to be from one to four cells deep. When configured for a depth of four cells, the TCA output signal transitions low to indicate a full FIFO when the FIFO contains four cells. To obtain maximum throughput with minimum FIFO latency, the FIFO level should be programmed to three cells. Note that a cell is not transmitted until the entire cell has been written into the FIFO.

When the FIFO is full and the upstream device writes into the FIFO, the TACP-622 indicates a FIFO overrun condition using a maskable interrupt and register bits. The offending write and all subsequent writes are ignored until there is room in the FIFO.

The FIFO interface provided to the system is a synchronous interface emulating commercial synchronous FIFOs. All transmit FIFO signals, TSOC, TWRENB, TCA, TXPRTY[1:0] and TDAT[15:0] are either sampled or updated on the rising edge of the TFCLK clock input.

9.15 SONET/SDH Section and Path Trace Buffers

The SONET/SDH Section Trace Buffer (SSTB) block and the SONET/SDH Path Trace Buffer (SPTB) block are identical. The blocks can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. The generic SONET/SDH Trace Buffer (STB) block is described below.

9.15.1 Receive Trace Buffer (RTB)

The RTB consists of two parts: the Trace Message Receiver and the Overhead Byte Receiver.

Trace Message Receiver:

The Trace Message Receiver (TMR) processes the trace message, and consists of three sub-processes: Framer, Persistency, and Compare.

Framer:

The TMR handles the incoming 16-byte message by synchronizing to the byte with the most significant bit set high, and places that byte in the first location in the capture page of the internal RAM. In the case of the 64-byte message, the TMR synchronizes to the trailing carriage return (0x0D), line feed (0x0A) sequence and places the next byte in the first location in the capture page of the internal RAM. The Framer block maintains an internal representation of the resulting 16-byte or 64-byte "frame" cycle. If the phase of the start of frame shifts, the framer adjusts accordingly and resets the persistency counter and increments the unstable counter.

Frame synchronization may be disabled, in which case the RAM acts as a circular buffer.

Persistency:

The Persistency process checks for repeated reception of the same 16-byte or 64-byte trace message. An unstable counter is incremented for each message that differs from the previous received message. For example, a single corrupted message in a field of constant messages causes the unstable count to increment twice, once on receipt of the corrupted message, and again on the next (uncorrupted) message. A section/path trace message unstable alarm is declared when the count reaches eight.

The persistency counter is reset to zero, the unstable alarm is removed, and the trace message is accepted when the same 16-byte or 64-byte message is received three or five times consecutively (as determined by an internal register bit). The accepted message is passed to the Compare process for comparison with the expected message.

Compare:

A receive trace message mismatch alarm is declared if the accepted message (i.e., the message that passed the persistency check) does not match the expected message (previously downloaded to the receive expected page by the microprocessor). The mismatch alarm is removed if the accepted message is all-zero, or if the accepted message is identical to the expected message.

Overhead Byte Receiver:

The Overhead Byte Receiver (OBR) processes the path signal label byte (C2) and the synchronization status byte (Z1). The OBR consists of two sub-processes: Persistency and Compare.

Persistency:

The Persistency process checks for the repeated reception of the same C2 (Z1) byte. An unstable counter is incremented for each received C2 (Z1) byte that differs from the byte received in the previous frame. For example, a single corrupted byte value in a sequence of constant values causes the unstable count to increment twice, once on receipt of the corrupted value, and again on the next (uncorrupted) value. A path signal label unstable alarm or a synchronization status unstable alarm is declared when either unstable counter reaches five.

The unstable counter is reset to zero, the unstable alarm is removed, and the byte value is accepted when the same label is received in five consecutive frames. The accepted value is passed to the Compare process for comparison with the expected value.

Compare:

A path signal label mismatch alarm or a synchronization status mismatch alarm is declared if the accepted C2 or Z1 byte (i.e., the byte value that has passed the persistency check) does not match the expected C2 or Z1 byte (previously downloaded by the microprocessor). The mismatch alarm is cleared when the accepted value matches the expected value.

The receive path signal label mismatch mechanism follows the table below:

Table 2 -

Expect	Receive	Action
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match

Expect	Receive	Action
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Note:

XX, YY = anything except 00H or 01H (XX not equal YY).

9.15.2 Transmit Trace Buffer (TTB)

The TTB sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

9.16 Line Side Interface

A byte-serial TTL-compatible receive and transmit line side interface is provided when configured for STS-12c (STM-4c), STS-3c (STM-1) or STS-1 operation. In addition, for STS-1 operation, a bit-serial interface is also supported.

9.16.1 Receive Interface

The receive interface is either a generic byte-wide interface for interconnection with an upstream serial-to-parallel converter or a bit-serial interface for operation with an internal serial-to-parallel converter.

When operating with the upstream serial-to-parallel converter, the upstream device is expected to provide data that is demultiplexed according to SONET/SDH byte boundaries along with a 77.76 MHz (STS-12c), 19.44 MHz (STS-3c) or 6.48 MHz (STS-1) clock. In addition, the upstream serial-to-parallel converter is expected to provide a framing pattern detector that performs part of the framing function. The serial-to-parallel converter need not perform descrambling as this is provided by the S/UNI-622. When enabled to search for frame alignment by the S/UNI-622 OOF output being high, the upstream device should realign to any occurrence of the SONET/SDH framing pattern and provide

an appropriate pulse on the S/UNI-622 FPIN input. The upstream device should ignore framing patterns and retain its byte alignment when the S/UNI-622 OOF output is low.

When operating in STS-1 mode, the bit-serial interface can be used. An internal Serial-to-Parallel Converter (SIPO) block provides the first stage of digital processing of the receive incoming STS-1 bit-serial data stream. The byte alignment in the incoming stream is determined by searching for the 16-bit frame alignment signal (A1, A2). The bit-serial stream (RSIN) is converted from serial to parallel format in accordance with the determined byte alignment. In this mode of operation, the generated divide-by-eight clock output on GROCLK should be used to drive the input receive clock, PICLK.

9.16.2 Transmit Interface

The transmit interface is either a generic byte-wide interface for interconnection with a downstream parallel-to-serial converter or a bit-serial interface for operation with an internal parallel-to-serial converter.

When operating with the downstream parallel-to-serial converter, the S/UNI-622 device provides a byte-serial 77.76 Mbits/s (STS-12c), 19.44 Mbits/s (STS-3c) or 6.48 Mbits/s (STS-1) stream depending on the operating mode. The downstream serializer is expected to accept the transmit stream in byte-serial format and serializes it at the appropriate line rate.

When operating in STS-1 mode, the bit-serial interface can be used. An internal Parallel-to-Serial Converter (PISO) block provides the final stage of digital processing for the transmit STS-1 data stream. The PISO block converts the data stream from parallel to serial format. In this mode of operation, the generated divide-by-eight clock output on GTOCLK should be used to drive the input transmit clock, TCLK.

9.17 Drop Side Interface

9.17.1 Receive Interface

The drop side receive interface can be accessed through a generic 19-bit wide interface. External circuitry is notified, using the RCA signal, when a cell is available in the receive FIFO. External circuitry may then read the cell from the buffer as a word-wide stream (along with a bit marking the first word of the cell) at instantaneous rates up to 52 MHz.

The cell data structure supported is described in the Receive ATM Cell Processor block description above.

9.17.2 Transmit Interface

The drop side transmit interface can be accessed through a generic 19-bit wide interface. External circuitry is notified using the TCA signal when a cell may be written to the transmit FIFO. The cell is written to the FIFO as a word-wide stream (along with a bit marking the first word of the cell) at instantaneous rates of up to 52 MHz.

The cell data structure supported is described in the Transmit ATM Cell Processor block description above.

9.18 Parallel I/O Port

The Parallel Input/Output Port block provides six generic outputs and four generic inputs that can be used to control and monitor front end devices. Typical front end devices include parallel-to-serial conversion, serial-to-parallel conversion, clock and data recovery, and clock synthesis integrated circuits.

9.19 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-622 identification code is 053550CD hexadecimal.

9.20 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-622. The register set is accessed as follows:

9.21 Register Memory Map

Table 3 -

Address	Register
0x00	S/UNI-622 Master Reset and Identity / Load Performance Meters

Address	Register
0x01	S/UNI-622 Master Configuration
0x02	S/UNI-622 Master Interrupt Status
0x03	PISO Interrupt
0x04	S/UNI-622 Master Control/Monitor
0x05	S/UNI-622 Master Auto Alarm
0x06	S/UNI-622 Parallel Output Port
0x07	S/UNI-622 Parallel Input Port
0x08	S/UNI-622 Parallel Input Port Value
0x09	S/UNI-622 Parallel Input Port Enable
0x0A	S/UNI-622 Transmit C1
0x0B	S/UNI-622 APS Control/Status
0x0C	S/UNI-622 Receive K1
0x0D	S/UNI-622 Receive K2
0x0E	S/UNI-622 Receive Z1
0x0F	S/UNI-622 Transmit Z1
0x10	RSOP Control/Interrupt Enable
0x11	RSOP Status/Interrupt Status
0x12	RSOP Section BIP-8 LSB
0x13	RSOP Section BIP-8 MSB
0x14	TSOP Control
0x15	TSOP Diagnostic
0x16-0x17	TSOP Reserved
0x18	RLOP Control/Status
0x19	RLOP Interrupt Enable/Interrupt Status
0x1A	RLOP Line BIP-96/24/8 LSB
0x1B	RLOP Line BIP-96/24/8
0x1C	RLOP Line BIP-96/24/8 MSB
0x1D	RLOP Line FEBE LSB

Address	Register
0x1E	RLOP Line FEBE
0x1F	RLOP Line FEBE MSB
0x20	TLOP Control
0x21	TLOP Diagnostic
0x22	TLOP Transmit K1
0x23	TLOP Transmit K2
0x24-0x25	BIDX Reserved
0x26	BIMX Reserved
0x27	BIMX Reserved
0x28	SSTB Control
0x29	SSTB Status
0x2A	SSTB Indirect Address
0x2B	SSTB Indirect Data
0x2C	SSTB Expected Clock Synchronization Message
0x2D	SSTB Clock Synchronization Message Status
0x2E-0x2F	SSTB Reserved
0x30	RPOP Status/Control
0x31	RPOP Interrupt Status
0x32	RPOP Pointer Interrupt Status
0x33	RPOP Interrupt Enable
0x34	RPOP Pointer Interrupt Enable
0x35	RPOP Pointer LSB
0x36	RPOP Pointer MSB
0x37	RPOP Path Signal Label
0x38	RPOP Path BIP-8 LSB
0x39	RPOP Path BIP-8 MSB
0x3A	RPOP Path FEBE LSB
0x3B	RPOP Path FEBE MSB

Address	Register
0x3C	RPOP RDI
0x3D	RPOP Ring Control
0x3E-0x3F	RPOP Reserved
0x40	TPOP Control/Diagnostic
0x41	TPOP Pointer Control
0x42	TPOP Reserved
0x43	TPOP Current Pointer LSB
0x44	TPOP Current Pointer MSB
0x45	TPOP Arbitrary Pointer LSB
0x46	TPOP Arbitrary Pointer MSB
0x47	TPOP Path Trace
0x48	TPOP Path Signal Label
0x49	TPOP Path Status
0x4A	TPOP Path User Channel
0x4B	TPOP Path Growth #1 (Z3)
0x4C	TPOP Path Growth #2 (Z4)
0x4D	TPOP Path Growth #3 (Z5)
0x4E-0x4F	TPOP Reserved
0x50	RACP Control
0x51	RACP Interrupt Status
0x52	RACP Interrupt Enable/Control
0x53	RACP Match Header Pattern
0x54	RACP Match Header Mask
0x55	RACP Correctable HCS Error Count (LSB)
0x56	RACP Correctable HCS Error Count (MSB)
0x57	RACP Uncorrectable HCS Error Count (LSB)
0x58	RACP Uncorrectable HCS Error Count (MSB)
0x59	RACP Receive Cell Counter (LSB)

Address	Register
0x5A	RACP Receive Cell Counter
0x5B	RACP Receive Cell Counter (MSB)
0x5C	RACP GFC Control/Misc. Control
0x5D-0x5F	RACP Reserved
0x60	TACP Control/Status
0x61	TACP Idle/Unassigned Cell Header Pattern
0x62	TACP Idle/Unassigned Cell Payload Octet Pattern
0x63	TACP FIFO Control
0x64	TACP Transmit Cell Counter (LSB)
0x65	TACP Transmit Cell Counter
0x66	TACP Transmit Cell Counter (MSB)
0x67	TACP Fixed Stuff / GFC
0x68	SPTB Control
0x69	SPTB Status
0x6A	SPTB Indirect Address
0x6B	SPTB Indirect Data
0x6C	SPTB Expected Path Signal Label
0x6D	SPTB Path Signal Label Status
0x6E-0x6F	SPTB Reserved
0x70	BERM Control*
0x71	BERM Interrupt*
0x72	BERM Line BIP Accumulation Period LSB*
0x73	BERM Line BIP Accumulation Period MSB*
0x74	BERM Line BIP Threshold LSB*
0x75	BERM Line BIP Threshold MSB*
0x76-0x7F	Reserved
0x80	S/UNI Master Test
0x81-0xFF	Reserved for Test

* Refer to the operations section for recommended settings

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-622. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[7]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-622 to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-622 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-622 operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 0x00: S/UNI-622 Master Reset and Identity / Load Performance Meters

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	1
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI-622 to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-622.

In addition, writing to this register simultaneously loads all the performance meter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

ID[3:0]:

The ID bits can be read to provide a binary S/UNI-622 revision number.

TYPE[2:0]:

The TYPE bits can be read to distinguish the S/UNI-622 from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-622 to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-622 is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-622 out of reset. Holding the S/UNI-622 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI-622 Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	TPTBEN	0
Bit 6	R/W	TSTBEN	0
Bit 5	R/W	SDH_C1	0
Bit 4	R/W	FIXPTR	1
Bit 3	R/W	TMODE[1]	1
Bit 2	R/W	TMODE[0]	1
Bit 1	R/W	RMODE[1]	1
Bit 0	R/W	RMODE[0]	1

RMODE[1:0]:

The RMODE[1:0] bits select the operation rate of the S/UNI-622's receive side. The default configuration selects STS-12c rate operation.

Table 4 -

RMODE[1:0]	MODE
00	STS-1 byte-serial
01	STS-3c (STM-1) byte-serial
10	STS-1 bit-serial
11	STS-12c (STM-4c) byte-serial

Note:

Mode switching may require the switching of external clocks (PICLK, RSICLK). The mode switch must be performed cleanly such that no internal clock glitches are generated. The mode switch is accomplished cleanly by first switching the external clock source, then resetting the S/UNI-622, then programming the RMODE bits to select the desired rate.

TMODE[1:0]:

The TMODE[1:0] bits select the operation rate of the S/UNI-622's transmit side. The default configuration selects STS-12c rate operation.

Table 5 -

TMODE[1:0]	MODE
00	STS-1 byte-serial
01	STS-3c (STM-1) byte-serial
10	STS-1 bit-serial
11	STS-12c (STM-4c) byte-serial

Note:

Mode switching may require the switching of external clocks (TCLK, TSICLK). The mode switch must be performed cleanly such that no internal clock glitches are generated. The mode switch is accomplished cleanly by first switching the external clock source, then resetting the S/UNI-622, then programming the TMODE bits to select the desired rate.

FIXPTR:

The FIXPTR bit disables trasnsmit payload pointer adjustments. If the FIXPTR bit is a logic one, the transmit payload pointer is set at 522. If FIXPTR is a logic zero, the payload pointer is controlled by the contents of the TPOP Pointer Control register.

SDH_C1

The SDH_C1 bit selects whether to insert SONET or SDH format C1 section overhead bytes into the transmit stream. When SDH_C1 is set high, SDH format C1 bytes are selected for insertion. For this case, all the C1 bytes are forced to the value programmed in the S/UNI-622 Transmit C1 register. When SDH_C1 is set low, SONET format C1 bytes are selected for insertion. For this case, the C1 bytes of a STS-N signal are numbered incrementally from 1 to N.

When SDH_C1 is set high, the transmit section trace buffer enable bit, TSTBEN can be used to overwrite the first C1 byte of a STS-N signal.

TSTBEN

The TSTBEN bit controls whether the section trace message stored in the SSTB block is inserted into the transmit stream (i.e., the first C1 byte). When TSTBEN is set high and the SDH_C1 is set high, the message stored in the SSTB is inserted into the transmit stream. When TSTBEN is set low or SDH_C1 is set low, the section trace message is supplied by the TSOP block

or via the corresponding TTOH input. Overhead insertion via the serial overhead insertion inputs, TTOHEN and TTOH[4:1], takes precedence over insertion via the SSTB block.

TPTBEN

The TPTBEN bit controls whether the path trace message stored in the SPTB block is inserted into the transmit stream (i.e., the J1 byte). When TPTBEN is set high, the message stored in the SPTB is inserted into the transmit stream. When TPTBEN is set low, the path trace message is supplied by the TPOP block or via the corresponding TPOH input. Overhead insertion via the serial overhead insertion inputs, TPOHEN and TPOH, takes precedence over insertion via the SPTB block.

Register 0x02: S/UNI-622 Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R	S/UNII	X
Bit 6	R	STBI	X
Bit 5	R	Reserved	X
Bit 4	R	TACPI	X
Bit 3	R	RACPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RACPI:

The RACPI bit is high when an interrupt request is active from the RACP block. The RACP interrupt sources are enabled in the RACP Interrupt Enable/Status Register.

TACPI:

The TACPI bit is high when an interrupt request is active from the TACP block. The TACP interrupt sources are enabled in the TACP Interrupt Control/Status Register.

STBI:

The STBI bit is high when an interrupt request is active from either the SSTB block or the SPTB block. The SSTB interrupt sources are enabled in the SSTB Control Register and the SSTB Clock Synchronization Message Status Register. The SPTB interrupt sources are enabled in the SPTB Control Register and the SPTB Path Signal Label Status Register.

S/UNII:

The S/UNII bit is high when an interrupt request is active from the Parallel Input/Output Block, the Z1 Change Block, the BERM Block, the PISO Block or the APS Block. The Parallel Input/Output interrupt sources are enabled in the S/UNI-622 Parallel Input Port Enable Register. The Z1 Change interrupt source and the APS interrupt sources are enabled in the S/UNI-622 APS Control/Status Register.

Register 0x03: PISO Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PAEE	0
Bit 0	R	PAEI	X

PAEI:

The PAEI bit is set high when a phase alignment error occurs. This bit is cleared when the PISO Interrupt register is read.

PAEE:

The PAEE bit is an interrupt mask for phase alignment error events. When PAEE is a logic one, an interrupt is generated when a phase alignment error occurs.

Register 0x04: S/UNI-622 Master Control/Monitor

Bit	Type	Function	Default
Bit 7	R/W	TCAINV	0
Bit 6	R/W	RCAINV	0
Bit 5	R/W	LLE	0
Bit 4	R/W	DLE	0
Bit 3	R/W	LOOPT	0
Bit 2	R/W	DPLE	0
Bit 1	R	PICLKA	X
Bit 0	R	TCLKA	X

This register provides polarity control for outputs RCA and TCA, STS-1 loopback control and activity monitoring on S/UNI-622 PICLK and TCLK clock inputs.

TCLKA:

The TCLK active (TCLKA) bit monitors activity on input TCLK to aid in the detection of a loss of clock state. When TCLK makes a low to high transition, the TCLKA bit is set high. The bit will remain high until this register is read at which point the TCLKA bit is cleared. Therefore, a lack of transitions on TCLK is indicated when TCLKA is low. This register should be read at periodic intervals to detect clock failures.

PICLKA:

The PICLK active (PICLKA) bit monitors activity on input PICLK to aid in the detection of a loss of clock state. When PICLK makes a low to high transition, the PICLKA bit is set high. The bit will remain high until this register is read at which point the PICLKA bit is cleared. Therefore, a lack of transitions on PICLK is indicated when PICLKA is low. This register should be read at periodic intervals to detect clock failures.

DPLE:

The Diagnostic Path Loopback, DPLE bit enables the S/UNI-622 diagnostic loopback where the S/UNI-622's Transmit Path Overhead Processor (TPOP) is directly connected to its Receive Path Overhead Processor (RPOP). When DPLE is logic one, loopback is enabled. Under this operating condition, the

S/UNI-622 continues to operates normally in the transmit direction. When DPLE is logic zero, the S/UNI-622 operates normally.

LOOPT:

The LOOPT bit can only be used when configured for STS-1 bit-serial mode in both the transmit and receive directions. In STS-1 bit-serial mode, the LOOPT bit selects the source of timing for the transmit section of the S/UNI-622.

When LOOPT is a logic zero, the transmitter timing is derived from input TSICLK. When LOOPT is a logic one, the transmitter timing is derived from receiver input RSICLK.

DLE:

The DLE bit can only be used when configured for STS-1 bit-serial mode in both the transmit and receive directions. The DLE bit enables the S/UNI-622 diagnostic loopback where the S/UNI-622 transmitter is looped back to the receiver.

When DLE is a logic one, output TSOUT is connected internally to input RSIN. In addition, input clock TSICLK is used to replace RSICLK as the main receive clock. When DLE is logic zero, the S/UNI-622 operates normally.

LLE:

The LLE bit can only be used when configured for STS-1 bit-serial mode in both the transmit and receive directions. The LLE bit enables the S/UNI line loopback where the receive bit stream is sampled, retimed and immediately transmitted.

When LLE is a logic one, input RSIN is connected internally to output TSOUT which is output with timing aligned to RSICLK. When LLE is logic zero, the S/UNI-622 operates normally.

RCAINV:

The RCAINV bits select the active polarity of the RCA signal. The default configuration selects RCA to be active high, indicating that a received cell is available when high. When RCAINV is set to logic one, the RCA signal becomes active low. If the state of the RCAINV bit has been changed, the receive FIFO must be reset via the FIFORST bit in the RACP Control register in order to properly initialize the RCA output.

TCAINV:

The TCAINV bits select the active polarity of the TCA signal. The default configuration selects TCA to be active high, indicating that a cell is available in the transmit FIFO when high. When TCAINV is set to logic one, the TCA signal becomes active low. If the state of the TCAINV bit has been changed, the transmit FIFO must be reset via the FIFORST bit in the TACP Control/Status register in order to properly initialize the TCA output.

Register 0x05: S/UNI-622 Master Auto Alarm

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	AUTOFEBE	1
Bit 1	R/W	AUTOLRDI	1
Bit 0	R/W	AUTOPRDI	1

AUTOPRDI

The AUTOPRDI bit determines whether the path remote defect indication is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, the path remote defect indication is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), line AIS, loss of pointer (LOP), or STS path AIS.

AUTOLRDI

The AUTOLRDI bit determines whether line remote defect indication (LRDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of loss of signal (LOS), loss of frame (LOF), or line AIS.

AUTOFEBE

The AUTOFEBE bit determines whether line and path far end block errors are sent upon detection of an incoming line and path BIP error events. When AUTOFEBE is set to logic one, one line or path FEBE is inserted for each line or path BIP error event. When AUTOFEBE is set to logic zero, incoming line or path BIP error events do not generate FEBE events.

Register 0x06: S/UNI-622 Parallel Output Port

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	POP[5]	1
Bit 4	R/W	POP[4]	1
Bit 3	R/W	POP[3]	1
Bit 2	R/W	POP[2]	0
Bit 1	R/W	POP[1]	0
Bit 0	R/W	POP[0]	0

POP[5:0]:

The values written to the POP[5:0] bit in the S/UNI-622 Parallel Output Port register directly correspond to the states set on the POP[5:0] output pins. This provides a generic port useful for controlling parallel-to-serial conversion devices, serial-to-parallel conversion devices, clock and data recovery devices or clock synthesis devices. The default states for this port are chosen so that POP[2:0] controls active-high signals while POP[5:3] controls active-low signals.

Register 0x07: S/UNI-622 Parallel Input Port

Bit	Type	Function	Default
Bit 7	R	PIPI[7]	X
Bit 6	R	PIPI[6]	X
Bit 5	R	PIPI[5]	X
Bit 4	R	PIPI[4]	X
Bit 3	R	PIPI[3]	X
Bit 2	R	PIPI[2]	X
Bit 1	R	PIPI[1]	X
Bit 0	R	PIPI[0]	X

PIPI[7:0]:

The PIPI[7:0] bits are interrupt indications. A logic one in any bit location indicates that an event has occurred on the corresponding PIP[3:0] inputs. A logic one in any of the PIPI[7:4] bit locations indicates that the signal on the corresponding PIP[3:0] input has transitioned from logic zero to logic one (i.e., upon detection of a rising edge). A logic one in any of the PIPI[3:0] bit locations indicates that the signal on the corresponding PIP[3:0] input has transitioned either from logic zero to logic one or from logic one to logic zero (i.e., upon a change of state). The PIPI[7:0] bits are cleared by reading this register.

These register bits function independently from the S/UNI-622 Parallel Input Port Enable register bits. The PIPI[7:0] bits will indicate events occurring on the PIP[3:0] inputs regardless of whether or not these events are enabled to generate an interrupt. The PIP[3:0] inputs are intended to monitor the frequency lock indications of the front end clock recovery and clock synthesis devices and one shot events like line code violations.

Register 0x08: S/UNI-622 Parallel Input Port Value

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	PIPV[3]	X
Bit 2	R	PIPV[2]	X
Bit 1	R	PIPV[1]	X
Bit 0	R	PIPV[0]	X

PIPV[3:0]:

The PIPV[3:0] bits are real-time input port state indications. A logic one in any bit location indicates that the signal on the corresponding PIP[3:0] input is a logic one. A logic zero in any bit location indicates that the signal on the corresponding PIP[3:0] input is a logic zero.

Register 0x09: S/UNI-622 Parallel Input Port Enable

Bit	Type	Function	Default
Bit 7	R/W	PIPE[7]	0
Bit 6	R/W	PIPE[6]	0
Bit 5	R/W	PIPE[5]	0
Bit 4	R/W	PIPE[4]	0
Bit 3	R/W	PIPE[3]	0
Bit 2	R/W	PIPE[2]	0
Bit 1	R/W	PIPE[1]	0
Bit 0	R/W	PIPE[0]	0

PIPE[7:0]:

The PIPE[7:0] bits are interrupt enables. When a logic one is written to these locations, the occurrence of an event indicated using the corresponding S/UNI-622 Parallel Input Port Register bit activates the interrupt, INTB. The interrupt is cleared by reading the S/UNI-622 Parallel Input Port Register. When a logic zero is written to these locations, the occurrence of an event as indicated in the S/UNI-622 Parallel Input Port Register is inhibited from activating the interrupt.

Register 0x0A: S/UNI-622 Transmit C1

Bit	Type	Function	Default
Bit 7	R/W	C1[7]	1
Bit 6	R/W	C1[6]	1
Bit 5	R/W	C1[5]	0
Bit 4	R/W	C1[4]	0
Bit 3	R/W	C1[3]	1
Bit 2	R/W	C1[2]	1
Bit 1	R/W	C1[1]	0
Bit 0	R/W	C1[0]	0

C1[7:0]:

The value written to these bit positions is inserted into the C1 byte positions of the transmit stream when enabled using the SDH_C1 bit in the S/UNI-622 Master Configuration register. C1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. C1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted.

Insertion of the C1 byte via the serial overhead insertion inputs, TTOHEN and TTOH[4:1], takes precedence over insertion via the Transmit C1 register. Insertion of the section trace message (the first C1 byte when SDH_C1 is high) also takes precedence over C1 insertion via the Transmit C1 register.

Register 0x0B: S/UNI-622 APS Control/Status

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1E	0
Bit 4	R	Z1I	X
Bit 3	R	PSBFI	X
Bit 2	R	COAPSI	X
Bit 1		Unused	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames, where no three consecutive frames contain identical K1 bytes, have been received. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the S/UNI-622 Receive K1/K2 Registers. The registers are updated when the same new K1/K2 byte values are observed for three consecutive frames. This bit is cleared when the S/UNI-622 APS Control/Status Register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the S/UNI-622 APS Control/Status Register is read.

Z1I:

The Z1I bit is set high when a new Z1 byte value has been extracted into the S/UNI-622 Receive Z1 Register. The register is updated when a Z1 byte value is extracted that is different than the Z1 byte value extracted in the previous frame. This bit is cleared when the S/UNI-622 APS Control/Status Register is read.

Z1E:

The change of Z1 interrupt enable is an interrupt mask for changes in the receive Z1 byte value. When Z1E is a logic one, an interrupt is generated when the extracted Z1 byte is different from the Z1 byte extracted in the previous frame.

COAPSE:

The change of APS byte interrupt enable is an interrupt mask for events detected by the receive APS processor. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value has been extracted into the S/UNI-622 Receive K1/K2 Registers.

PSBFE:

The change of protection switch byte failure alarm interrupt enable is an interrupt mask for events detected by the receive APS processor. When PSBFE is a logic one, an interrupt is generated upon a change in the protection switch byte failure alarm state.

Register 0x0C: S/UNI-622 Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the S/UNI-622 APS Control Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0x0D: S/UNI-622 Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the S/UNI-622 APS Control Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0x0E: S/UNI-622 Receive Z1

Bit	Type	Function	Default
Bit 7	R	Z1[7]	X
Bit 6	R	Z1[6]	X
Bit 5	R	Z1[5]	X
Bit 4	R	Z1[4]	X
Bit 3	R	Z1[3]	X
Bit 2	R	Z1[2]	X
Bit 1	R	Z1[1]	X
Bit 0	R	Z1[0]	X

Z1[7:0]:

The first Z1 byte contained in the receive stream is extracted into this register. The Z1 byte is used to carry synchronization status messages between line terminating network elements. Z1[7] is the most significant bit corresponding to bit 1, the first bit received. Z1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame using the Z1E bit in the APS Control/Status Register.

Register 0x0F: S/UNI-622 Transmit Z1

Bit	Type	Function	Default
Bit 7	R/W	Z1[7]	0
Bit 6	R/W	Z1[6]	0
Bit 5	R/W	Z1[5]	0
Bit 4	R/W	Z1[4]	0
Bit 3	R/W	Z1[3]	0
Bit 2	R/W	Z1[2]	0
Bit 1	R/W	Z1[1]	0
Bit 0	R/W	Z1[0]	0

Z1[7:0]:

The value written to these bit positions is inserted in the first Z1 byte position of the transmit stream. The Z1 byte is used to carry synchronization status messages between line terminating network elements. Z1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. Insertion of the Z1 byte via the serial transport overhead insertion inputs TTOHEN and TTOH[1] takes prececence over Z1 insertion via the S/UNI-622 Transmit Z1 register.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out-of-frame alarm. When OOFE is set to logic one, an interrupt is generated when the out-of-frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to determine and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the first A2 framing

byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit, register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-12c/3c/1 stream. When DDS is a logic zero, descrambling is enabled.

BIPWORD:

The BIPWORD bit position enables the reporting and accumulating of section BIP word errors. When a logic one is written to the BIPWORD bit position, one or more errors in the BIP-8 byte result in a single error being accumulated in the B1 error counter. When a logic zero is written to the BIPWORD bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out-of-frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out-of-frame interrupt status bit. OOFI is set high when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET frame being set to 1 prior to scrambling except for the section overhead. The LAIS bit is logically ORed with the external TLAIS input.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-12c/3c/1 stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the STS-12c/3c/1 stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BIPWORDO	0
Bit 2		Unused	X
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is read to determine the remote defect indication state of the RLOP. When LRDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

BIPWORDO:

The BIPWORDO bit controls the indication of B2 errors reported to the TLOP block for insertion as FEBEs. When BIPWORDO is logic one, the BIP errors are indicated once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORDO is logic zero, BIP errors are indicated once for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BIPWORD register bit.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the line AIS alarm detection algorithm. When AISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When AISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically forcing the SONET frame passed to downstream blocks to logical all-ones whenever line AIS is detected. When ALLONES is set to logic one, the SONET frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the outputs are immediately returned to carrying the data sampled on PIN[7:0]. When ALLONES is set to logic zero, the outputs carry the data sampled on PIN[7:0] regardless of the state of the line AIS alarm.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is increment for each and every B2 bit error that occurs during that frame.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the remote defect indication interrupt status bit. LRDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP-96/24/8 interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (Z2) is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the line remote defect indication alarm. When LRDIE is set to logic one, an interrupt is generated when the line RDI state changes.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-96/24/8 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-96/24/8 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBE (Z2) is detected.

Register 0x1A: RLOP Line BIP-96/24/8 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-96/24/8

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-96/24/8 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-96/24/8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-96/24/8 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP-96/24/8 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-96/24/8 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of line remote defect indication (LRDI). When LRDI is set to logic one, the TLOP inserts line RDI into the transmit SONET stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7 and 8 of the K2 byte of the STS-12c/3c/1 stream. The LRDI bit is logically ORed with the external TLRDI input.

APSREG:

The APSREG bit selects the source for the transmit APS channel. When APSREG is a logic zero, 0x0000 is inserted in the transmit APS channel. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register. The APS bytes may also be inserted upstream of the TLOP using the TTOHEN and TTOH[4:1] inputs. Values inserted using the TTOHEN input take precedence over the source selected by the APSREG bit.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP96/24/8	0

DBIP96/24/8:

The DBIP96/24/8 bit controls the insertion of bit errors continuously in the line BIP-96/24/8 bytes (B2). When DBIP96/24/8 is set to logic one, the B2 bytes are inverted.

Register 0x22: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x23: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x28 SSTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SSTB.

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes. When set high, a 16-byte section trace message is selected. If set low, a 64-byte section trace message is selected.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zeros section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignored and all-zeros bytes are provided to the TSOP block. When TNULL is set low the contents of the transmit section trace buffer is sent to TSOP for insertion into the C1 transmit section

overhead byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive section trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, section trace identifier message state changes will not affect INTB.

RTIUIE:

The receive section trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for six consecutive messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received section trace identifier message stable/unstable state of will activate the interrupt (INTB) output. When RTIUIE is set low, section trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the S/UNI-622. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 0x29: SSTB Section Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace identifier status of the SSTB.

RTIMV:

The receive section trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message.

RTIMI:

The receive section trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit and the interrupt are cleared when this register is read.

RTIUV:

The receive section trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. RTIUV is set high when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is set low when the current message becomes the accepted message as determined by the PER5 bit in the SSTB Control register.

RTIUI:

The receive section trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer

changes state. This bit and the interrupt are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SSTB Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the SSTB Indirect Data register.

Register 0x2A: SSTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message downloaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the section trace byte, the first C1 byte, of each frame in the transmit stream. When RRAMACC is set low, addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the addressed location in the static page.

Register 0x2B: SSTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 0x2C: SSTB Expected Clock Synchronization Message

Bit	Type	Function	Default
Bit 7	R/W	EZ1[7]	0
Bit 6	R/W	EZ1[6]	0
Bit 5	R/W	EZ1[5]	0
Bit 4	R/W	EZ1[4]	0
Bit 3	R/W	EZ1[3]	0
Bit 2	R/W	EZ1[2]	0
Bit 1	R/W	EZ1[1]	0
Bit 0	R/W	EZ1[0]	0

This register contains the expected clock synchronization message byte (Z1) in the receive stream.

EZ1[7:0]:

The EZ1[7] - EZ1[0] bits contain the expected clock synchronization message byte (Z1). EZ1[7:0] is compared with the clock synchronization message byte extracted from the receive stream. A clock synchronization message byte mismatch (CSMM) is declared if the accepted clock synchronization message byte differs from the expected clock synchronization message byte. If enabled, an interrupt is asserted upon declaration and removal of CSMM.

Register 0x2D: SSTB Clock Synchronization Message Status

Bit	Type	Function	Default
Bit 7	R/W	RCSMUIE	0
Bit 6	R/W	RCSMMIE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RCSMUI	X
Bit 2	R	RCSMUV	X
Bit 1	R	RCSMMI	X
Bit 0	R	RCSMMV	X

This register reports the clock synchronization message status of the SSTB.

RCSMMV:

The receive clock synchronization message mismatch status bit (RCSMMV) reports the match/mismatch status between the expected and the accepted clock synchronization message. RCSMMV is set high when the accepted CSM differs from the expected CSM written by the microprocessor. CSMMV is set low when the accepted CSM matches the expected CSM.

RCSMMI:

The receive clock synchronization message mismatch interrupt status bit (RCSMMI) is set high when the match/mismatch status between the accepted and the expected clock synchronization message changes state. This bit (and the interrupt) are cleared when this register is read.

RCSMUV:

The receive clock synchronization message unstable status bit (RCSMUV) reports the stable/unstable status of the clock synchronization message in the receive stream. RCSMUV is set high when the current received Z1 byte differs from the previous Z1 byte for five consecutive frames. RCSMUV is set low when the same CSM code is received for five consecutive frames.

RCSMUI:

The receive clock synchronization message unstable interrupt status bit (RCSMUI) is set high when the stable/unstable status of the clock

synchronization message changes state. This bit and the interrupt are cleared when this register is read.

RCSMMIE:

The receive clock synchronization message mismatch interrupt enable bit (RCSMMIE) controls the activation of the interrupt output when the comparison between accepted and the expected clock synchronization message changes state from match to mismatch and vice versa. When RCSMMIE is set high, changes in match state activates the interrupt (INTB) output. When RCSMMIE is set low, clock synchronization message state changes will not affect INTB.

RCSMUIE:

The receive clock synchronization message unstable interrupt enable bit (RCSMUIE) controls the activation of the interrupt output when the received clock synchronization message changes state from stable to unstable and vice versa. When RCSMUIE is set high, changes in stable state activates the interrupt (INTB) output. When RCSMUIE is set low, clock synchronization message state changes will not affect INTB.

Register 0x30: RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOP	X
Bit 4		Unused	X
Bit 3	R	PAIS	X
Bit 2	R	PRDI	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register allows the status of path level alarms to be monitored.

NEWPTRE:

When a 1 is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt output.

NEWPTRI:

The NEWPTRI bit is set to logic one upon the reception of a new_pointer indication.

PRDI, PAIS LOP:

The PRDI, PAIS and LOP bits reflect the current state of the corresponding path level alarms.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x31: RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI, BIPEI:

The BIPEI and FEBEI bits are set to logic one when the corresponding event, a path BIP-8 error or path FEBE is detected.

PRDII:

The PRDII bit is set to logic one when a change is detected in the path remote defect indication or the auxiliary path remote defect indication bits.

PAISI, LOPI:

The PAISI, and LOPI bits are set to logic one when a transition occurs in the corresponding alarm state.

PSLI:

The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register.

All bits in this register (and the interrupt) are cleared when this register is read.

Register 0x32: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6		Unused	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

NDFI:

The NDFI bit is set to logic one when the RPOP detects an active NDF event to a valid pointer value. NDFI is cleared when the RPOP Pointer Interrupt Status register is read.

PSEI:

The PSEI bit is set to logic one when the RPOP detects a positive stuff event. PSEI is cleared when the RPOP Pointer Interrupt Status register is read.

NSEI:

The NSEI bit is set to logic one when the RPOP detects a negative stuff event. NSEI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLPTRI:

The ILLPTRI bit is set to logic one when the RPOP detects an illegal pointer event. ILLPTRI is cleared when the RPOP Pointer Interrupt Status register is read.

INVNDFI:

The INVNDFI bit is set to logic one when the RPOP detects an invalid NDF event. INVNDFI is cleared when the RPOP Pointer Interrupt Status register is read.

DISCOPAI:

The DISCOPAI bit is set to logic one when the RPOP detects a discontinuous change of pointer. DISCOPAI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLJREQI:

The ILLJREQI bit is set to logic one when the RPOP detects an illegal pointer justification request event. ILLJREQI is cleared when the RPOP Pointer Interrupt Status register is read.

Register 0x33: RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

When a logic one is written to the FEBEE interrupt enable bit position, the reception of one or more FEBEs will activate the interrupt output.

BIPEE:

When a logic one is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt output.

PRDIE:

When a logic one is written to the PRDIE interrupt enable bit position, a change in the path remote defect indication state will activate the interrupt output.

PAISE:

When a logic one is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt output.

LOPE:

When a logic one is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt output.

PSLE:

When a logic one is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt output.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x34: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register is used to enable pointer event interrupts.

NDFE:

When a logic one is written to the NDFE interrupt enable bit position, a change in active offset due to the reception of an enabled NDF (NDF_enabled indication) will activate the interrupt output, INTB.

PSEE:

When a logic one is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt output, INTB.

NSEE:

When a logic one is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt output, INTB.

ILLPTRE:

When a logic one is written to the ILLPTRE interrupt enable bit position, an illegal pointer will activate the interrupt output, INTB.

INVNDFE:

When a logic one is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt output, INTB.

DISCOPAE:

When a logic one is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt output, INTB.

ILLJREQE:

When a logic one is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt output, INTB.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x35: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

PTR[7:0]:

The PTR[7:0] bits contain the eight LSBs of the current pointer value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Register 0x36: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RDI10	0
Bit 4		Unused	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

PTR[9:8]:

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication and the auxiliary remote defect indication. When RDI10 is set to logic one, the PRDI and ARDI statuses are updated when the same value is received in the corresponding bit of the G1 byte for 10 consecutive frames. When PRDI10 is set to logic zero, the PRDI and ARDI statuses are updated when the same value is received for 5 consecutive frames.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for two consecutive frames.

Register 0x38: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

Bits PBE[15:0] represent the number of path BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost. The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x3C: RPOP RDI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BLKFEBE	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARDIE	0
Bit 0	R	ARDIV	X

ARDIV:

The auxiliary RDI bit (ARDIV) reports the current state of the path auxiliary RDI within the receive path overhead processor.

ARDIE:

When a 1 is written to the ARDIE interrupt enable bit position, a change in the path auxiliary RDI state will activate the interrupt (INTB) output.

BLKFEBE:

When set high, the block FEBE bit (BLKFEBE) causes path FEBE errors to be reported and accumulated on a block basis. A single path FEBE error is accumulated for a block if the received FEBE code for that block is between 1 and 8 inclusive. When BLKFEBE is set low, path FEBE errors are accumulated on a error basis.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x3D: RPOP Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register contains ring control bits.

BLKBIPO:

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported on a block basis to the transmit path overhead processor, TPOP, block. A single path BIP error is reported to the return transmit path overhead processor if any of the path BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are reported on a bit basis.

DISFS:

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU-3 carrying a VC-3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 stream. This bit is ignored when the RPOP is processing an STS-3c (STM-1) stream.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be accumulated on a block basis. A single BIP error is accumulated if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic one is written to this bit, an incorrect SS bit pattern

(i.e.,≠10).will prevent RPOP from issuing NDF_enable, inc_ind, new_point and dec_ind indications. When a logic zero is written to this bit, the SS bits received do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic one is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic zero is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EXCFS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DB3	0
Bit 0	R/W	PAIS	0

This register allows insertion of path level alarms and diagnostic signals.

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. This register bit value is logically ORed with the input TPAIS. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all-ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.

DB3:

The DB3 bit controls the inversion of the B3 byte value. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted which causes the insertion of eight path BIP-8 errors per frame. This bit overrides the state of the B3 error insertion mask controlled by the TPOHEN primary input. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted.

EXCFS:

The fixed stuff column BIP-8 exclusion bit (EXCFS) controls the inclusion of bytes in the fixed stuff columns of the STS-1/AU-3 payload in path BIP-8 calculations. When EXCFS is a logic one, the value of the bytes in columns 30 and 59 do not affect the value of the path BIP-8 byte (B3). When EXCFS is logic zero, data in the fixed stuff bytes are included in the path BIP-8 calculations. This bit is only active if the TPOP is processing a STS-1 stream.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally the TPOP Arbitrary Pointer Registers

are written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one. This bit is automatically cleared after the new payload pointer has been loaded.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value will of course be inserted in the STS-12c/3c/1 stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry which should be in a loss of pointer state.

This bit is automatically cleared after the new payload pointer has been loaded.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the POUT[7:0] stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by downstream circuitry which should be in a loss of pointer state. If FTPTR is set to logic one, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the POUT[7:0] stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic zero, a valid pointer is inserted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

For the J1 byte, the SPTB block can also be selected as a source when configured by a bit in the S/UNI-622 Master Configuration register. When a logic one is written to SRCJ1, the J1 byte is inserted from the data sampled on

primary input TPOH during the J1 byte position or from the SPTB block as controlled by the S/UNI-622 Master Configuration register. When a logic zero is written to SRCJ1, the J1 byte source is determined by input TPOHEN or the S/UNI-622 Master Configuration register.

Register 0x43: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

CPTR[7:0]:

The CPTR[7:0] bits, along with the CPTR[9:8] bits in the TPOP Current Pointer MSB Register reflect the value of the current payload pointer being inserted in the outgoing stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

Register 0x44: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:8]:

The CPTR[9:8] bits, along with the CPTR[7:0] bits in the TPOP Current Pointer LSB Register reflect the value of the current payload pointer being inserted in the outgoing stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the POUT[7:0] stream.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	0
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the POUT[7:0] stream.

S[1], S[0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x47: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register allows control over the path trace byte.

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path trace bit positions in the path overhead input stream, TPOH and when insertion via the SPTB is disabled.

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	1
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	1
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label. Upon reset the register defaults to 13H, which represents "ATM Payload."

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path signal label bit positions in the path overhead input stream, TPOH.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

FEBE[3:0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte when the SRCG1 bit of the TPOP Source Control Register is logic zero and primary input TPOHEN is low during the path status FEBE bit positions in the path overhead input stream, TPOH. The value contained in FEBE[3:0] is cleared after being inserted in the path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated on primary input FEBE during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication. This register bit value is logically ORed with the input TPRDI. When a logic one is written to this bit position, the PRDI bit position in the path status byte is set high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low. This bit has no effect if the SRCG1 bit of the TPOP Source Control Register is logic one or primary input TPOHEN is high during the path status remote defect indication bit position in the path overhead input stream, POH, in which case the value is inserted from TPOH.

G1[2], G1[1], G1[0]:

The G1[2:0] bits are inserted in the unused bit positions in the path status byte when the SRCG1 bit of the TPOP Source Control Register is logic zero and primary input TPOHEN is low during the unused bit positions in the path overhead input stream, TPOH.

Register 0x4A: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register allows control over the path user channel.

F2[7:0]:

The F2[7:0] bits are inserted in the F2 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path user channel bit positions in the path overhead input stream, TPOH.

Register 0x4B: TPOP Path Growth #1 (Z3)

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register allows control over path growth byte #1 (Z3).

Z3[7:0]:

The Z3[7:0] bits are inserted in the Z3 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path growth #1 bit positions in the path overhead input stream, TPOH.

Register 0x4C: TPOP Path Growth #2 (Z4)

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register allows control over path growth byte #2 (Z4).

Z4[7:0]:

The Z4[7:0] bits are inserted in the Z4 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path growth #2 bit positions in the path overhead input stream, TPOH.

Register 0x4D TPOP Path Growth #3 (Z5)

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register allows control over path growth byte #3 (Z5).

Z5[7:0]:

The Z5[7:0] bits are inserted in the Z5 byte position in the POUT[7:0] stream when primary input TPOHEN is low during the path growth #3 bit positions in the path overhead input stream, TPOH.

Register 0x50: RACP Control

Bit	Type	Function	Default
Bit 7	R/W	FSEN	1
Bit 6	R/W	RXPTYP	0
Bit 5	R/W	PASS	0
Bit 4	R/W	DISCOR	0
Bit 3	R/W	HCSPASS	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DDSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload. When DDSCR is a logic one, cell payload descrambling is disabled. When DDSCR is a logic zero, payload descrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared. Note that HCSADD can also be used to force the S/UNI-622 out of cell delineation.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. In

addition, the HCS verification finite state machine never exits the correction mode. Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states.

DISCOR:

The DISCOR bit disables the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

PASS:

The PASS bit controls the function of the cell filter. When PASS is written with a logic zero, all cells which match the header cell filter and which have VPI and VCI fields set to 0 are dropped. When PASS is a logic one, the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to 0 is not performed. The default state of this bit together with the default states of the bits in the Match Mask and Match Pattern registers enable the dropping of cells containing all zero VCI and VPI fields.

RXPTYP:

The RXPTYP bit selects even or odd parity for outputs RXPRTY[1:0]. When RXPTYP is set to logic one, even parity is calculated for the output data on RDAT[15:0]; conversely, when RXPTYP is set to logic zero, odd parity is calculated for output data. In word parity mode, when RXPTYP is set to logic one, output RXPRTY[1] is the even parity bit for outputs RDAT[15:0]. In word parity mode, when RXPTYP is set to logic zero, output RXPRTY[1] is the odd parity bit for outputs RDAT[15:0]. (In word parity mode, RXPRTY[0] is held low.) In byte parity mode, when RXPTYP is set to logic one, output RXPRTY[1] is the even parity bit for outputs RDAT[15:8] and output RXPRTY[0] is the even parity bit for outputs RDAT[7:0]. In byte parity mode, when RXPTYP is set to logic zero, RXPRTY[1] is the odd parity bit for outputs RDAT[15:8] and output RXPRTY[0] is the odd parity bit for outputs RDAT[7:0].

FSEN:

The active-high fix stuff control enable bit FSEN determines the payload mapping of ATM cells when STS-1 (AU-3) mapping is selected. When FSEN is set to logic one, the S/UNI-622 does not insert ATM cells into the two stuff columns in the SPE. When FSEN is set to logic zero, the S/UNI-622 inserts cells into the entire SPE.

Register 0x51: RACP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OCDV	X
Bit 6	R	LCDV	X
Bit 5	R	OCDI	X
Bit 4	R	LCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	FUDRI	X

FUDRI:

The FUDRI bit is set high when a FIFO underrun occurs. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register.

UHCSI:

The UHCSI bit is set high when an uncorrectable HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a correctable HCS error is detected. This bit is reset immediately after a read to this register.

LCDI:

The LCDI bit is set high when the S/UNI-622 enters or exits the loss of cell delineation state. Loss of cell delineation is declared when out of cell delineation persists for 4 ms or more. Loss of cell delineation is removed when out of cell delineation is absent for 4 ms. This bit is reset immediately after a read to this register.

OCDI:

The OCDI bit is set high when a change of cell delineation state has occurred. The OCDI bit is set high when the S/UNI-622's cell delineation state machine transitions from the PRESYNC state to the SYNC state and from the SYNC state to the HUNT state.

The cell delineation state machine transitions from the SYNC state to the HUNT state immediately when either loss of signal (LOS), loss of frame (LOF), loss of pointer (LOP), line AIS or path AIS is declared or when seven consecutive cells with incorrect HCS's are detected. The cell delineation state machine remains in HUNT state as long as one of the above alarms is active or if a cells with a correct HCS can not be found.

This bit is reset immediately after a read to this register.

LCDV:

The LCDV bit indicates if the RACP-622 is in the loss of cell delineation state. When LCDV is set high, the RACP-622 is in the loss of cell delineation state. If LCDV is low, the RACP-622 is not in the loss of cell delineation state.

OCDV:

The OCDV bit indicates the cell delineation state. When OCDV is set high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states, and is hunting for the cell boundaries in the synchronous payload envelope. When OCDV is set low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x52: RACP Interrupt Enable/Control

Bit	Type	Function	Default
Bit 7	R/W	OCDE	0
Bit 6	R/W	LCDE	0
Bit 5	R/W	HCSE	0
Bit 4	R/W	FIFOE	0
Bit 3	R/W	LCDDROP	0
Bit 2	R/W	RCALEVEL0	1
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]:

The HCS filter bits, HSCFTR[1:0] indicate the number of error free cells required while in detection mode before reverting back to correction mode. Please refer to Figure 12 for details.

Table 6 -

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell correction.
01	Two ATM cells with correct HCS before resumption of cell correction.
10	Four ATM cells with correct HCS before resumption of cell correction.
11	Eight ATM cells with correct HCS before resumption of cell correction.

RCALEVEL0:

The active-high RCA level 0 bit, RCALEVEL0 determines what output RCA indicates when it transitions low. When RCALEVEL0 is set to logic one, a high to low transition on output RCA indicates that the receive FIFO is empty. When RCALEVEL0 is set to logic zero, a high to low transition on output RCA

indicates that the receive FIFO is near empty and contains only four words. Please refer to figures 36 a) and 36 b) for more information on RCALEVEL0.

LCDDROP:

The LCD drop bit, LCDDROP, enables the dropping of cells while the S/UNI-622 is in the loss of delineation (LCD) state. The S/UNI-622 enters the LCD state after continuously being out of cell delineation for 4 ms. Once in the LCD state, the S/UNI-622 exits the LCD state only after continuously being in cell delineation for 4 ms. When LCDDROP is set to logic one, received cells are not written into the receive FIFO unless the S/UNI-622 is not in the LCD state. When LCDDROP is set to logic zero, cells are written to the receive FIFO when the S/UNI-622 is in cell delineation, regardless whether the S/UNI-622 is in the LCD state or not.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun. When FIFOE is set to logic one, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a correctable or an uncorrectable HCS error. When HCSE is set to logic one, the interrupt is enabled.

LCDE:

The LCDE bit enables the generation of an interrupt when loss of cell delineation is asserted and removed. When LCDE is set to logic one, the interrupt is enabled.

OCDE:

The OCDE bit enables the generation of an interrupt due to a change of cell delineation state. When OCDE is set to logic one, the interrupt is enabled.

Register 0x53: RACP Match Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third and fourth bits of the first octet of the 53-octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the RACP Match Header Mask Register. The PASS bit in the RACP Control Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 0x54: RACP Match Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	0
Bit 6	R/W	MGFC[2]	0
Bit 5	R/W	MGFC[1]	0
Bit 4	R/W	MGFC[0]	0
Bit 3	R/W	MPTI2]	0
Bit 2	R/W	MPTI[1]	0
Bit 1	R/W	MPTI[0]	0
Bit 0	R/W	MCLP	0

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third and fourth bits of the first octet of the 53-octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the RACP Match Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 0x55: RACP Correctable HCS Error Count (LSB)

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

Register 0x56: RACP Correctable HCS Error Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CHCS[11]	X
Bit 2	R	CHCS[10]	X
Bit 1	R	CHCS[9]	X
Bit 0	R	CHCS[8]	X

CHCS[11:0]:

The CHCS[11:0] bits indicate the number of correctable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x57: RACP Uncorrectable HCS Error Count (LSB)

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

Register 0x58: RACP Uncorrectable HCS Error Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	UHCS[11]	X
Bit 2	R	UHCS[10]	X
Bit 1	R	UHCS[9]	X
Bit 0	R	UHCS[8]	X

UHCS[11:0]:

The UHCS[11:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x59: RACP Receive Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x5A: RACP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x5B: RACP Receive Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[20:0]:

The RCELL[20:0] bits indicate the number of cells receive and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle/Unassigned cell matches are not counted. The counter should be polled every second to avoid saturating. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the receive cell count register space, the correctable HCS error count register space, or to the uncorrectable HCS error count register space.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x5C: GFC Control/Misc. Control

Bit	Type	Function	Default
Bit 7	R/W	CDDIS	0
Bit 6	R/W	RXBYTEPRTY	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RGFCE[3]	1
Bit 2	R/W	RGFCE[2]	1
Bit 1	R/W	RGFCE[1]	1
Bit 0	R/W	RGFCE[0]	1

RGFCE[3:0]:

The receive GFC enable bits, RGFCE[3:0], determine which generic flow control bits are presented on output RGFC. If the enable bit for a GFC bit is set, the RGFC output changes, in the appropriate bit location, to the value of the corresponding GFC bit in the current cell; otherwise, RGFC is low. The RGFCE[3:0] bits are the mask bits for the GFC[3:0] bits. GFC[3], the most significant GFC bit (the first bit in the cell) is the first bit output on RGFC. For example, when RGFCE[3] is set to logic one, the GFC[3] bit is output on RGFC in the first RGFC bit period (marked by the RCP output). When RGFCE[3] is set to logic zero, RGFC is held low in the first RGFC bit period.

RXBYTEPRTY:

The receive byte parity, RXBYTEPRTY, mode bit selects between byte and word parity mode for outputs RXPRTY[1:0]. When the RXBYTEPRTY bit is set to logic one, byte parity mode is selected, otherwise, word parity mode is selected. In byte parity mode, RXPRTY[1] is the (odd or even) parity bit for outputs RDAT[15:8], and RXPRTY[0] is the parity bit for outputs RDAT[7:0]. In word parity mode, RXPRTY[1] is the (odd or even) parity bit calculated for all 16 outputs RDAT[15:0], and RXPRTY[0] is held low. Word parity mode can only be selected when the BUS8 input is low (i.e., the 16-bit FIFO interface is selected).

CDDIS:

The cell delineation disable bit, CDDIS, is used to defeat the cell delineation function of the S/UNI-622. When the CDDIS bit is set to logic one, HCS

errors are ignored, which makes every byte appear like a valid cell boundary. Ignoring HCS errors causes the cell delineation state machine to lock onto an arbitrary cell boundary and to enter and remain in the SYNC state. Once in the SYNC state, the incoming data is written to the FIFO. The CDDIS bit can be used to cause the S/UNI-622 to transparently pass SPE data through the FIFO.

Register 0x60: TACP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	FIFOE	0
Bit 6	R	TSOCI	X
Bit 5	R	FOVRI	X
Bit 4	R/W	DHCS	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell transmit FIFO. When FIFORST is set to logic zero, the transmit FIFO operates normally. When FIFORST is set to logic one, the transmit FIFO is immediately emptied and reset to allow normal operation. Null/unassigned cells are transmitted until a subsequent cell is written to the transmit FIFO.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the transmit FIFO.

HCSB:

The HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is a logic zero, the HCS is generated and inserted internally. When HCSB is a logic one, the HCS octet read from the FIFO is inserted transparently into the transmit cell stream. An HCS is generated for null/unassigned cells regardless of the state of this bit. An HCS is generated for null/unassigned cells regardless of the state of this bit.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

FOVRI:

The FOVRI bit is set high when a FIFO overrun occurs. This bit is reset immediately after a read to this register

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the cell data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FIFOE:

The FIFOE bit enables the generation of an interrupt due to a FIFO overrun error condition or when the TSOC input is sampled high during any position other than the first word of the cell data structure. When FIFOE is set to logic one, the interrupt is enabled.

Register 0x61: TACP Idle/Unassigned Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	0

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

PTI[3:0]:

The PTI[3:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TACP detects that no outstanding cells exist in the transmit FIFO.

Register 0x62: TACP Idle/Unassigned Cell Payload Octet Pattern

Bit	Type	Function	Default
Bit 7	R/W	ICP[7]	0
Bit 6	R/W	ICP[6]	1
Bit 5	R/W	ICP[5]	1
Bit 4	R/W	ICP[4]	0
Bit 3	R/W	ICP[3]	1
Bit 2	R/W	ICP[2]	0
Bit 1	R/W	ICP[1]	1
Bit 0	R/W	ICP[0]	0

ICP[7:0]:

The ICP[7:0] bits contain the pattern inserted in the payload octets of the idle or unassigned cell. Cell rate decoupling is accomplished by transmitting idle/unassigned cells when the TACP detects that no outstanding cells exist in the transmit FIFO. Bit ICP[7] corresponds to the most significant bit of the octet, the first bit transmitted.

Register 0x63: TACP FIFO Control

Bit	Type	Function	Default
Bit 7	R/W	TXPTYP	0
Bit 6	R/W	TXPRTYE	0
Bit 5	R	TXPRTYI[1]	X
Bit 4	R	TXPRTYI[0]	X
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	TCALEVEL0	0
Bit 0	R/W	HCSCTLEB	1

HCSCTLEB:

The active-low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS before insertion into the SPE stream. When set to logic zero, the HCS Control byte provided in the third word of the 27-word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

TCALEVEL0:

The active-high TCA level 0 bit, TCALEVEL0 determines what output TCA indicates when it transitions low. When TCALEVEL0 is set to logic one, output TCA indicates that the transmit FIFO is full and can accept no more writes. When TCALEVEL0 is set to logic zero, output TCA indicates that the transmit FIFO is near full and can accept no more than four additional writes. Please refer to figure 38 for more information on TCALEVEL0.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the transmit FIFO must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal (TCA) transitions to a logic zero. The selectable FIFO cell depths are shown below. Use of 1 or 2 cell FIFO DEPTHs is not recommended because a link utilisation of 100% can not be guaranteed.

Table 7 -

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TXPRTYI[1:0]:

The TXPRTYI[1:0] bits indicate if a parity error was detected on the TDAT[15:0] bus. When logic one, the TXPRTYI[1] bit indicates a parity error over inputs TDAT[15:0] (in word parity mode) or TDAT[15:8] (in byte parity mode). Similarly, when logic one, the TXPRTYI[0] bit indicates a parity error over inputs TDAT[7:0] in byte parity mode. (TXPRTYI[0] is unused in word parity mode, i.e., when the TXBYTEPRTY register bit is logic zero). Both parity error indication bits are cleared when this register is read. Odd or even parity is selected using the TXPTYP bit.

TXPRTYE:

The TXPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors on inputs TDAT[15:0] are indicated using bits TXPRTYI[1:0] and output INTB. When set to logic zero, parity errors are indicated using bits TXPRTYI[1:0] but are not indicated on output INTB.

TXPTYP:

The TXPTYP bit selects even or odd parity for inputs TXPRTY[1:0]. In byte parity mode, when TXPTYP is set to logic one, input TXPRTY[1] is the even parity bit for inputs TDAT[15:8] while input TXPRTY[0] is the even parity bit for inputs TDAT[7:0]. In byte parity mode, when set to logic zero, inputs TXPRTY[1:0] are the odd parity bits for inputs TDAT[15:0]. In word parity mode, when TXPTYP is set to logic one, input TXPRTY[1] is the even parity bit for inputs TDAT[15:0] and TXPRTY[0] is ignored. In word parity mode, when TXPTYP is set to logic zero, input TXPRTY[1] is the odd parity bit for inputs TDAT[15:0] and TXPRTY[0] is ignored.

Register 0x64: TACP Transmit Cell Counter (LSB)

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x65: TACP Transmit Cell Counter

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x66: TACP Transmit Cell Counter (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[20:0]:

The TCELL[20:0] bits indicate the number of cells read from the transmit FIFO and inserted into the SPE during the last accumulation interval. Idle/Unassigned cells inserted into the SPE are not counted. The counter should be polled every second to avoid saturating. The contents of these registers are valid 7 µs after a transfer is triggered by a write to the transmit cell count register space.

The count can also be polled by writing to the S/UNI-622 Master Reset and Identity / Load Performance Meters register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, RACP and TACP blocks.

Register 0x67: TACP Fixed Stuff / GFC

Bit	Type	Function	Default
Bit 7	R/W	TGFCE[3]	0
Bit 6	R/W	TGFCE[2]	0
Bit 5	R/W	TGFCE[1]	0
Bit 4	R/W	TGFCE[0]	0
Bit 3	R/W	FSEN	1
Bit 2	R/W	TXBYTEPRTY	0
Bit 1	R/W	FIXBYTE[1]	0
Bit 0	R/W	FIXBYTE[0]	0

FIXBYTE[1:0]:

The FIXBYTE[1:0] bits identify the byte pattern inserted into fixed byte columns of the synchronous payload envelope.

Table 8 -

FIXBYTE[1]	FIXBYTE[0]	BYTE
0	0	00H
0	1	55H
1	0	AAH
1	1	FFH

TXBYTEPRTY:

The active-high transmit byte parity selector bit, TXBYTEPRTY, selects between byte parity (2 parity bits, each over an 8-bit byte) or word parity (1 parity bit over a 16-bit word). If TXBYTEPRTY is set high, TXPRTY[1] is expected to be the parity over TDAT[15:8] and TXPRTY[0] is expected to be the parity over TDAT[7:0]. If TXBYTEPRTY is set low, TXPRTY[1] is expected to be the parity over TDAT[15:0] and TXPRTY[0] is ignored.

FSEN:

The active-high fix stuff control enable bit, FSEN determines the payload mapping of ATM cells when STS-1 (AU-3) mapping is selected. When FSEN

is set to logic one, the S/UNI-622 does not map ATM cells into columns 30 and 59 of a STS-1 SPE. When FSEN is set to logic zero, the S/UNI-622 maps ATM cells into the entire STS-1 SPE. The FSEN bit is ignored in STS-12c (STM-4c) and STS-3c (STM-1) modes.

TGFCE[3:0]:

The TGFCE[3:0] bits select the source of the GFC bits. For example, when the TGFCE[3] bit is set high, the TGFC input is used to source the GFC[3] bit of transmit cell headers. If the TGFCE[3] bit is set low, the GFC[3] bit of an idle/unassigned cell is programmed in the TACP Idle/Unassigned Cell Header register while the GFC[3] bit of a user cell read from the FIFO is transmitted unaltered.

Register 0x68 SPTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes. When set high, a 16-byte path trace message is selected. If set low, a 64-byte path trace message is selected.

NOSYNC:

The path trace message synchronization disable bit (NOSYNC) disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignored and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit path trace buffer is sent to TPOP for insertion into the J1 transmit path overhead

byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) control the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The receive path trace identifier message mismatch interrupt enable bit (RTIMIE) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state activates the interrupt (INTB) output. When RTIMIE is set low, path trace identifier message state changes will not affect INTB.

RTIUIE:

The receive path trace identifier message unstable interrupt enable bit (RTIUIE) controls the activation of the interrupt output when the receive identifier message state changes from stable to unstable and vice versa. The unstable state is entered when the current identifier message differs from the previous message for six consecutive messages. The stable state is entered when the same identifier message is received for three or five consecutive messages as controlled by the PER5 bit. When RTIUIE is set high, changes in the received path trace identifier message stable/unstable state of will activate the interrupt (INTB) output. When RTIUIE is set low, path trace identifier state changes will not affect INTB.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the S/UNI-622. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 0x69: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

The receive path trace identifier message mismatch status bit (RTIMV) reports the match/mismatch status of the identifier message framer. RTIMV is set high when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is set low when the accepted message matches the expected message.

RTIMI:

The receive path trace identifier mismatch interrupt status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit and the interrupt are cleared when this register is read.

RTIUV:

The receive path trace identifier message unstable status bit (RTIUV) reports the stable/unstable status of the identifier message framer. RTIUV is set high when the current received path trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is set low when the current message becomes the accepted message as determined by the PER5 bit in the SPTB Control register.

RTIUI:

The receive path trace identifier message unstable interrupt status bit (RTIUI) is set high when stable/unstable status of the trace identifier framer changes state. This bit and the interrupt are cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SPTB Indirect Address register, and stays high until the initiated access has completed. At which point, BUSY is set low. This register should be polled to determine when new data is available in the SPTB Indirect Data register.

Register 0x6A: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the path trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the J1 bytes of the transmit stream. For this case, addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the path trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the path trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the addressed location in the static page.

Register 0x6B: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 0x6C: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL7	0
Bit 6	R/W	EPSL6	0
Bit 5	R/W	EPSL5	0
Bit 4	R/W	EPSL4	0
Bit 3	R/W	EPSL3	0
Bit 2	R/W	EPSL2	0
Bit 1	R/W	EPSL1	0
Bit 0	R/W	EPSL0	0

This register contains the expected path signal label byte in the receive stream..

EPSL[7:0]:

The EPSL7 - EPSL0 bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. If enabled, an interrupt is asserted upon declaration and removal of PSLM.

Register 0x6D: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV:

The receive path signal label mismatch status bit (RPSLMV) reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is set high when the accepted PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL.

RPSLMI:

The receive path signal label mismatch interrupt status bit (RPSLMI) is set high when the match/mismatch status between the accepted and the expected path signal label changes state. This bit (and the interrupt) are cleared when this register is read.

RPSLUV:

The receive path signal label unstable status bit (RPSLUV) reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is set high when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is set low when the same PSL code is received for five consecutive frames.

RPSLUI:

The receive path signal label unstable interrupt status bit (RPSLUI) is set high when the stable/unstable status of the path signal label changes state. This bit and the interrupt are cleared when this register is read.

RPSLMIE:

The receive path signal label mismatch interrupt enable bit (RPSLMIE) controls the activation of the interrupt output when the comparison between accepted and the expected path signal label changes state from match to mismatch and vice versa. When RPSLMIE is set high, changes in match state activates the interrupt (INTB) output. When RPSLMIE is set low, path signal label state changes will not affect INTB.

RPSLUIE:

The receive path signal label unstable interrupt enable bit (RPSLUIE) controls the activation of the interrupt output when the received path signal label changes state from stable to unstable and vice versa. When RPSLUIE is set high, changes in stable state activates the interrupt (INTB) output. When RPSLUIE is set low, path signal label state changes will not affect INTB.

Register 0x70: BERM Control

Bit	Type	Function	Default
Bit 7	R/W	BERTEN	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	BERIE	0

This register controls the automatic bit error rate alarm circuitry.

BERIE:

The Bit Error Rate interrupt enable bit enables and disables BERI interrupts. When BERIE is set high, BERI interrupts are reflected on output INTB. When BERIE is set low, BERI interrupts are not reflected on output INTB.

BERTEN:

The Bit Error Rate test enable bit enables and disables automatic monitoring of line BIP errors. When BERTEN is set high, the S/UNI-622 continuously accumulates line BIP errors over a period defined in the BERM Line BIP Accumulation Period registers. If, at any point, the accumulated count equals the value defined in the BERM Line BIP Threshold registers, an interrupt is asserted. Both the BERM Line BIP Accumulation Period and BERM Line BIP Threshold registers should be set up before the BERTEN bit is set high. When BERTEN is set low, the BIP accumulation logic is disabled.

Register 0x71: BERM Interrupt

Bit	Type	Function	Default
Bit 7	W	BERM_TST[3]	0
Bit 6	W	BERM_TST[2]	0
Bit 5	W	BERM_TST[1]	0
Bit 4	W	BERM_TST[0]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	BERI	X

This register indicates the automatic bit error rate interrupts.

BERIE:

The Bit Error Rate interrupt bit indicates that the incoming bit error rate has exceeded the user programmed maximum. When BERI is set high, the S/UNI-622 has accumulated more line BIP errors then the number indicated in the Line BIP Threshold registers over the period defined by the BIP Accumulation Period registers. BERI is cleared when this register is read.

BERM_TST[3:0]:

The BERM_TST[3:0] bits are used for production test of the BERM block. The BERM_TST[3] bit is the LB_AP_REGLOAD / LB_AP_REG_COMPARE bit. The BERM_TST[2] bit is the LB_AP_REGHOLD bit. The BERM_TST[1] bit is the LB_TH_REGLOAD / LB_TH_REG_COMPARE bit. The BERM_TST[0] bit is the LB_TH_REGHOLD bit. Please see the Test Vector Description section for details. These bits are write-only bits.

Register 0x72: BERM Line BIP Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	LB_AP[7]	0
Bit 6	R/W	LB_AP[6]	0
Bit 5	R/W	LB_AP[5]	0
Bit 4	R/W	LB_AP[4]	0
Bit 3	R/W	LB_AP[3]	0
Bit 2	R/W	LB_AP[2]	0
Bit 1	R/W	LB_AP[1]	0
Bit 0	R/W	LB_AP[0]	0

Register 0x73: BERM Line BIP Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	LB_AP[15]	0
Bit 6	R/W	LB_AP[14]	0
Bit 5	R/W	LB_AP[13]	0
Bit 4	R/W	LB_AP[12]	0
Bit 3	R/W	LB_AP[11]	0
Bit 2	R/W	LB_AP[10]	0
Bit 1	R/W	LB_AP[9]	0
Bit 0	R/W	LB_AP[8]	0

LB_AP[15:0]:

The LB_AP[15:0] bits represent the number of 125 µs frames which define a line BIP accumulation period. Please refer to the Operations section for recommended values of LB_AP[15:0] to detect various bit error rates.

Register 0x74: BERM Line BIP Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	LB_TH[7]	0
Bit 6	R/W	LB_TH[6]	0
Bit 5	R/W	LB_TH[5]	0
Bit 4	R/W	LB_TH[4]	0
Bit 3	R/W	LB_TH[3]	0
Bit 2	R/W	LB_TH[2]	0
Bit 1	R/W	LB_TH[1]	0
Bit 0	R/W	LB_TH[0]	0

Register 0x75: BERM Line BIP Threshold MSB

Bit	Type	Function	Default
Bit 7	R/W	LB_TH[15]	0
Bit 6	R/W	LB_TH[14]	0
Bit 5	R/W	LB_TH[13]	0
Bit 4	R/W	LB_TH[12]	0
Bit 3	R/W	LB_TH[11]	0
Bit 2	R/W	LB_TH[10]	0
Bit 1	R/W	LB_TH[9]	0
Bit 0	R/W	LB_TH[8]	0

LB_TH[15:0]:

The LB_TH[15:0] bits represent the allowable number of line BIP errors that can be accumulated during a line BIP accumulation period before an BERI interrupt is asserted. Please refer to the Operations section for recommended values of LB_TH[15:0] to detect various bit error rates.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-622. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the S/UNI-622 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the S/UNI-622 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced with the exception of the POUT[7:0] bus via the JTAG test port.

11.1 Test Mode Register Memory Map

Table 9 -

Address	Register
0x00-0x7F	Normal Mode Registers
0x80	Master Test
0x88	PISO Test Register 0
0x89	PISO Test Register 1
0x8A	PISO Test Register 2
0x8B	Reserved
0x8C	SIPO Test Register 0
0x8D	SIPO Test Register 1
0x8E-0x8F	Reserved
0x90	RSOP Test Register 0
0x91	RSOP Test Register 1

Address	Register
0x92	RSOP Test Register 2
0x93	RSOP Test Register 3
0x94	TSOP Test Register 0
0x95	TSOP Test Register 1
0x96	TSOP Test Register 2
0x97	TSOP Test Register 3
0x98	RLOP Test Register 0
0x99	RLOP Test Register 1
0x9A	RLOP Test Register 2
0x9B-0x9F	Reserved
0xA0	TLOP Test Register 0
0xA1	TLOP Test Register 1
0xA2	TLOP Test Register 2
0xA3	TLOP Test Register 3
0xA4	BIDX Test Register 0
0xA5	BIDX Test Register 1
0xA6	BIMX Test Register 0
0xA7	BIMX Test Register 1
0xA8	SSTB Test Register 0
0xA9	SSTB Test Register 1
0xAA	SSTB Test Register 2
0xAB	SSTB Test Register 3
0xAC-0xAF	Reserved
0xB0	RPOP Test Register 0
0xB1	RPOP Test Register 1
0xB2	RPOP Test Register 2
0xB3-0xBF	Reserved
0xC0	TPOP Test Register 0

Address	Register
0xC1	TPOP Test Register 1
0xC2	TPOP Test Register 2
0xC3	TPOP Test Register 3
0xC4	TPOP Test Register 4
0xC5-0xCF	Reserved
0xD0	RACP Test Register 0
0xD1	RACP Test Register 1
0xD2	RACP Test Register 2
0xD3	RACP Test Register 3
0xD4	RACP Test Register 4
0xD5-0xDF	Reserved
0xE0	TACP Test Register 0
0xE1	TACP Test Register 1
0xE2	TACP Test Register 2
0xE3	TACP Test Register 3
0xE4-0xE7	Reserved
0xE8	SPTB Test Register 0
0xE9	SPTB Test Register 1
0xEA	SPTB Test Register 2
0xEB	SPTB Test Register 3
0xEC-0xFF	Reserved

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x80: Master Test

Bit	Type	Function	Default
Bit 7	W	DS27_53	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-622 test features. All bits, except PMCTST, are reset to zero by a reset of the S/UNI-622.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-622 . While the HIZIO bit is a logic one, all output pins of the S/UNI-622 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-622 for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-622 to drive the data bus and holding the CSB pin low tri-states the data bus. The

DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-622 for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-622 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

DS27_53:

The DS27_53 bit is use to select between the long data structure (27 words in 16-bit mode and 53 bytes in 8-bit mode) and the short data structure (26 words in 16-bit mode and 52 bytes in 8-bit mode). When DS27_53 is set to logic one, the RACP-622 and TACP-622 blocks are configured to operate with the long data structure; when DS27_53 is set to logic zerio, the RACP-622 and TACP-622 blocks are configured to operate with the short data structure.

11.2 Test Mode 0 Details

In test mode 0, the S/UNI-622 allows the logic levels on the device inputs to be read through the microprocessor interface and allows the device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one and the following addresses must be written with 00H: 89H, 8DH, 91H, 95H, 99H, A1H, A5H, A7H, A9H, B1H, C1H, D1H, E1H, E9H. Clock edges must be provided on inputs TCLK and PICLK when these clocks are not being tested.

Reading the following address locations returns the values on the indicated inputs:

Table 10 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08H					PIP[3]	PIP[2]	PIP[1]	PIP[0]
0FH				TTOH[4]	TTOH[3]	TTOH[2]	TTOH[1]	TTOHEN
8BH							TSICLK[1]	
8CH							RSICLK[2]	RSIN[3]
90H							FPIN[4]	PICLK
92H	PIN[7]	PIN[6]	PIN[5]	PIN[4]	PIN[3]	PIN[2]	PIN[1]	PIN[0]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
94H	TSUC[5]	TSOW[5]	TSD			TLAIS		
A0H		TLOW	TLD	TLDRI[6]				TCLK
C0H				TPRDI[7]	TPAIS			
C3H							TPOH[8]	TPOHEN[9]
C4H								TFP
E0H				XOFF	TGFC			

The following inputs cannot be read using the IOTST feature: TDAT[15:0], TSOC, TXPRTY[1:0], TWRENB, TFCLK, FPOS, RFCLK, TSEN, RRDENB, D[7:0], A[7:0], ALE, CSB, WRB, RDB, RSTB, TRSTB, TMS, TCK, and TDI.

1. To read TSICLK, TMODE[1:0] should be set to binary '10' in the Master Configuration Register and LOOPT should be set to 0 in the Master Control/Monitor Register.

2. To read RSICLK, RMODE[1:0] should be set to binary '10' in the Master Configuration Register and DLE should be set to 0 in the Master Control/Monitor Register.

3. To read RSIN, RMODE[1:0] should be set to binary '10' in the Master Configuration Register and DLE should be set to 0 in the Master Control/Monitor Register. Additionally, RSICLK must be toggled to a logic zero and then back to a logic one to capture the value on the RSIN input.

4. To read FPIN, FPOS must be set to a logic zero.

5. TOWCLK must be toggled to a logic zero and then back to a logic one in order to capture the value on these inputs.

6. To read TLDRI, AUTOLRDI must be set to 0 in the Master Auto Alarm Register.

7. To read TPRDI, AUTOPRDI must be set to 0 in the Master Auto Alarm Register.

8. To read TPOH, TPOHEN must be set to a logic one.

9. To read TPOHEN, TPTBEN must be set to 0 in the Master Configuration Register.

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 11 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06H			POP[5]	POP[4]	POP[3]	POP[2]	POP[1]	POP[0]
8BH					INT[1]		TSOUT[2]	
8CH								GROCLK[3]
90H			LOF	OOF	LOS			
92H			RSOW		RSD	RSDCLK	RSUC	
94H					TSDCLK			
96H	POUT[7]	POUT[6]	POUT[5]	POUT[4]	POUT[3]	POUT[2]	POUT[1]	POUT[0]/
								FPOUT
98H				LRDI	LAIS	OHFP[3]		
9AH					RLD	RLDCLK	RLOW	ROWCLK
9BH			RTOHFP[3]	RTOHCLK[3]	RTOH[4][3]	RTOH[3][3]	RTOH[2][3]	RTOH[1][3]
A0H				TOWCLK	TLDCLK			
A6H			TTOHCLK	TTOHFP		GTOCLK[4]		
B0H				PAIS				
B2H			LOP					
B3H					PRDI	RPOHFP	RPOH	RPOHCLK
C3H					TPOHCLK	TPOHFP		
D0H				RCP	RGFC		LCD	
E0H							TCP	

The following outputs can not be controlled using the IOTST feature: TCA, RSOC, RDAT[15:0], RXPRTY[1:0], RCA, D[7:0], and TDO.

1. INT corresponds to output INTB. INTB is an open drain output and should be pulled high for proper operation. Writing a logic one to the INT bit allows the S/UNI-622 to drive INTB low. Writing a logic zero to the INT bit tristates the INTB output.

2. After the TSOUT value has been written to the test bit, TSICLK must be toggled to a logic low and then back to a logic high before the test value appears on the TSOUT output pin.

3. To control these outputs, RMODE[1:0] should be set to binary '10' in the Master Configuration Register.

4. To control GTOCLK, TMODE[1:0] should be set to binary '11' in the Master Configuration Register.

11.3 JTAG Test Port

The S/UNI-622 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 12 - Instruction Register

Length - 3 bits		
Instructions	**Selected**	**Instruction**
Register	Codes, IR[2:0]	
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 0H

Part Number - 5355H

Manufacturer's identification code - 0CDH

Device identification - 053550CDH

Boundary Scan Register

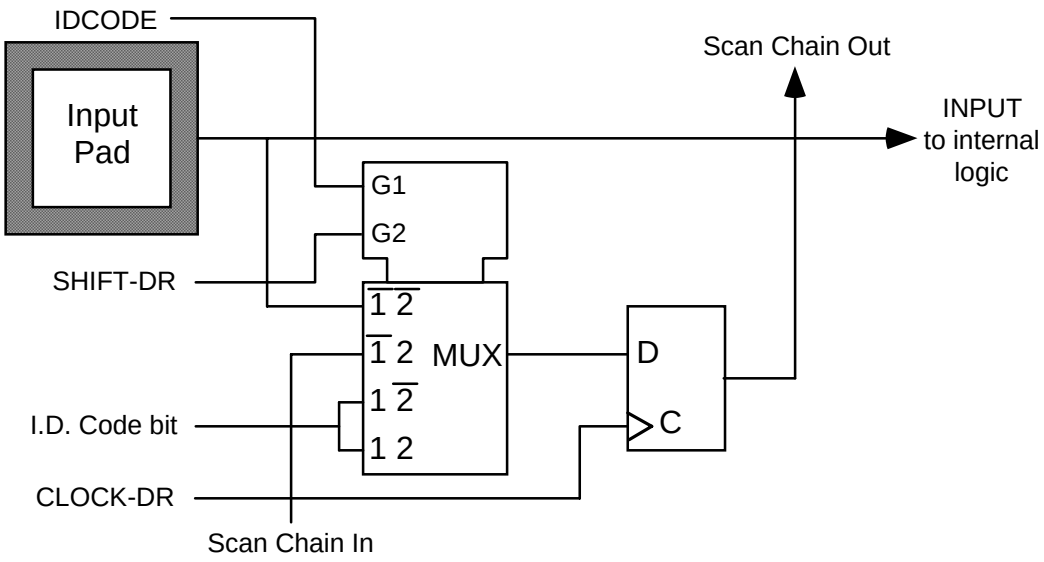
The boundary scan register is made up of 155 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells form the ID code register, and carry the code 053550CD. The cells are arranged as follows:

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit

NOTES:

1. OENB is the active low output enable for D[7:0].
2. RDATENB is the active low output enable for RSOC, RDAT[15:0], and RXPRTY[1:0].
3. When set high, INTB will be set to high impedance.
4. HIZ is the active low output enable for all OUT_CELL types except D[7:0], RXPRTY[1:0], RDAT[15:0], and INTB
5. A[7] is the first bit of the boundary scan chain.

Figure 13 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 14 - Output Cell (OUT_CELL)

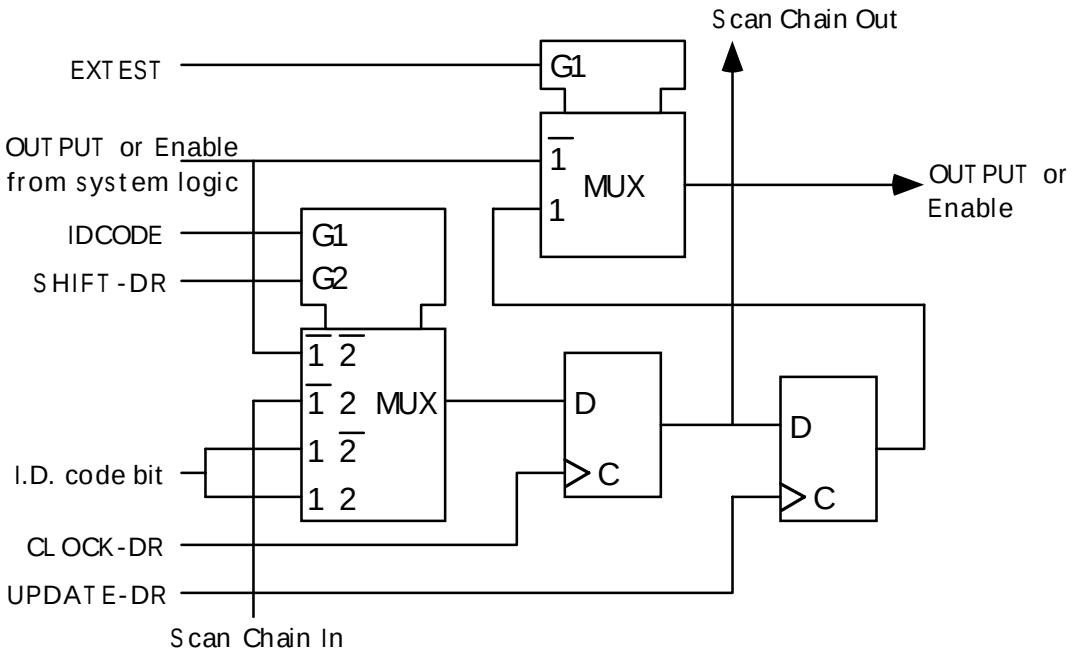


Figure 15 - Bidirectional Cell (IO_CELL)

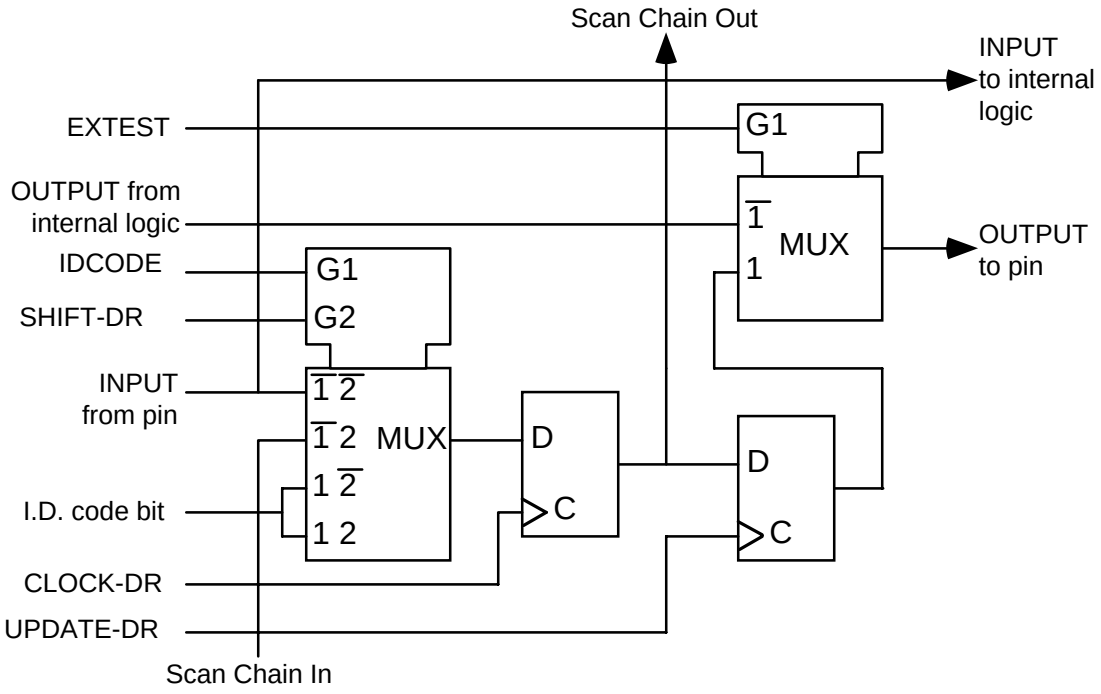
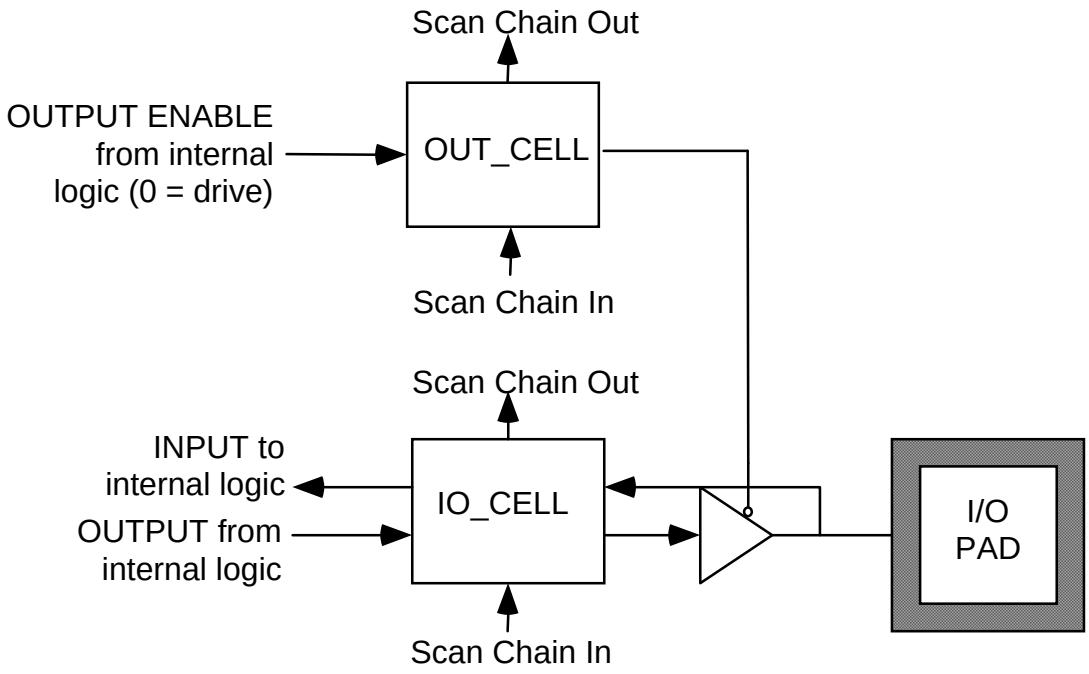


Figure 16 - Layout of Output Enable and Bidirectional Cells



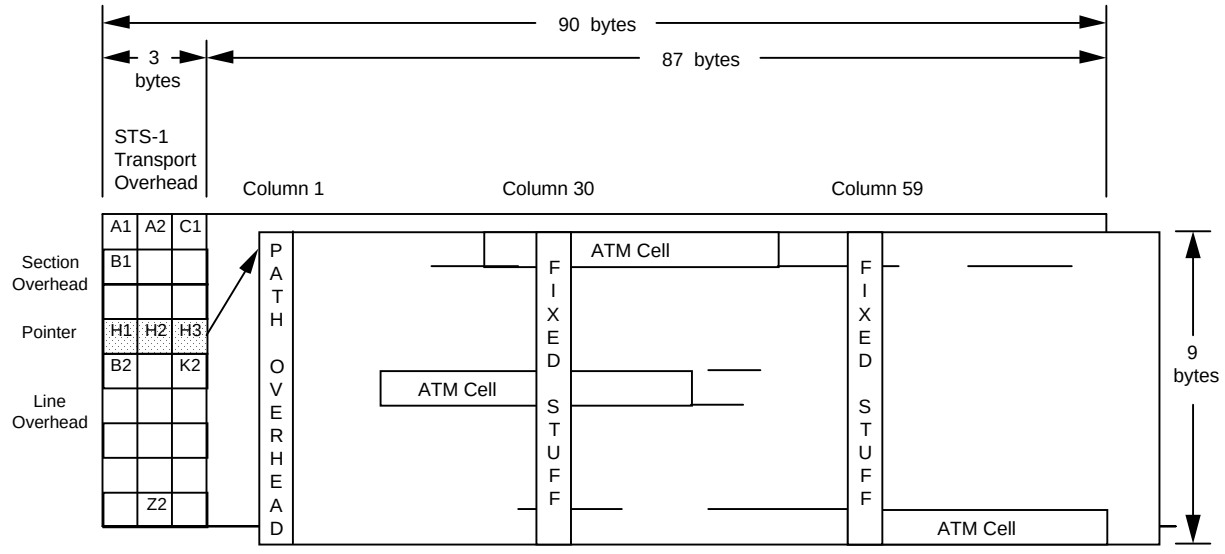
12 OPERATION

ATM Mapping and Overhead Byte Usage

The S/UNI-622 processes the ATM cell mappings for STS-12c (STS-4c), STS-3c (STM-1) and STS-1 as shown below in Figures 10 through 12. The S/UNI-622 processes the subset of the complete transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-622 provides support for the APS bytes, the data communication channels and provides full external control and observability of the transport and path overhead bytes.

Figure 17 shows the STS-1 mapping. The S/UNI-622 supports two STS-1 mappings, one with the indicated stuff columns containing fixed stuff bytes and the other with the indicated stuff columns used for ATM cells.

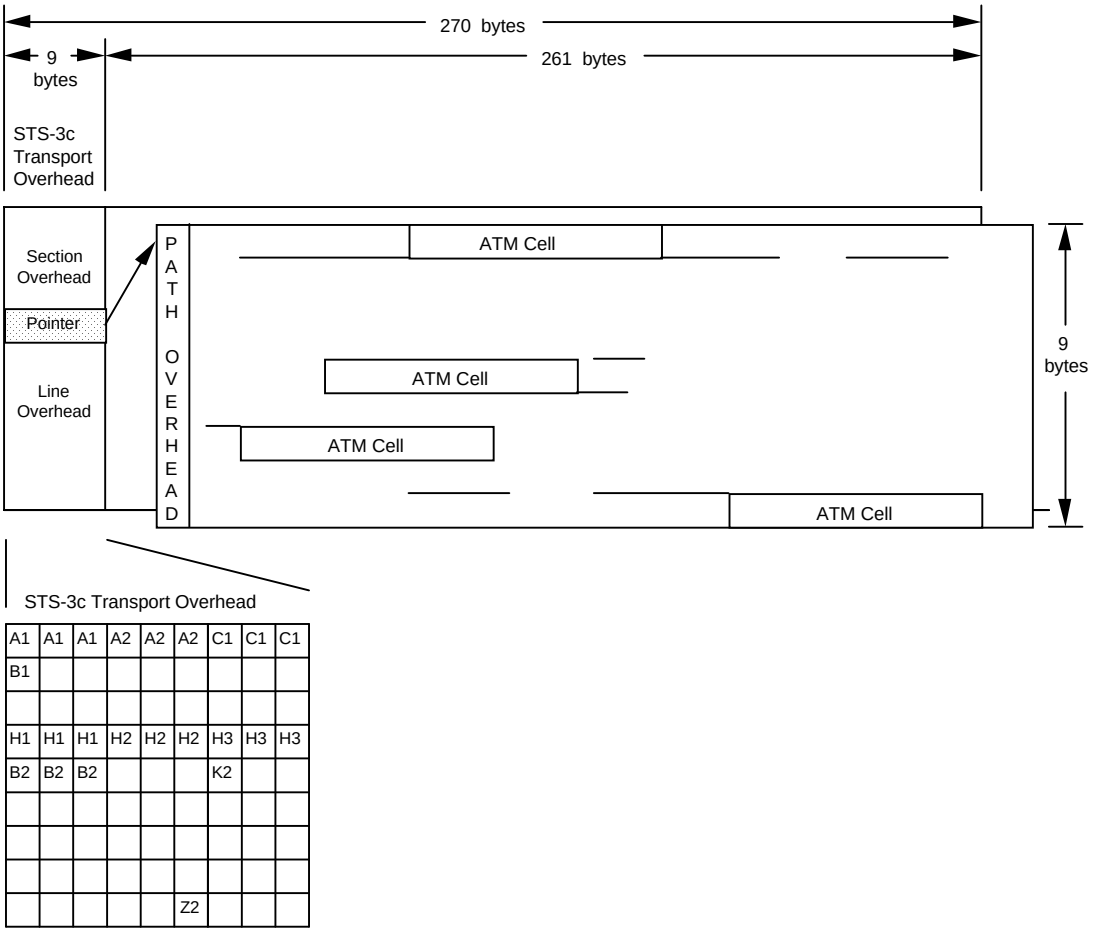
Figure 17 - STS-1 Mapping



* Fixed stuff columns optionally filled with cells

Figure 18 shows the STS-3c (STM-1) mapping. In this mapping, no stuff columns are included in the SPE. The entire SPE is used for ATM cells.

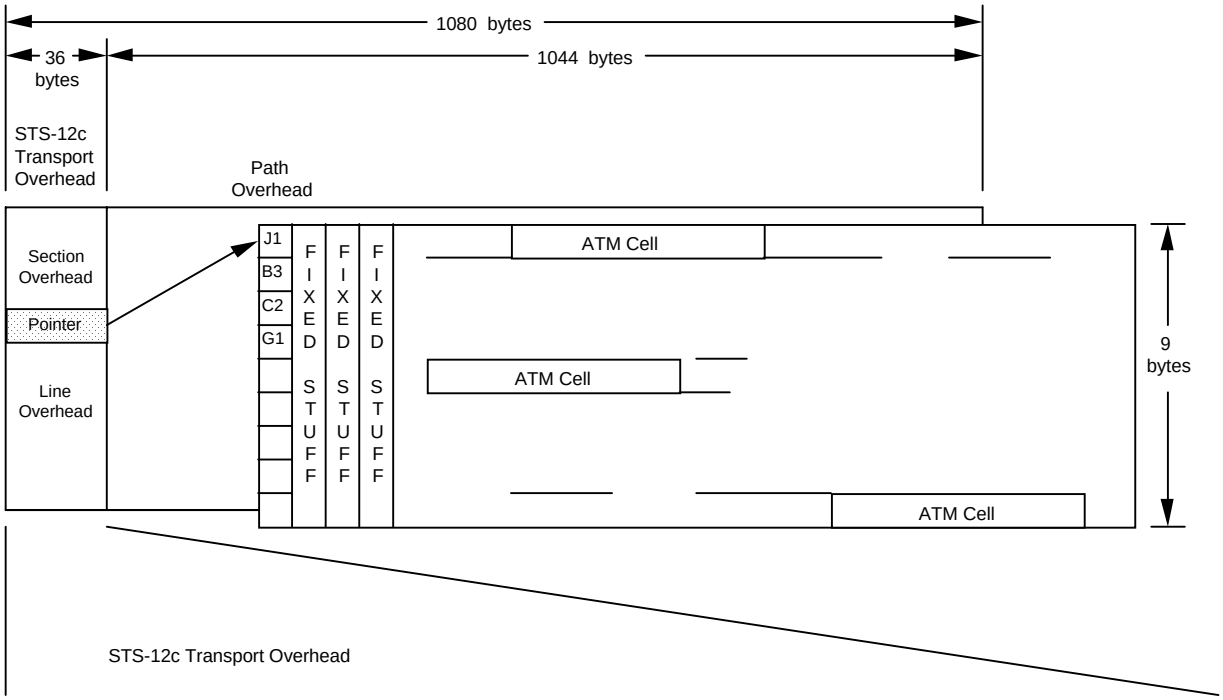
Figure 18 - STS-3c (STM-1) Mapping



A1	A1	A1	A2	A2	A2	C1	C1	C1
B1								
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2				K2		
					Z2			

Figure 19 shows the STS-12c (STM-4c) mapping. For this mapping, three stuff columns are provided. In this mode of operation, the S/UNI-622 always stuffs the fixed stuff columns with the byte contained in the TACP Fixed Stuff / GFC register. No other options are provided.

Figure 19 - STS-12c (STM-4c) ATM Mapping



A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1
B1																																	
H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2												K2										
													Z2																				

Transport Overhead Bytes

A1, A2:

The frame alignment bytes (A1, A2) locate the SONET frame in the STS-12c/3c/1 bit-serial stream.

In the transmit direction, the S/UNI-622 inserts these bytes into the outgoing stream either automatically or using the TTOH[4:1] inputs.

The A1 and A2 bytes are not scrambled by the frame synchronous SONET scrambler.

In the receive direction when configured for STS-1 bit-serial operation, the S/UNI-622 searches for the A1, A2 bit sequence in the incoming stream to find the SONET frame boundary. When configured for STS-1, STS-3c (STM-1), or STS-12c (STM-4c) byte-serial operation, the S/UNI-622 relies on an upstream pre-framer to determine the byte alignment by finding the A1, A2 bit sequence in the SONET bit stream. Given the byte alignment, the S/UNI-622 verifies the SONET frame boundary. For all modes, the received A1 and A2 bytes are output on RTOH[4:1].

C1:

The C1 bytes are currently defined as the STS-1 identification bytes for SONET and as the section trace message byte for SDH. For either case, C1 is not scrambled by the frame synchronous scrambler.

In the transmit direction for an STS-N signal, the S/UNI-622 inserts the sequence 0x01,. . . 0xN for SONET applications and the value programmed in the S/UNI-622 Transmit C1 register for SDH applications. Pattern selection can be made using the S/UNI-622 Master Configuration register. For the first C1 byte, the S/UNI-622 can optionally overwrite the selected pattern with the section trace message. Internal insertion of all C1 bytes can be overridden by patterns applied to inputs TTOH[4:1].

In the receive direction, C1 bytes are output on RTOH[4:1]. In addition, the first C1 byte can be accumulated in the SSTB RAM.

B1:

The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI-622 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling. B1 bit errors can be induced using the TTOH[4:1] inputs.

In the receive direction, the S/UNI-622 calculates the B1 code over the current SONET frame and compares this calculation with the B1 byte received in the following frame. Receive B1 errors are accumulated in an error event counter. The received B1 code is output on RTOH[4:1].

H1, H2:

The pointer value bytes locate the start of the synchronous payload envelope (SPE) in the SONET/SDH frame.

In the transmit direction, the S/UNI-622 inserts a fixed pointer value, with a normal new data flag indication in the first H1-H2 pair. The concatenation indication is inserted in the remaining H1-H2 pairs. Pointer movements can be induced using the TPOP registers. H1 and H2 bit errors can be induced using the TTOH[4:1] inputs.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1 and H2 contain all ones patterns. The received H1 and H2 codes are output on RTOH[4:1].

H3:

The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2:

The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI-622 calculates the B2 bytes over the line overhead bits and the entire SPE before scrambling. The calculated code is then placed in the current frame. B2 bit errors can be induced using the TTOH[4:1] inputs.

In the receive direction, the S/UNI-622 calculates the B2 code over the current SONET frame and compares this calculation with the B2 code received in the following frame. Receive B2 errors are accumulated in an error event counter. The received B2 code is output on RTOH[4:1].

K2:

The K2 byte is used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7 and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7 and 8 of the K2 byte are set to the pattern '111' and the entire SPE is set to an all ones pattern.

In the transmit direction, the S/UNI-622 provides inputs TLAIS and TLRDI and internal register bits to control assertion and removal of Line AIS and Line RDI. In addition, the K2 byte can be asserted using the TTOH[4:1] inputs or the TLOP Transmit K2 register. Line AIS and Line RDI insertion has higher precedence than K2 byte assertion via inputs, TTOH[4:1] which in turn has higher precedence than insertion using the TLOP Transmit K2 register.

In the receive direction, the S/UNI-622 examines the K2 byte to determine the presence of the line AIS, or the line RDI maintenance signals. In addition, the K2 byte is captured into the S/UNI-622 Receive K2 register and is also output on RTOP[4:1].

Z2:

The growth byte provides a line far end block error function for remote performance monitoring. When configured for STS-1 mode, the first and only Z2 byte is used. When configured for STS-3c (STM-1) or STS-12c (STM-4c) mode, the third Z2 byte is used.

In the transmit direction, the S/UNI-622 allows the Z2 byte to be sourced from the TTOH[4:1] inputs or to be internally generated. When internal generation is enabled, the number of B2 errors detected in the previous interval is inserted. This number has 9 (0 to 8), 25 (0 to 24) or 97 (0 to 96) legal values depending on the selected operating mode.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter. In addition, the received Z2 bytes are output on RTOH[4:1].

Path Overhead Bytes

J1:

The Path Trace byte is used to repetitively transmit a 64-byte or 16-byte, fixed-length string. When not used, this byte should be set to 64 NULL characters. NULL is defined by the ASCII code, 0x00.

On the transmit side, characters can be transmitted using either the TPOH input , the TPOP Path Trace register or the SPTB block. The register is the default selection and resets to 0x00 to facilitate transmission of NULL characters following reset.

On the receive side, the J1 byte is brought out serially via the RPOH output and is accumulated in the SPTB RAM.

B3:

The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI-622 calculates the B3 bytes over all bits of the SPE capacity (including the fixed bytes if configured). The calculated code is then placed in the current frame. B3 bit errors can be induced using the TPOH inputs.

In the receive direction, the S/UNI-622 calculates the B3 code over all the bits of the SPE capacity (including the fixed bytes if configured) and compares this calculation with the B3 byte received in the following frame. Receive B3 errors are accumulated in an error event counter. The received B3 code is output on RPOH.

C2:

The path signal label indicator identifies the SPE mapping. For ATM mappings, the identification code is 0x13.

On the transmit side, the S/UNI-622 inserts this code using the TPOP Path Signal Label register or the TPOH input. On reset, the register resets to 0x13 and is the default source.

On the receive side, the received code is made available in the RPOP Path Signal Label register and is output on RPOH. In addition, the SPTB block also provides circuits to detect unstable Path Signal Labels.

G1:

The path status byte provides a path far end block error (path FEBE) function, and provides control over the path remote defect indication signal.

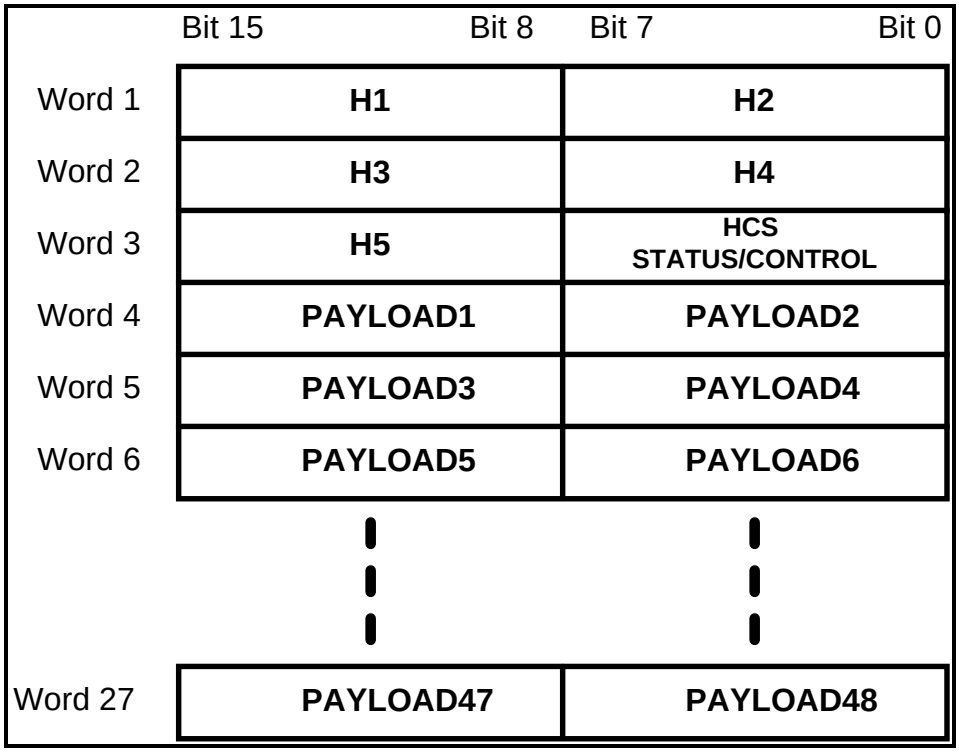
In the transmit direction, the S/UNI-622 provides the TPRDI input and a register bit to assert the path remote defect indication. For path FEBE, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path FEBE code has 9 legal values, namely 0 to 8 errors. In addition, the entire G1 byte can be inserted using the TPOH input. Insertion using the TPOH input has the highest precedence.

In the receive direction, a legal path FEBE value is added to the path FEBE event counter. In addition, the path remote defect indication is detected and the entire G1 byte is output on RPOH.

Cell Data Structure

ATM cells may be passed to/from the S/UNI-622 using the twenty-seven word data structure shown in Figure 20:

Figure 20 -16- bit Wide, 27-Word Structure



Twenty-seven 16-bit words are contained in this data structure. Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all zeros pattern in these 8 bits indicates that the associated header is error free. An all ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RACP Control Register is set to logic zero, the all

ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TACP Control Register determines whether the HCS is calculated internally, or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted).

Bit Error Rate Monitor

The S/UNI-622 Bit Error Rate Monitor (BERM) block counts line BIP errors over programmable periods of time and monitors whether the accumulated count of line BIP errors exceeds a programmable threshold within that specific period. The BERM block can be used to monitor the bit error rate (BER) of the line. The following tables list the recommended contents of the BERM Line BIP Accumulation Period and BERM Line BIP Threshold Period registers to detect various BERs.

In STS-1 mode, the following register contents are recommended:

Table 13 -

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-4}	0x87	0x01	0xCA	0x00
10^{-5}	0x19	0x0F	0xD9	0x00
10^{-6}	0xFA	0x9C	0xDB	0x00

In STS-3c mode, the following register contents are recommended:

Table 14 -

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-4}	0x85	0x00	0xCA	0x00
10^{-5}	0x08	0x05	0xD9	0x00

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-6}	0x53	0x34	0xDB	0x00

In STS-12c mode, the following register contents are recommended:

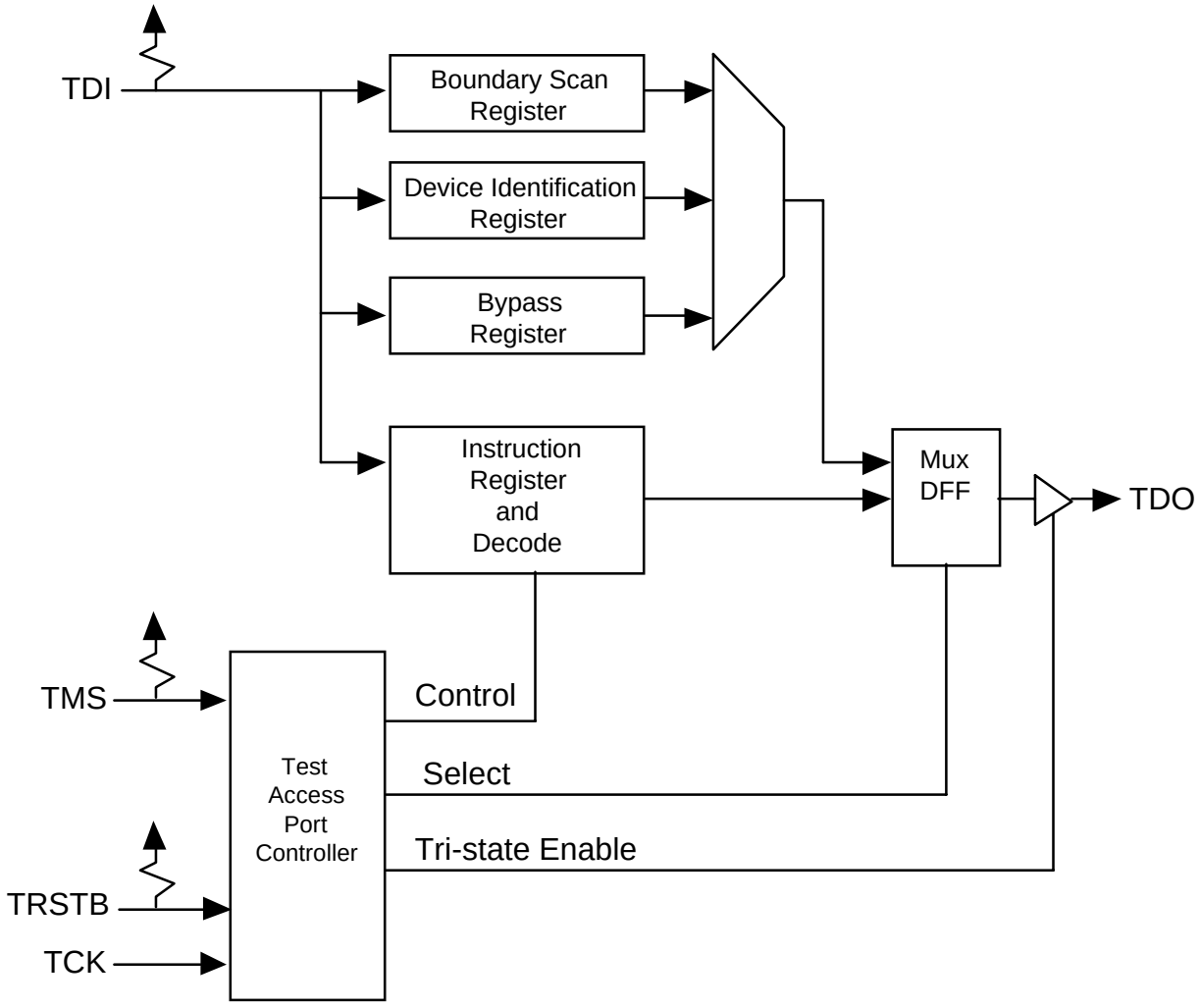
Table 15 -

BER	Accumulation Period LSB	Accumulation Period MSB	Threshold LSB	Threshold MSB
10^{-4}	0x21	0x00	0xCA	0x00
10^{-5}	0x44	0x01	0xD9	0x00
10^{-6}	0x99	0x0D	0xDB	0x00
10^{-7}	0xD0	0x82	0xDB	0x00

JTAG Support

The S/UNI-622 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 21 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

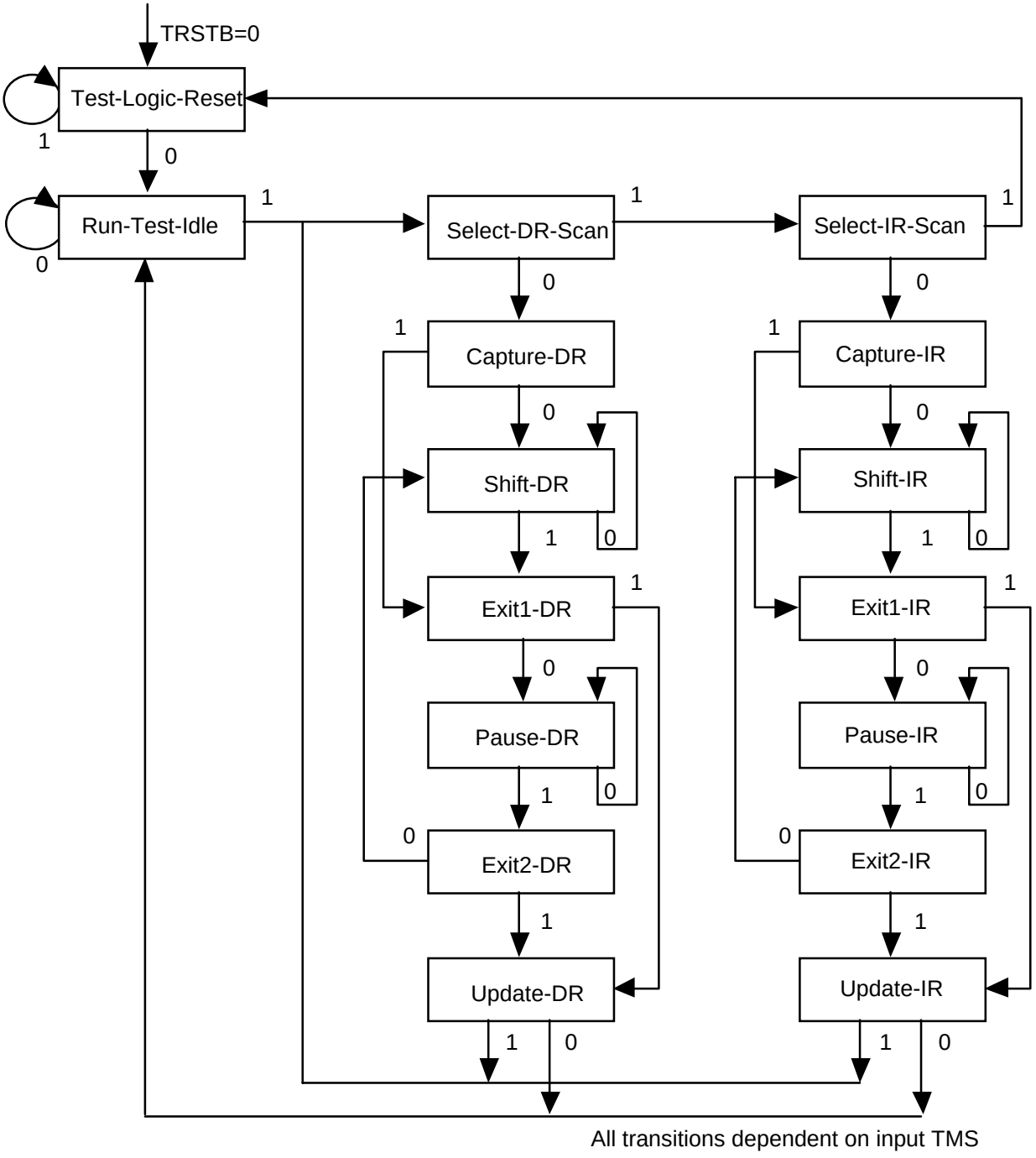
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 22 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

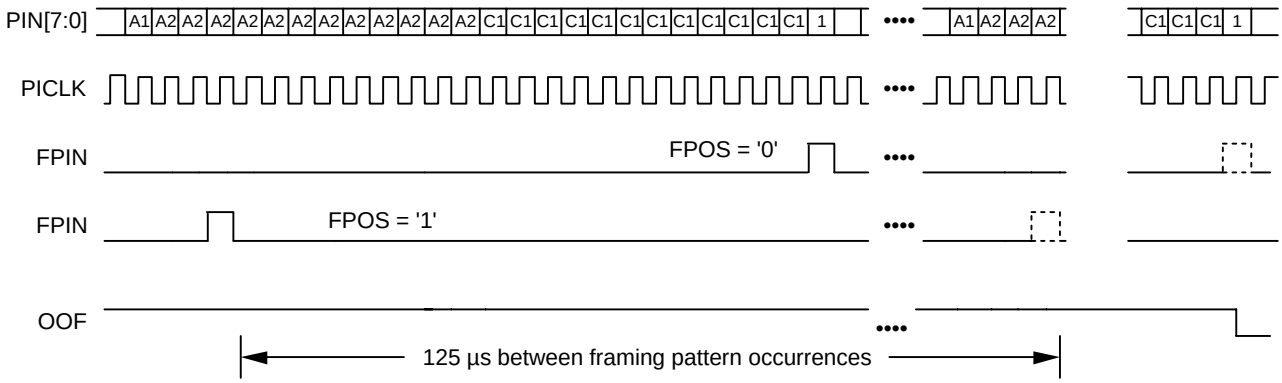
STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13 FUNCTIONAL TIMING

13.1 Line Side Receive Interface

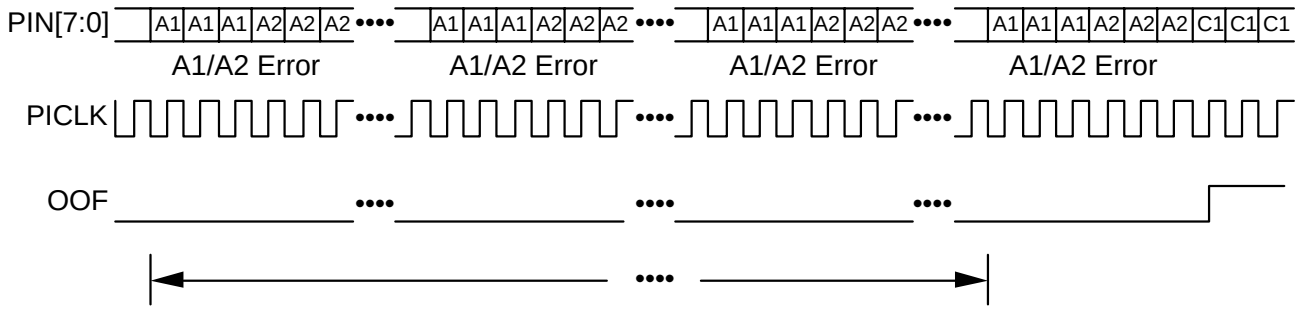
Figure 23 - In Frame Declaration



The In Frame Declaration Timing Diagram (Figure 23) illustrates the declaration of the in-frame state by the S/UNI-622 when processing a 77.76-Mbyte/s STS-12c (STM-4c) stream on PIN[7:0]. An upstream serial-to-parallel converter indicates the location of the SONET frame using the FPIN input. The byte position marked by FPIN may be controlled using the FPOS input as illustrated in timing diagram. The frame verification is initialized by a pulse on FPIN while the S/UNI-622 is out of frame. The in-frame state is declared if the framing pattern is observed in the correct byte positions in the following frame, and in the intervening period (125 µs) no additional pulses were present on FPIN. The S/UNI-622 ignores pulses on FPIN while in frame. This algorithm results in a maximum average reframe time of 250 µs in the absence of mimic framing patterns.

A diagram for a STS-3c (STM-1) interface would be the same as illustrated above. As selected by the FPOS input, the FPIN would identify either the third A2 byte or the byte after the C1 bytes on the PIN[7:0] input bus. However, the diagram for a STS-1 byte-serial interface would differ in that the FPIN input always identifies the byte after the C1 byte when configured for STS-1 byte-serial operation.

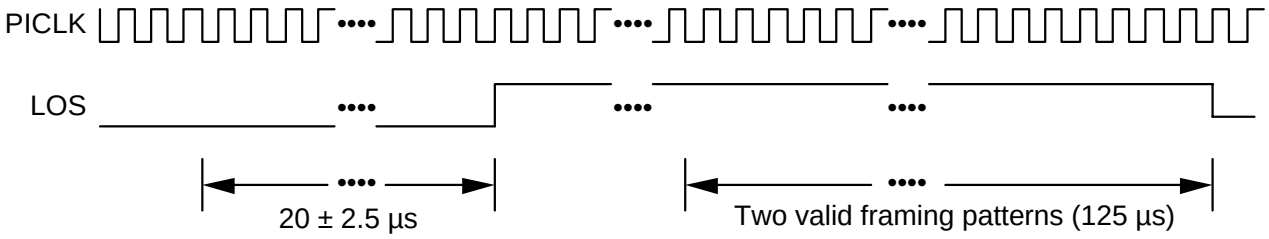
Figure 24 - Out of Frame Declaration



Four consecutive frames containing framing pattern errors

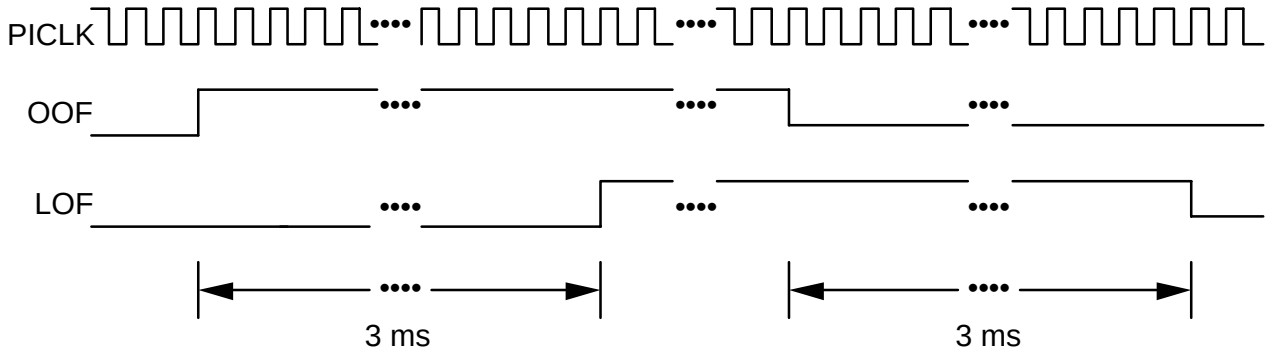
The Out of Frame Declaration Timing Diagram (Figure 24) illustrates the declaration of out of frame for a STS-3c stream. In an STS-1 stream, the framing pattern is a 16-bit pattern that repeats once per frame. In an STS-3c (STM-1) stream, the framing pattern is a 48-bit pattern that repeats once per frame. In an STS-12c stream, the framing pattern is a 196-bit pattern that repeats once per frame. For the purposes of OOF declaration, the framing pattern may be modified using the ALGO2 bit in the RSOP Control Register. Out of frame is declared when one or more errors are detected in this pattern for four consecutive frames as illustrated. In the presence of random data, out of frame will normally be declared within 500 µs.

Figure 25 - Loss of Signal Declaration/Removal



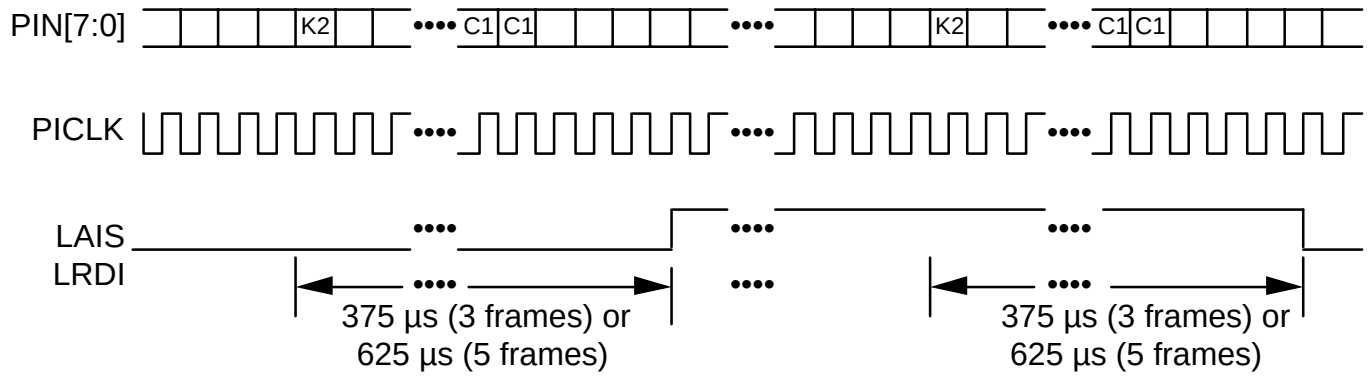
The Loss of Signal Declaration/Removal Timing Diagram (Figure 25) illustrates the operation of the LOS output. LOS is declared when a violating period of all zeros (20 ± 2.5 µs) is observed on PIN[7:0]. LOS is removed when two valid framing patterns are observed, and in the intervening period (125 µs), no violating periods of all zeros is observed.

Figure 26 - Loss of Frame Declaration/Removal



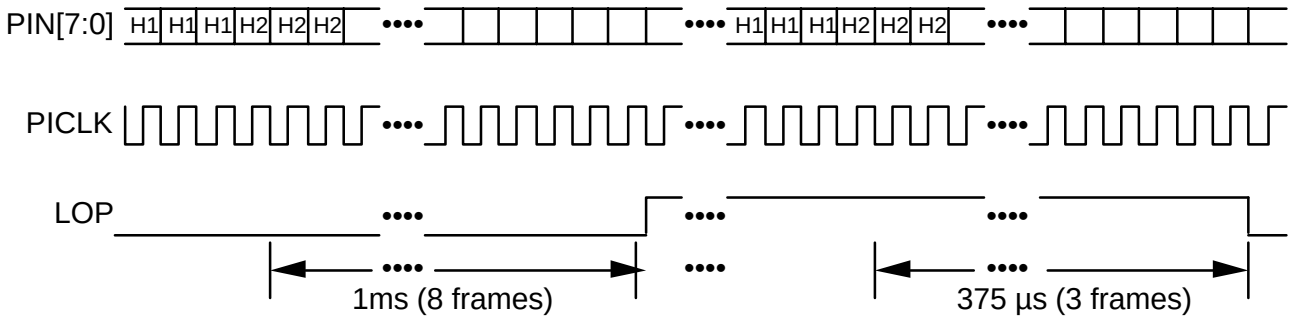
The Loss of Frame Declaration/Removal Timing Diagram (Figure 26) illustrates the operation of the LOF output. LOF is an integrated version of OOF. LOF is declared when an out-of-frame condition persists for 3 ms. LOF is removed when an in frame condition persists for 3 ms.

Figure 27 - Line AIS and Line RDI Declaration/Removal



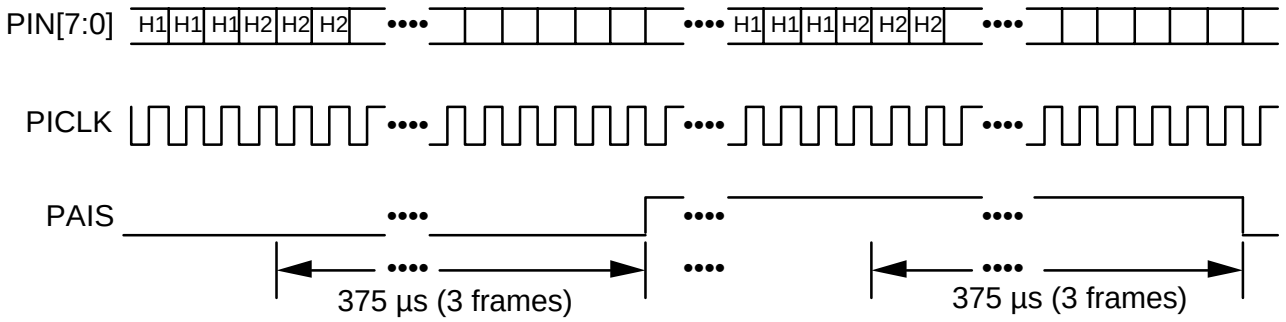
The Line AIS and Line RDI Declaration/Removal Timing Diagram (Figure 27) illustrates the operation of the LAIS and LRDI outputs. LAIS (LRDI) is declared when the binary pattern '111' ('110') is observed in bits 6,7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. LAIS (LRDI) is removed when any pattern other than the binary pattern '111' ('110') is observed in bits 6,7 and 8 of the K2 byte for three or five consecutive frames as programmed using the RLOP Control/Status register. LAIS and LRDI may be declared or removed once per frame.

Figure 28 - Loss of Pointer Declaration/Removal



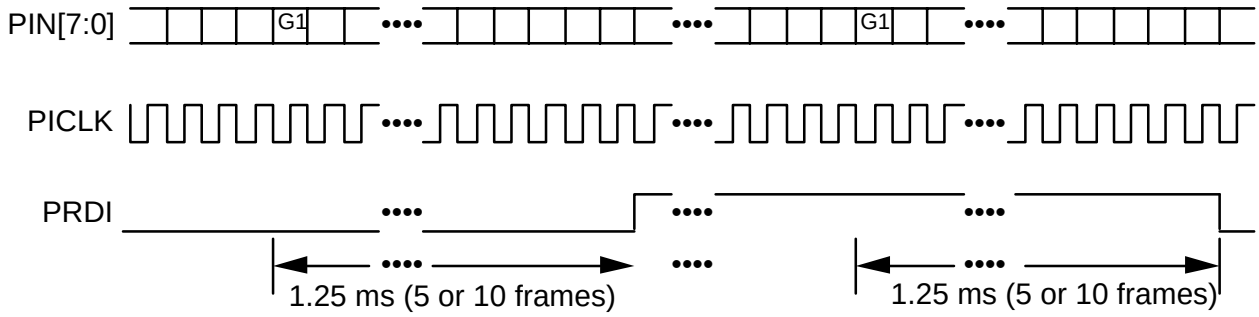
The Loss of Pointer Declaration/Removal Timing Diagram (Figure 28) illustrates the operation of the LOP output. LOP is declared when a valid pointer cannot be determined (according to the pointer interpretation rules contained in the references) for eight consecutive frames. LOP is removed as soon as a valid pointer is determined.

Figure 29 - Path AIS Declaration/Removal



The Path AIS Declaration/Removal Timing Diagram (Figure 29) illustrates the operation of the PAIS output. PAIS is declared when an all-ones pattern is detected in the pointer value bytes (H1, H2) for three consecutive frames. PAIS is removed as soon as a valid pointer is determined.

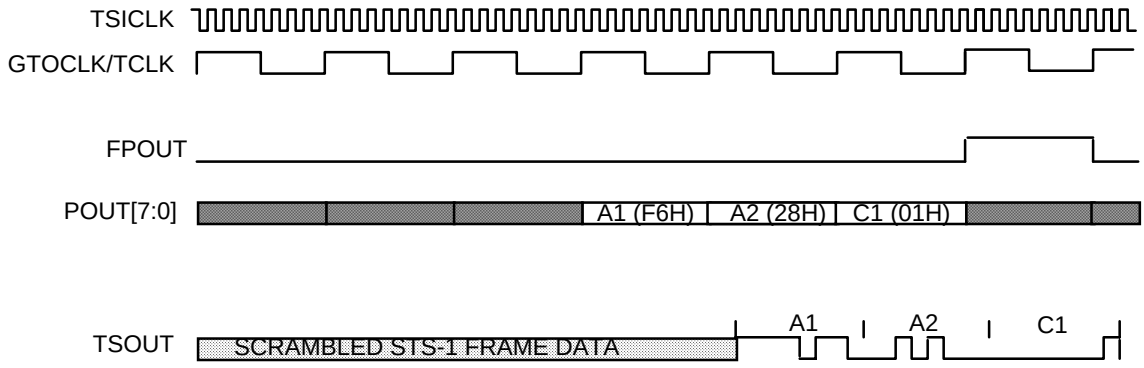
Figure 30 - Path Remote Defect Indication Declaration/Removal



The Path Remote Defect Indication Declaration/Removal Timing Diagram (Figure 30) illustrates the operation of the PRDI output. RDI-P is declared when the remote defect indication bit position in the path status byte (G1) is set to logic one for five (or ten) consecutive frames. RDI-P is removed when the remote defect indication bit position is set to logic zero for five (or ten) consecutive frames.

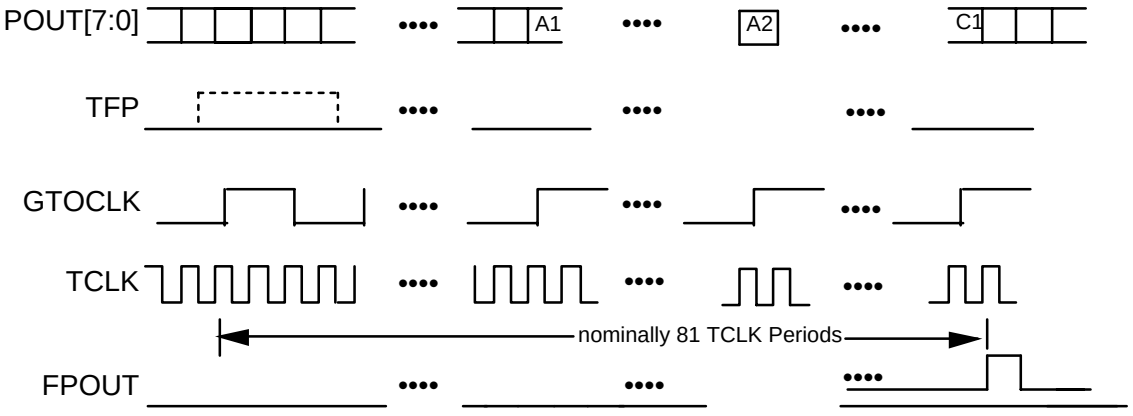
13.2 Line Side Transmit Interface

Figure 31 - STS-1 Bit-Serial Transmit Frame Alignment



The STS-1 Bit-Serial Transmit Frame alignment timing diagram (Figure 31) illustrates STS-1 bit-serial operation. The STS-1 transmit clock, TSICLK, is divided by eight to produce the byte-serial transmit clock, GTOCLK. In this application, GTOCLK is connected directly to TCLK.

Figure 32 - STS-12c Byte-Serial Transmit Frame Alignment

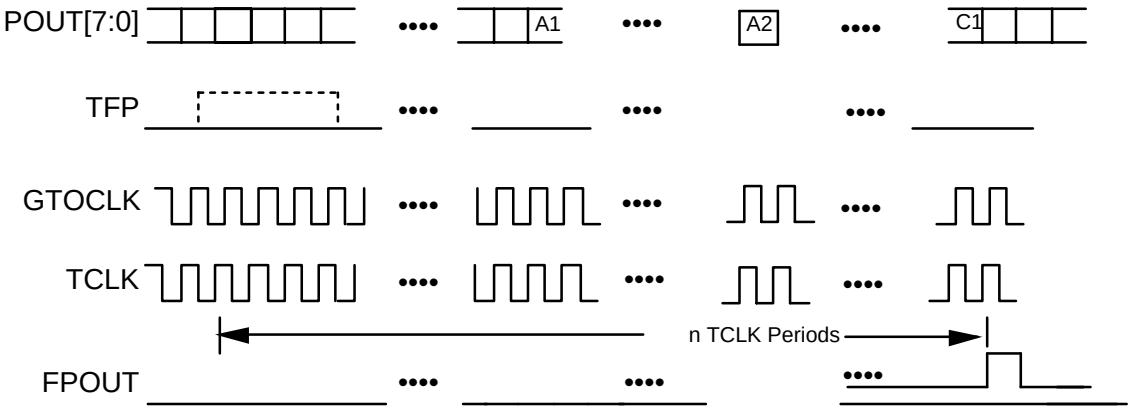


The STS-12c Byte-Serial Transmit Frame Alignment Timing Diagram (Figure 32) illustrates the alignment of the STS-12c byte-serial transmit stream to the outgoing frame position marker (FPOUT).

Input TFP is used to align the transport overhead in the transmit stream. The offset between the TFP alignment input, and the FPOUT alignment marker is nominally 81 clock periods. TFP is sampled by an internally generated version of GTOCLK that is advanced in phase relative to GTOCLK. The nominal delay is 81 TCLK cycles between the sampling of TFP and the generation of FPOUT.

TFP is shown as a dotted pulse because it is not necessary for TFP to be asserted on every frame.

Figure 33 - STS-3c/1 Byte-Serial Transmit Frame Alignment



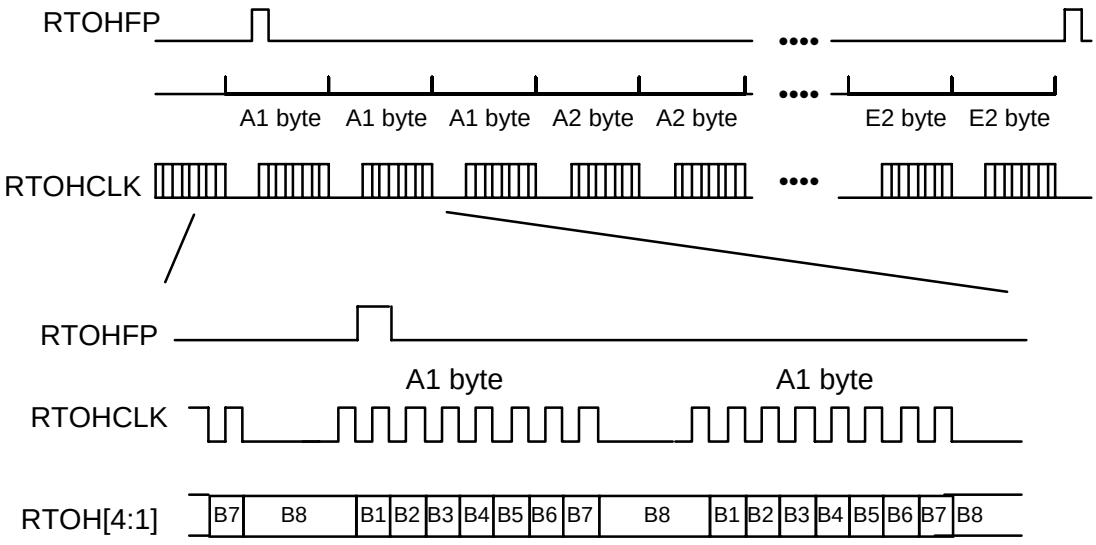
The STS-3c/1 Byte-Serial Transmit Frame Alignment Timing Diagram (Figure 33) illustrates the alignment of the STS-3c/1 byte-serial transmit stream to the outgoing frame position marker (FPOUT).

Input TFP is used to align the transport overhead in the transmit stream. The offset between the TFP alignment input, and the FPOUT alignment marker is n where n = 18 or 26 TCLK periods when configured for STS-1 or STS-3c (STM-1) operation, respectively.

TFP is shown as a dotted pulse because it is not necessary for TFP to be asserted on every frame.

13.3 Overhead Access

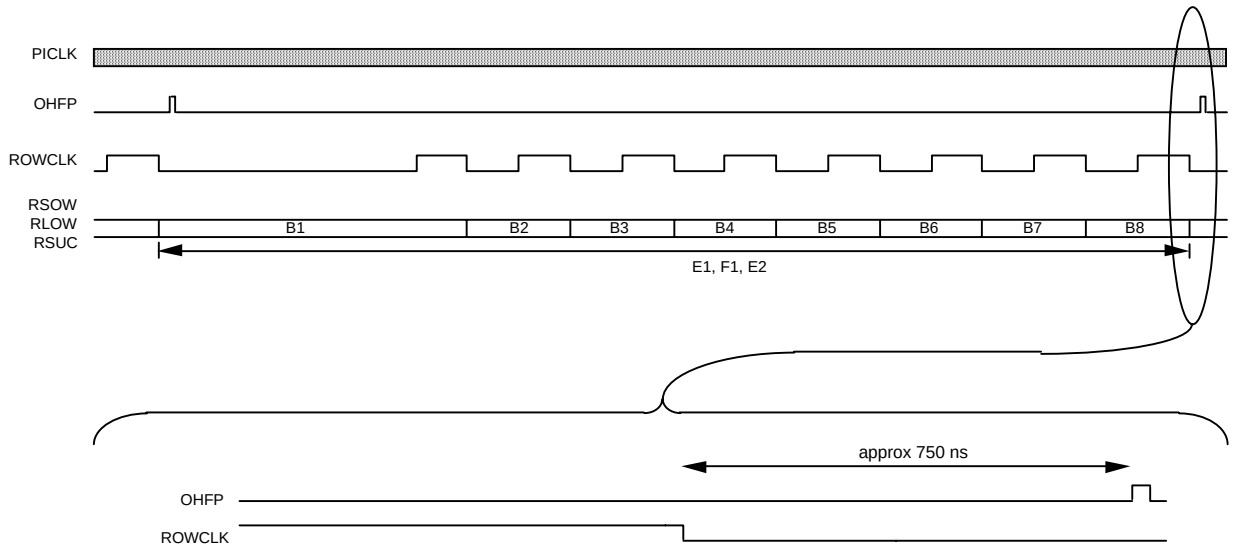
Figure 34 - Transport Overhead Extraction



The Transport Overhead Extraction timing diagram (Figure 34) illustrates the transport overhead extraction interface. The transport overhead extraction clock, RTOHCLK is nominally a 5.184 MHz (1.728 MHz for an STS-1 stream) clock and is derived from the receive line clock, PICLK. The entire 9 row by 36, 9 or 3 column transport overhead structure is extracted and serialized on RTOH[4:1] over a frame period (125 µs). When configured for STS-12 (STM-4c) operation,
RTOH[1] contains the transport overhead bytes in columns 1, 5, 9, . . 33.
RTOH[2] contains the transport overhead bytes in columns 2, 6, 10, . . 34.
RTOH[3] contains the transport overhead bytes in columns 3, 7, 11, . . 35.
RTOH[4] contains the transport overhead bytes in columns 4, 8, 12, . . 36.

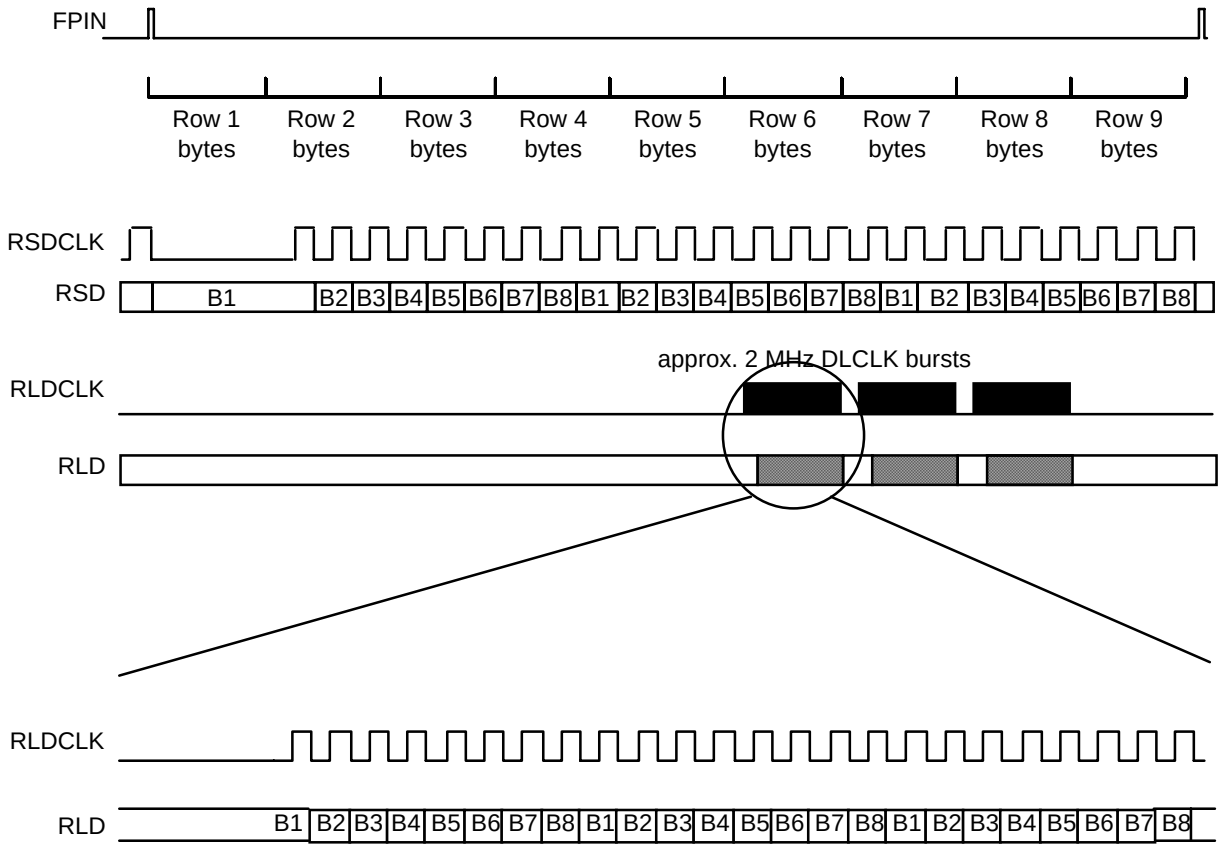
When configured for STS-3c (STM-1) or STS-1 operation, RTOH[1] contains all the transport overhead bytes.

Figure 35 - Transport Overhead Orderwire and User Channel Extraction



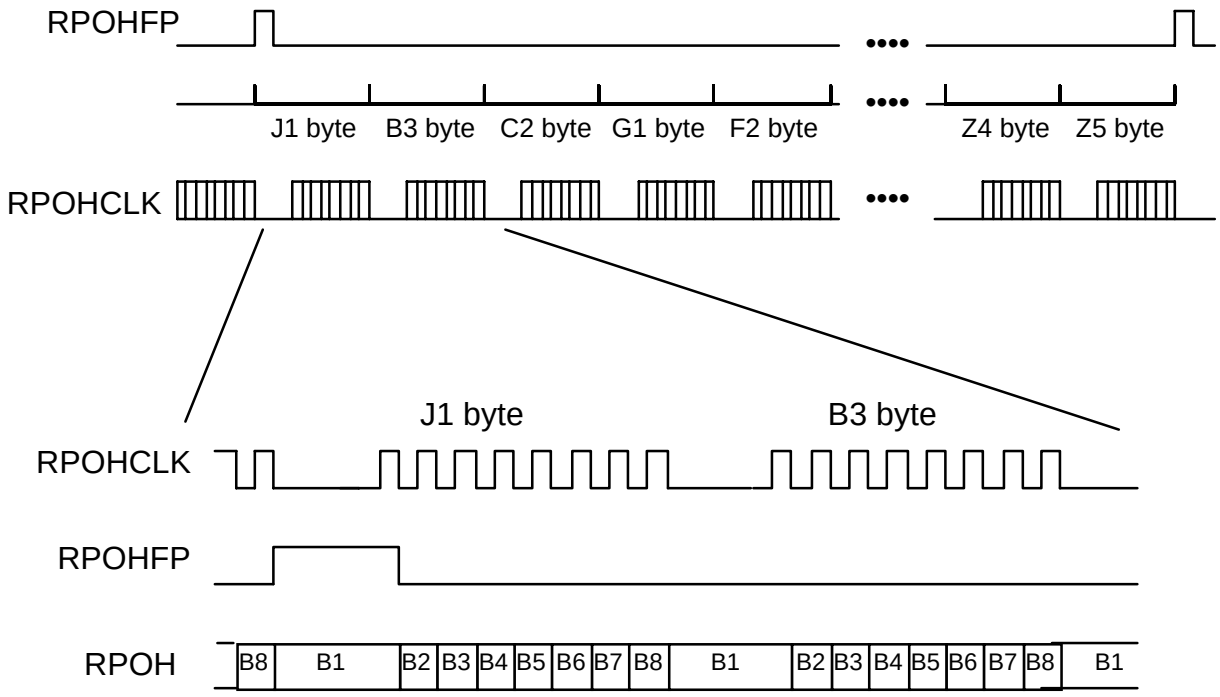
The Transport Overhead Orderwire and User Channel Extraction diagram (Figure 35) shows the relationship between the RSOW, RSUC and RLOW serial data outputs and their associated clock, ROWCLK. ROWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. The E1, F1 and E2 bytes shifted out of the S/UNI-622 on RSOW, RSUC and RLOW in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 36 - Transport Overhead Data Link Clock and Data Extraction



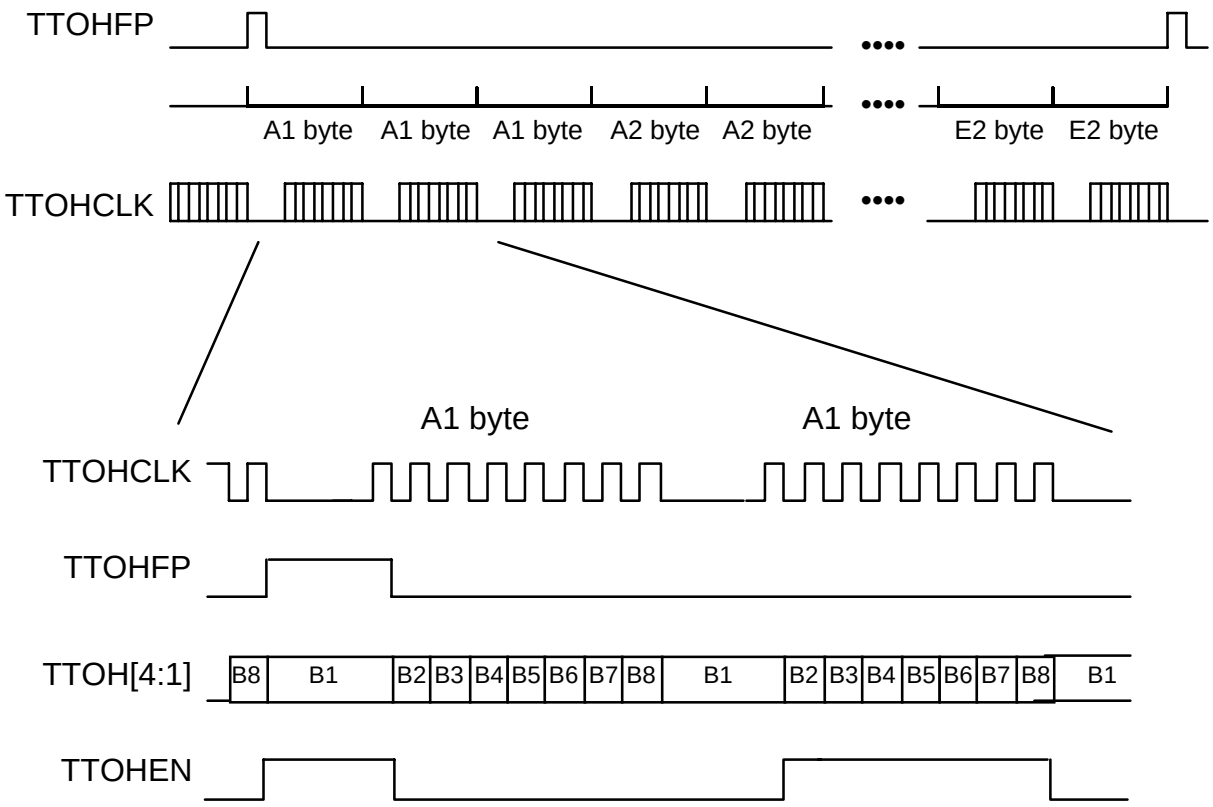
The Transport Overhead Data Link Clock and Data Extraction timing diagram (Figure 36) shows the relationship between the RSD and RLD serial data outputs, and their associated clocks, RSDCLK and RLDCLK. RSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate that is aligned with FPIN as shown in the timing diagram. RLDCLK is a 2.16 MHz, 67%/33% (high/low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with FPIN as shown in the timing diagram. RSD (RLD) is updated on the falling RSDCLK (RLDCLK) edge. The D1-D3 and D4-D12 bytes shifted out of the S/UNI-622 in the frame shown are extracted from the corresponding receive line overhead channels in the previous frame.

Figure 37 - Path Overhead Extraction



The Path Overhead Extraction Timing Diagram (Figure 37) illustrates the path overhead extraction interface. The path overhead extraction clock, RPOHCLK, is nominally a 576 kHz clock and is derived from the receive line clock, PICLK. The entire path overhead (the complete 9-byte structure) is extracted, serialized and output on RPOH over a frame time.

Figure 38 - Transport Overhead Insertion

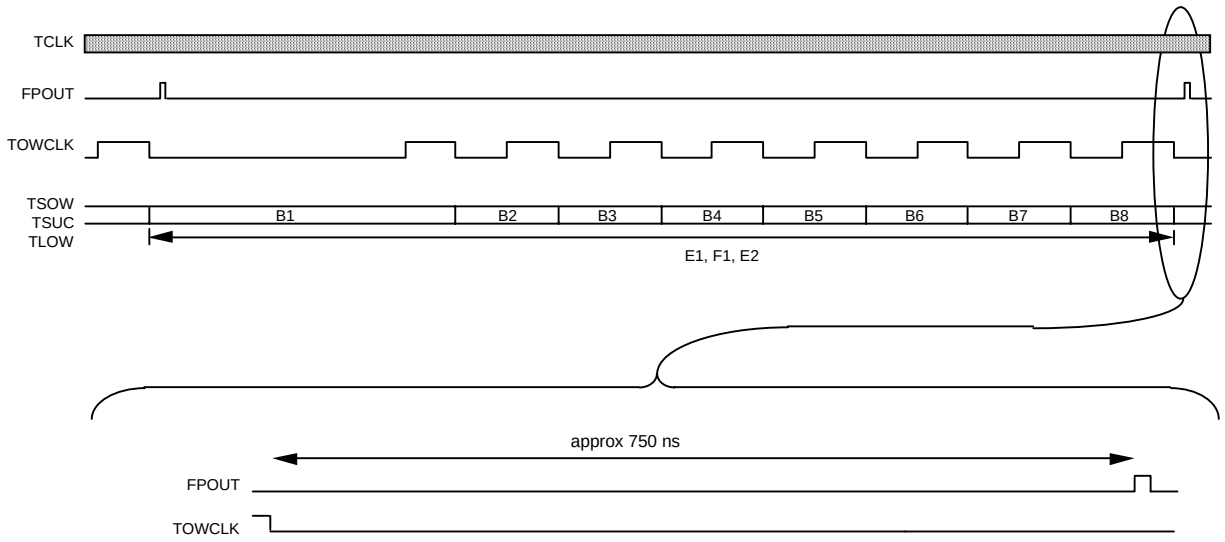


The transport overhead insertion timing diagram (Figure 38) illustrates the transport overhead insertion interface. Output TTOHCLK is nominally a 5.184 MHz clock (1.728 MHz for an STS-1 stream) and is used to update output TTOHFP, and to sample inputs TTOH[4:1] and TTOHEN. The value sampled on TTOHEN during the first overhead bit position of a given set of overhead bytes determines whether the values sampled on TTOH[4:1] are inserted in the STS-12c/3c/1 stream. In Figure 38, the STS-12c (STM-4c) case is shown. TTOHEN is held high during the position of bit 1 of the first group of four A1 bytes in the TTOH[4:1] stream. The eight bits sampled on input TTOH[4:1] during the first A1 byte period are inserted in the first through fourth A1 byte positions in the STS-12c stream. Similarly, TTOHEN is held low during the bit 1 position of the second group of four A1 bytes. The default value (F6H) is inserted in the fifth through eighth A1 byte positions in the STS-12c stream. For the STS-3c (STM-1) and STS-1 cases, only input TTOH[1] is used.

An error insertion feature is also provided for the B1, H1, H2, and B2 byte positions. When TTOH[4:1] is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being

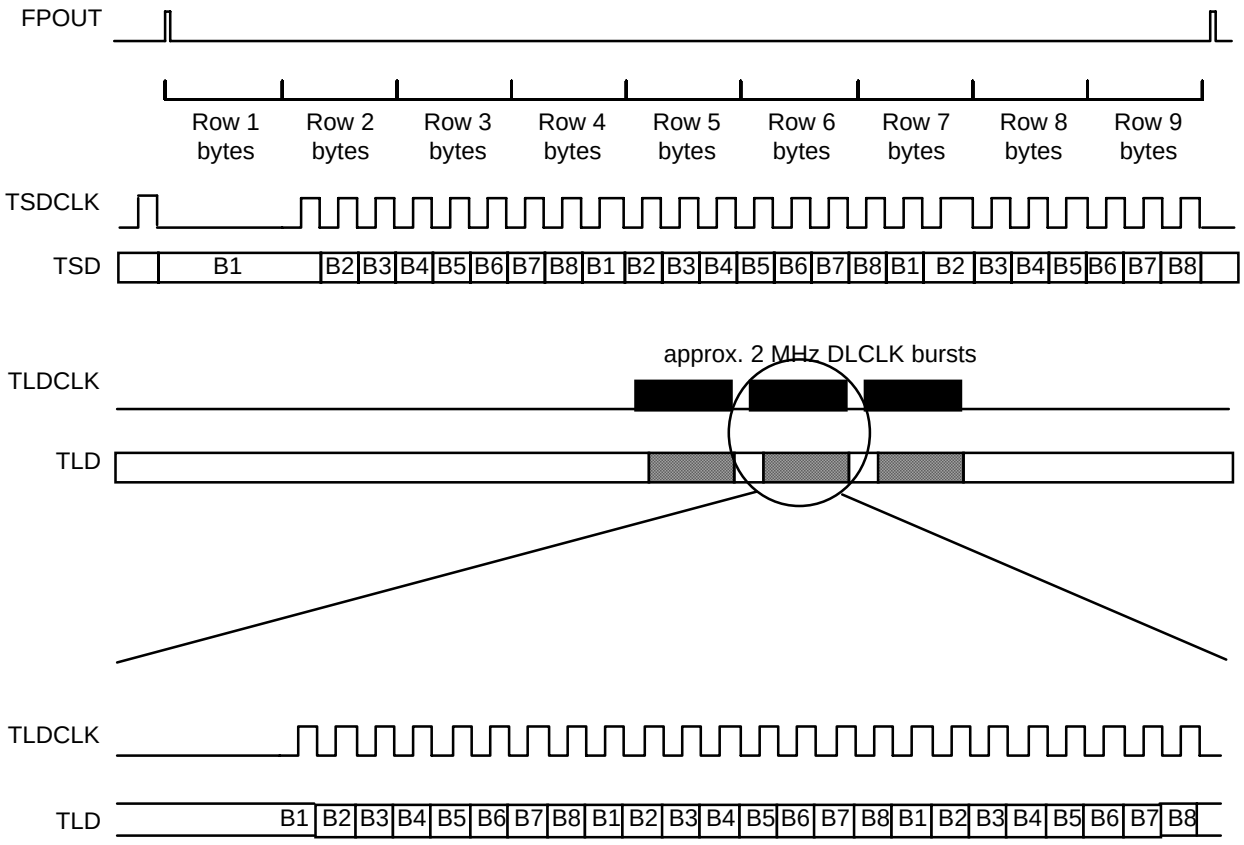
inserted in the STS-12c/3c/1 stream (TTOHEN must be sampled high during the first bit position to enable the error insertion mask).

Figure 39 - Transport Overhead Orderwire and User Channel Insertion



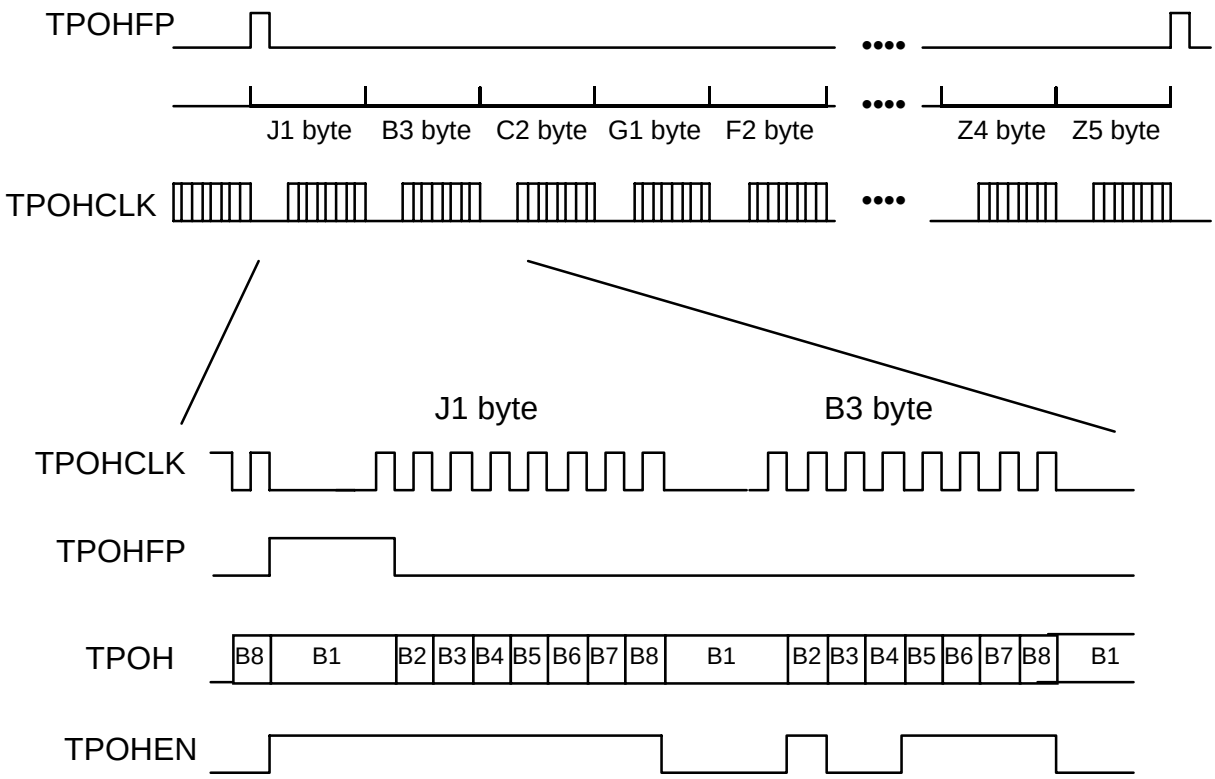
The Transport Overhead Orderwire and User Channel Insertion diagram (Figure 39) shows the relationship between the TSOW, TLOW and TSUC serial data inputs and their associated clock TOWCLK. TOWCLK is a 72 kHz 50% duty cycle clock that is gapped to produce a 64 kHz nominal rate and is aligned as shown in the timing diagram. The E1, E2 and F1 bytes shifted into the S/UNI-622 on TSOW, TLOW and TSUC in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 40 - Transport Overhead Data Link Clock and Data Insertion



The Transport Overhead Data Link Clock and Data Insertion timing diagram (Figure 40) shows the relationship between the TSD and TLD serial data inputs, and their associated clocks TSDCLK and TLDCLK respectively. TSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate that is aligned with FPOUT as shown in the timing diagram. TLDCLK is a 2.16 MHz 67%/33% (high/low) duty cycle clock that is gapped to produce a 576 kHz nominal rate that is aligned with FPOUT as shown in the timing diagram. TSD (TLD) is sampled on the rising TSDCLK (TLDCLK) edge. The D1-D3, and D4-D12 bytes shifted into the S/UNI-622 in the frame shown are inserted in the corresponding transport overhead channels in the following frame.

Figure 41 - Path Overhead Insertion

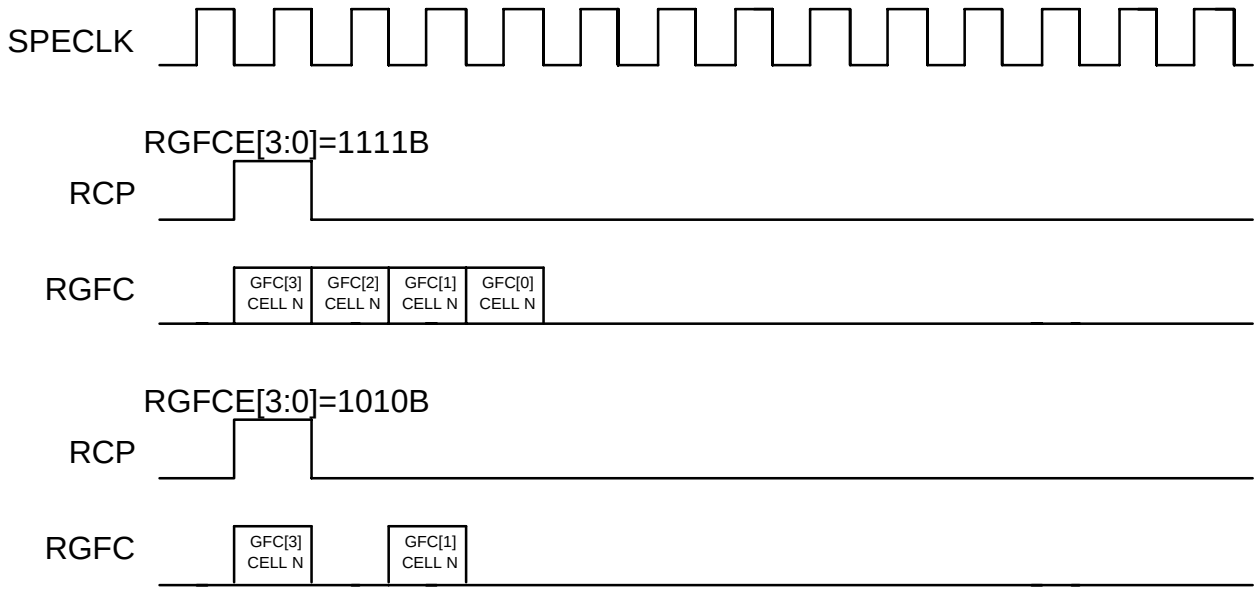


The Path Overhead Insertion Timing Diagram (Figure 41) illustrates the path overhead insertion interface. Output TPOHCLK is nominally a 576 kHz clock, and is used to update output TPOHFP, and to sample inputs TPOH and TPOHEN. In Figure 41, TPOHEN is held high throughout the eight bit positions of the J1 byte. The eight bits sampled on input TPOH are inserted in the J1 byte position in the STS-12c/3c/1 stream. If TPOHEN was low during any of the eight bit locations, the internally generated bit values of the corresponding bit positions would be inserted in the J1 byte.

For the B3 and H4 byte positions, an error insertion feature is provided. TPOHEN is held high during bit positions 2, 5, 6, 7 and 8 of the B3 byte. The values sampled on input TPOH are used as an error mask in the corresponding bit positions (2, 5, 6, 7 and 8) of the B3 byte in the STS-12c/3c/1 stream. If TPOH and TPOHEN are high during a bit location, the corresponding bit of the internally generated B3 byte is inverted before transmission.

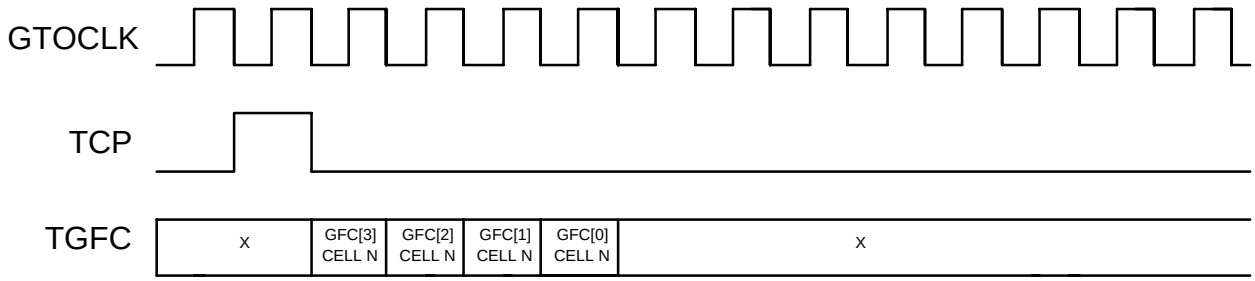
13.4 GFC Access

Figure 42 - GFC Extraction Port



The GFC Control Port Diagram (Figure 42) illustrates the operation of the receive generic flow control, RGFC, and receive GFC control pulse, RCP, outputs. The first RGFC bit position, which is coincident with the RCP being high, contains the first GFC bit received and corresponds to the first bit of the cell. Extraction of the GFC[3:0] bits is controlled by the four RGFC enable (RGFCE[3:0]) bits in the RACP GFC Control register. The output value in each GFC bit postition can be forced low by setting the corresponding RGFCE bit to zero. The serial link is inactive (forced low) if the S/UNI-622 is out of cell delineation or if the current cell contains an uncorrected header.

Figure 43 - GFC Insertion Port



The GFC Insertion Port Diagram (Figure 43) illustrates the relationship between the transmit cell pulse, TCP output and the transmit generic flow control, TGFC input. The MSB (GFC[3]) of the four-bit GFC code on the TGFC input is identified using the TCP output. The S/UNI-622 accumulates the code and transmits the code in the next transmit cell. If the next transmit cell is an idle/unassigned cell, the GFC code provided in the Idle/Unassigned Cell Header Pattern register is overwritten. If the next transmit cell was read from the FIFO, the GFC code passed through the FIFO is overwritten.

13.5 Drop Side Receive Interface

Figure 44 - Receive Synchronous FIFO, TSEN=0, RCALEVEL0=1

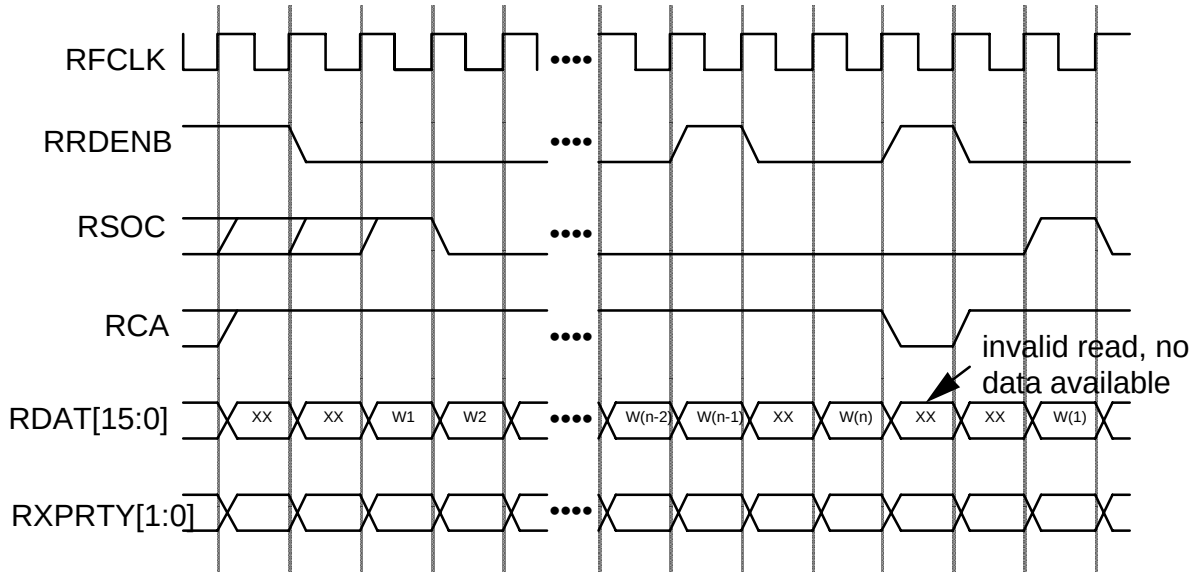
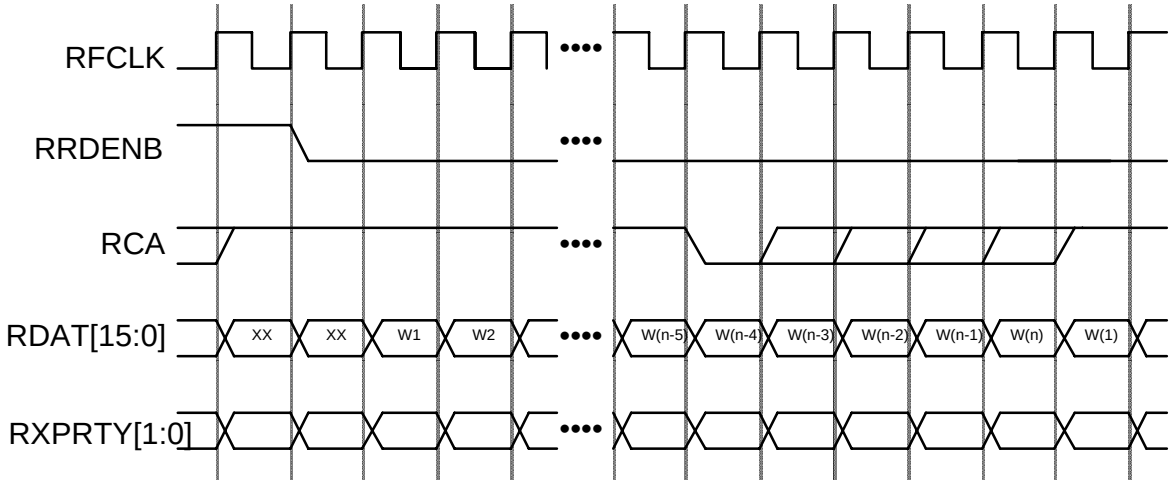


Figure 45 - Receive Synchronous FIFO, TSEN=0, RCALEVEL0=0



The receive synchronous FIFO is controlled by the ATM Layer device using the RRDENB signal. All signals must be updated and sampled using the rising edge of the receive FIFO clock, RFCLK.

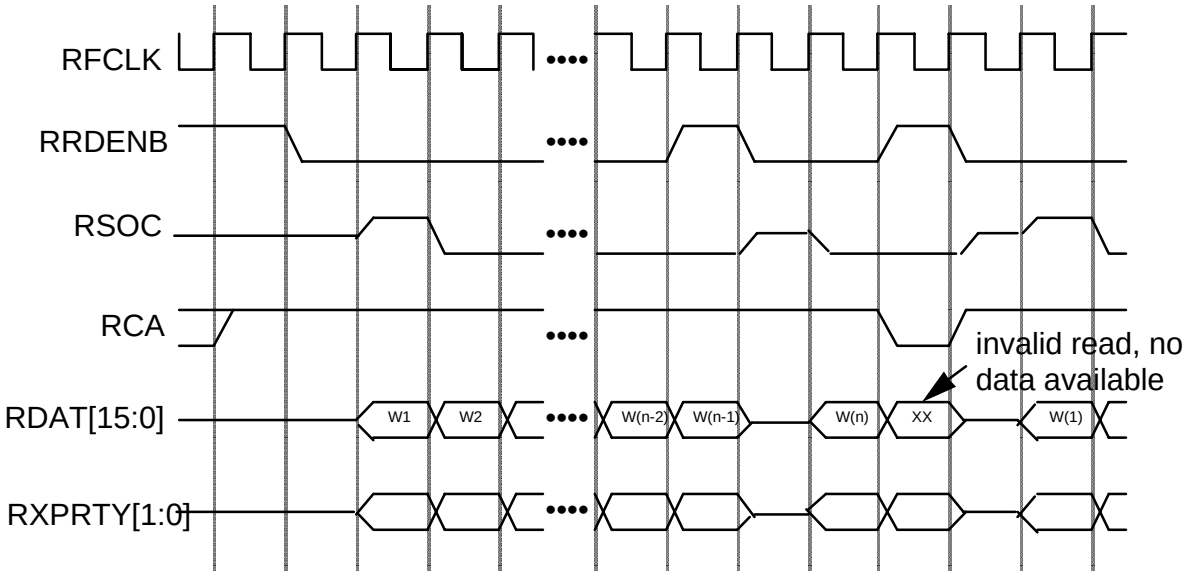
The PHY layer device indicates that a cell is available by asserting the receive cell available signal, RCA. RCA remains high until the internal FIFO of the PHY layer device is near empty or empty. Near empty implies that the ATM Layer device can initiate at most four additional reads. The selection of the empty or near empty operating modes is made by the RCALEVEL0 bit in register 0x52. The ATM Layer device indicates, by asserting the RRDENB signal, that the data on the RDAT bus during the next RFCLK cycle will be read from the PHY layer device.

Figure 44 illustrates the empty operating mode. RCA transitions low when the last word of the last cell is available on the RDAT bus. The RDAT bus, RXPRTY and RSOC are valid in cycles for which RCA is high and RRDENB was low is the previous cycle. If the ATM Layer device requests a read while RCA is deasserted, the PHY layer device will ignore the additional reads.

Figure 45 illustrates the near empty operating mode. RCA transitions low four words before the last word of the last cell is read from the PHY layer device. RCA remains low for a minimum of one RFCLK clock cycle and then can transition high to indicate that there are additional cells available from the PHY layer device.

Once RCA is deasserted and has been sampled, the ATM Layer device can issue no more than four reads. If the ATM Layer device issues more reads than the allowable number, and RCA remains deasserted throughout, the PHY layer device will ignore the additional reads.

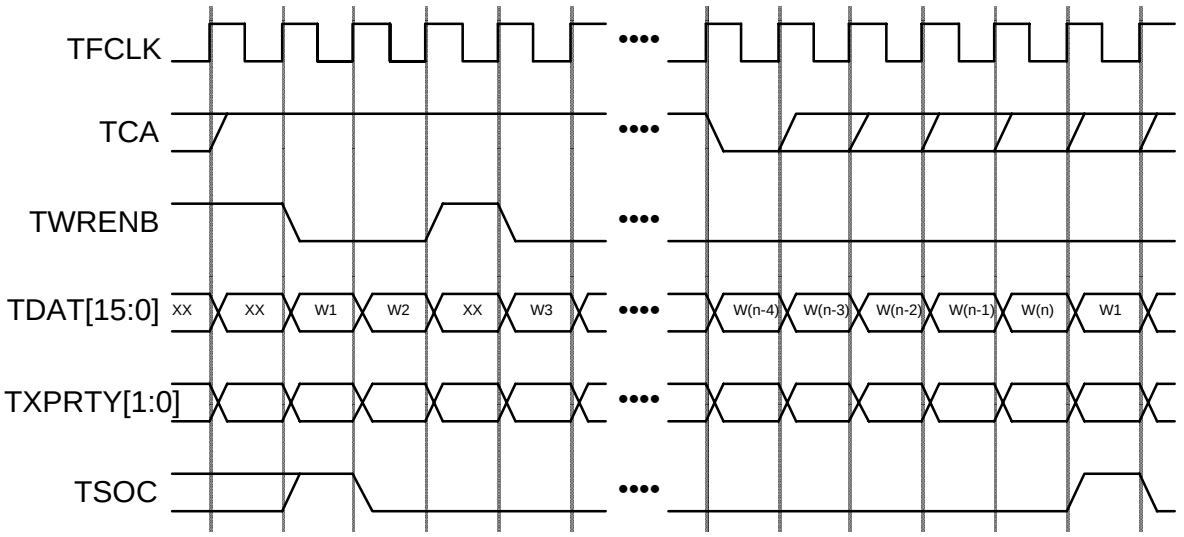
Figure 46 - Receive Synchronous FIFO, TSEN=1, RCALEVEL0=1



The Receive Synchronous FIFO Timing, TSEN=1, RCALEVEL0=1 Diagram (Figure 46) illustrates the operation of the drop side receive interface with tristating enabled. Figure 46 is similar to figure Figure 44 except that outputs RSOC, RDAT[15:0] and RXPRTY[1:0] are tristated in the clock cycle following the removal of RRDENB.

13.6 Drop Side Transmit Interface

Figure 47 - Transmit Synchronous FIFO



The S/UNI-622 transmit interface is controlled by the ATM Layer device using the TWRENB signal. All signals must be updated and sampled using the rising edge of the transmit FIFO clock, TFCLK.

As shown in Figure 47, the S/ UNI-622 layer device indicates that there is space available for a full cell in its internal FIFO by asserting the transmit cell available signal, TCA. TCA remains asserted until the transmit FIFO is almost full or full. Almost full implies that the S/UNI-622 can accept at most an additional four writes after the current write (TCALEVEL0 is logic 0) while full implies that the S/UNI-622 can accept no additional writes after the completion of the current write (TCALEVEL0 is logic 1). The TCALEVEL0 bit is contained in register 0x63

If TCA is asserted and the ATM Layer device is ready to write a word, it should assert TWRENB low and present the word on the TDAT bus. If the presented word is the first word of a cell, the ATM Layer device should also assert signal TSOC. At any time, if the ATM Layer device does not have a word to write, it can deassert TWRENB.

When TCA is deasserted and it has been sampled, the ATM Layer device can write no more than four bytes or words to the PHY layer device. If the ATM Layer writes more than four words and TCA remains deasserted throughout, the PHY layer device will indicate an error condition and ignore additional writes until it asserts TCA again.

14 ABSOLUTE MAXIMUM RATINGS

Table 16 - Absolute Maximum Ratings

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±500 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

15 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = 5 V ±5%

(Typical Conditions: T_C = 25°C, V_{DD} = 5 V)

Table 17 -

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.75	5	5.25	Volts	
V_{IL}	Input Low Voltage (TTL Only)	-0.5	1.4	0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage (TTL Only)	2.0	1.4	V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage (TTL Only)		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -4 mA for D[7:0], POUT[7:0], FPOUT, TSOUT, GTOCLK, GROCLK, TCA, RDAT[15:0], RXPRTY[1:0], RCA and RSOC, and -2 mA for all other outputs. Note 3
V_{OH}	Output or Bidirectional High Voltage (TTL Only)	2.4	4.7		Volts	V_{DD} = min, I_{OH} = 4 mA for D[7:0], POUT[7:0], FPOUT, TSOUT, GTOCLK, GROCLK, TCA, RDAT[15:0], RXPRTY[1:0], RCA and RSOC, and 2 mA for all other outputs. Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+175	+350	+525	µA	V_{IL} = GND. Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP1s}	Operating Current Processing Cells		60	90	mA	V_{DD} = 5.25 V, Outputs Unloaded, RSICLK = 51.84 MHz TSICLK = 51.84 MHz RFCLK = 52 MHz TFCLK = 52 MHz
I_{DDOP1}	Operating Current Processing Cells			Note 4	mA	V_{DD} = 5.25 V, Outputs Unloaded, PICLK = 6.48 MHz TCLK = 6.48 MHz RFCLK = 52 MHz TFCLK = 52 MHz
I_{DDOP3c}	Operating Current Processing Cells			Note 4	mA	V_{DD} = 5.25 V, Outputs Unloaded, PICLK = 19.44 MHz TCLK = 19.44 MHz RFCLK = 52 MHz TFCLK = 52 MHz
$I_{DDOP12c}$	Operating Current Processing Cells		210	270	mA	V_{DD} = 5.25 V, Outputs Unloaded, PICLK = 77.76 MHz TCLK = 77.76 MHz RFCLK = 52 MHz TFCLK = 52 MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. Characterization data for I_{DDOP1} and I_{DDOP3c} is not available at this time.

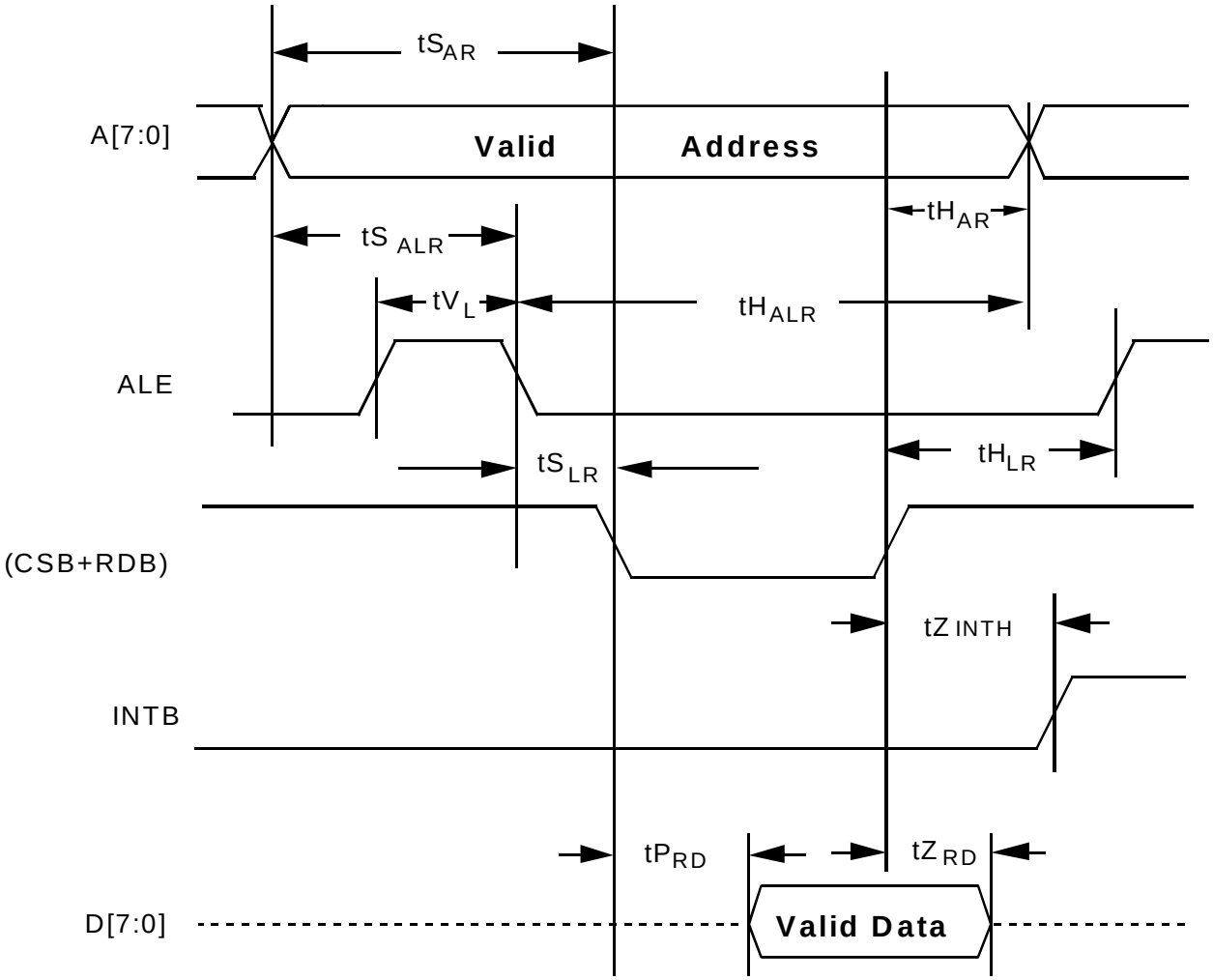
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Table 18 - Microprocessor Interface Read Access (Figure 48)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to Output Tri-state		50	ns

Figure 48 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point o\ the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.

6. Parameter tH_{AR} is not applicable if address latching is used.

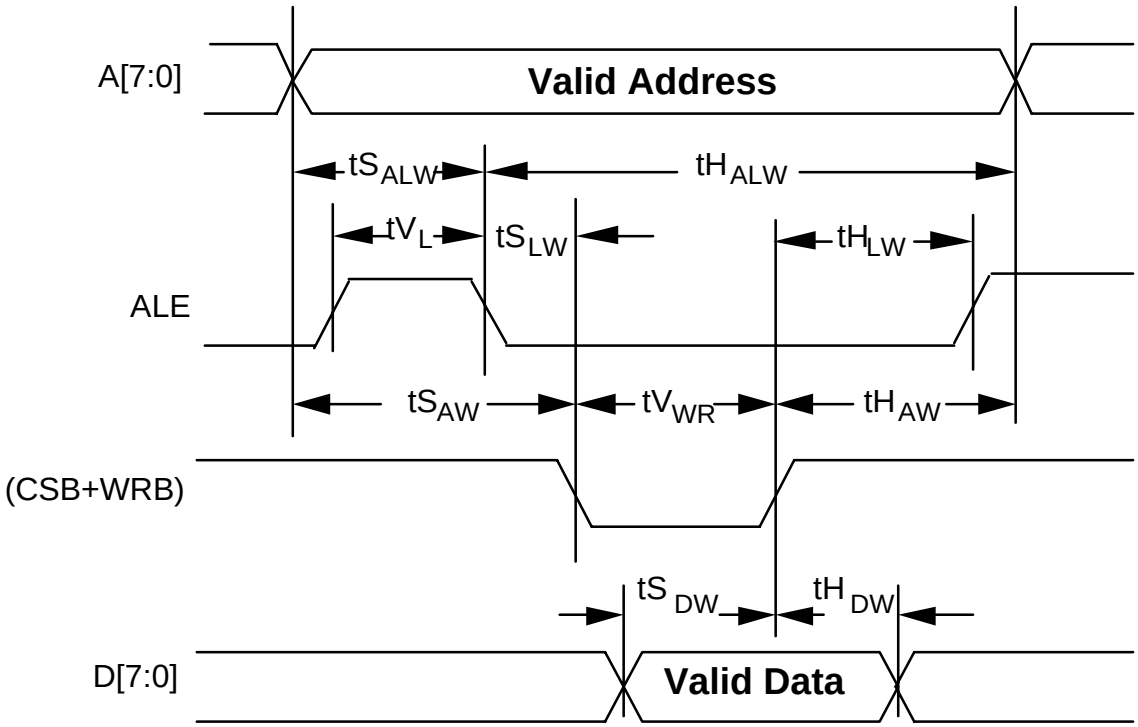
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 19 - Microprocessor Interface Write Access (Figure 49)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 49 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

4. Parameter tH_{AW} is not applicable if address latching is used.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 S/UNI-622 TIMING CHARACTERISTICS

(T_C = -40°C to +85°C, V_{DD} = 5 V ±5%)

Table 20 - Line Side Receive Interface (Figure 50)

Symbol	Description	Min	Max	Units
	PICLK Frequency (nominally 77.76 MHz)		78	MHz
	PICLK Duty Cycle	40	60	%
tS_{PIN}	PIN[7:0] Set-up time to PICLK	3.5		ns
tH_{PIN}	PIN[7:0] Hold time to PICLK	1		ns
tS_{FPIN}	FPIN Set-up time to PICLK	3.5		ns
tH_{FPIN}	FPIN Hold time to PICLK	1		ns
	RSICLK Frequency (nominally 51.84 MHz)		52	MHz
	RSICLK Duty Cycle	33	67	%
tS_{RSIN}	RSIN Set-up Time to RSICLK	5		ns
tH_{RSIN}	RSIN Hold Time to RSICLK	2		ns
tP_{GROCLK}	RSICLK High to GROCLK Valid Prop Delay	5	30	ns

Figure 50 - Line Side Receive Interface Timing

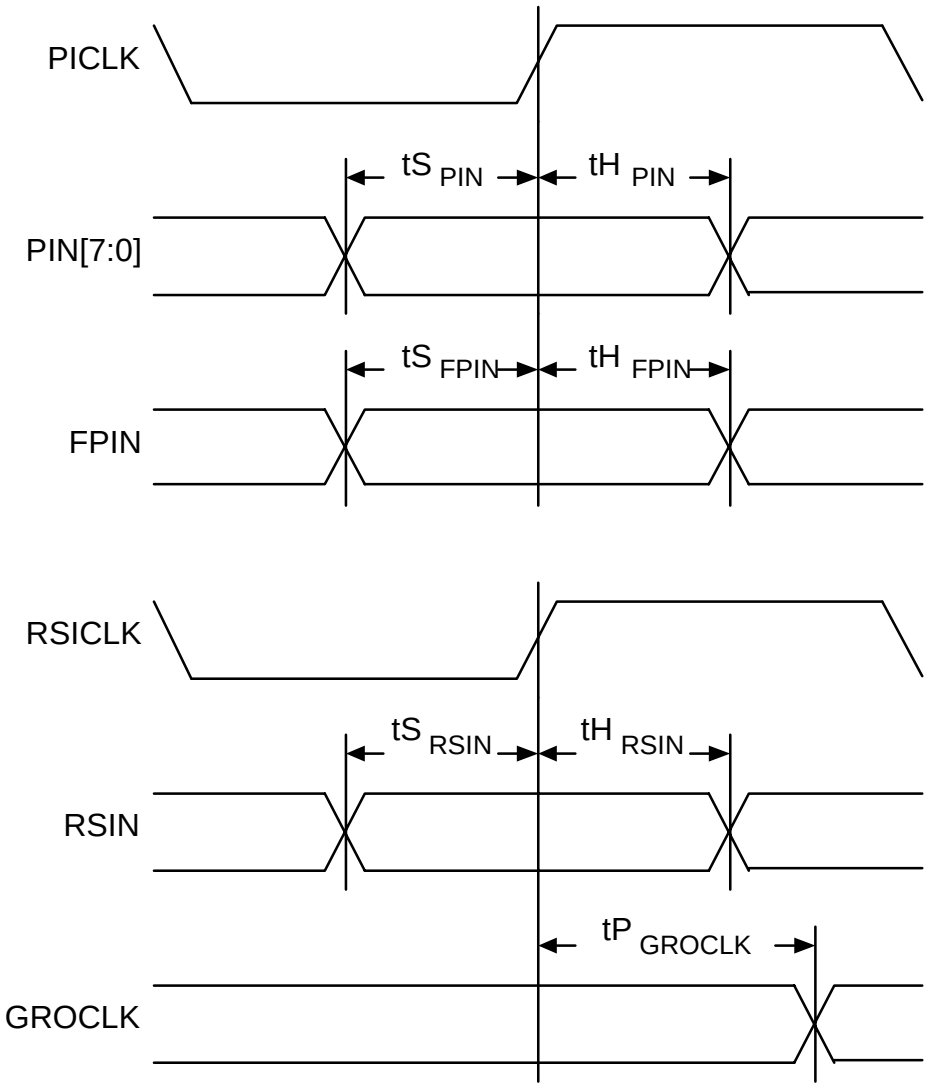
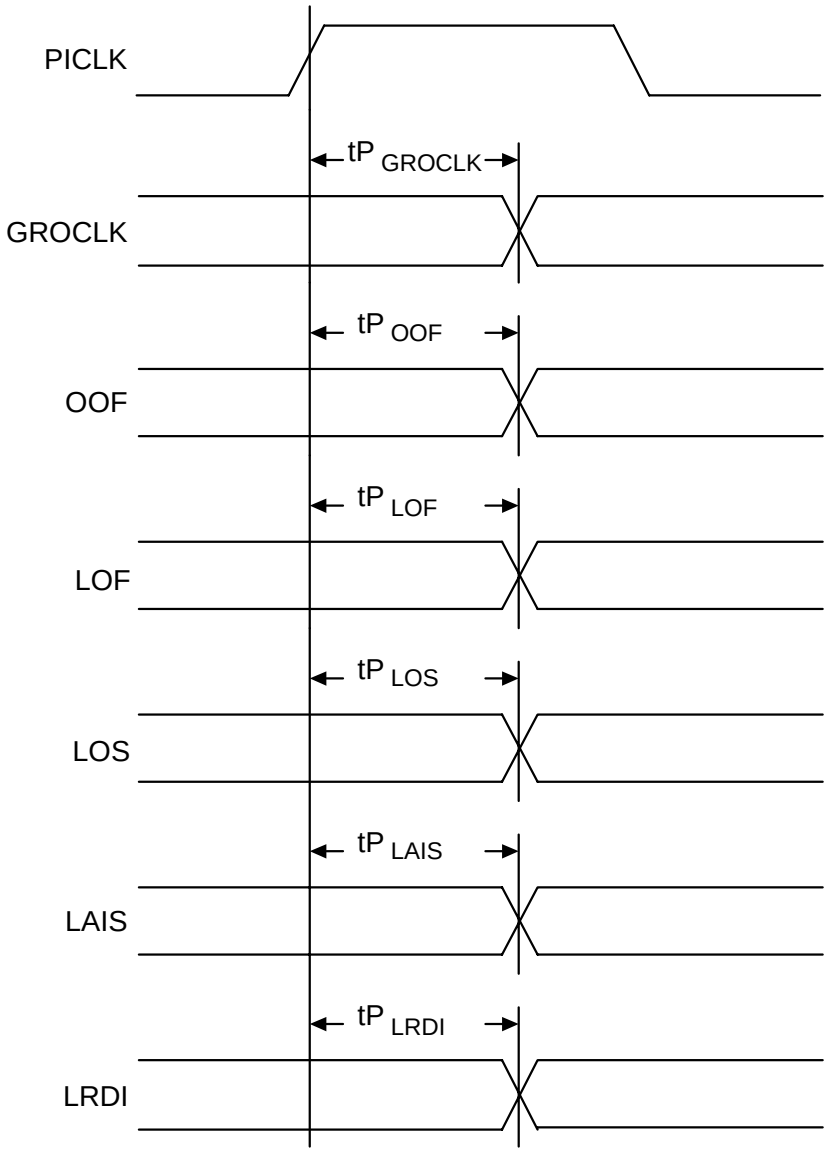


Table 21 - Receive Alarm Output (Figure 51)

Symbol	Description	Min	Max	Units
$t_{PGROCLK}$	PICLK High to GROCLK Edge	3	25	ns
t_{POOF}	PICLK High to OOF Valid	3	30	ns
t_{PLOF}	PICLK High to LOF Valid	3	30	ns
t_{PLOS}	PICLK High to LOS Valid	3	30	ns

Symbol	Description	Min	Max	Units
t_{PLAIS}	PICLK High to LAIS Valid	3	30	ns
t_{PLRDI}	PICLK High to LRDI Valid	3	30	ns
t_{PLOP}	GROCLK Low to LOP Valid	3	25	ns
t_{PPAIS}	GROCLK Low to PAIS Valid	3	25	ns
P_{PRDI}	GROCLK Low to PRDI Valid	3	25	ns
t_{PLCD}	GROCLK Low to LCD Valid	3	25	ns

Figure 51 - Receive Alarm Output Timing



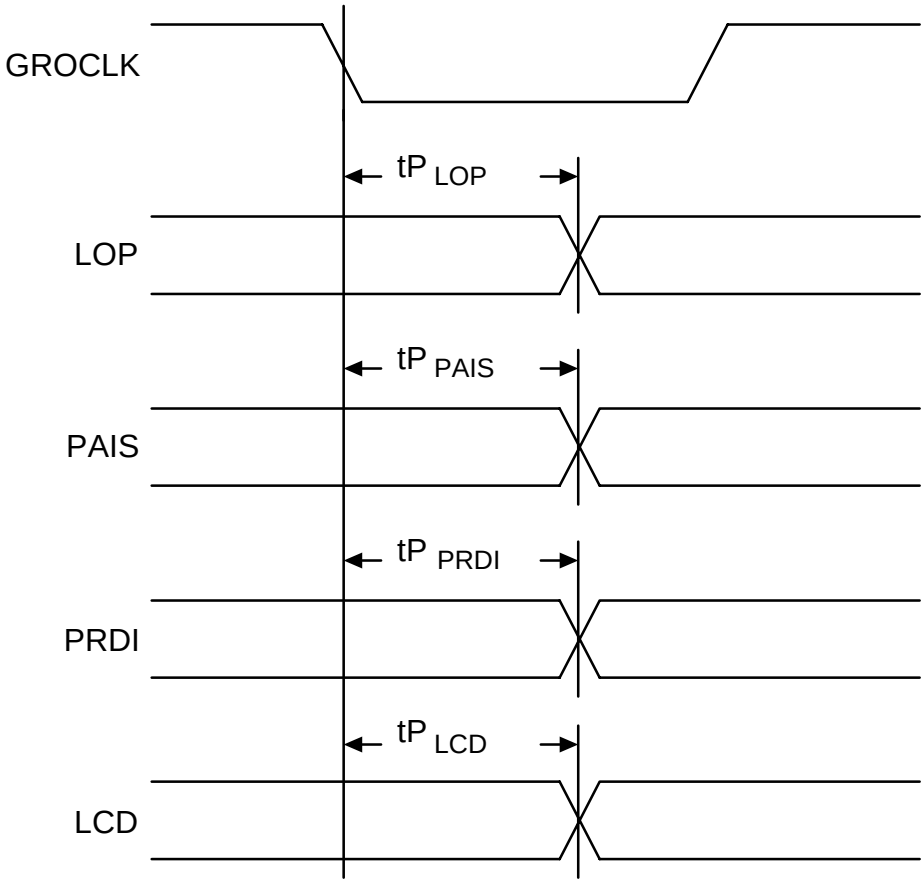
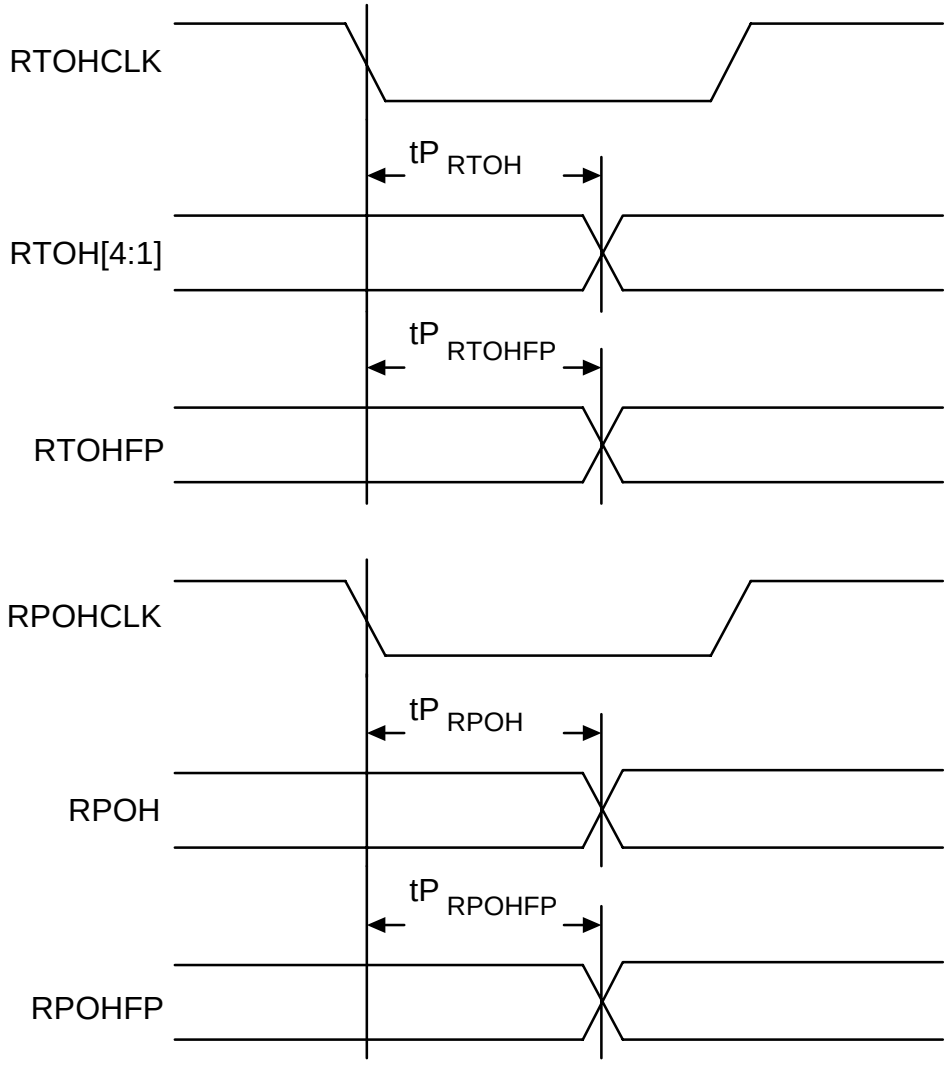


Table 22 - Receive Overhead Access (Figure 52)

Symbol	Description	Min	Max	Units
t_{PRTOH}	RTOHCLK Low to RTOH[4:1] Valid	-15	15	ns
$t_{PRTOHFP}$	RTOHCLK Low to RTOHFP Valid	-15	15	ns
t_{PROW}	ROWCLK Low to RSOW, RSUC,			
	RLOW Valid Prop Delay	-250	250	ns
t_{PRSD}	RSDCLK Low to RSD Valid	-15	15	ns
t_{PRLD}	RLDCLK Low to RLD Valid	-15	15	ns
t_{PRPOH}	RPOHCLK Low to RPOH Valid	-15	15	ns
$t_{PRPOHFP}$	RPOHCLK Low to RPOHFP Valid	-15	15	ns

Figure 52 - Receive Overhead Access Timing



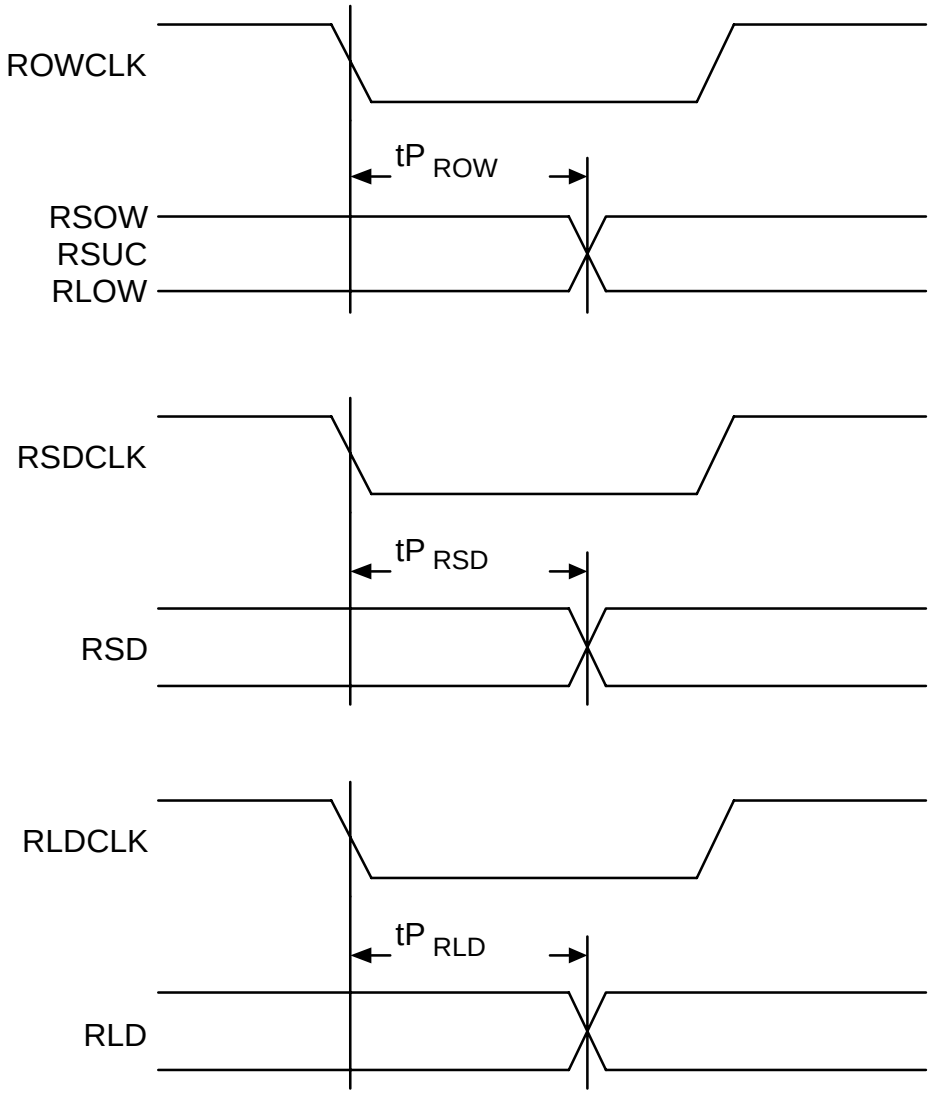


Table 23 - Receive Overhead Access (Figure 53)

Symbol	Description	Min	Max	Units
tP_{RCP}	GROCLK Low to RCP Valid	3	25	ns
tP_{RGFC}	GROCLK Low to RGFC Valid	3	25	ns

Figure 53 - Receive GFC Access Timing

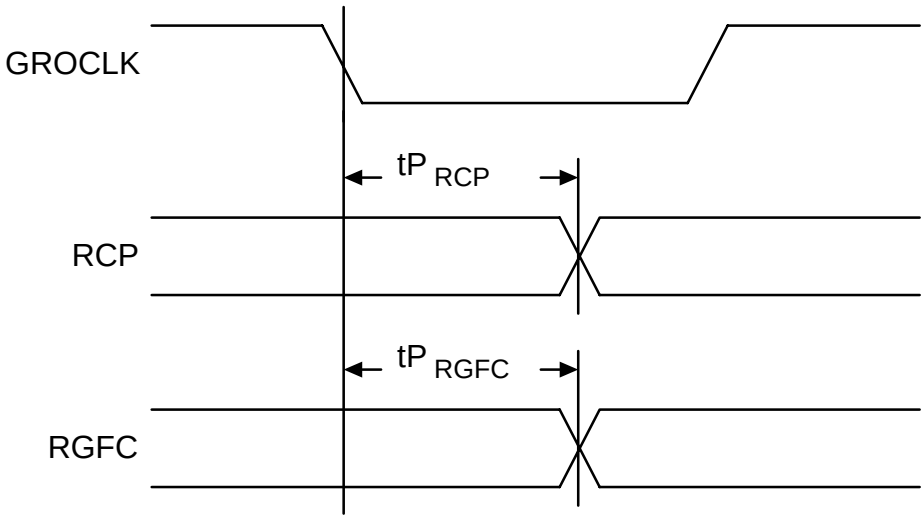


Table 24 - Line Side Transmit Interface (Figure 54)

Symbol	Description	Min	Max	Units
	TCLK Frequency (nominally 77.76 MHz)		78	MHz
	TCLK Duty Cycle	40	60	%
tP_{FPOUT}	TCLK High to FPOUT Valid	1	11	ns
tP_{POUT}	TCLK High to POUT[7:0] Valid	1	11	ns
tP_{GTOCLK}	TCLK Edge to GTOCLK Edge	2	25	ns
	TSICLK Frequency (nominally 51.84 MHz)		52	MHz
	TSICLK Duty Cycle	33	67	%
tP_{TSOUT}	TSICLK High to TSOUT Valid Prop Delay	2	15	ns
tP_{GTOCLK}	TSICLK High to GTOCLK Valid Prop Delay	4	25	ns

Figure 54 - Line Side Transmit Interface Timing

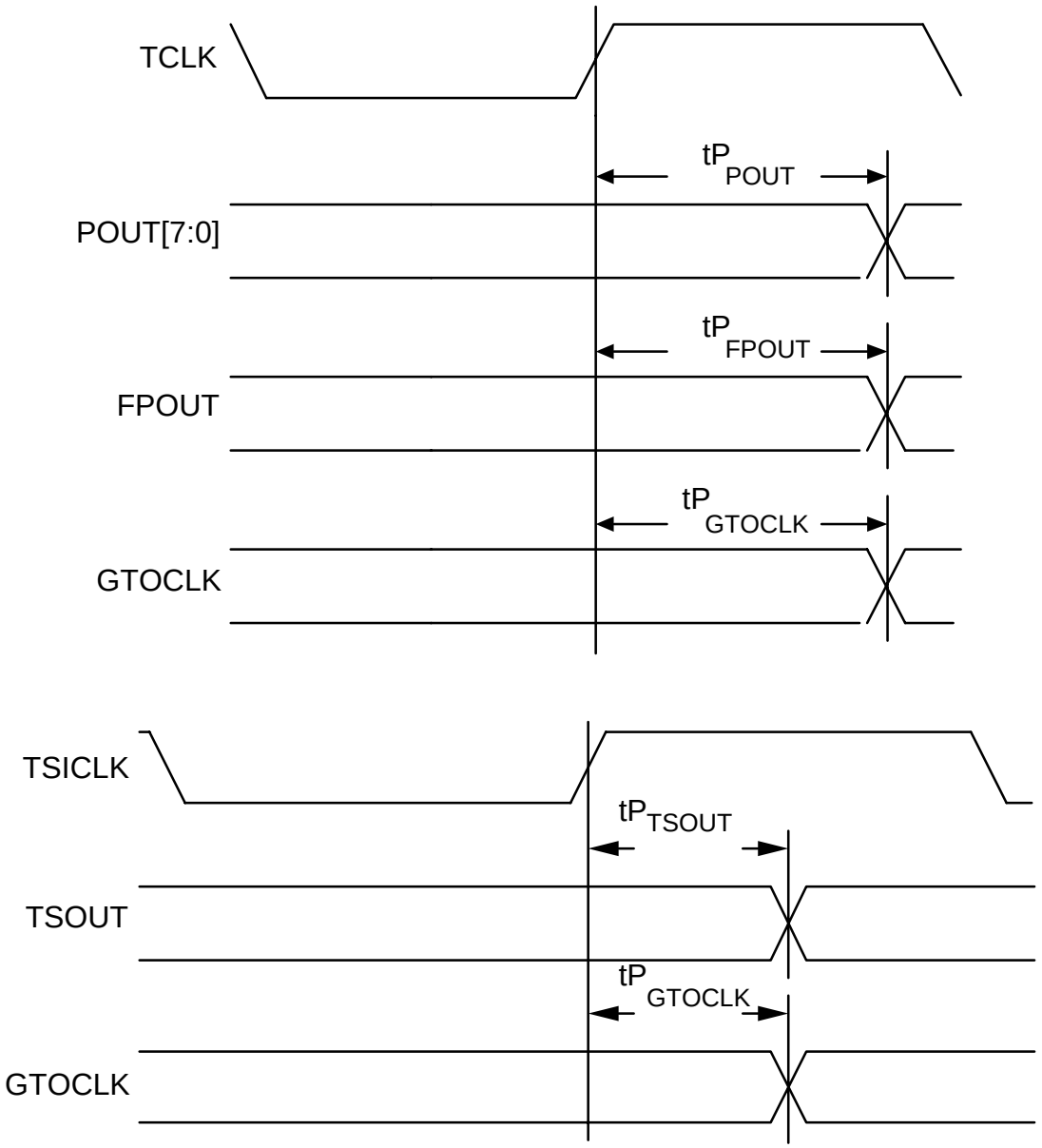
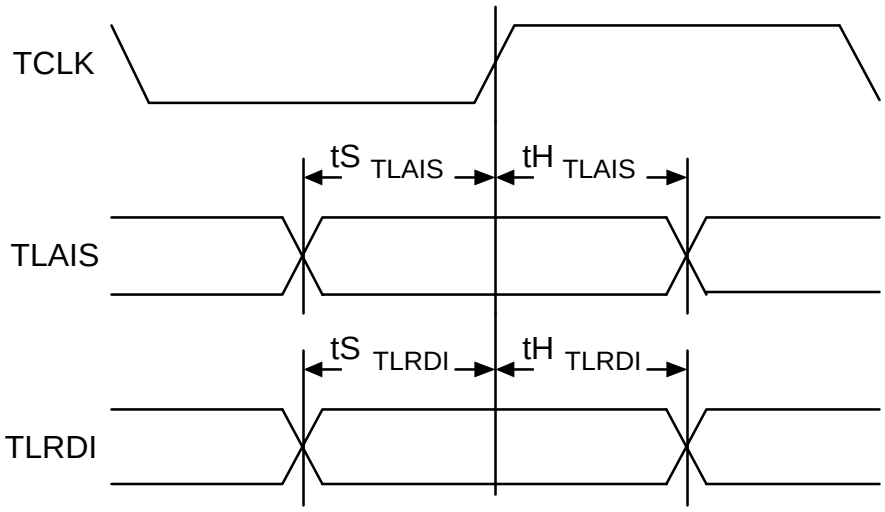


Table 25 - Transmit Alarm Input (Figure 55)

Symbol	Description	Min	Max	Units
tS_{TLAIS}	TLAIS Set-up time to TCLK	3		ns
tH_{TLAIS}	TLAIS Hold time to TCLK	3		ns

Symbol	Description	Min	Max	Units
tS_{TLRDI}	TLRDI Set-up time to TCLK	3		ns
tH_{TLRDI}	TLRDI Hold time to TCLK	3		ns
tS_{TPAIS}	TPAIS Set-up time to GTOCLK	10		ns
tH_{TPAIS}	TPAIS Hold time to GTOCLK	5		ns
tS_{TPRDI}	TPRDI Set-up time to GTOCLK	10		ns
tH_{TPRDI}	TPRDI Hold time to GTOCLK	5		ns
tS_{TFP}	TFP Set-up time to GTOCLK	10		ns
tH_{TFP}	TFP Hold time to GTOCLK	5		ns

Figure 55 - Transmit Alarm Input Timing



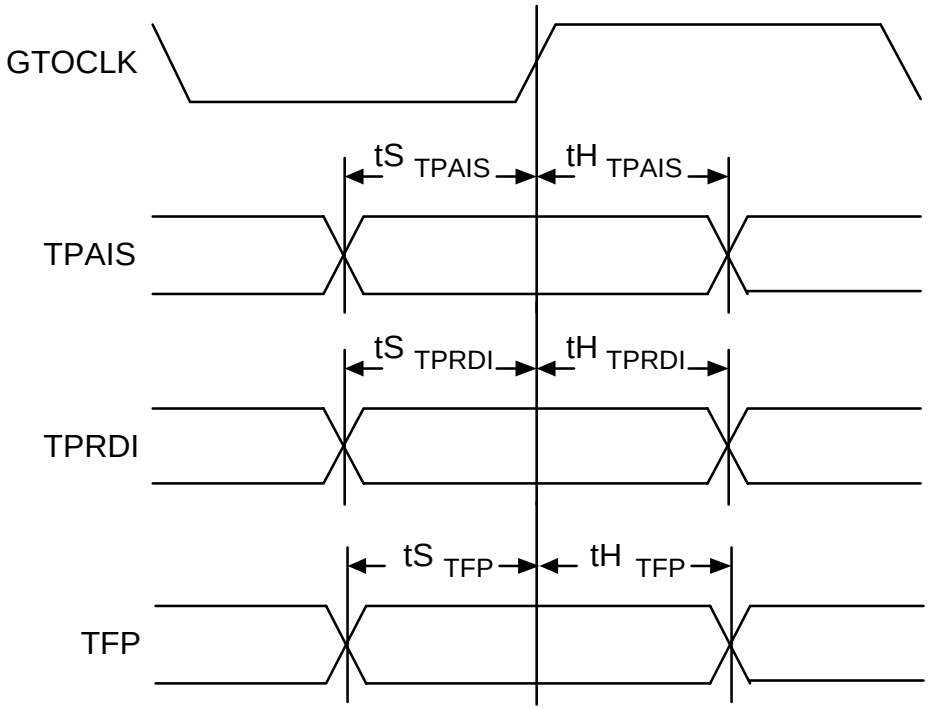
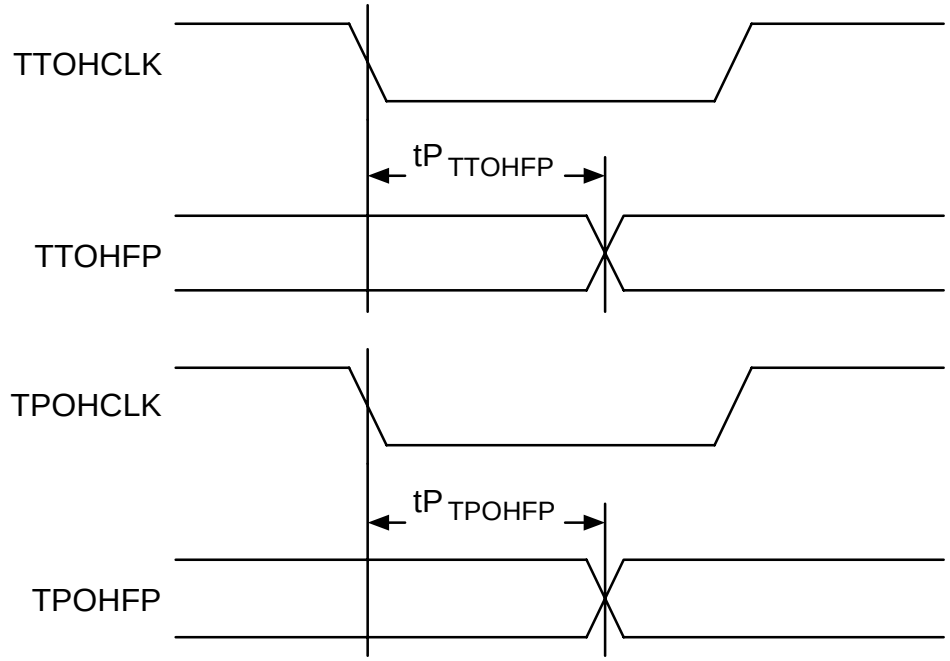


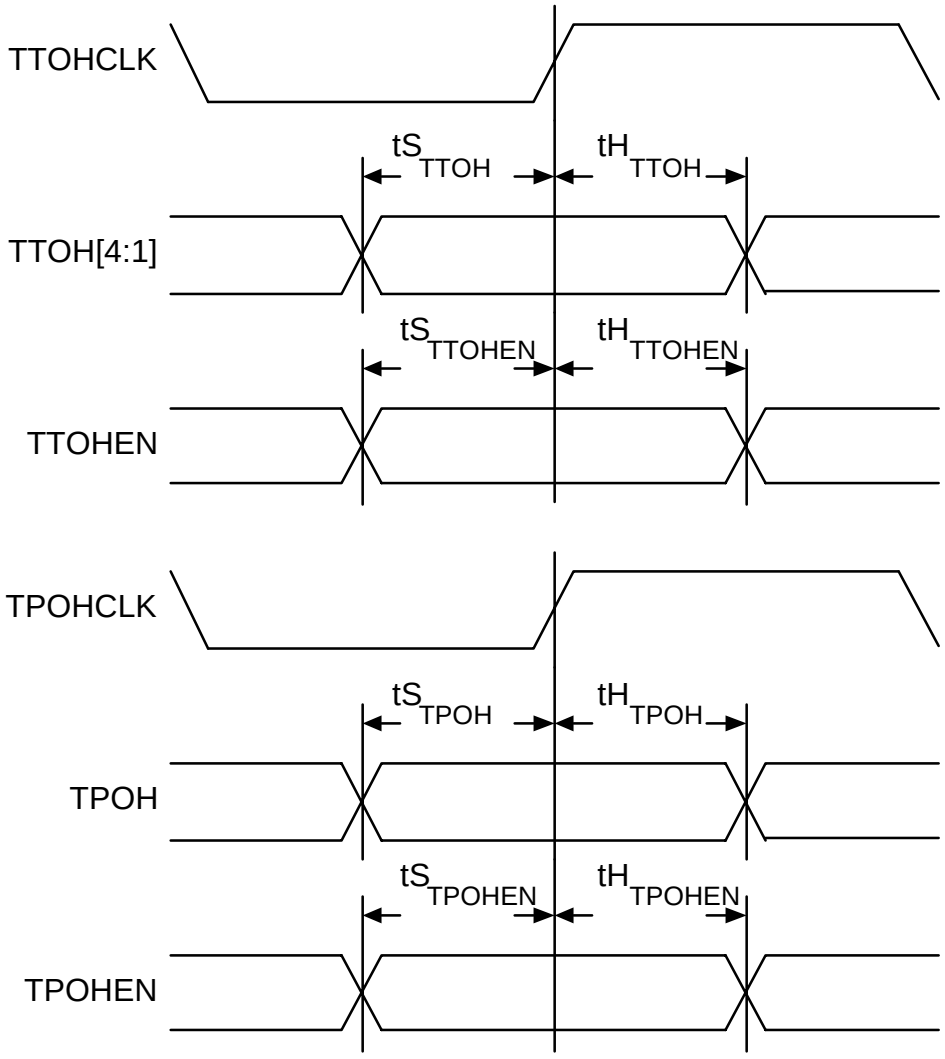
Table 26 - Transmit Overhead Access (Figure 56)

Symbol	Description	Min	Max	Units
$t_{PTTOHFP}$	TTOHCLK Low to TTOHFP Valid	-15	15	ns
$t_{PTPOHFP}$	TPOHCLK Low to TPOHFP Valid	-15	15	ns
t_{STTOH}	TTOH[4:1] Set-up time to TTOHCLK	15		ns
t_{HTTOH}	TTOH[4:1] Hold time to TTOHCLK	5		ns
$t_{STTOHEN}$	TTOHEN Set-up time to TTOHCLK	15		ns
$t_{HTTOHEN}$	TTOHEN Hold time to TTOHCLK	5		ns
t_{STOW}	TSOW, TSUC, TLOW Set-up Time to TOWCLK	15		ns
t_{HTOW}	TSOW, TSUC, TLOW Hold Time to TOWCLK	10		ns
t_{STSD}	TSD Set-up Time to TSDCLK	15		ns
t_{HTSD}	TSD Hold Time to TSDCLK	10		ns

Symbol	Description	Min	Max	Units
tS_{TLD}	TLD Set-up Time to TLDCLK	15		ns
tH_{TLD}	TLD Hold Time to TLDCLK	10		ns
tS_{TPOH}	TPOH Set-up time to TPOHCLK	15		ns
tH_{TPOH}	TPOH Hold time to TPOHCLK	5		ns
tS_{TPOHEN}	TPOHEN Set-up time to TPOHCLK	15		ns
tH_{TPOHEN}	TPOHEN Hold time to TPOHCLK	5		ns

Figure 56 - Transmit Overhead Access Timing





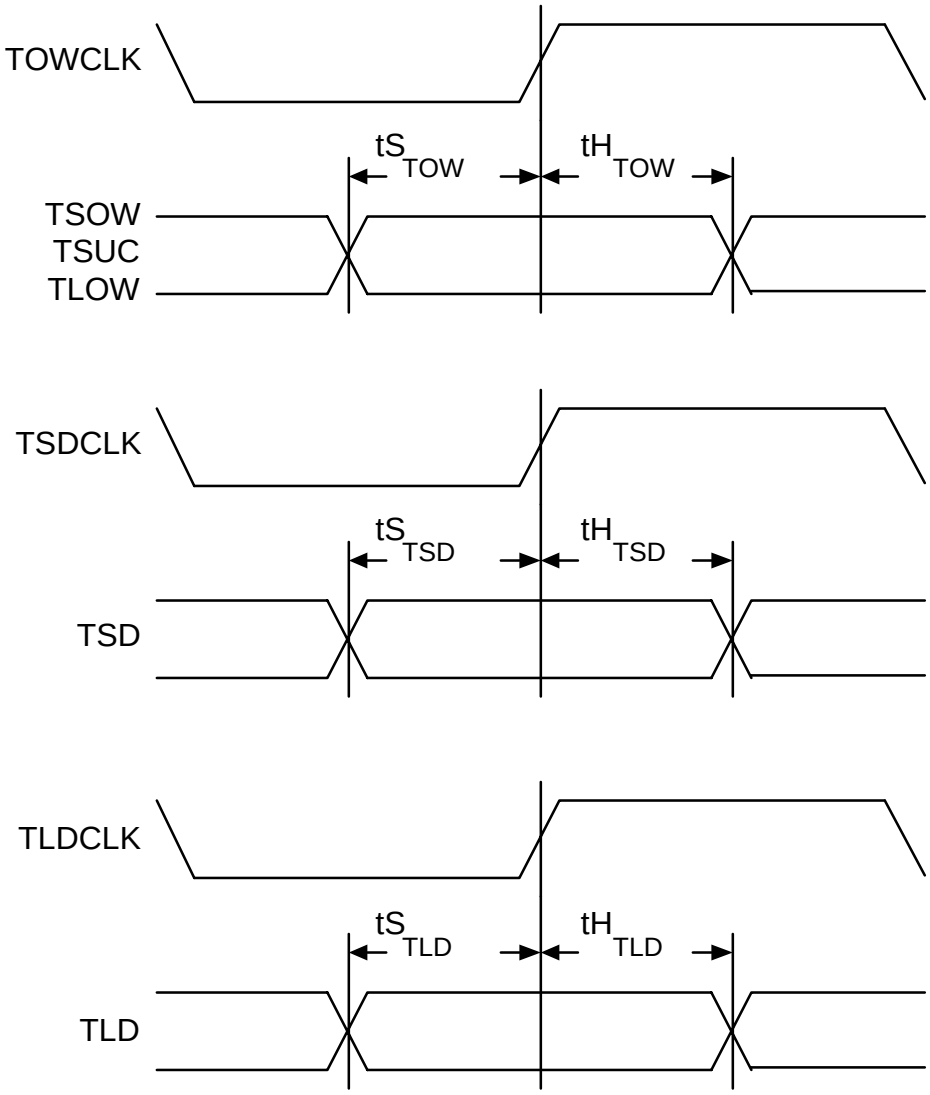


Table 27 - Transmit GFC Access (Figure 57)

Symbol	Description	Min	Max	Units
tP_{TCP}	GTOCLK Low to TCP Valid	3	20	ns
tS_{TGFC}	TGFC Set-up time to GTOCLK	5		ns
tH_{TGFC}	TGFC Hold time to GTOCLK	1		ns

Figure 57 - Transmit GFC Access Timing

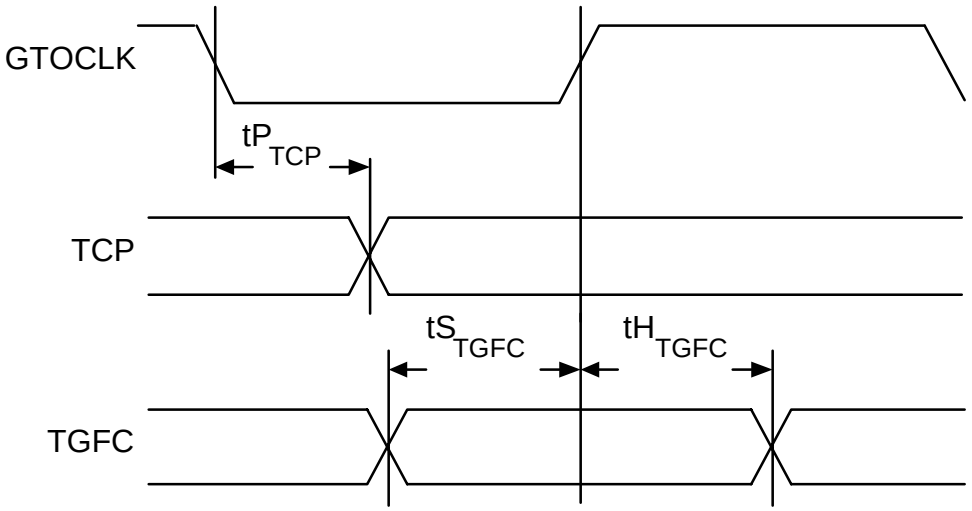
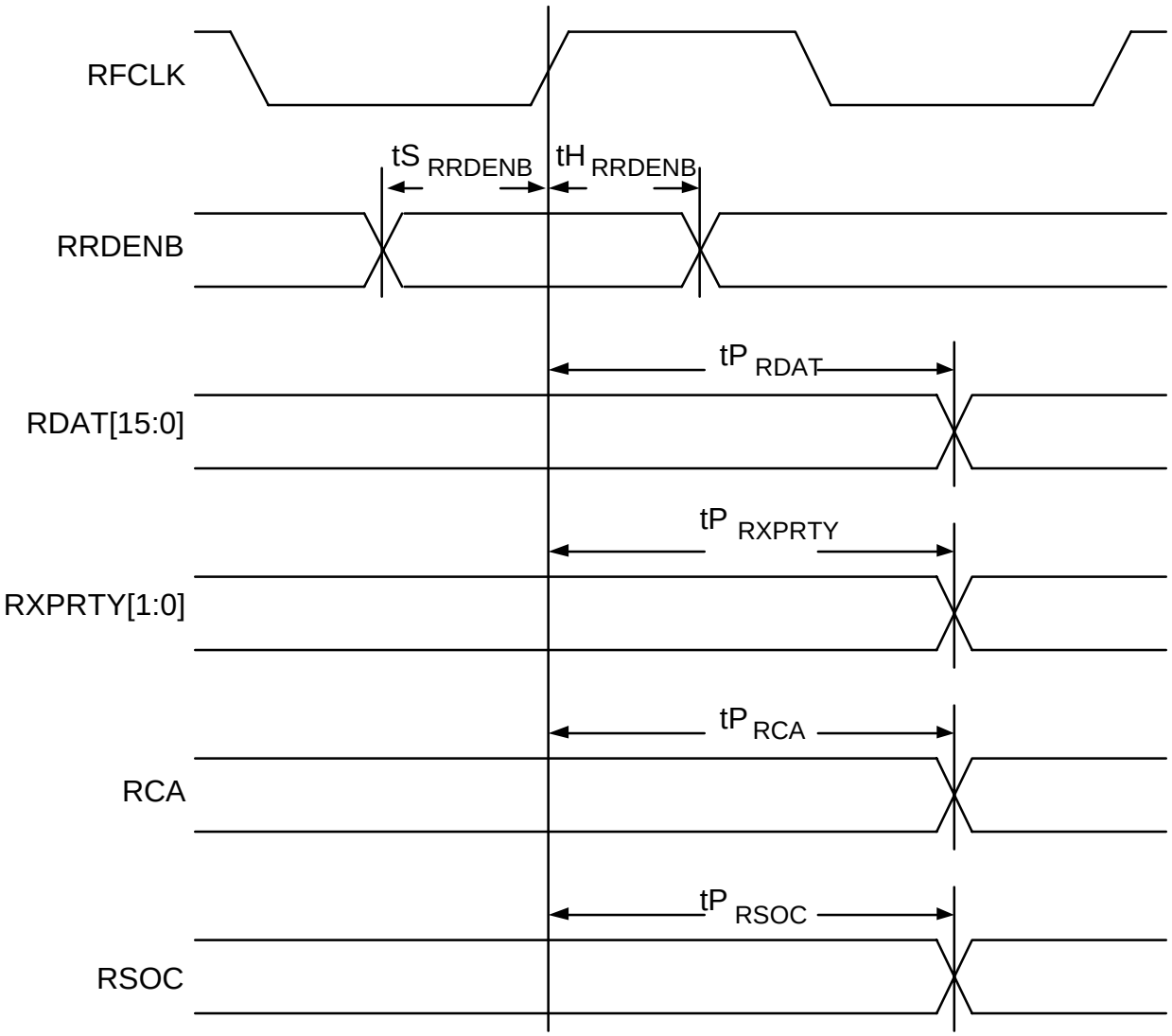


Table 28 - Drop Side Receive Interface (Figure 58)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		52	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB Set-up time to RFCLK	4		ns
tH_{RRDENB}	RRDENB Hold time to RFCLK	1		ns
tP_{RCA}	RFCLK High to RCA Valid	2	14	ns
tP_{RSOC}	RFCLK High to RSOC Valid	2	14	ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	2	14	ns
tP_{RXPRTY}	RFCLK High to RXPRTY[1:0] Valid	2	14	ns
tP_{RFCLK}	RFCLK High to Output Enable	2	14	ns
tZ_{RFCLK}	RFCLK High to Output Tristate	2	14	ns

Figure 58 - Drop Side Receive Interface Timing



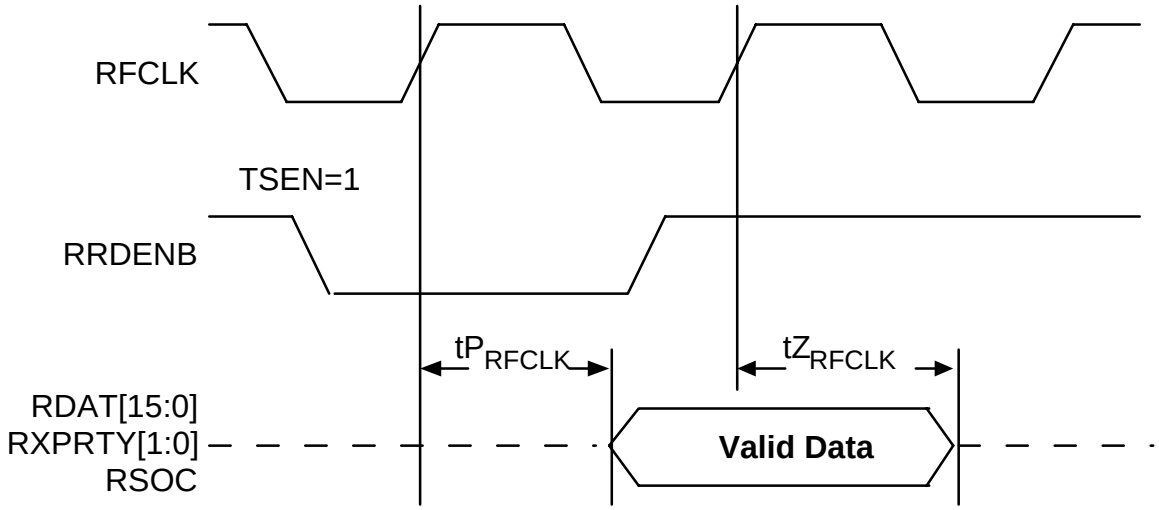


Table 29 - Drop Side Transmit Interface (Figure 59)

Symbol	Description	Min	Max	Units
	TFCLK Frequency		52	MHz
	TFCLK Duty Cycle	40	60	%
tS_{TWRENB}	TWRENB Set-up time to TFCLK	4		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK	1		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	4		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	1		ns
tS_{TXPRTY}	TXPRTY[1:0] Set-up time to TFCLK	4		ns
tH_{TXPRTY}	TXPRTY[1:0] Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	4		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK High to TCA Valid	2	14	ns

Figure 59 - Drop Side Transmit Interface

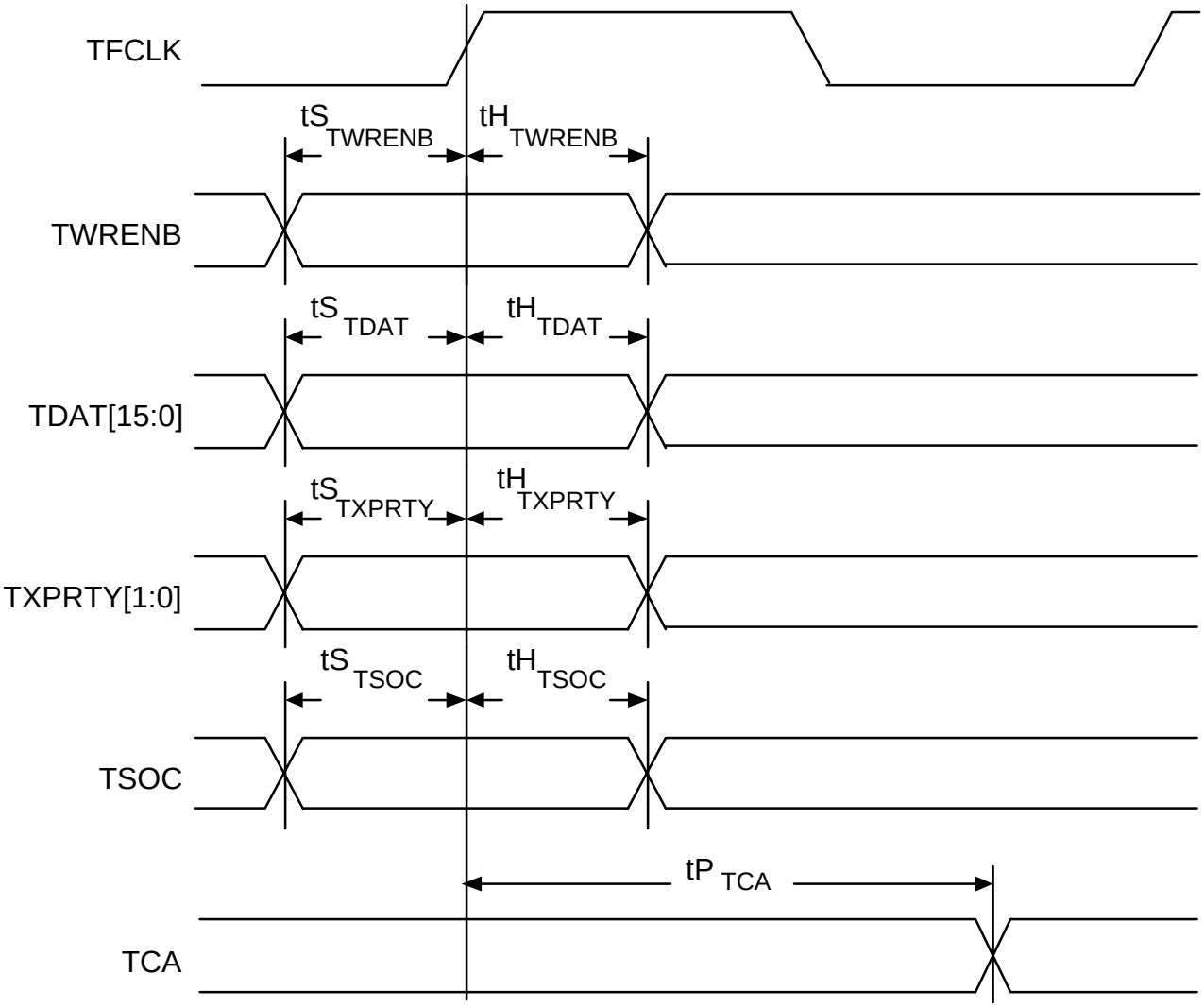
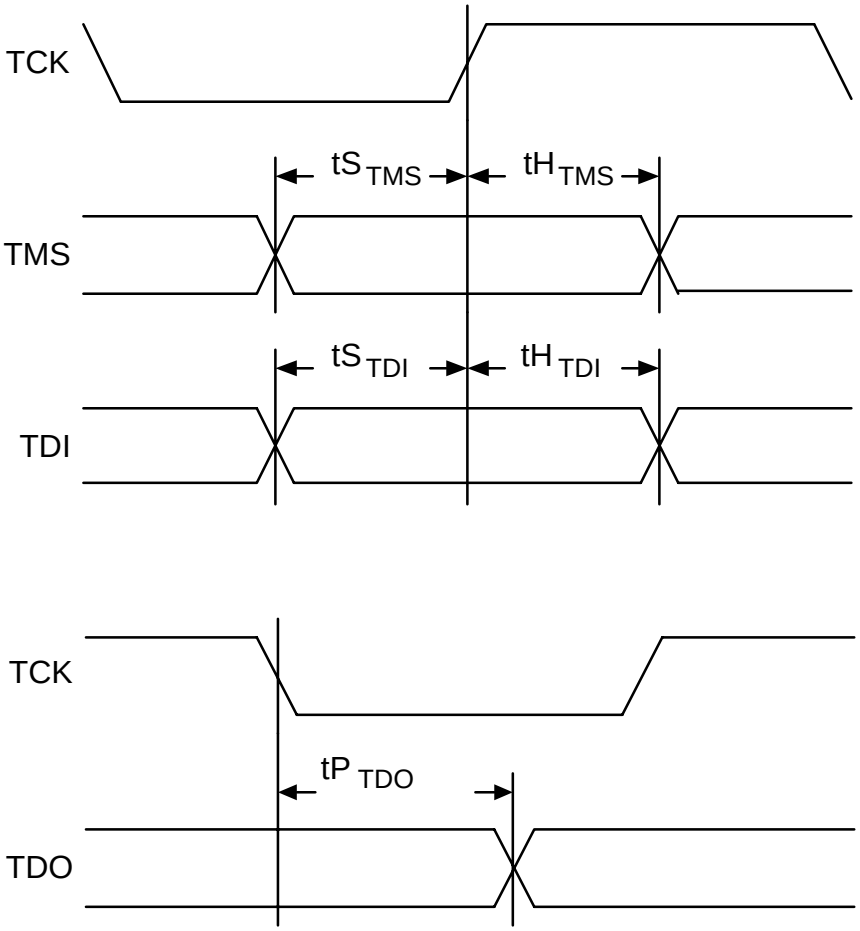


Table 30 - JTAG Port Interface (Figure 60)

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns

Symbol	Description	Min	Max	Units
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 60 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs with the exception of the POUT[7:0], FPOUT and TSOUT outputs. The POUT[7:0], FPOUT and TSOUT output propagation delays are measured with a 30 pF load.

18 ORDERING AND THERMAL INFORMATION

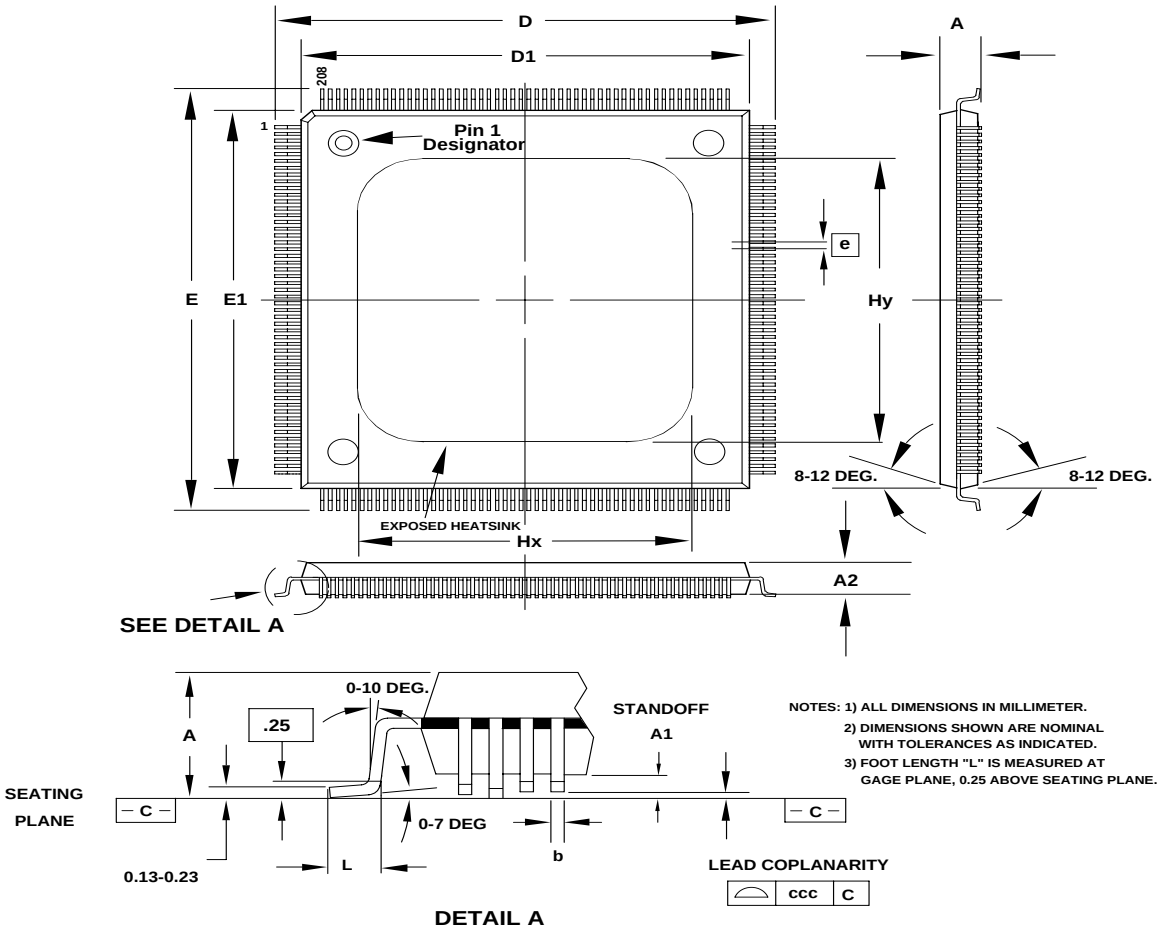
Table 31 -

PART NO.	DESCRIPTION
PM5355-SI	208 Slugged Plastic Quad Flat Pack (PQFP)

Table 32 -

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM5355-SI	-40°C to 85°C	24 °C/W	8 °C/W

19 MECHANICAL INFORMATION



DETAIL A

PACKAGE TYPE: 208 PIN SLUGGED METRIC PLASTIC QUAD FLATPACK-SMQFP													
BODY SIZE: 28 x 28 x 3.49 MM													
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc	Hx	Hy
Min.	3.45	0.25	3.17	30.35	27.80	30.35	27.80	0.45		0.17			
Nom.	3.75	0.35	3.40	30.60	28.00	30.60	28.00	0.60	0.50	0.22		21.00	21.00
Max.	4.10	0.43	3.67	30.85	28.20	30.85	28.20	0.75		0.27	0.10		

NOTES

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