Data Sheet
VSC7121

Quad Port Bypass Circuit for 1.0625 Gbit/sec Fibre Channel Arbitrated Loop Disk Arrays

Description

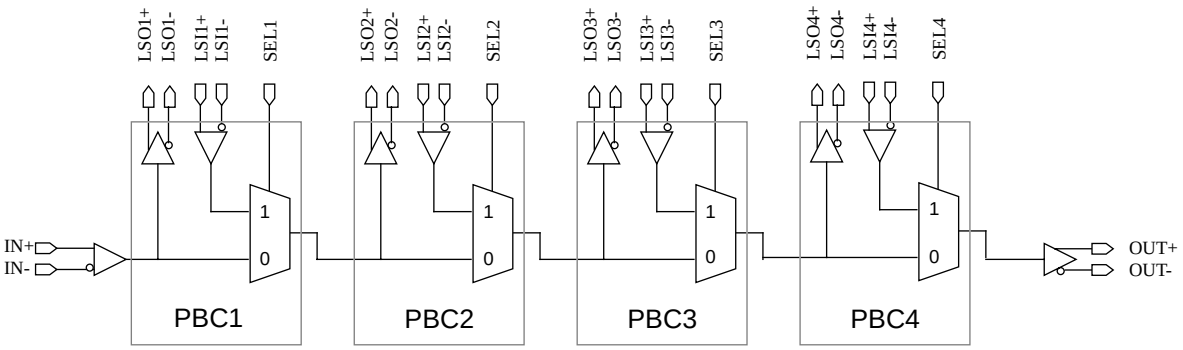
- Supports ANSI X3T11 1.0625 Gbit/sec FC-AL Disk Attach for Resiliency
- Fully Differential for Minimum Jitter Accumulation.
- Quad PBC's in Single Package
- TTL Bypass Select
- High Speed, PECL I/O's Referenced to V_{DD}.
- 0.5W Typical Power Dissipation
- 3.3V Power Supply
- 44-Pin, 10mm PQFP

The VSC7121 is a Quad Port Bypass Circuit (PBC). Four Fibre Channel PBC's are cascaded into a single part to minimize part count, cost, high frequency routing, and jitter accumulation. Port Bypass Circuits are used to provide resiliency in Fibre Channel Arbitrated Loop (FC-AL) architectures. PBC's are used within FC-AL disk arrays to allow for resiliency and hot swapping of FC-AL drives.

A Port Bypass Circuit is a 2:1 Multiplexer with two modes of operation: NORMAL and BYPASS. In NORMAL mode, the disk drive is connected to the loop. Data goes from the 7121's L_SOn pin to the Disk Drive RX input and data from the disk drive TX output goes to the 7121's L_SIn pin. Refer to Figure 2 for disk drive application. In BYPASS mode, the disk drive is either absent or non-functional and data bypasses to the next available disk drive. Normal mode is enabled with a HIGH on the SEL pin and BYPASS mode is enabled by a LOW on the SEL pin. Direct Attach Fibre Channel Disk Drives have an "LRC Interlock" signal defined to control the SEL function.

Using a VSC7121 in a single loop of a disk array is illustrated in Figure 2: "Disk Array Application". FC-AL drives are all expected to be dual loop. The VSC7121 is cascaded in a manner such that all the 7121's internal PBC's are used in the same loop. For dual loop implementations, two or more VSC7121's should be used. Allocating each VSC7121 to only one of two loops preserves redundancy, prevents a single point of failure and lends itself to on-line maintainability.

7121 Block Diagram



The VSC7121 can be cascaded through the IN and OUT pins for arrays of disk drives greater than 4. For disk arrays with a noninteger multiple of 4 disk drives, the unused PBC's can be hardwired to bypass with a external pulldown resistor.

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Table 1 is a truth table detailing the data flow through the VSC7121. Figure 1 shows a timing diagram of the data relationship in the VSC7121. There are no critical timing (setup, hold, or delay) parameters for the VSC7121 as this part routes the serial data encoded with the baud clock that is extracted by a Fibre Channel receiver. The primary AC parameter of importance is the jitter or data eye degradation inserted by the port bypass circuit. The design of the VSC7121 minimizes jitter accumulation by using fully differential circuits. This provides for symmetric rise and fall delays as well as noise rejection.

Table 1: Truth Table

SELECT STATE				*DATA OUTPUTS*				
SEL1	***SEL2***	***SEL3***	***SEL4***	***OUT***	***SO4***	***SO3***	***SO2***	***SO1***
L	L	L	L	IN	IN	IN	IN	IN
L	L	L	H	SI4	IN	IN	IN	IN
L	L	H	L	SI3	SI3	IN	IN	IN
L	H	L	L	SI2	SI2	SI2	IN	IN
H	L	L	L	SI1	SI1	SI1	SI1	IN
H	H	H	H	SI4	SI3	SI2	SI1	IN

Figure 1: Timing Waveforms

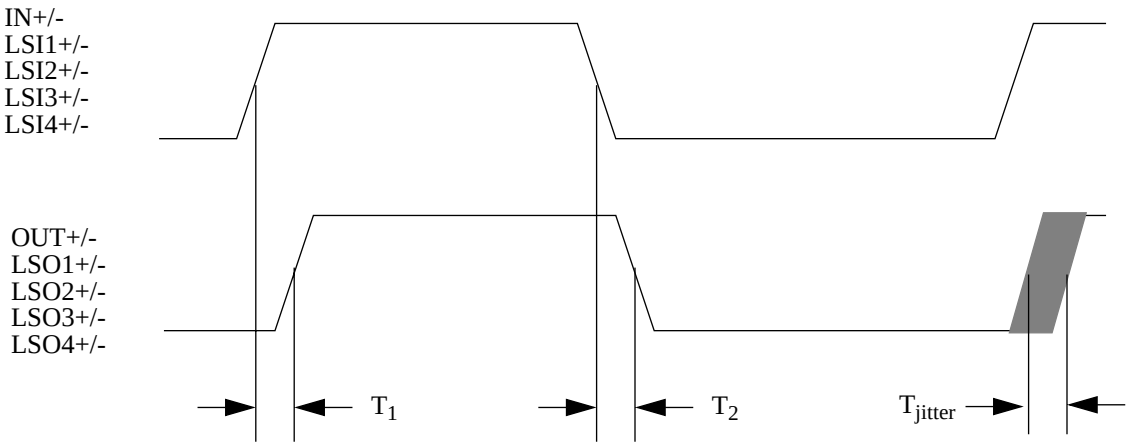

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Figure 2: Disk Array Application

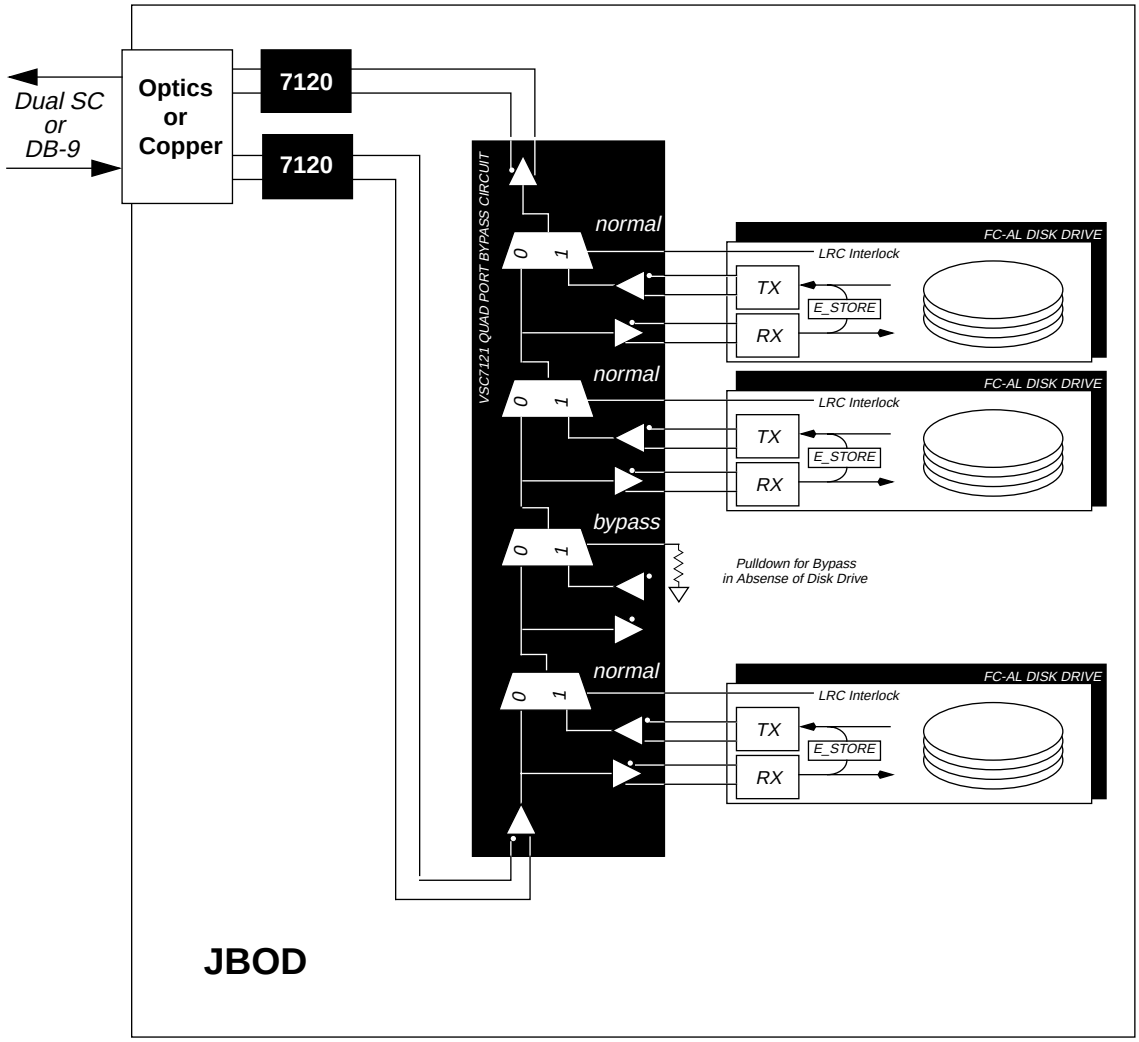

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Table 2: AC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	Flow-Through Propagation Delay Rising Edge to Rising Edge		7.0	ns	Delay with all circuits bypassed. 75 Ohm Load
T_2	Flow through Propagation Delay Falling Edge to Falling Edge		7.0	ns	Delay with all circuits bypassed. 75 Ohm load.
T_{SDR}, T_{SDF}	Serial data rise and fall time	—	300	ps.	20% to 80%, tested on a sample basis

Table 3: DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$V_{IH(TTL)}$	Input HIGH voltage (SEL - TTL)	2.0	—	5.5	V	I_{IH} < 6.6 mA @ V_{IH} = 5.5 V
$V_{IL(TTL)}$	Input LOW voltage (SEL - TTL)	0	—	0.8	V	—
$I_{IH(TTL)}$	Input HIGH current (SEL- TTL)	—	50	500	µA	V_{IN} = 2.4 V
$I_{IL(TTL)}$	Input LOW current (SEL - TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.10	—	3.50	V	V_{DD} = 3.30V ± 5%
I_{DD}	Supply current	—	—	170	mA	Outputs open, V_{DD} = V_{DD} max
P_D	Power Dissipation			0.6	W	Outputs open, V_{DD} = V_{DD} max
$\Delta V_{IN(DF)}$	Receiver differential peak-to-peak Input Sensitivity, IN+/- & L_SIn+/-	300		2600	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
$\Delta V_{OUT(L\_SO)}$	L_SOn+/- output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
$\Delta V_{OUT(OUT)}$	OUT+/- output differential peak-to-peak voltage swing	1200		2200	mVp-p	50Ω to V_{DD} – 2.0 V

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Absolute Maximum Ratings (1)

TTL Power Supply Voltage, (V_{DD}) ..... 0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State, ($V_{IN\ TTL}$) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High) 50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD ..... 1500 V

Recommended Operating Conditions(2)

Power Supply Voltage, (V_{DD}) ..... +3.1V to 3.5V
Ambient Operating Temperature Range, (T) ..... 0°C to +70°C

Notes:

1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
2) *Vitesse guarantees the functional and parametric operation of the part under "Recommended Operating Conditions: except where specifically noted in the AC and DC Parametric Tables*

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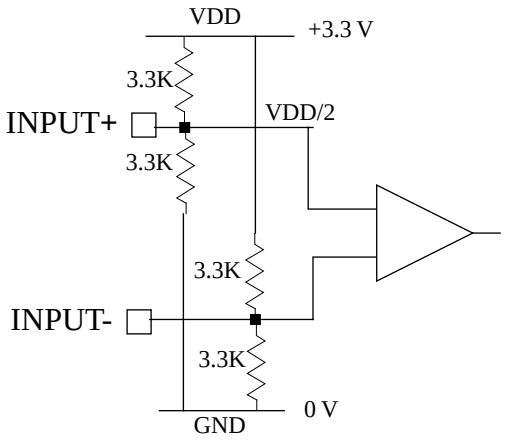
Input Structures

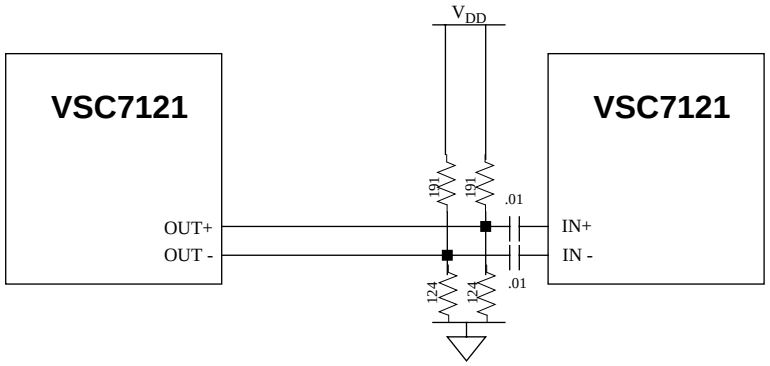
Two input structures exists in this part; TTL and High Speed, Differential Inputs. The TTL Inputs will interface with any TTL or 3.3V or 5V CMOS outputs. The High Speed, Differential Inputs are intended to be AC Coupled per the FC-PH specification. Being AC Coupled, the High Speed, Differential Input buffers are biased at $V_{DD}/2$. Refer to Figure 3 for High Speed, Differential Input structure.

Figure 3: High Speed, Differential Inputs (L_SIn/IN)



Because the VSC7121 output buffers are PECL outputs referenced to V_{DD}, the High Speed Differential outputs may not be direct coupled to the high speed differential inputs. One example of how to differentially cascade the two VSC7121 is shown in Figure 4. This circuit only applies if trace lengths are less than three inches.

Figure 4: Cascading Two VSC7121



75 Ohm Board/Termination Example

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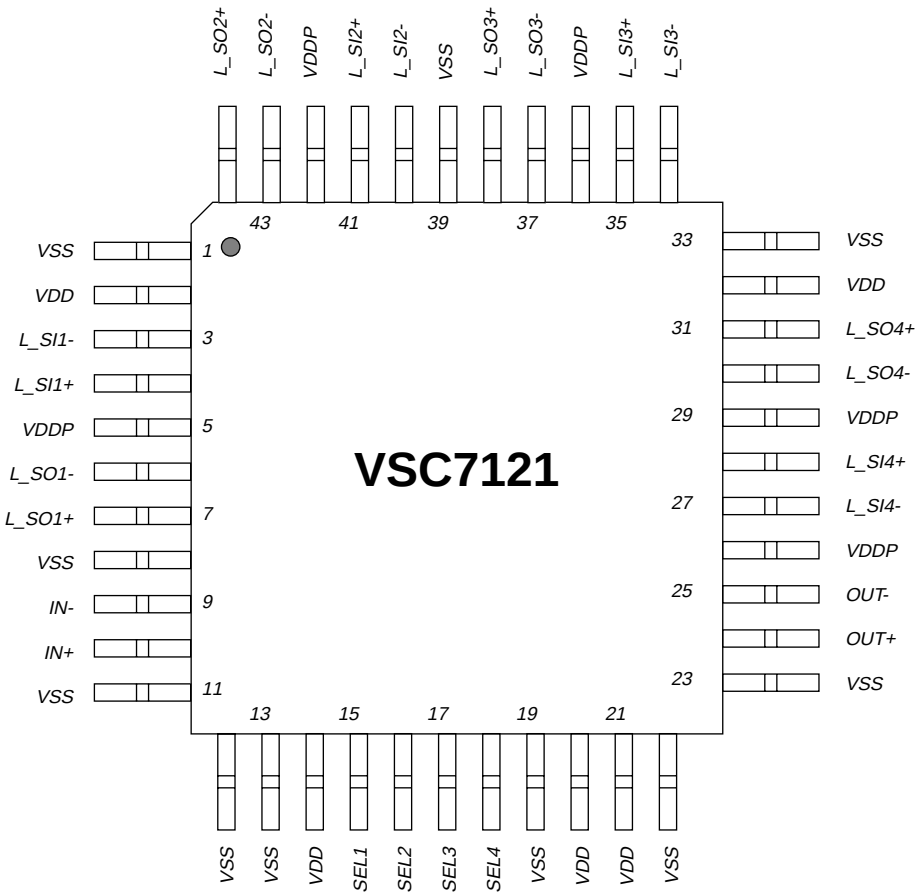
Figure 5: Pin Diagram



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Package Pin Description

Table 4: Pin Description

Pin #	*Name*	*Description*
9, 10	IN-, IN+	INPUT - Differential (Biased at VDD/2). Differential inputs from the downstream PBC port.
3, 4	L_SI1-, L_SI1+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 1.
40, 41	L_SI2-, L_SI2+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 2.
34, 35	L_SI3-, L_SI3+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 3.
27, 28	L_SI4-, L_SI4+	INPUT - Differential (Biased at VDD/2). Serial input from the local transmitter on PBC port 4.
15-18	SEL1, SEL2, SEL3, SEL4	INPUT - TTL. A LOW selects the “BYPASS” mode causing the output of the previous port to propagate to next port or OUT. When HIGH, this signal selects “NORMAL” mode which routes the previous port to the local output, L_SOn, and routes the local input, L_SIn, to the next port or OUT .
6, 7	L_SO1-, L_SO1+	OUTPUT - Differential (Biased at VDD-1.32V). Serial output driving the local receiver corresponding to PBC port 1.
43, 44	L_SO2-, L_SO2+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 2.
37, 38	L_SO3-, L_SO3+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 3.
30, 31	L_SO4-, L_SO4+	OUTPUT - Differential (Biased at VDD-1.32V) Serial output driving the local receiver corresponding to PBC port 4.
25, 24	OUT-, OUT+	OUTPUT - Differential (Biased at VDD - 1.32V) Serial output driving the upstream PBC port.
2, 14, 20-21, 32	VDD	Digital Logic Power Supply. 3.3V Supply for digital logic.
5, 26, 29 36, 42	VDDP	High-Speed Output Power Supply. 3.3V Supply for PECL drivers.
1, 8, 11-13, 19, 22-23, 33, 39	VSS	Ground. Ground pins are physically attached to the die mounting surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.

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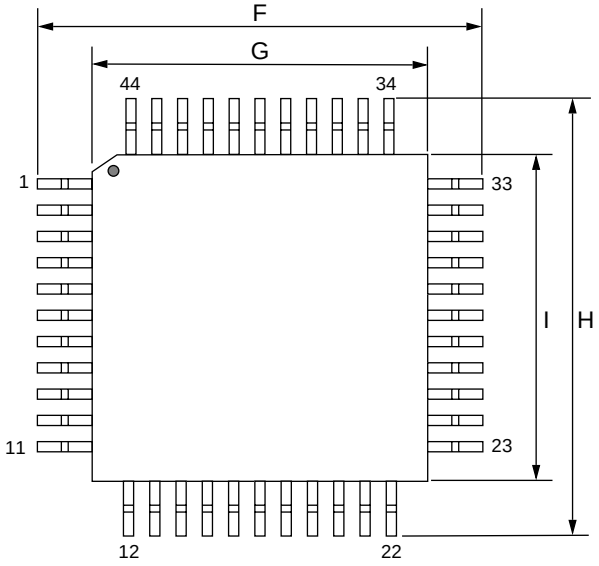
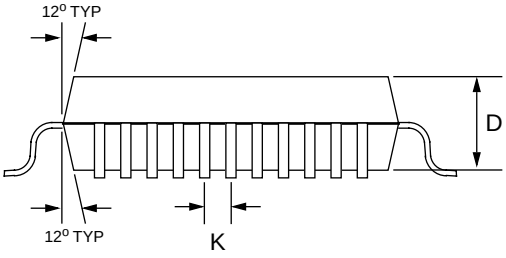
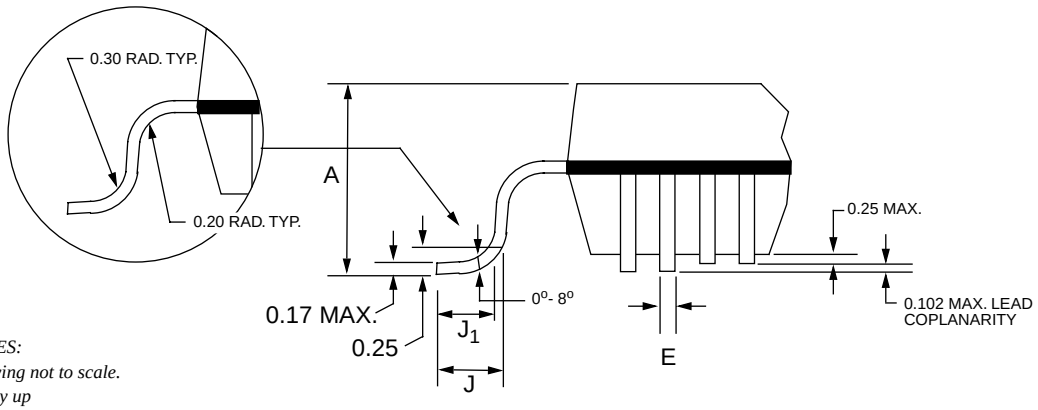
Package Information

44-Pin PQFP 10 x 10 mm



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10
E	0.35	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
K	0.80	BASIC





NOTES:
Drawing not to scale.
Cavity up
All units in mm unless otherwise noted.

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Package Thermal Characteristics

The VSC7121 is packaged into a standard plastic quad flatpack with an embedded, but unexposed thermal slug. This package adheres to industry standard EIAJ footprints for a 10x10mm body, 44 lead PQFP. The package construction is as shown in Figure 6. The 44 PQFP with embedded slug has the thermal properties shown in Table 5. This package allows the VSC7121 to operate with ambient temperatures up to 70°C in still air.

Figure 6: Package Cross Reference

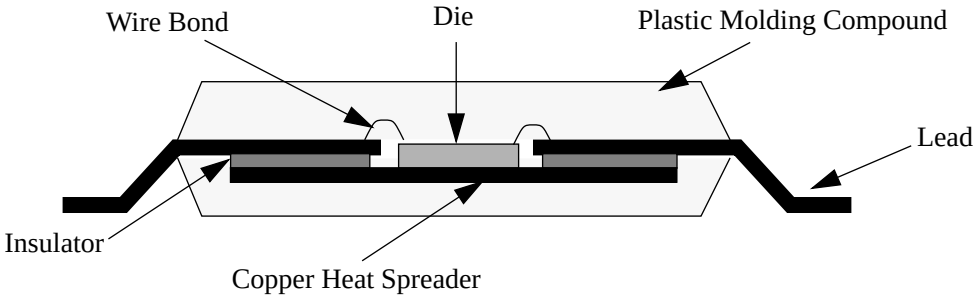

Table 5: 44 PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
$\theta_{ca\text{-}0}$	Thermal resistance from case to ambient, still air	50	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient, 100 LFPM air	43	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient, 200 LFPM air	39	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient, 400 LFPM air	36	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient, 600 LFPM air	34	°C/W

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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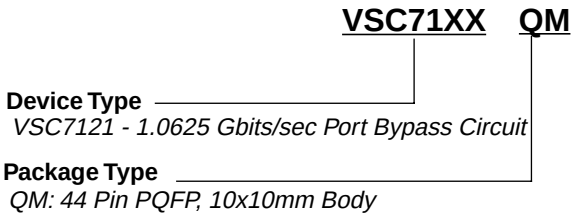
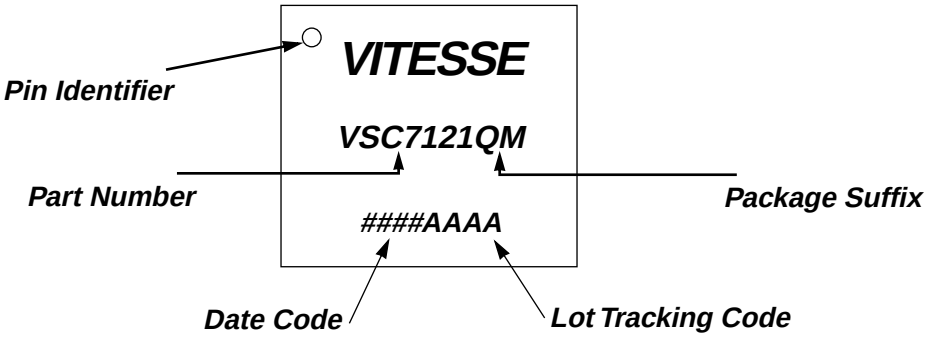
Ordering Information

The order number for this product is formed by a combination of the device number and package type.



Marking Information

The package is marked with three lines of text as shown below (QM Package):



Notice

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Warning

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