National Semiconductor

December 1994

DAC1218/DAC1219
12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved though the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors and allows the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

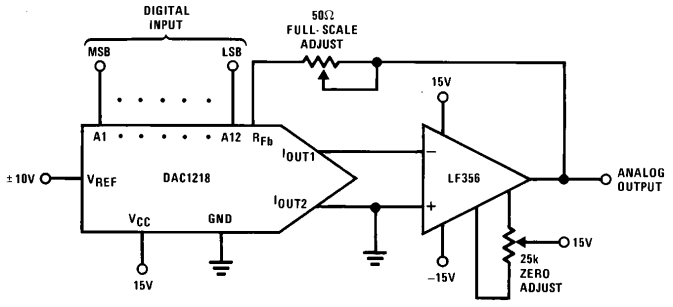
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



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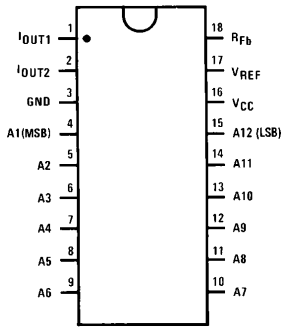
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



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Top View

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	Package Outline
Non Linearity	0.012%	DAC1218LCJ-1	DAC1218LCJ	J18A Cerdip
	0.024%		DAC1219LCJ	J18A Cerdip

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 11)	800V

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1218LCJ, DAC1219LCJ	$-40°C \le T_A \le +85°C$
DAC1218LCJ-1	$0°C \le T_A \le 70°C$
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 9);** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted	4, 5, 9				
	DAC1218			**±0.018**	**±0.018**	% of FSR
	DAC1219			**±0.024**	**±0.024**	% of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted	4, 5, 9				
	DAC1218			**±0.018**	**±0.018**	% of FSR
	DAC1219			**±0.024**	**±0.024**	% of FSR
Monotonicity		4	12	12	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb}, V_{REF} = ±10V, ±1V	5	−0.1	0.0		% of FSR
Gain Error (Max)		5	−0.1	−0.2		% of FSR
Gain Error Tempco		5	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs High	5	±3.0	±30		ppm of FSR/V
Reference Input Resistance	(Min)	9	15	**10**	**10**	kΩ
	(Max)	9	15	**20**	**20**	kΩ
Output Feedthrough Error	V_{REF} = 120 Vp-p, f = 100 kHz All Data Inputs Low	6	3.0			mVp-p
Output Capacitance	All Data Inputs High I_{OUT1}				200	pF
	All Data Inputs High I_{OUT2}				70	pF
	All Data Inputs Low I_{OUT1}				70	pF
	All Data Inputs Low I_{OUT2}				200	pF
Supply Current Drain		9		2.0	**2.5**	mA
Output Leakage Current		7, 9				
I_{OUT1}	All Data Inputs Low			**10**	**10**	nA
I_{OUT2}	All Data Inputs High			**10**	**10**	nA
Digital Input Threshold	Low Threshold	9		**0.8**	**0.8**	V_{DC}
	High Threshold			**2.2**	**2.2**	V_{DC}
Digital Input Currents	Digital Inputs <0.8V	9		**−200**	**−200**	μA_{DC}
	Digital Inputs >2.2V			**10**	**10**	μA_{DC}
t_s Current Settling Time	R_L = 100Ω, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously		1			μs

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% $\times$ V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of FSR $= V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ± 6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from -40°C to $+85$°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is $\pm 0.075\%$ of V_{REF}.

Note 6: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 7: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 8: Human body model, 100 pF discharged through 1.5 kΩ resistor.

Note 9: Tested limit for -1 suffix parts applies only at 25°C.

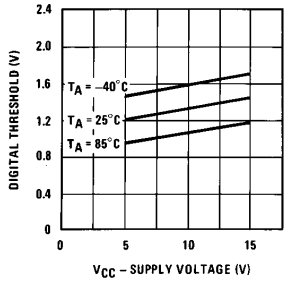
Note 10: Typicals are at 25°C and represent the most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

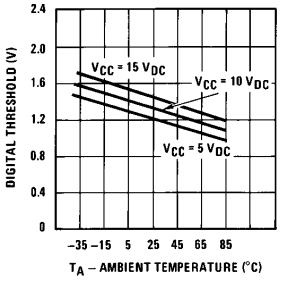
Note 12: Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

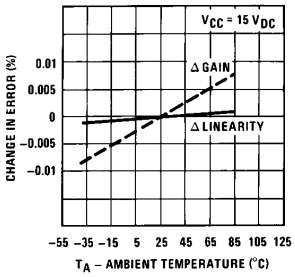
Digital Input Threshold vs V_{CC}



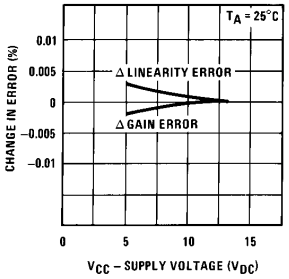
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



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Definition of Package Pinouts

(A1–A12): Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} =$ constant (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error in the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

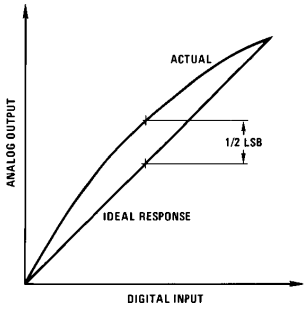
Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

Full-scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

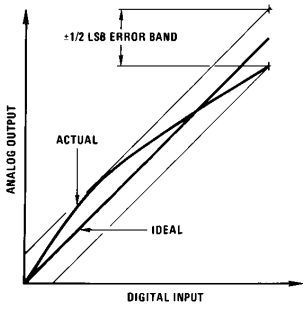
Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.

a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test



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Application Hints

The DAC1218 and DAC1219 are pin-for-pin compatible with the DAC1220 series but feature 12 and 11-bit linearity specifications. To preserve this degree of accuracy, care must be taken in the selection and adjustments of the output amplifier and reference voltage. Careful PC board layout is important, with emphasis made on compactness of components to prevent inadvertent noise pickup and utilization of single point grounding and supply distribution.

1.0 BASIC CIRCUIT DESCRIPTION

Figure 1 illustrates the R-2R current switching ladder network used in the DAC1218 and DAC1219. As a function of the logic state of each digital input, the binarily weighted current in each leg of the ladder is switched to either I_{OUT1} or I_{OUT2}. The voltage potential at I_{OUT1} and I_{OUT2} must be at zero volts to keep the current in each leg the same, independent of the switch state.

The switches operate with a small voltage drop across them and can therefore conduct currents of either polarity. This permits the reference to be positive or negative, thereby allowing 4-quadrant multiplication by the digital input word. The reference can be a stable DC source or a bipolar AC signal within the range of ± 10V, for specified accuracy, with an absolute maximum range of ± 25V. The reference can also exceed the applied V_{CC} of the DAC.

The maximum output current from either I_{OUT1} or I_{OUT2} is equal to

$$\frac{V_{REF(max)}}{R}\left(\frac{4095}{4096}\right),$$

where R is the reference input resistance (typically 15 kΩ). A high level on any digital input steers current to I_{OUT1} and a low level steers current to I_{OUT2}.

2.0 CREATING A UNIPOLAR OUTPUT VOLTAGE (A DIGITAL ATTENUATOR)

To generate an output voltage and keep the potential at the current output terminals at 0V, an op amp current to voltage converter is used. As shown in *Figure 2*, the current from I_{OUT1} flows through the feedback resistor, forcing a proportional voltage at the amplifier output. The voltage at I_{OUT1} is held at a virtual ground potential. The feedback resistor is provided on the chip and should always be used as it matches and tracks the R value of the R-2R ladder. The output voltage is the opposite polarity of the applied reference voltage.

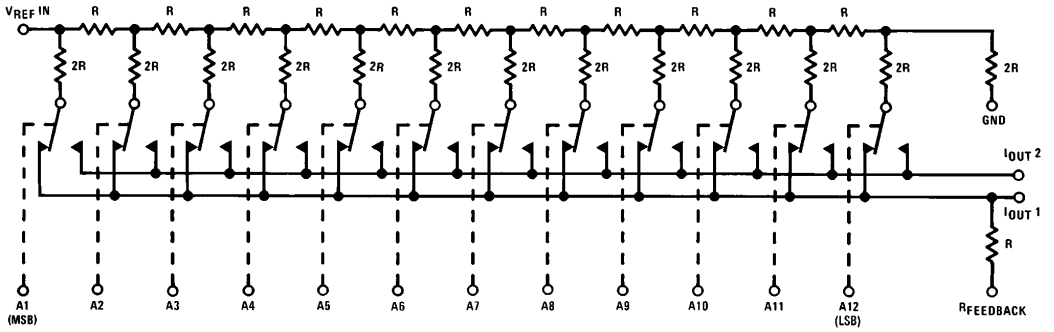
2.1 Amplifier Considerations

To maintain linearity of the output voltage with changing digital input codes the input offset voltage of the amplifier must be nulled. The resistance from I_{OUT1} to ground ($R_{I_{OUT1}}$) varies non-linearly with the applied digital code from a minimum of R with all ones applied to the input to near ∞ with an all zeros code. Any offset voltage between the amplifier inputs appears at the output with a gain of

$$1 + \frac{R_F}{R_{I_{OUT1}}}.$$

Since $R_{I_{OUT1}}$ varies with the input code, any offset will degrade output linearity. (See Note 4 of Electrical Characteristics.)

If the desired amplifier does not have offset balancing pins available (it could be part of a dual or quad package) the nulling circuit of *Figure 3* can be used. The voltage at the non-inverting input will be set to $-V_{OS}$ initially to force the inverting input to 0V. The common technique of summing current into the amplifier summing junction cannot be used as it directly introduces a zero code output current error.



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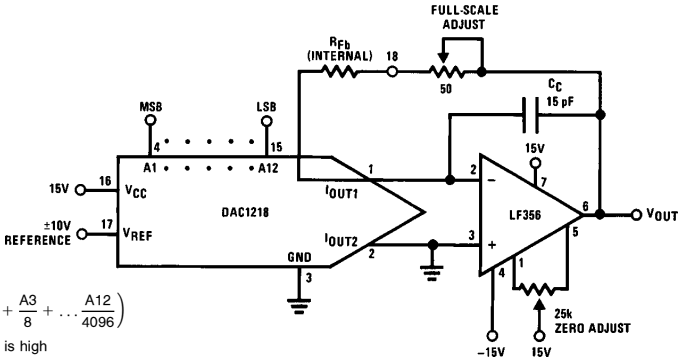
Note: Switches shown in digital high state.

FIGURE 1. The R-2R Current Switching Ladder Network

Application Hints (Continued)



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

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FIGURE 2. Unipolar Output Voltage

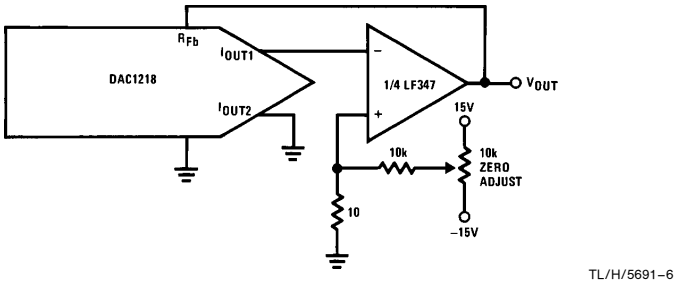

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FIGURE 3. Zeroing an Amplifier Which Does Not Have Balancing Provisions

The selected amplifier should have as low an input bias current as possible since input bias current contributes to the current flowing through the feedback resistor. BI-FET™ op amps such as the LF356 or LF351 or bipolar op amps with super β input transistors like the LM11 or LM308A produce negligible errors.

2.2 Zero and Full-Scale Adjustments

The fundamental purpose is to make the output voltages as near 0 V_{DC} as possible. This is accomplished in the circuit of *Figure 2* by shorting out the amplifier feedback resistance, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital input of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The feedback short is then removed and the converter is zero adjusted.

A unique characteristic of these DACs is that any full-scale or gain error is always negative. This means that for a full-scale input code the output voltage, if not inherently correct, will always be less than what it should be. This ensures that adding an appropriate resistance in series with the internal feedback resistor, R_{Fb}, will always correct for any gain error. The 50Ω potentiometer in *Figure 2* is all that is needed to adjust the worst case DAC gain error.

Conversion accuracy is only as good as the applied reference voltage, so providing a source that is stable over time and temperature is important.

2.3 Output Settling Time

The output voltage settling time for this circuit in response to a change of the digital input code (a full-scale change is the worst case) is a combination of the DAC's output current settling characteristics and the settling characteristics of the output amplifier. The amplifier settling is further degraded by a feedback pole formed by the feedback resistance and the DAC output capacitance (which varies with the digital code). First order compensation for this pole is achieved by adding a feedback zero with capacitor C_C shown in *Figure 2*.

In many applications output response time and settling is just as important as accuracy. It can be difficult to find a single op amp that combines excellent DC characteristics (low V_{OS}, V_{OS} drift and bias current) with fast response and settling time. BI-FET op amps offer a reasonable compromise of high speed and good DC characteristics. The circuit of *Figure 4* illustrates a composite amplifier connection that combines the speed of a BI-FET LF351 with the excellent DC input characteristics of the LM11. If output settling time is not so critical, the LM11 can be used alone.

Figure 5 is a settling time test circuit for the complete voltage output DAC circuit. The circuit allows the settling time of the DAC amplifier to be measured to a resolution of 1 mV out of a zero to ±10V full-scale output change on an oscilloscope. *Figure 6* summarizes the measured settling times for several output amplifiers and feedback compensation capacitors.

Application Hints (Continued)

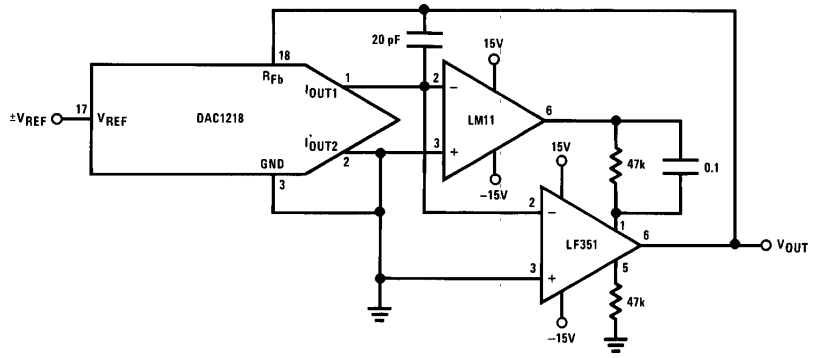

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FIGURE 4. Composite Output Amplifier Connection

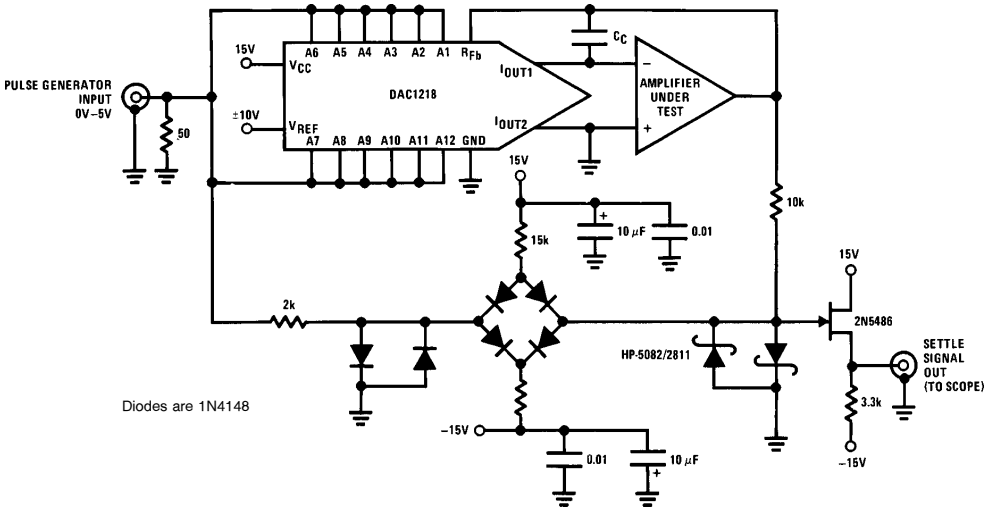

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FIGURE 5. DAC Settling Time Test Circuit

Amplifier	C_C	Settling Time to 0.01%
LM11	20 pF	30 µs
LF351	15 pF	8 µs
LF351	30 pF	5 µs
Composite LM11-LF351	20 pF	8 µs
LF356	15 pF	6 µs

FIGURE 6. Some Measured Settling Times

Application Hints (Continued)

3.0 OBTAINING A BIPOLAR OUTPUT VOLTAGE FROM A FIXED REFERENCE

The addition of a second op amp to the circuit of *Figure 2* can generate a bipolar output voltage from a fixed reference voltage (*Figure 7*). This, in effect gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference voltage can also be reversed to realize full 4-quadrant multiplication.

The output responds in accordance to the following expression:

$$V_O = V_{REF}\left(\frac{D - 2048}{2048}\right), 0 \le D \le 4095$$

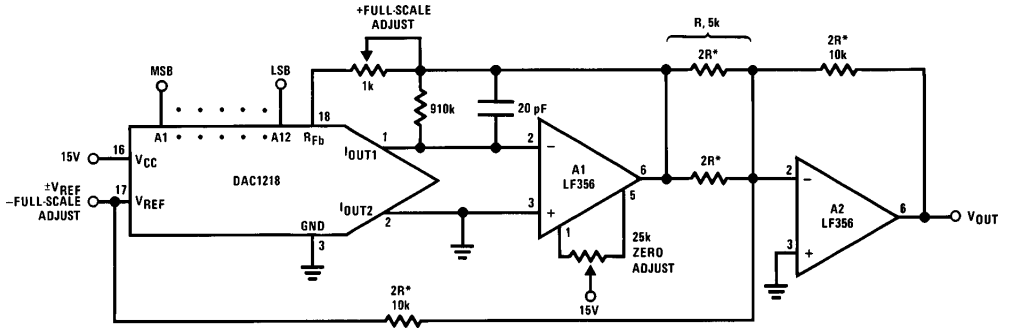
where D is the decimal equivalent of the true binary input word. This configuration inherently accepts a code (half-scale or D = 2048) to provide 0V out without requiring an external ½ LSB offset as needed by other bipolar multiplying DAC circuits.

Only the offset voltage of amplifier A1 need be nulled to preserve linearity. The gain setting resistors around A2 must match and track each other. A thin film, 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four resistors can be paralleled to form R and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

Applied Digital Input MSB											LSB	Decimal Equivalent	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
1	1	1	1	1	1	1	1	1	1	1	1	4095	$V_{REF} - 1$ LSB	$-\|V_{REF}\| + 1$ LSB
1	1	0	0	0	0	0	0	0	0	0	0	3072	$V_{REF}/2$	$-\|V_{REF}\|/2$
1	0	0	0	0	0	0	0	0	0	0	0	2048	0	0
0	1	1	1	1	1	1	1	1	1	1	1	2047	-1 LSB	$+1$ LSB
0	1	0	0	0	0	0	0	0	0	0	0	1024	$-V_{REF}/2$	$+\|V_{REF}\|/2$
0	0	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}$	$+\|V_{REF}\|$

Where 1 LSB $= \frac{|V_{REF}|}{2048}$



*0.1% matching

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FIGURE 7. Obtaining a Bipolar Output from a Fixed Reference

Application Hints (Continued)

3.1 Zero and Full-Scale Adjustments

The three adjustments needed for this circuit are shown in *Figure 7*. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adjust" for zero volts at the inverting input (pin 2) of OA1. Next, with a code of all zeros still applied, adjust "- full-scale adjust", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+ full-scale adjust" for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. This + full-scale adjustment scheme takes into account the effects of the V_{OS} of amplifier A2 (as long as this offset is less than 0.1% of V_{REF}) and any gain errors due to external resistor mismatch.

4.0 MISCELLANEOUS APPLICATION HINTS

The devices are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to electrostatic discharge.

During power-up supply voltage sequencing, the negative supply of the output amplifier may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is clamped to one diode drop below ground.

As a general rule, any unused digital inputs should be tied high or low as required by the application. As a troubleshooting aid, if any digital input is left floating, the DAC will interpret that input as a logical 1 level.

Additional Application Ideas

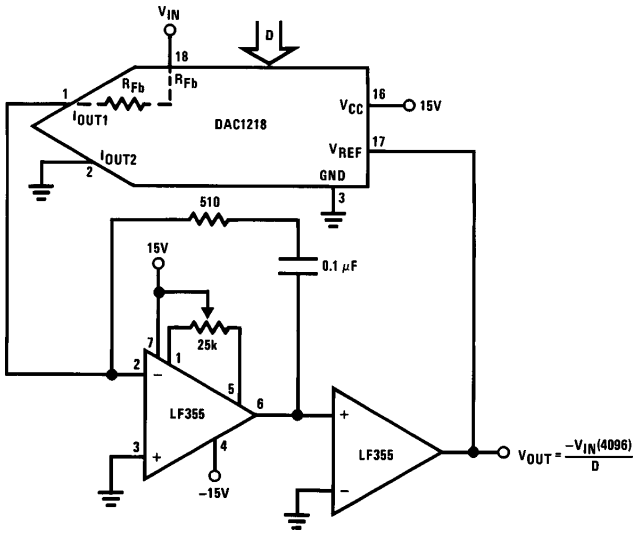
For the circuits shown, D represents the decimal equivalent of the binary digital input code. D ranges from 0 (for an all zeros input code) to 4095 (for an all ones input code) and for any code can be determined from:

$$D = 2048(A1) + 1024(A2) + 512(A2) + \ldots 2(A11) + 1(A12)$$

where AN = 1 if that input is high

AN = 0 if that input is low

DAC Controlled Amplifier



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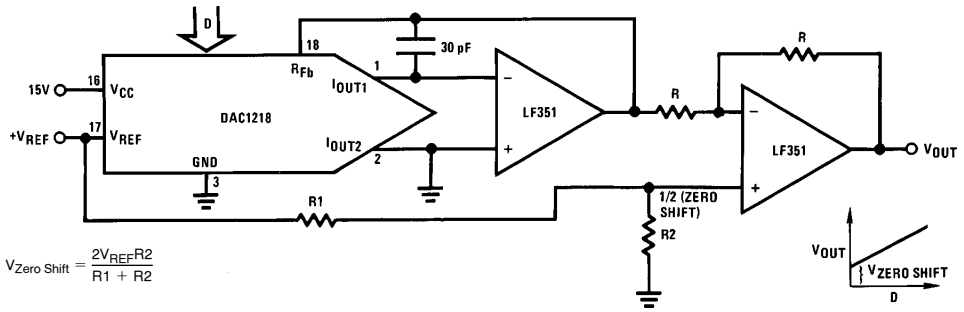
Additional Application Ideas (Continued)

Offsetting the Zero Code Output Voltage



$$V_{Zero\ Shift} = \frac{2V_{REF}R2}{R1 + R2}$$

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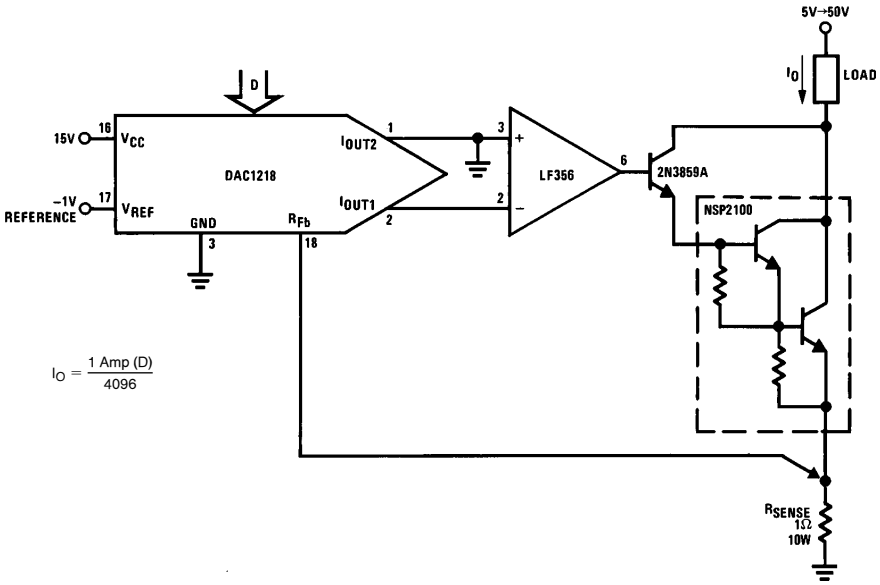
High Current Controller



$$I_O = \frac{1\ Amp\ (D)}{4096}$$

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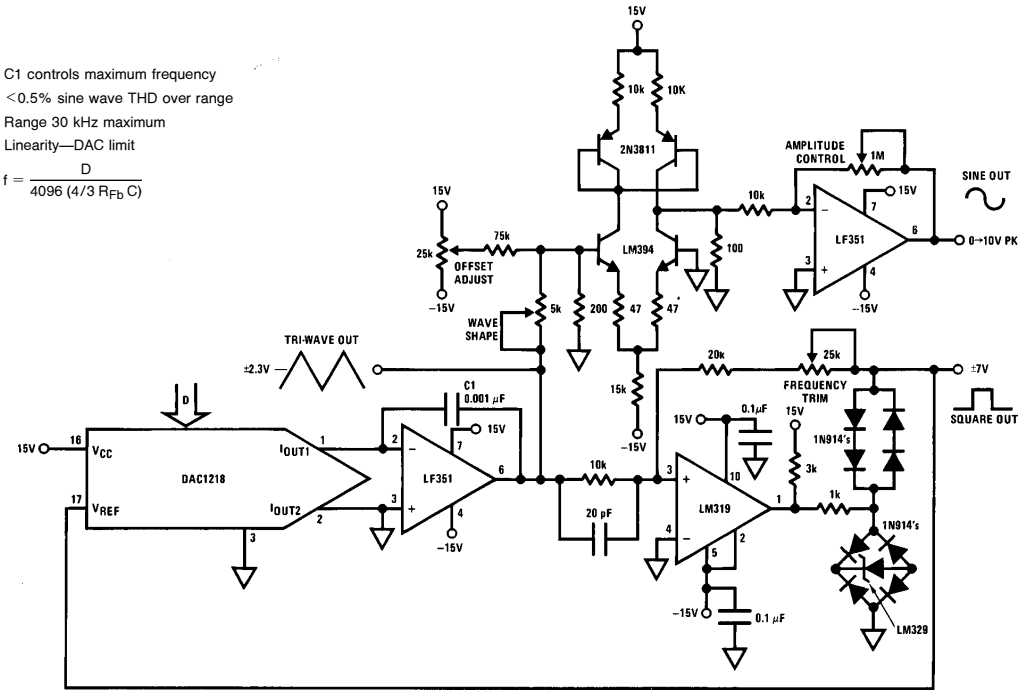
Additional Application Ideas (Continued)

DAC Controlled Function Generator

- C1 controls maximum frequency
- <0.5% sine wave THD over range
- Range 30 kHz maximum
- Linearity—DAC limit
- $f = \frac{D}{4096\ (4/3\ R_{Fb}\ C)}$



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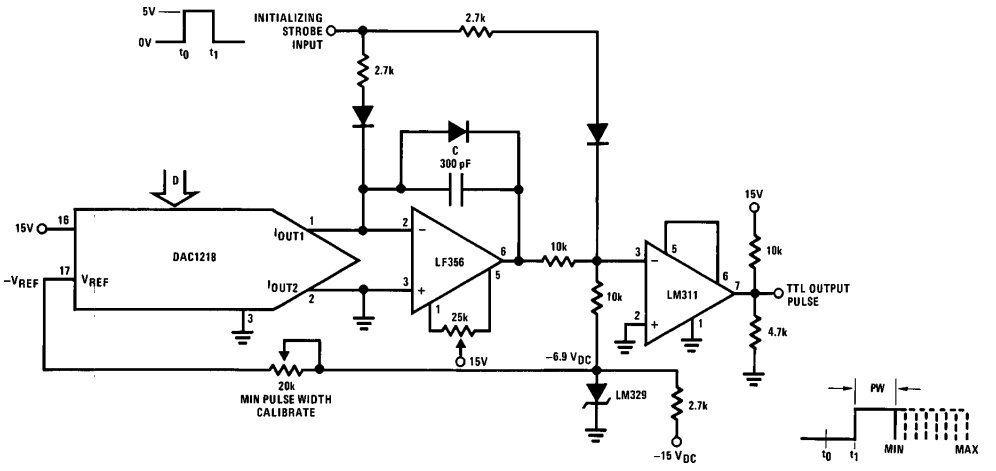
Digitally Programmable Pulse-Width Generator



$PW \cong \frac{C(7.5V)\ (4096)\ (R_{Fb})}{D V_{REF}}$

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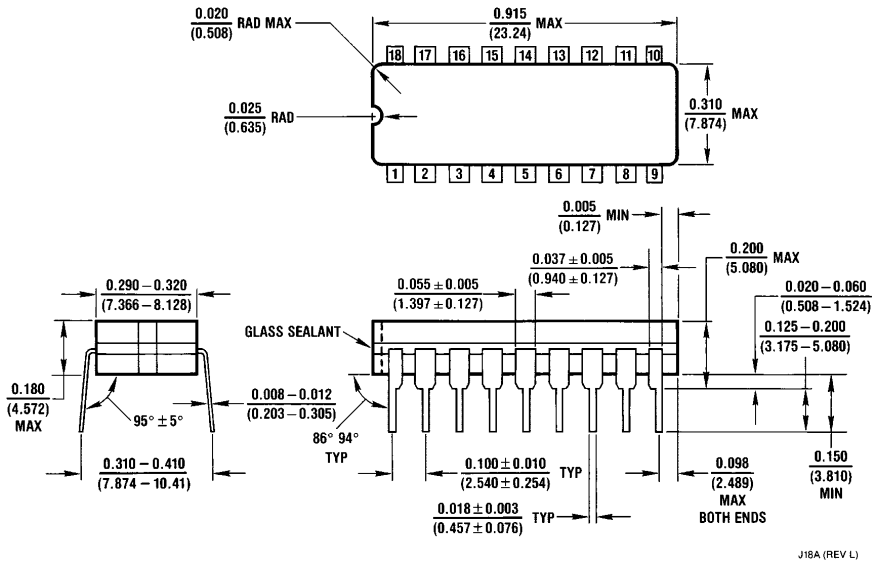
Physical Dimensions inches (millimeters)



Order Number DAC1218LCJ-1, DAC1218LCJ or DAC1219LCJ
NS Package Number J18A

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