SONY

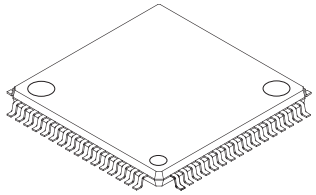
CXA3512R

LCD Driver

Description

The CXA3512R is a driver IC for the analog inputs of SVGA or higher Sony polycrystalline silicon TFT LCD panels. It has a line invert amplifier and analog demultiplexers, as well as the timing generator and output buffers required for these. The CXA3512R can directly drive an LCD panel. The VCOM setting circuit and precharge pulse waveform generator are also on-chip.

64 pin LQFP (Plastic)



Features

- High-speed signal processing supports XGA high refresh signal
- Overall wide band response
- Low output deviation by on-chip output offset cancel circuit
- Invert amplifier with small phase delay difference between inverted signal and non-inverted signal
- On-chip timing generator with ECL
- Dot clock phase adjustment function
- VCOM voltage generation circuit
- Precharge pulse waveform generation circuit

Absolute Maximum Ratings

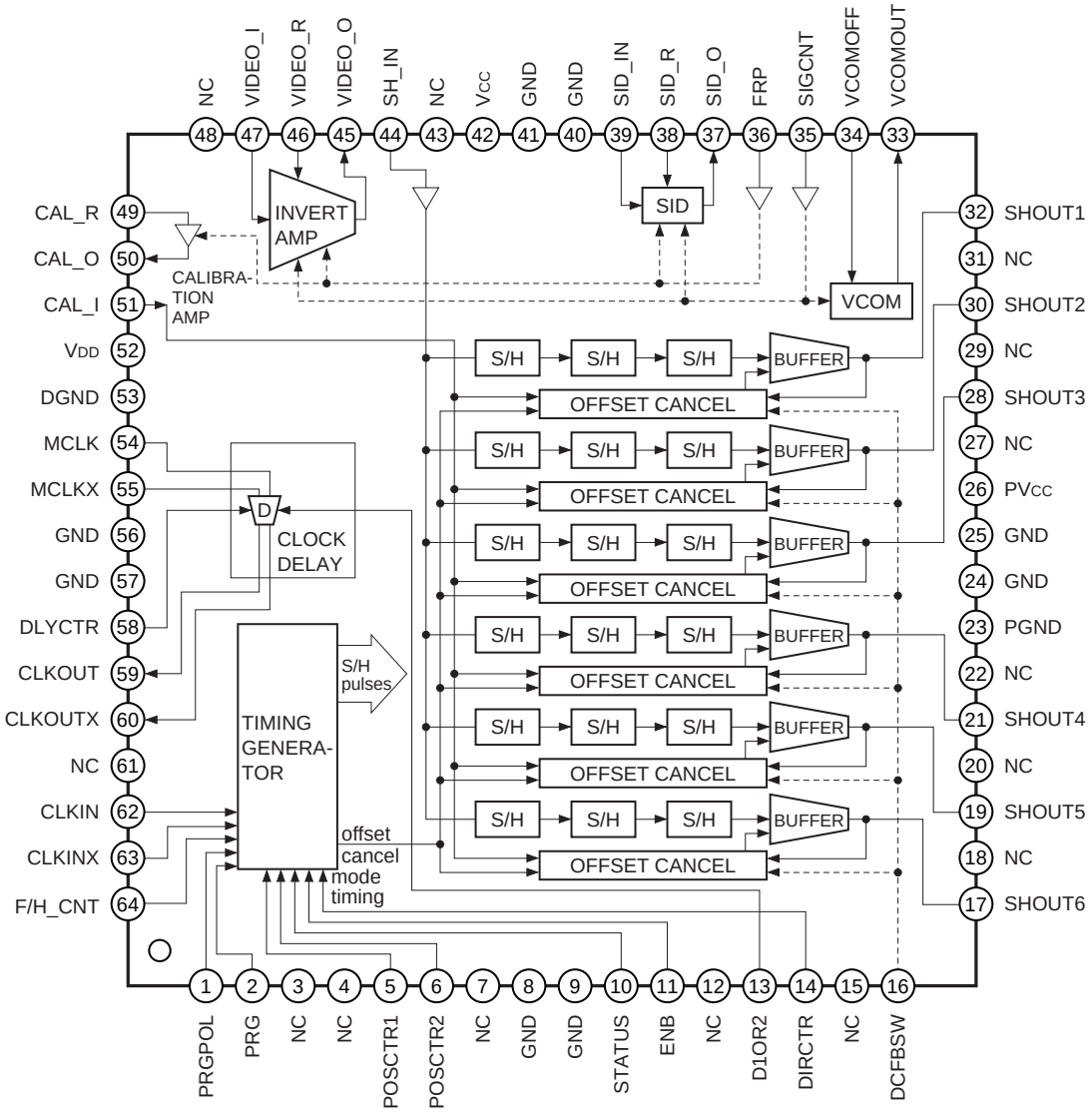
• Supply voltage	Vcc	16	V	
	V_{DD}	5.5	V	
• Operating temperature		–20 to +70	°C	
• Storage temperature		–65 to +150	°C	
• Allowable power dissipation	P_D	2300	mW	(single layered board mounted)

Recommended Operating Conditions

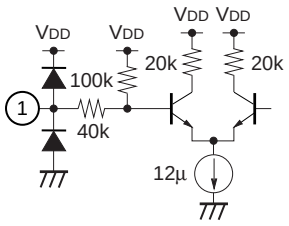
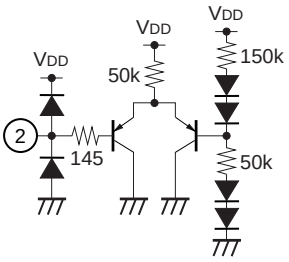
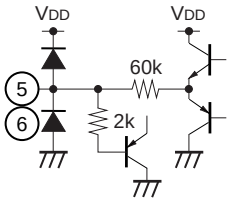
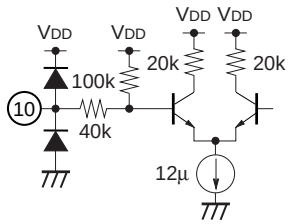
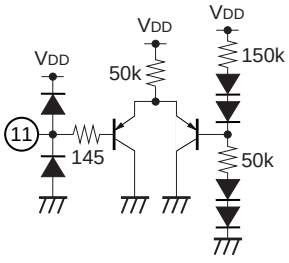
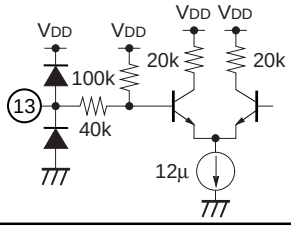
• Supply voltage	Vcc	15.0 to 15.5	V
	V_{DD}	4.75 to 5.25	V
• Ambient temperature		–20 to +70	°C

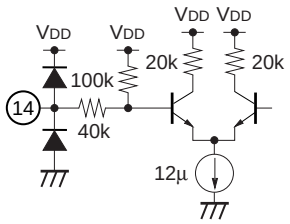
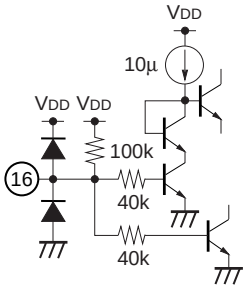
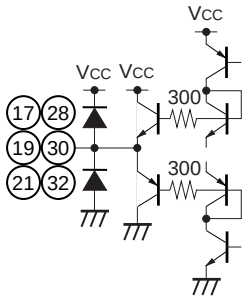
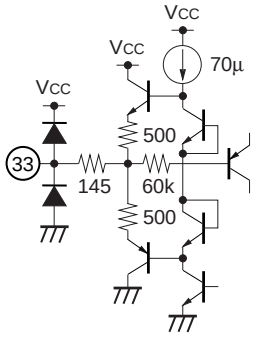
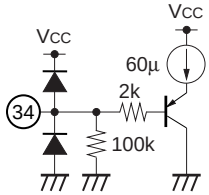
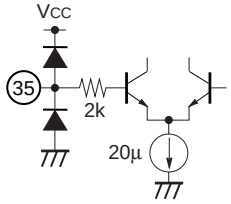
E99803A9Z-PS

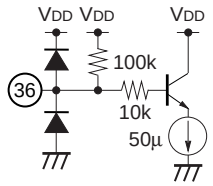
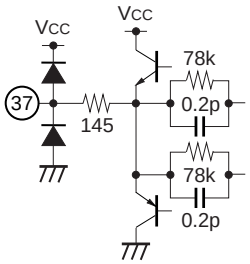
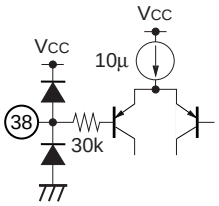
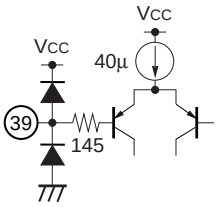
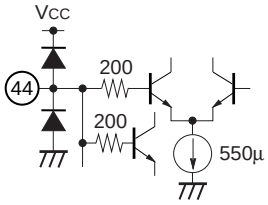
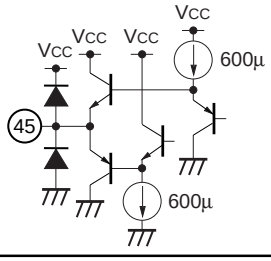
Block Diagram

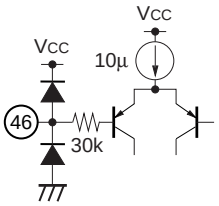
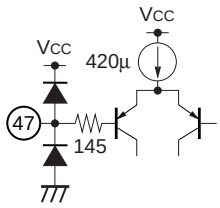
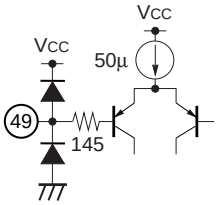
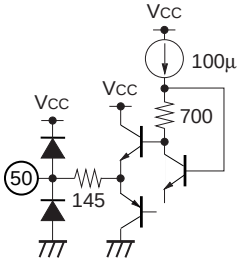
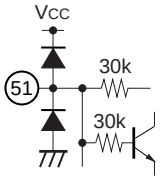
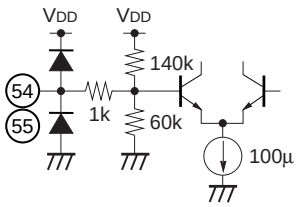


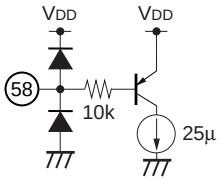
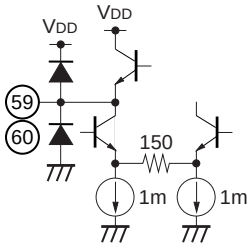
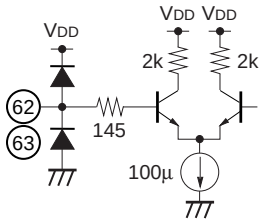
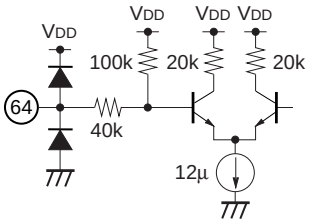
Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	PRGPOL	I	High: ≥ 2.5V Low: ≤ 0.8V OPEN High		Selects the latch polarity of the PRG pulse used as the time reference. High: PRG pulse is latched at the falling edge of CLKIN. Low: PRG pulse is latched at the rising edge of CLKIN. Select the polarity with sufficient timing margin after adjusting the analog video and CLKIN phases with DLYCTR.
2	PRG	I	High: ≥ 2.5V Low: ≤ 0.8V		PRG pulse input. See the Timing Chart.
5 6	POSCTR1 POSCTR2	I	See Table A-1.		Output phase adjustment. Each pin has 4 setting values, for a total of 16 settings. (Adjustment in 1 dot clock units in XGA mode, 1/2 dot clock units in SVGA mode, and 1 dot clock units in SXGA mode.) See Tables A-1, A-2 and A-3.
10	STATUS	I	High: ≥ 2.5V Low: ≤ 0.8V OPEN High		Used in XGA and UXGA modes (when using 2 ICs for a gamma-corrected IC). During forward scan, high: 2nd device, low: 1st device During reverse scan, high: 1st device, low: 2nd device See Table B.
11	ENB	I	High: ≥ 2.5V Low: ≤ 0.8V		ENB pulse input. See the Timing Chart.
13	D1OR2	I	High: ≥ 2.5V Low: ≤ 0.8V OPEN High		CLKOUT pin frequency selection. High: same frequency as MCLK Low: double the MCLK frequency

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
14	DIRCTR	I	High: ≥ 2.5V Low: ≤ 0.8V OPEN High		Scan direction setting. Low: output as a time series in descending order (reverse scan) of output pin symbol (in order from SHOUT6 to SHOUT1) High: output in ascending order (forward scan)
16	DCFBSW	I	OPEN High		Offset cancel circuit on/off switch. High: cancel circuit on Use this pin at on (open).
17 19 21 28 30 32	SHOUT6 SHOUT5 SHOUT4 SHOUT3 SHOUT2 SHOUT1	O	1.5 to 13.5V		Demultiplexer outputs. Can be connected directly to the LCD input pins.
33	VCOMOUT	O	3 to 7V		LCD common voltage of panel output. Can be set to V_{SIGCNT} to (V_{SIGCNT} – 3V) by the Pin 34 input.
34	VCOMOFF	I	0 to 10V		VCOMOUT (Pin 33) voltage setting. VCOMOUT is the same potential as SIGCNT for input of 0V, and approximately 3V lower than that for input of 10V.
35	SIGCNT	I	7V		Signal center voltage (inversion folded voltage) input. Normally, set to 7V.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
36	FRP	I	High: ≥ 2.5V Low: ≤ 0.8V		Invert pulse input. High: inverse Low: non-inverse See the Timing Chart.
37	SID_O	O	2 to 12V		SID block output. Provide an external buffer for precharge.
38	SID_R	I	3.3V		Precharge signal invert offset adjustment. When using the CXA2111R SID, connect to the V33 output of the CXA2111R.
39	SID_IN	I	2.3 to 3.3V		Precharge waveform input. Can be connected directly to the CXA2111R SID output. Connect to 5V when not using the SID block.
44	SH_IN	I	2 to 10V		Analog demultiplexer input. Connect to the VIDEO_O (Pin 45) output. Do not input 2V or less.
45	VIDEO_O	O	2 to 10V		Invert amplifier output. Connect directly to Pin 44. When using two CXA3512R in parallel in XGA or UXGA mode, use the invert amplifier of only one IC, and connect the output to Pin 44 of both ICs.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
46	VIDEO_R	I	3.3V		Input the 100% white level DC of the signal input to VIDEO_I. When using the CXA2111R, connect to the V33 output of the CXA2111R. When using bipolar DAC output for VIDEO_I, connect to the DAC supply voltage.
47	VIDEO_I	I	2 to 3.3V		Video input. Connect a gamma-corrected 1.5Vp-p analog video output. Can be connected directly to the CXA2111R video output. Connect to 5V when not using the invert amplifier.
49	CAL_R	I	2.7V		Calibration level input for offset cancel. Input the DC level during non-inverse with the most highly visible gradation. Normally, approximately 2.5 to 3V.
50	CAL_O	O	3 to 11V		Calibration amplifier output. Connect directly to Pin 51. When using two CXA3512R in parallel in XGA or UXGA mode, use the calibration amplifier of only one IC, and connect the output to Pin 51 of both ICs.
51	CAL_I	I	3 to 11V		Calibration level input for offset cancel. Connect to CAL_O.
54 55	MCLK MCLKX	I	PECL differential (amplitude 0.4V or more between V_{DD} and 2V) or TTL input		Dot clock inputs. PECL differential input or TTL input. For TTL input, input to MCLK and connect MCLKX to GND via a capacitor. Always input the dot clock or equivalent signal to these pins even when not using CLKOUT. (Otherwise, noise may result.)

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
58	DLYCTR	I	3 to 5V		Dot clock phase adjustment. The CLKOUT phase relative to MCLK can be changed by the voltage of this pin. Connection to the CXA2111R DLY_CNT output allows digital control using the I²C register of the CXA2111R.
59 60	CLKOUT CLKOUTX	O	V_{DD} – 0.3V to V_{DD}		Phase-adjusted dot clock outputs.
62 63	CLKIN CLKINX	I	V_{DD} – 0.3V to V_{DD}		Dot clock inputs for timing generation. Connect the CLKOUT (CLKOUTX) pin. When not using the CLK phase adjustment function, the dot clock can also be input directly to these pins by PECL differential input.
64	F/H_CNT	I	High: ≥ 2.5V Low: ≤ 0.8V OPEN High		SHOUT output timing selection. High: SHOUT 1 to 3 and SHOUT 4 to 6 are output at different timing. Low: SHOUT 1 to 6 are output at the same timing.
23	PGND		GND		Power GND.
26	PV_{CC}		15.5V		Power V_{CC}. Connect directly to V_{CC}.
42	V_{CC}		15.5V		15V power supply.
52	V_{DD}		5V		5V power supply.
53	DGND		GND		Digital GND.
8, 9, 24, 25, 40, 41, 56, 57	GND		GND		Analog GND.
3, 4, 7, 12, 15, 18, 20, 22, 27, 29, 31, 43, 48, 61	NC				No connection. Not connected to anything.

Electrical Characteristics (See Electrical Characteristics Measurement Circuit)

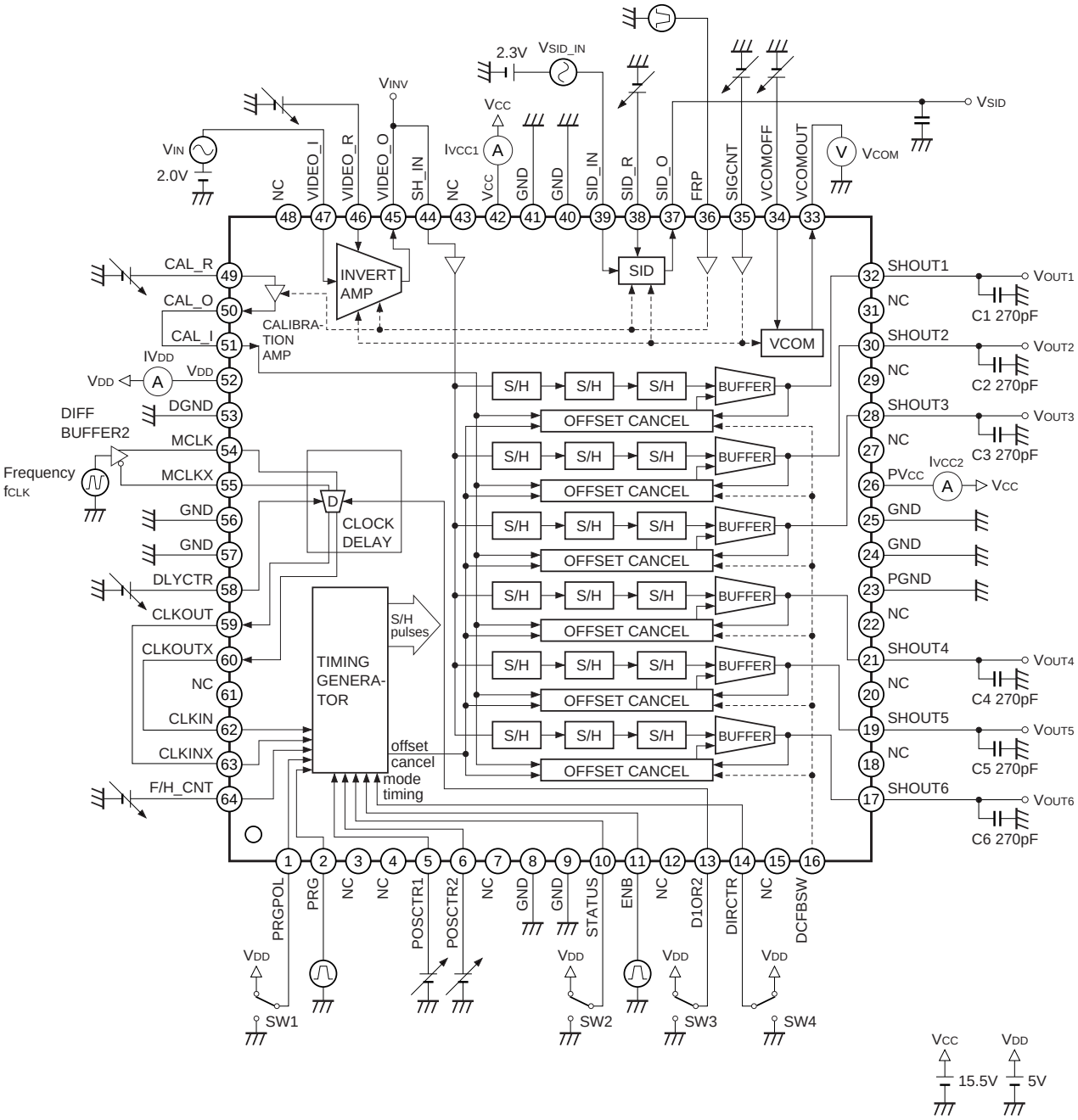
(V_{DD} = 5V, V_{CC} = 15.5V, V_{SIGCEN} = 7V, Ta = 25 ± 3°C)

No.	Item	Symbol	Measurement points	Measurement contents	Min.	Typ.	Max.	Unit
1	V_{DD} current consumption	I_{DD}	I_{VDD}	$I_{DD} = I_{VDD}$	20	28	42	mA
2	V_{CC} current consumption	I_{CC}	I_{VCC1} I_{VCC2}	$I_{CC} = I_{VCC1} + I_{VCC2}$	30	45	65	mA
3	Input – output gain	A_{SHOUT}	V_{SHOUT} V_{IN}	$A_{SHOUT} = V_{SHOUT}$ (AC)/V_{IN}	—	3	—	times
4	Invert amplifier gain	A_{INV}	V_{INV} V_{IN}	$A_{INV} = V_{INV}$ (AC)/V_{IN}	—	2	—	times
5	Invert amplifier slew rate	SR_{INV}	V_{INV}	Input a square wave from V_{IN} so that the V_{INV} output amplitude is 3.0Vp-p. Measure the slew rate at 10 to 90% of output waveform rise or fall. (for inverse or non-inverse)	—	700	—	V/µs
6	Invert amplifier output band width	BW_{INV}	V_{INV}	Input 2.5V DC, 100mVp-p AC from Pin 47 (VIDEO_IN) and measure V_{INV}. The frequency that is –3dB to 100kHz. (for inverse or non-inverse)	—	90	—	MHz
7	Output delay deviation for inverse/non-inverse	T_{DIFF}	V_{INV}	Invert amplifier delay time difference for inverse and non-inverse.	—	2	4	ns
8	SID output gain	A_{SID}	V_{SID} V_{SID_IN}	$A_{SID} = V_{SID}$ (AC)/V_{SID_IN}	—	4	4.4	times
9	SID block output slew rate	SR_{SID}	V_{SID}	Input an invert pulse to Pin 44 (FRP), load capacitance C7 = 47pF, and apply DC input voltage to V_{SID_IN} so that V_{SID} is 2.5V/11.5V. Measure the slew rate at 10 to 90% of output waveform rise or fall.	30	50	—	V/µs
10	VCOM adjustable range	V_{COM}	V_{COM}	VCOM output voltage when Pin 34 (VCOMOFF) is varied from 0 to 10V.	Vsig – 2	—	Vsig	V
11	First stage SH_OUT slew rate	SR_{SH1}	—	First stage sample-and-hold slew rate on Block Diagram.	—	700	—	V/µs
12	SH_OUT slew rate	SR_{OUT}	V_{OUT1} to V_{OUT6}	Input a square wave from V_{IN} so that the V_{OUT1} to V_{OUT6} output amplitude is 3.5Vp-p. Measure the slew rate at 10 to 90% of output waveform rise or fall. (load 270pF, for inverse or non-inverse)	—	150	—	V/µs

No.	Item	Symbol	Measurement points	Measurement contents	Min.	Typ.	Max.	Unit
13	MCLK input frequency range	f_{MCLK}		D1OR2 = High (CLKOUT = MCLK)	14	—	65	MHz
14	TG operating frequency range	f_{TG}	—	Maximum frequency at which the sample-and-hold timing pulse is output properly.	—	—	120	MHz
15	VIDEO_I input signal range	V_{INR}	—	VIDEO_I input voltage range when VIDEO_R is set to 3.3V.	1.5	—	3.7	V
16	VIDEO_I input signal amplitude range	V_{IN}	—	Maximum signal amplitude range of VIDEO_I input signal	—	—	1.5	V
17	SHOUT minimum output voltage	V_{MIN}	V_{OUT1} to V_{OUT6}	Minimum voltage at which sample-and-hold output (SHOUT 1 to SHOUT 6) can be output.	1.5	2	—	V
18	SHOUT maximum output voltage	V_{MAX}	V_{OUT1} to V_{OUT6}	Maximum voltage at which sample-and-hold output (SHOUT 1 to SHOUT 6) can be output.	—	13	13.5	V
19	Output deviation between channels 1	D_{OUT1}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value when CAL_R = 2.6V and VIDEO_I = 2.6V.	—	4	10	mVp-p
20	Output deviation between channels 2	D_{OUT2}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value when CAL_R = 2.6V and VIDEO_I = 3.3V or 1.9V.	—	4	40	mVp-p
21	Output deviation between ICs 1	D_{IC1}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value when CAL_R = 2.6V and VIDEO_I = 2.6V. (when using two CXA3512R)	—	10	20	mVp-p
22	Output deviation between ICs 2	D_{IC2}	V_{OUT1} to V_{OUT6}	Value obtained by subtracting minimum V_{OUT1} to V_{OUT6} value from maximum V_{OUT1} to V_{OUT6} value when CAL_R = 2.6V and VIDEO_I = 3.3V or 1.9V. (when using two CXA3512R)	—	10	60	mVp-p

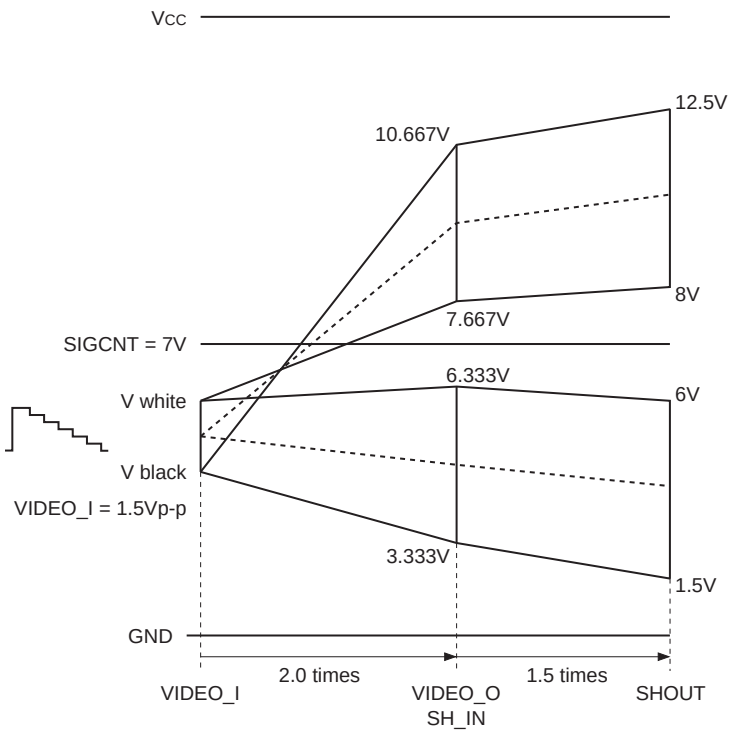
Unless otherwise specified, pin setting conditions are as follows.
(46) VIDEO_R = 3.3V, (47) VIDEO_I = 2.0V, (39) SID_IN = 2.3V, (38) SID_R = 3.3V, (35) SIGCNT = 7.0V,
(34) VCOMOFF = 0V, (1) PRGPOL = 0V, (5) POSCTR1 = 0V, (6) POSCTR2 = 0V, (10) STATUS = 0V,
(13) D1OR2 = 5V, (14) DIRCTR = 5V, (49) CAL_R = 2.6V, (58) DLYCTR = 4.0V, (64) F/H_CNT = 0V,
(36) FRP = 0V, f_{CLK}32.5MHz

Electrical Characteristics Measurement Circuit



Level Diagram

VIDEO_I to SHOUT
(SIGCNT = 7V, VIDEO_R = input 100% white level)



VIDEO_I to VIDEO_O

The formulas for calculating the VIDEO_I to SHOUT internal DC gain are as follows.

For non-inverse:

$$VIDEO\_O = 2.0 \times (VIDEO\_I - VIDEO\_R) + SIGCNT \times (1 - 1/10.5)$$

$$SHOUT = 3.0 \times (VIDEO\_I - VIDEO\_R) + SIGCNT \times (1 - 1/7)$$

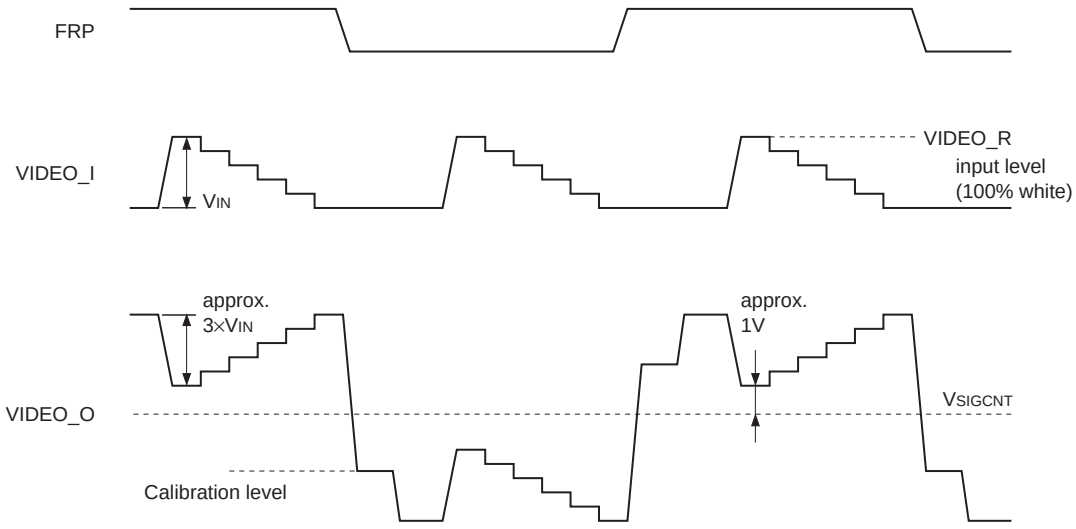
For inverse:

$$VIDEO\_O = -2.0 \times (VIDEO\_I - VIDEO\_R) + SIGCNT \times (1 + 1/10.5)$$

$$SHOUT = -3.0 \times (VIDEO\_I - VIDEO\_R) + SIGCNT \times (1 + 1/7)$$

Description of Operation

1. Invert Amplifier Block



The CXA3512R is designed so that the optimal signal for the LCD panel is output from the SHOUT pins when a signal in the range from 1.8 to 3.3V is applied to the VIDEO_I input. As shown in the figure above, when a γ corrected video signal is input to VIDEO_I, the signal is inverse/non-inverse amplified according to the FRP input (TTL level) and output from VIDEO_O. The DC level is determined by the VIDEO_R input. Input a level equivalent to 100% white of input. Also, when not using the invert amplifier, connect VIDEO_I to 5V.

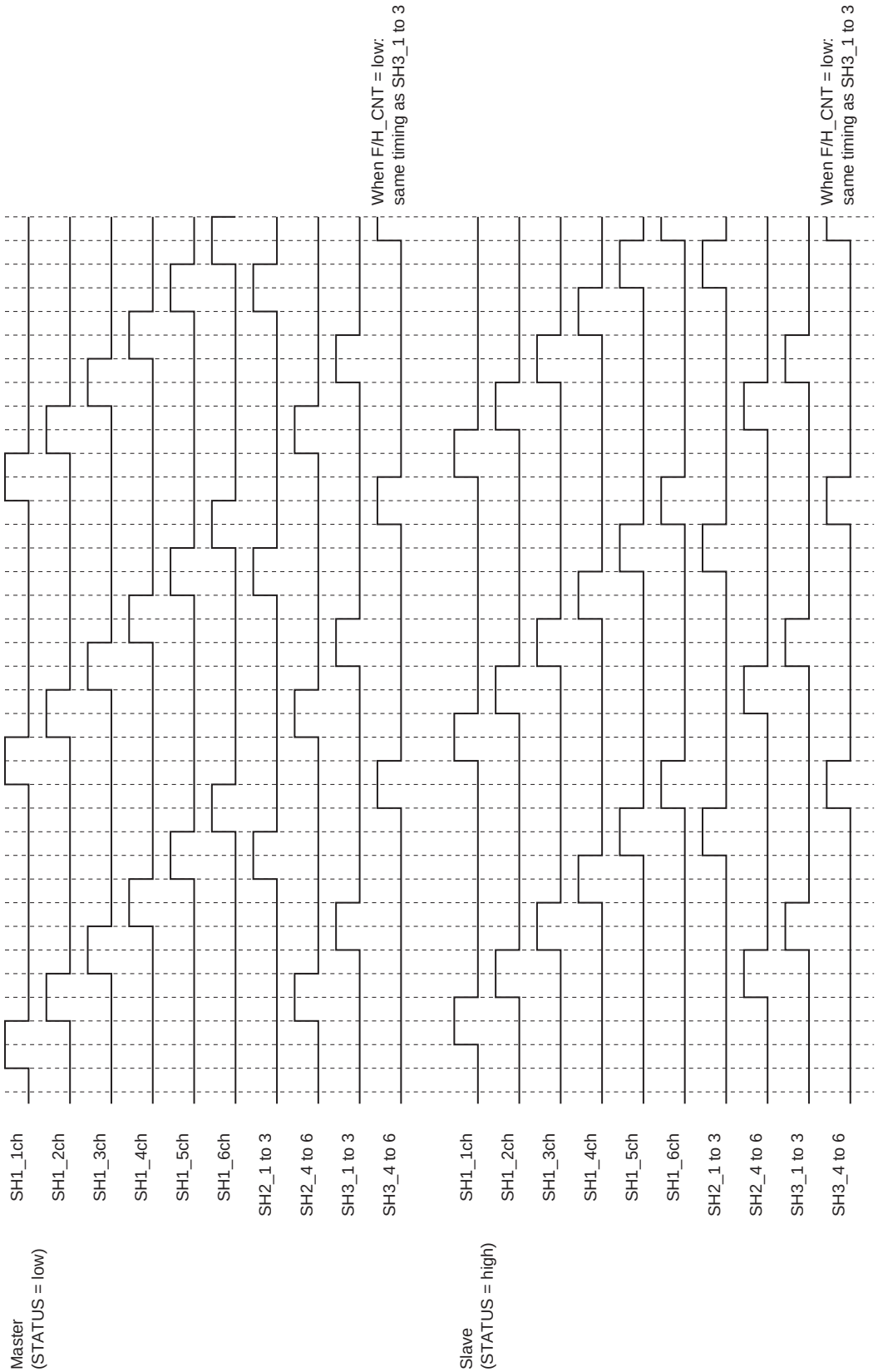
2. Analog Demultiplexer Block

The SH_IN analog input signal is converted from a time series signal to a 6-channel (or 12-channel) cyclic parallel signal by the sample-and-hold group which is appropriately controlled by the on-chip timing generator. These signals pass through a fixed-gain (= 1.5 times) buffer amplifier and are output to SHOUT. These outputs can directly drive the input load of the LCD panel.

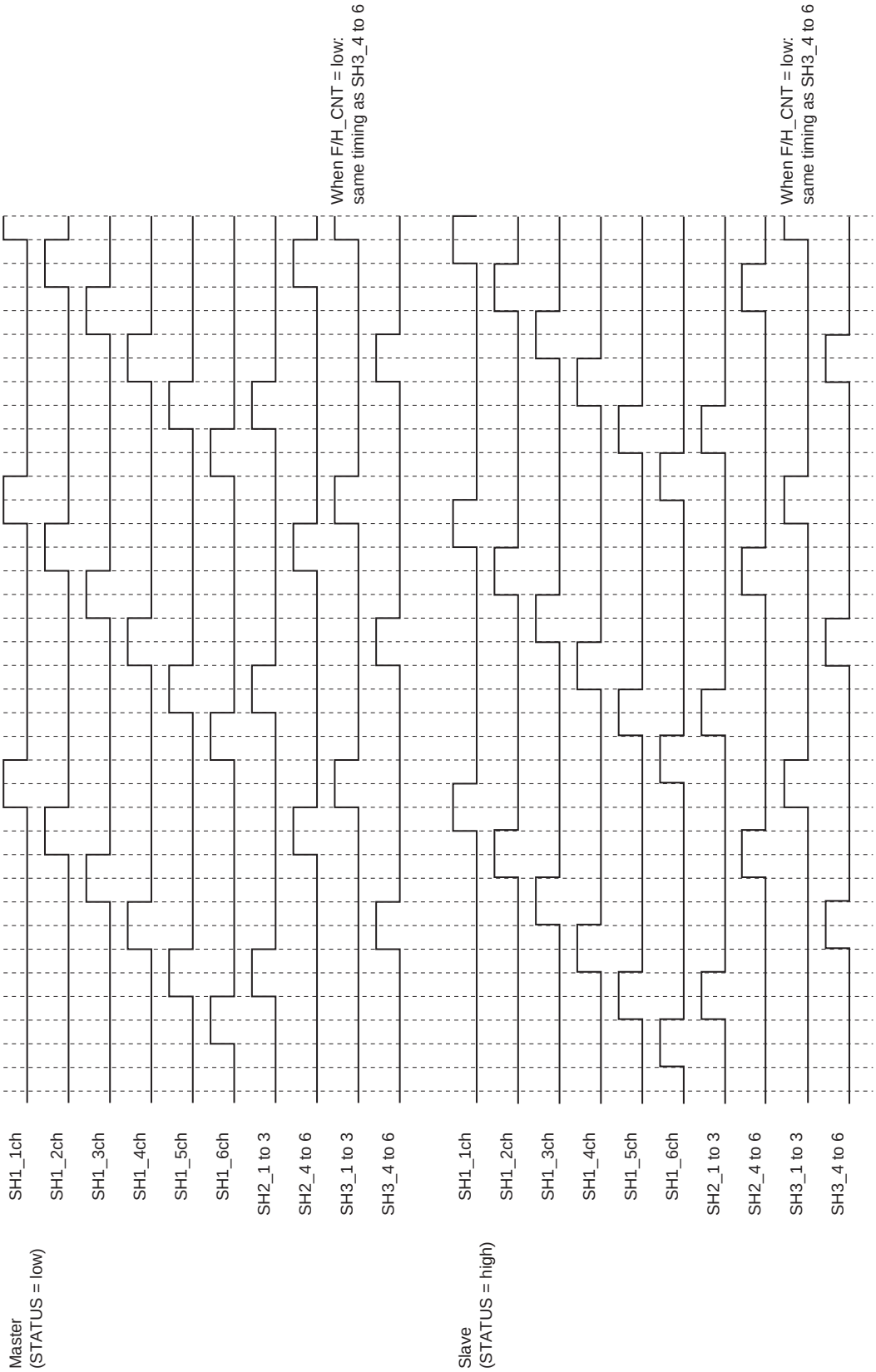
When using a SVGA panel, connect the (6-channel output) VIDEO_O output directly to the adjacent SH_IN. XGA panels use 12-channel output, so short the SH_IN of two CXA3512R and connect them to the VIDEO_O output of one of the IC. The on-chip TG recognizes master/slave by the low/high STATUS (Pin 10) input. For forward scan, the output alternates between the ICs in the order of master SHOUT1 → slave SHOUT1 → master SHOUT2 → slave SHOUT2 → master SHOUT3 and so on. Connect the wiring to the LCD panel inputs in this order.

The sample-and-hold pulse generation timing is shown on the following pages. These pulses are not output and are used only inside the IC.

Internal Sample-and-Hold Pulse Timing Chart 1
Forward scan (DIRCTR = high), F/H_CNT = high



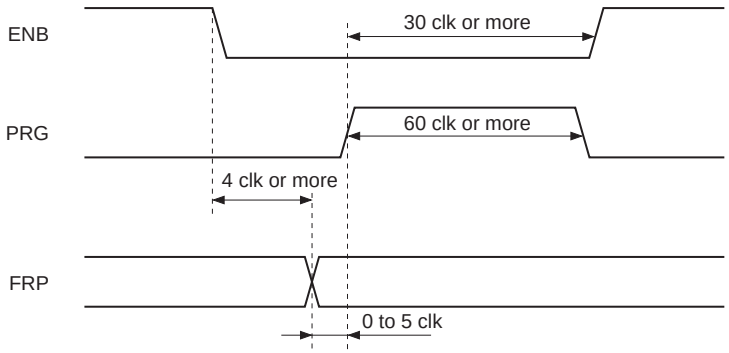
Internal Sample-and-Hold Pulse Timing Chart 2
Reverse scan (DIRCTR = low), F/H_CNT = high



3. Timing Generator (TG) Block

The on-chip TG operates by one pair of differential clock inputs (CLK_IN, CLK_INX) and two horizontal sync signal inputs (PRG, ENB), and generates the timing pulses needed by the demultiplexer block and the output deviation cancel circuit. The various operation modes can be designated by the pin voltage settings.

• Input timing signal conditions



Maintain the ENB, PRG and FRP phase relationship shown in the timing chart above, with the CLK_IN input sync as 1 clk. In particular, when FRP changes between high and low, be sure to input ENB and PRG as shown above. Otherwise, the IC may suffer irrecoverable deterioration in the worst case.

• Operation mode setting

Table B.

	SVGA (6-channel mode) SXGA (12-channel mode)	XGA/UXGA (12-channel/24-channel mode)	
		Master	Slave
STATUS	H/L*1	L	H
D1OR2	L	H	H

*1 The output phase can be shifted by 1/2-dot clock in SVGA/SXGA mode by changing STATUS.

• Scan direction setting

The output scan direction can be changed by the DIRCTR (Pin 14) input.

Pin 14	Direction	Scan order
H	Forward	SHOUT1 → SHOUT2 → SHOUT3 → SHOUT4 → SHOUT5 → SHOUT6 → SHOUT1 →
L	Reverse	SHOUT6 → SHOUT5 → SHOUT4 → SHOUT3 → SHOUT2 → SHOUT1 → SHOUT6 →

The scan direction can be changed by the Pin 14 setting without changing other connections even when using two CXA3512R such as in XGA mode.

• Output phase setting

The phase of each SHOUT output relative to the analog input can be adjusted in CLK_IN clock units by the Pins 5 and 6 input levels.

Each input pin has 4 setting values, for a total of 16 settings.

POSCTR1 is the lower bits setting, POSCTR2 is the upper bits setting, and the setting values are as shown in Table A-1.

Table A-1. Setting Voltage Range for Output Phase

Setting value	Threshold
0	to 0.75V
1	1.15 to 1.50V
2	1.70 to 2.55V
3	2.95V to

Table A-2. CMOS Logic Connection Setting Value and CMOS Output Pins

Setting value	a	b
0	L	L
1	Hi-Z	L
2	Hi-Z	H
3	H	H

There are two ways to use these pins.

A. Connect directly to the CXA2111R

Connect to the corresponding CXA2111R pins POS_CNT1 and POS_CNT2. This allows bit setting via the CXA2111R I^2C bus.

B. Connect to CMOS logic

Connect CMOS logic as shown in the figure. This allows digital control by tri-state control of Pin a. See Table A-2.

R1 is a threshold setting resistor that provides the voltage for setting values 1 and 2. The appropriate resistance value changes depending on the number of CXA3512R driven by one CMOS logic (1-channel or 3-channel RGB drive, or one CXA3512R (6-outputs/ch) or two CXA3512R (12-outputs/ch)).

Recommended resistance values are given in Table A-3.

CMOS Logic Connection

CXA3512R Usage and Threshold Setting Resistor R1

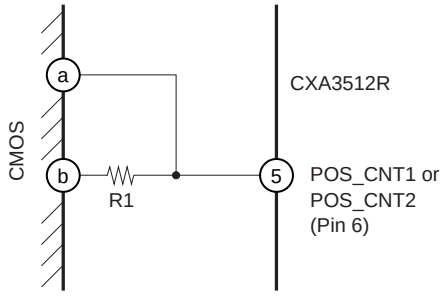


Table A-3.

	RGB 1-channel drive		RGB 3-channel drive	
	6 outputs	12 outputs	6 outputs	12 outputs
R1 value	250kΩ	150kΩ	100kΩ	47kΩ

CMOS supply voltage = 3.3 to 5V

4. Dot Clock Phase Adjustment Block

The CXA3512R has a function for adjusting the phase between the analog video input and the dot clock input to achieve stable reproduction of high definition images. Images with no jitter and flicker can be reproduced by optimizing the setting.

The 1/2-dot clock input to MCLK and MCLKX (PECL level) is input to the phase comparator of the on-chip PLL clock generator. The output from CLKOUT and CLKOUTX becomes the internal VCO output. CLKOUT is the same frequency as MCLK when the D10R2 (Pin 13) input is high, and twice the MCLK frequency when the D10R2 input is low.

A large amplitude logic with a threshold value of 1.5V can also be connected directly to MCLK instead of PECL. In this case, connect MCLKX to GND via a capacitor of approximately 100pF. (PECL level input is recommended when the MCLK input is used around 50MHz.)

The CLKOUT phase can be adjusted up to ±180° according to the DC level (3 to 5V) of the DLYCTR (Pin 58) input.

By connecting CLKOUT to the TG clock input, the analog video signal and first stage sample-and-hold phases can be finely adjusted using the DLYCTR DC level.

When using two CXA3512R in XGA mode, input the CLKOUT of one CXA3512R to the CLKIN of both in order to match the timing of both ICs. In this case, input the same clock to MLCK of both ICs.

5. Calibration Amplifier Block

The CXA3512R generates the deviation cancel circuit reference with a calibration amplifier in order to minimize the deviation between channels at the highest visibility level.

Input DC level equivalent to approximately 50% gray at VIDEO_I to CAL_R (Pin 49). In addition, directly connect the CAL_O (Pin 50) output to the adjacent CAL_I.

When using two CXA3512R in XGA mode, connect the CAL_O of one IC to the CAL_I of both ICs, and connect the unused CAL_R to 5V.

6. SID Block

This block generates the precharge signal used by the LCD panel.

The signal input to SID_IN (Pin 39) is folded at the SIGCNT potential by FRP in the same manner as the invert amplifier, and output to SID_O (Pin 37). The gain is designed at approximately 4 times. The DC level is determined by SID_R, and is normally approximately 3.3V.

SID_O cannot directly drive the precharge signal input of the LCD panel. Therefore, connect SID_O via a buffer having sufficient current supply capability.

SID_O DC calculation formula

Pin 36: low = non-inverse

$SID\_O = 4 \times (SID\_IN - SID\_R) + 6/7\ (SIGCNT)$

Pin 36: high = inverse

$SID\_O = 4 \times (SID\_R - SID\_IN) + 8/7\ (SIGCNT)$

7. VCOM Block

This block sets the DC potential of the VCOM level.

The VCOMOFF (Pin 34) potential sets the deviation relative to the SIGCNT potential as follows.

VCOMOFF = 0V: VCOMOUT = SIGCNT

VCOMOFF = 10V: VCOMOUT = SIGCNT – 3V

Combination with the CXA2111R

Used together with the CXA2111R, the CXA3512R can achieve most of the analog signal processing (γ correction, precharge waveform generation) required by LCD panels.
In addition, I^2C serial control of the following functions is possible using the I^2C-controlled registers built into the CXA2111R.

- Output phase adjustment (POSCTR1, 2)
- Clock phase adjustment (DLYCTR)
- Scan direction (DIRCTR)

Connect the pins as shown in the table below to use the various functions.
For details, see the CXA2111R specifications.

	CXA2111R	CXA3512R
Video signal	ROUT (18), GOUT (16) or BOUT (14)	VIDE_IN (47)
Precharge waveform	SIDOUT (6)	SID_IN (39)
Output phase	POS_CNT (1)	POSCTR1 (5)
	POS_CNT (2)	POSCTR2 (6)
Clock phase	DLK_CNT (3)	DLYCTR (58)
Scan direction	DIR_CNT (4)	DIRCTR (14)
Reference level	V33 (8)	VIDEO_R (46) SID_R (38)

Notes on Operation

1. Notes on Mounting

- The CXA3512R consumes power of approximately 1W. Be sure to take the following measures to prevent the IC temperature from rising.

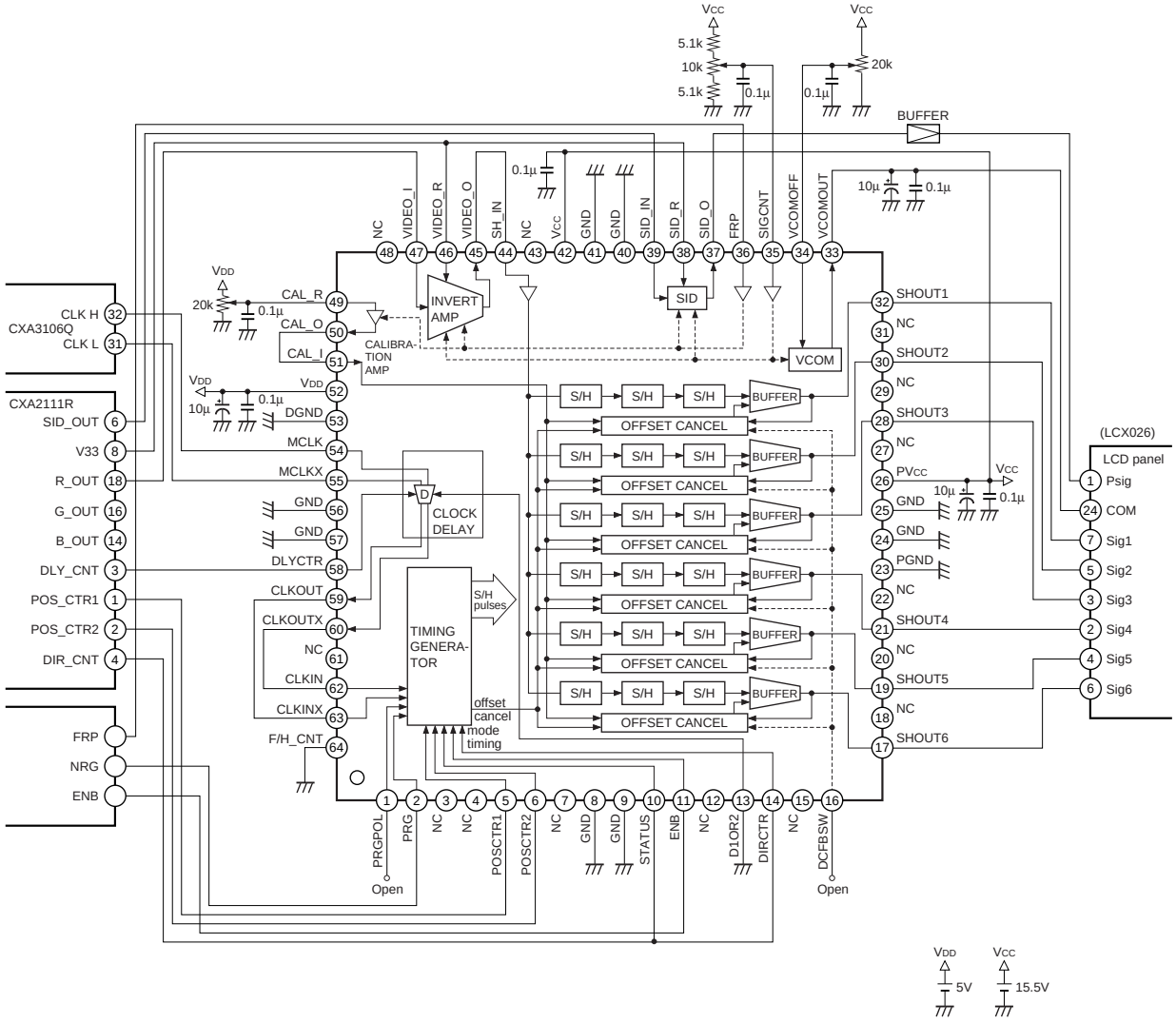
  A. Pins 8, 9, 24, 25, 40, 41, 56 and 57 (total 8 pins) are connected directly to the "die pad". Electrically and thermally connect these pins to the inner layer GND plane of a 4-layer substrate using multiple via.
  B. Do not mount in high density on a small substrate. Mounting to a 4-layer substrate with an inner layer copper foil thickness of 30µm or more is recommended.
  C. Do not locate the CXA3512R downwind of high thermal loads (lamp, etc.) in sets with fans.
  Do not locate the CXA3512R in portions with stagnant air flows in sets without fans.

- The wiring for the CXA3512R alone does not require special consideration, the skew with the PRG pulse rise timing may cause problems when using a high-speed dot clock. Particularly when using multiple CXA3512R, the timing of the PRG used as the time reference inside the IC must be matched at the IC input pins. Care should be taken when designing the board for the effects of propagation time and reflection, with the PRG line also considered an analog line like MCLK.
  If skew with the PRG pulse poses a problem after adjusting the phase relationship between the analog video input and CLK_IN, it may be possible to solve this problem by adjusting the PRGPOL (Pin 1) H/L setting for each IC.

2. Input Signals

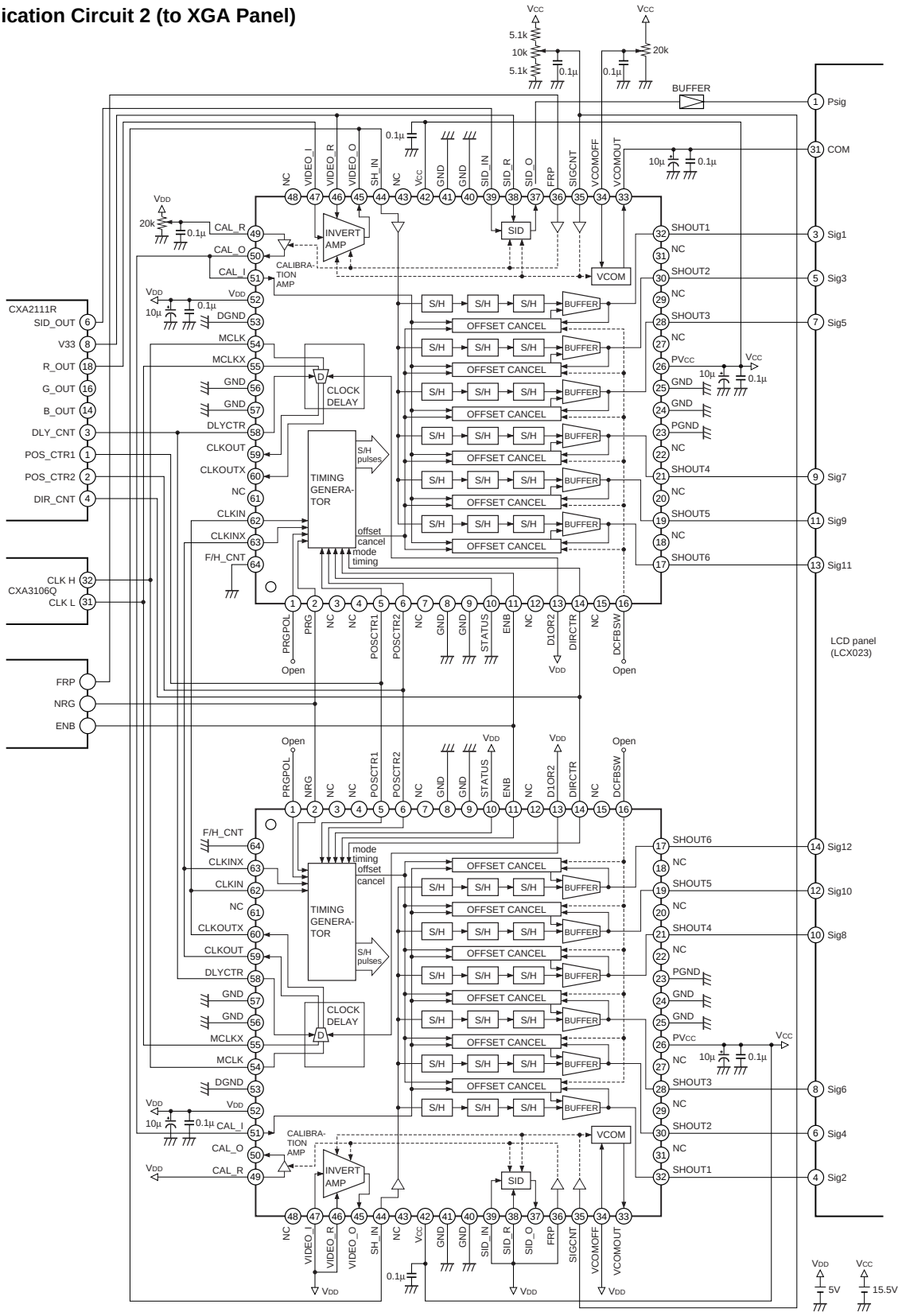
- Be sure to maintain the FRP, ENB and PRG timings noted in "Description of Operation 3. Timing Generator (TG) Block".
  Special care should be taken to avoid FRP transition without ENB and PRG.
- There is no particular problem when connecting the VIDEO_O output to SH_IN, but in this case do not input voltages of 2V or less, or (V_{DD} – 2V) or more.

Application Circuit 1 (to SVGA Panel)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

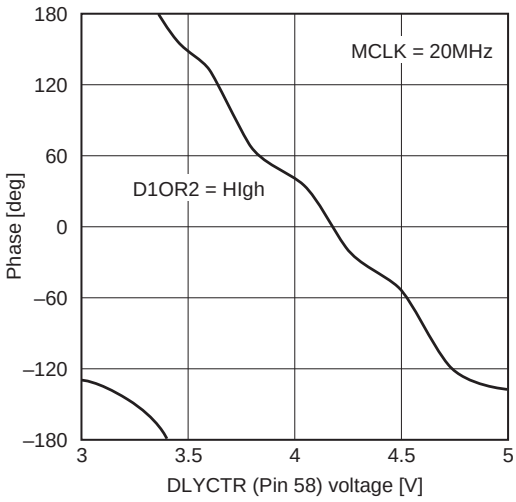
Application Circuit 2 (to XGA Panel)



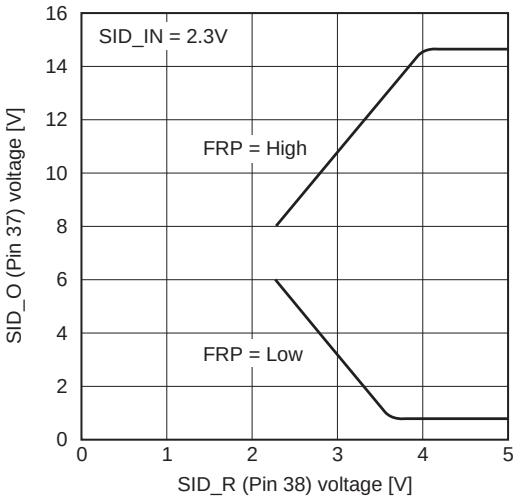
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{CC} = 15.5V, V_{DD} = 5.0V, SIGCNT = 7.0V, Ta = 25 ± 3°C)

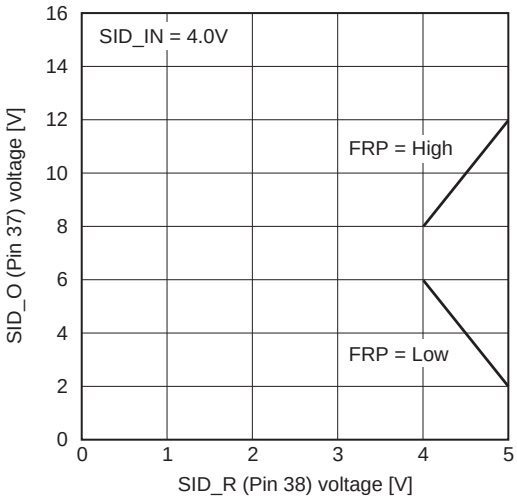
CLKOUT phase to MCLK vs. DLYCTR voltage



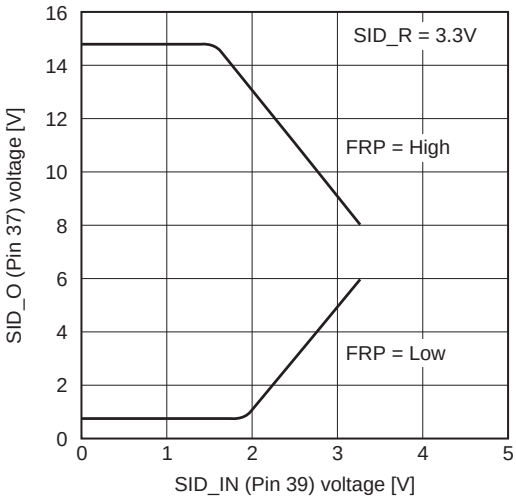
SID_O voltage vs. SID_R voltage (1)



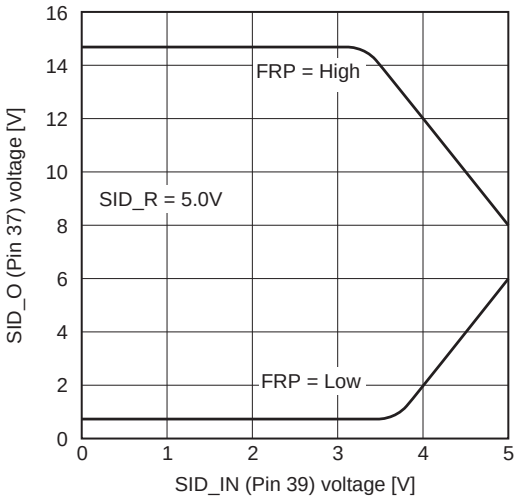
SID_O voltage vs. SID_R voltage (2)



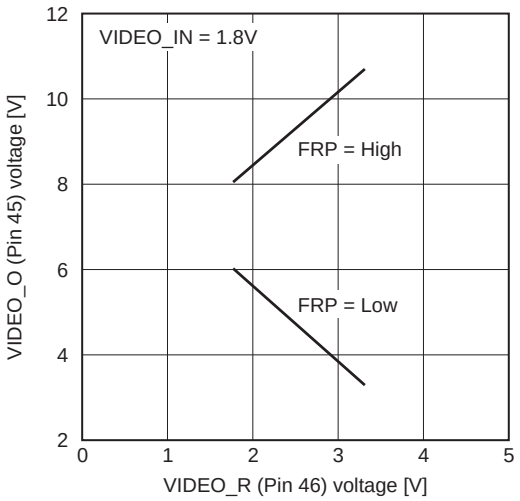
SID_O voltage vs. SID_IN voltage (1)



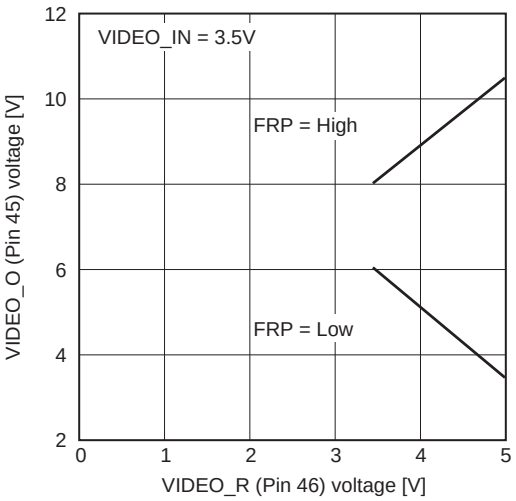
SID_O voltage vs. SID_IN voltage (2)



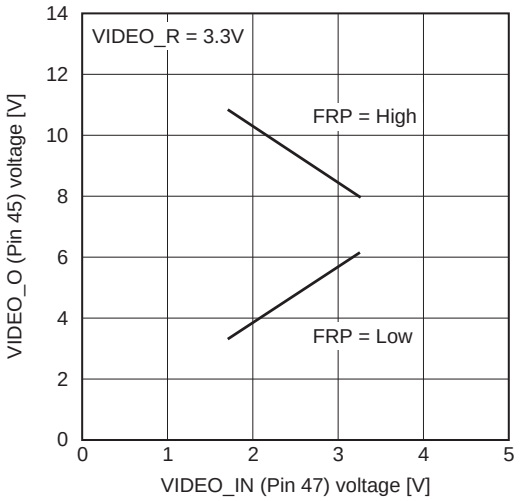
VIDEO_O voltage vs. VIDEO_R voltage (1)



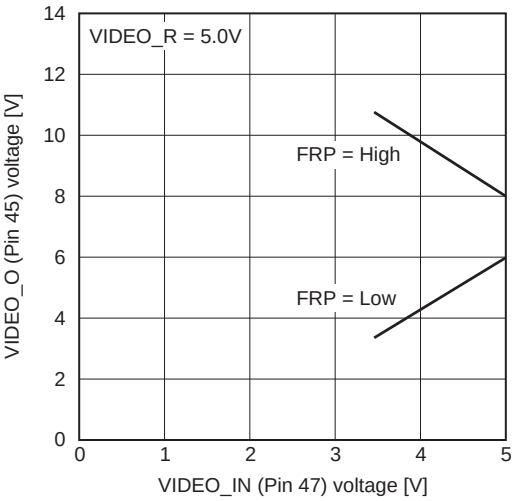
VIDEO_O voltage vs. VIDEO_R voltage (2)



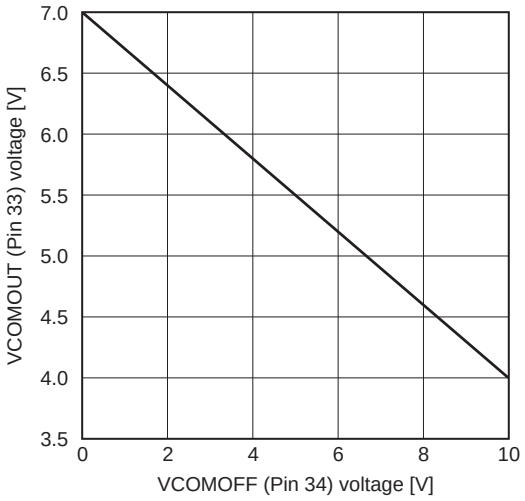
VIDEO_O voltage vs. VIDEO_IN voltage (1)



VIDEO_O voltage vs. VIDEO_IN voltage (2)

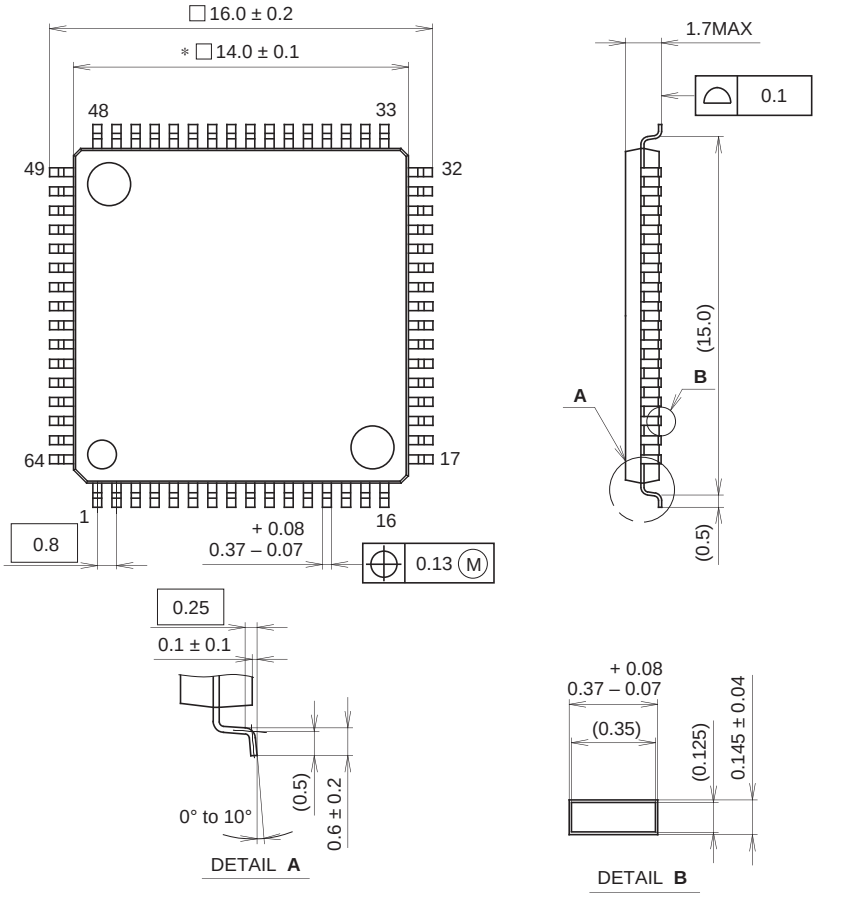


VCOMOUT voltage vs. VCOMOFF voltage



Package Outline Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L02
EIAJ CODE	LQFP064-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).