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8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

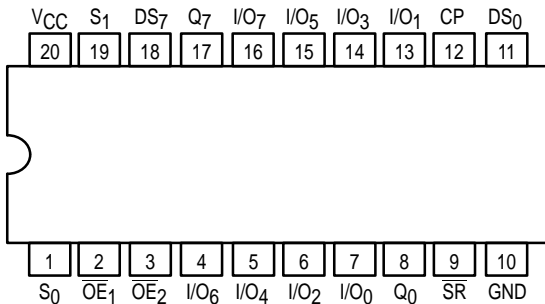
The MC74F323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the F299 with the exception of Synchronous Reset.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Four modes of operation are possible: hold (store), shift left, shift right and parallel load. All modes are activated on the LOW-to-HIGH transition of the clock.

- Common I/O For Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Parallel Load and Store
- Separate Continuous Inputs and Outputs from Q₀ and Q₇ Allow Easy Cascading
- Fully Synchronous Reset
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects

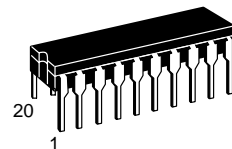
CONNECTION DIAGRAM



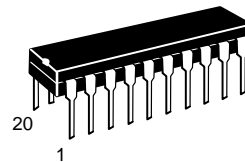
MC74F323

8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

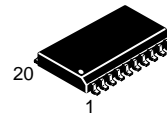
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0/-3.0	mA
I _{OL}	Output Current — Low	74			20/24	mA

MC74F323

FUNCTION TABLE

Inputs				Response
SR	S ₁	S ₀	CP	
L	X	X	↑	Synchronous Reset: Q ₀ –Q ₇ = LOW
H	H	H	↑	Parallel Load: I/O _n Q _n
H	L	H	↑	Shift Right: DS ₀ Q ₀ , Q ₀ Q ₁ , etc.
H	H	L	↑	Shift Left: DS ₇ Q ₇ , Q ₇ Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH clock transition.

FUNCTIONAL DESCRIPTION

The MC74F323 contains eight edge-triggered D-type flips-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{SR} overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other

state changes are initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE₁ or OE₂ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	Q ₀ /Q ₇	74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.5 V
			74	2.7			V _{CC} = 4.75 V
		I/O	74	2.7	3.4	V	I _{OH} = -3.0 mA, V _{CC} = 4.75 V
			74	2.4			V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	Q ₀ /Q ₇			V	I _{OL} = 20 mA, V _{CC} = MIN	
		I/O				I _{OL} = 24 mA	
I _{IH}	Input HIGH Current	Q ₀ /Q ₇			μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		I/O					20
		Q ₀ /Q ₇			mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		I/O					0.1
I _{IL}	Input LOW Current	S ₀ , S ₁			mA	V _{CC} = MAX, V _{IN} = 0.5 V	
		Other Inputs					-1.2
I _{OZH}	Off-State Output Current, High-Level Voltage Applied				μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
							70
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied				mA	V _{CC} = MAX, V _{OUT} = 0.5 V	
							-0.6
I _{OS}	Output Short Circuit Current (Note 2)				mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Total Supply Current						95

NOTES:

- For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F323

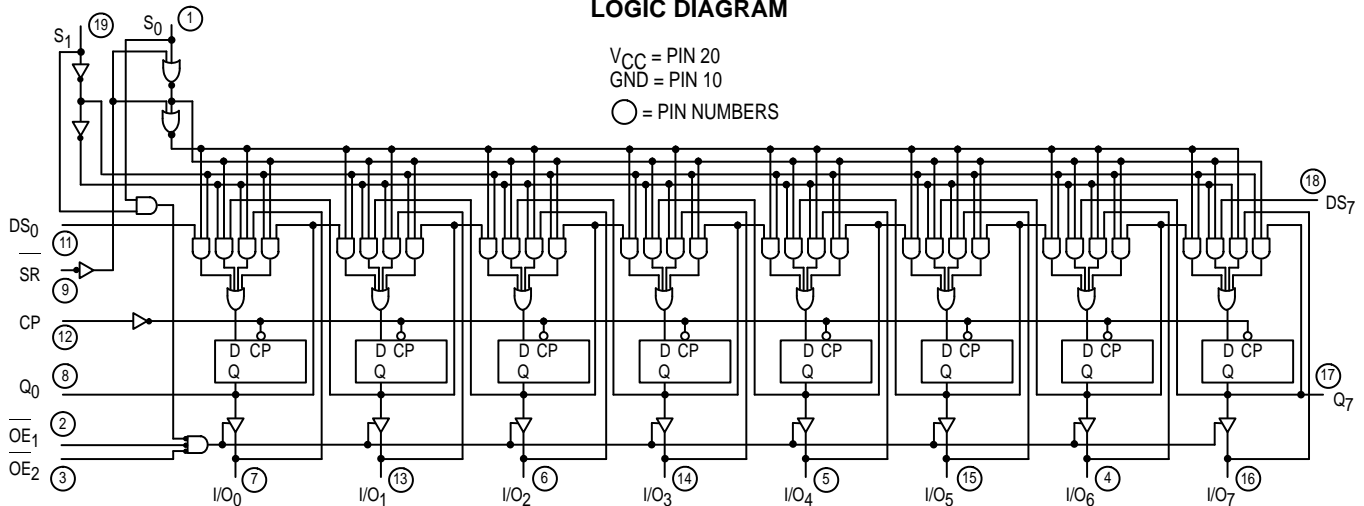
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{MAX}	Maximum Input Frequency	70		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.5	9.0	3.5	10	ns
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	3.5	9.0	3.5	10	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	3.5	8.0	3.5	9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time to HIGH or LOW Level	2.0	6.0	2.0	7.0	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Set-Up Time, HIGH or LOW S ₀ or S ₁ to CP	8.5			8.5		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	0.0			0.0		ns
t _s (H) t _s (L)	Set-Up Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0			5.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	2.0			2.0		ns
t _s (H) t _s (L)	Set-Up Time, HIGH or LOW SR to CP	10			10		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW SR to CP	0.0			0.0		ns
t _w (H) t _w (L)	CP Pulse Width, HIGH or LOW	7.0			7.0		ns

LOGIC DIAGRAM



FAST AND LS TTL DATA