# Advance Information

# 128K x 8 Bit Fast Static Random Access Memory

The MCM6926A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes. \_\_

Output enable (G) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

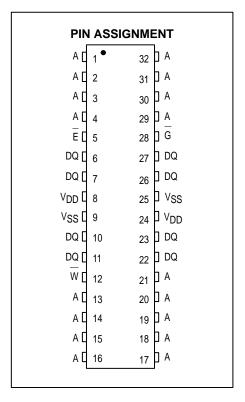
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small—outline J—leaded package.

- Single 3.3 V Power Supply
- Fully Static No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- · Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

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# **MCM6926A**





PIN NAMES							
A         Address Input           E         Chip Enable           W         Write Enable           G         Output Enable           DQ         Data Input/Output           VDD         + 3.3 V Power Supply           VSS         Ground							

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 1 2/25/97



#### TRUTH TABLE (X = Don't Care)

Е	G	w	Mode	V <sub>DD</sub> Current	Output	Cycle
Н	Х	Х	Not Selected	I <sub>SB1</sub> , I <sub>SB2</sub>	High–Z	_
L	Н	Н	Output Disabled	IDDA	High-Z	_
L	L	Н	Read	IDDA	D <sub>out</sub>	Read Cycle
L	Х	L	Write	I <sub>DDA</sub>	High–Z	Write Cycle

# ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{DD}$	- 0.5 to + 4.6	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{DD}$	V <sub>in</sub> , V <sub>out</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
Output Current	l <sub>out</sub>	± 30	mA
Power Dissipation	PD	0.6	W
Temperature Under Bias	T <sub>bias</sub>	– 10 to + 85	°C
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Storage Temperature — Plastic	T <sub>stg</sub>	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

 $(V_{DD} = 3.3 \text{ V} + 10\%, -5\%, T_A = 0 \text{ to } 70^{\circ}\text{C}, \text{ Unless Otherwise Noted})$ 

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>DD</sub>	3.135	3.3	3.6	V
Input High Voltage	VIH	2.2	_	V <sub>DD</sub> + 0.3**	V
Input Low Voltage	VIL	<b>-</b> 0.5*	_	0.8	V

## DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>DD</sub> )	I <sub>lkg(I)</sub>		± 1.0	μΑ
Output Leakage Current (E = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>DD</sub> )	I <sub>lkg(O)</sub>	_	± 1.0	μΑ
Output Low Voltage (I <sub>OL</sub> = + 8.0 mA)	VOL	_	0.4	V
Output High Voltage (I <sub>OH</sub> = - 4.0 mA)	Voн	2.4	_	V

<sup>\*</sup> $V_{IL}$  (min) = -0.5 V dc;  $V_{IL}$  (min) = -2.0 V ac (pulse width  $\leq 2.0$  ns) for I  $\leq 20.0$  mA. \*\* $V_{IH}$  (max) =  $V_{DD}$  + 0.3 V dc;  $V_{IH}$  (max) =  $V_{DD}$  + 2 V ac (pulse width  $\leq 2.0$  ns) for I  $\leq 20.0$  mA.

# POWER SUPPLY CURRENTS (See Note 1)

		6926	6A-8	6926	A-10	6926	A-12	6926	A-15		
Parameter	Symbol	Тур	Max	Тур	Max	Тур	Max	Тур	Max	Unit	Notes
AC Active Supply Current (I <sub>out</sub> = 0 mA) (V <sub>DD</sub> = max, f = f <sub>max</sub> )	I <sub>DDA</sub>		150	ı	130	ı	120		110	mA	2, 3, 4
Act <u>iv</u> e Quiescent Current (E = V <sub>IL</sub> , V <sub>DD</sub> = max, f = 0 MHz)	I <sub>DD2</sub>	_	80		80		80		80	mA	
AC_Standby Current (E = V <sub>IH</sub> , V <sub>DD</sub> = max, f = f <sub>max</sub> )	ISB1	_	50		45	_	40		35	mA	2, 3, 4
CMOS Standby Current	I <sub>SB2</sub>	_	20		20	ı	20		20	mA	

## NOTES:

- 1. Typical current =  $25^{\circ}$ C @ 3.3 V.
- 2. Reference AC Operating Conditions and Characteristics for input and timing (V<sub>IH</sub>/V<sub>IL</sub>, t<sub>r</sub>/t<sub>f</sub>, pulse level 0 to 3.0 V, V<sub>IH</sub> = 3.0 V).
  3. All address transition simultaneously low (LSB) and then high (MSB).
- 4. Data states are all zero.

# $\textbf{CAPACITANCE} \text{ (f = 1.0 MHz, dV = 3.0 V, T}_{A} = 25^{\circ}\text{C}, \text{ Periodically Sampled Rather Than 100\% Tested)}$

Parameter	Symbol	Тур	Max	Unit
Address Input Capacitance	C <sub>in</sub>	_	6	pF
Control Pin Input Capacitance	C <sub>in</sub>	_	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	_	8	pF

MOTOROLA FAST SRAM MCM6926A

#### **AC OPERATING CONDITIONS AND CHARACTERISTICS**

 $(V_{DD} = 3.3 \text{ V} + 10\%, -5\%, T_{A} = 0 \text{ to } +70^{\circ}\text{C}, \text{ Unless Otherwise Noted})$ 

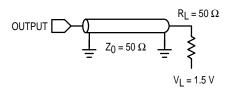
Input Timing Measurement Reference Level 1.5 V	Output Timing Measurement Reference Level 1.5 V
Input Pulse Levels 0 to 3.0 V	Output Load See Figure 1
Input Rise/Fall Time	

#### READ CYCLE TIMING (See Notes 1 and 2)

		6926	6A-8	6926	A-10	6926	A-12	6926	A-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Time	<sup>t</sup> AVAV	8	_	10	_	12	_	15	_	ns	3
Address Access Time	<sup>t</sup> AVQV	_	8	_	10	_	12	_	15	ns	
Enable Access Time	<sup>t</sup> ELQV	_	8	_	10	_	12	_	15	ns	
Output Enable Access Time	<sup>t</sup> GLQV	_	4	_	5	_	6	_	7	ns	
Output Hold from Address Change	<sup>t</sup> AXQX	3	_	3	_	3	_	3	_	ns	
Enable Low to Output Active	t <sub>ELQX</sub>	3	_	3	_	3	_	3	_	ns	4, 5, 6
Output Enable Low to Output Active	<sup>t</sup> GLQX	0	_	0	_	0	_	0	_	ns	4, 5, 6
Enable High to Output High–Z	<sup>t</sup> EHQZ	_	4	_	5	_	6	_	7	ns	4, 5, 6
Output Enable High to Output High–Z	<sup>t</sup> GHQZ	_	4	_	5	_	6	_	7	ns	4, 5, 6

#### NOTES:

- 1. W is high for read cycle.
- 2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
- 3. All read cycle timings are referenced from the last valid address to the first transitioning address.
- 4. At any given voltage and temperature, t<sub>EHQZ</sub> max < t<sub>ELQX</sub> min, and t<sub>GHQZ</sub> max < t<sub>GLQX</sub> min, both for a given device and from device to device.
- 5. Transition is measured 200 mV from steady-state voltage.
- 6. This parameter is sampled and not 100% tested.
- 7. Device is continuously selected (E =  $V_{IL}$ ,  $\underline{G}$  =  $V_{IL}$ ).
- 8. Addresses valid prior to or coincident with E going low.

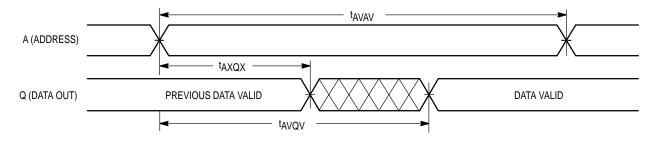


# **TIMING LIMITS**

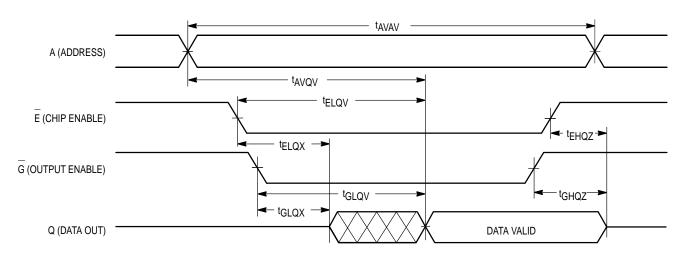
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

# READ CYCLE 1 (See Note 7)



# READ CYCLE 2 (See Note 8)



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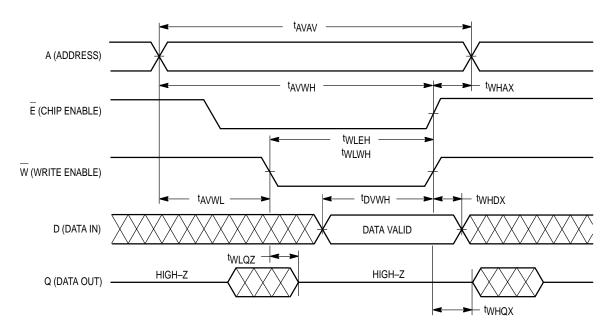
WRITE CYCLE 1 (W Controlled, See Notes 1 and 2)

		6926A-8 6926A-10		6926	6926A-12 6926A-		A-15				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	t <sub>AVAV</sub>	8	_	10	_	12	_	15	_	ns	3
Address Setup Time	tAVWL	0	_	0	_	0	_	0	_	ns	
Address Valid to End of Write	<sup>t</sup> AVWH	8	_	9	_	10	_	12	_	ns	
Address Valid to End of Write, G High	<sup>t</sup> AVWH	7	_	8	_	9	_	10	_	ns	
Write Pulse Width	tWLWH, tWLEH	8	_	9	_	10	_	12	_	ns	
Write Pulse Width, G High	tWLWH, tWLEH	7	_	8	_	9	_	10	_	ns	
Data Valid to End of Write	<sup>t</sup> DVWH	4	_	5	_	6	_	7	_	ns	
Data Hold Time	tWHDX	0	_	0	_	0	_	0	_	ns	
Write Low to Data High–Z	tWLQZ	_	4	_	5	_	6	_	7	ns	4,5,6
Write High to Output Active	tWHQX	3	_	3	_	3	_	3	_	ns	4,5,6
Write Recovery Time	<sup>t</sup> WHAX	0	_	0	_	0	_	0	_	ns	

# NOTES:

- 1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- 2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
- 3. All write cycle timings are referenced from the last valid address to the first transitioning address.
- 4. Transition is measured 200 mV from steady-state voltage.
- 5. This parameter is sampled and not 100% tested.
- 6. At any given voltage and temperature, tWLQZ max < tWHQX min both for a given device and from device to device.

# **WRITE CYCLE 1**



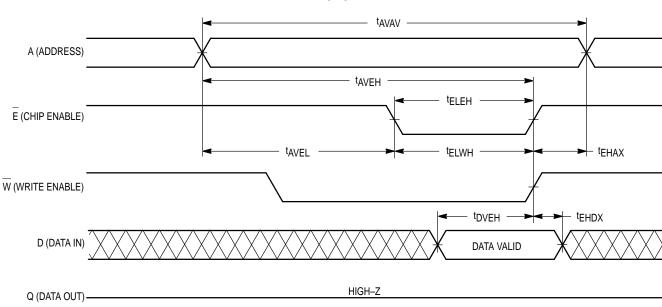
# WRITE CYCLE 2 (E Controlled, See Notes 1 and 2)

		6926	6A-8	6926	A-10	6926	A-12	6926	A-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	tAVAV	8	_	10	_	12	_	15	_	ns	3
Address Setup Time	<sup>t</sup> AVEL	0	_	0	_	0	_	0		ns	
Address Valid to End of Write	<sup>t</sup> AVEH	7	_	8	_	9	_	10	-	ns	
Enable to End of Write	<sup>t</sup> ELEH <sup>,</sup> <sup>t</sup> ELWH	7	_	8	_	9	_	10		ns	4,5
Data Valid to End of Write	<sup>t</sup> DVEH	4	_	5	_	6	_	7		ns	
Data Hold Time	<sup>t</sup> EHDX	0	_	0	_	0	_	0	_	ns	
Write Recovery Time	<sup>t</sup> EHAX	0	_	0	_	0	_	0		ns	

#### NOTES:

- 1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.
- 2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
- 3. All write cycle timings are referenced from the last valid address to the first transitioning address.
- 4. If <u>E</u> goes low coincident with or after W goes low, the output will remain in a high impedance condition.
- 5. If E goes high coincident with or before W goes high, the output will remain in a high impedance condition.

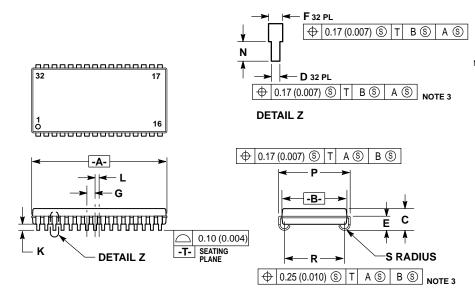
## **WRITE CYCLE 2**



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#### PACKAGE DIMENSIONS

32-LEAD 400 MIL SOJ CASE 857A-02

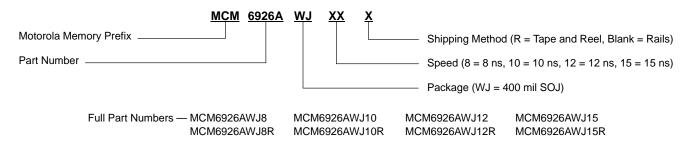


#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
  TO BE DETERMINED AT PLANE -T-
- DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INC	HES	MILLIN	IETERS			
DIM	MIN	MAX	MIN	MAX			
Α	0.820	0.830	20.83	21.08			
В	0.395	0.405	10.03	10.29			
С	0.128	0.148	3.26	3.75			
D	0.016	0.020	0.41	0.50			
E	0.088	0.098	2.24	2.48			
F	0.026	0.032	0.67	0.81			
G	0.050	BSC	1.27 BSC				
K	0.035	0.045	0.89	1.14			
L	0.025	BSC	0.64	BSC			
N	0.030	0.045	0.76	1.14			
Р	0.435	0.445	11.05	11.30			
R	0.365	0.375	9.27	9.52			
S	0.030	0.040	0.77	1.01			

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