

Am9519A

Universal Interrupt Controller

FINAL

DISTINCTIVE CHARACTERISTICS

- Eight individually maskable interrupt inputs reduce CPU overhead
- Unlimited interrupt channel expansion with no extra hardware
- Programmable 1-byte to 4-byte response provides vector address and message protocol for 8-bit CPUs
- Rotating and fixed priority resolution logic
- Software interrupt request capability
- Common vector and polled mode options
- Automatic hardware clear of in-service interrupts reduces software overhead
- Polarity control of interrupt inputs and outputs
- Reset minimizes software initialization by automatically generating CALL to location zero
- SMD/DESC qualified

GENERAL DESCRIPTION

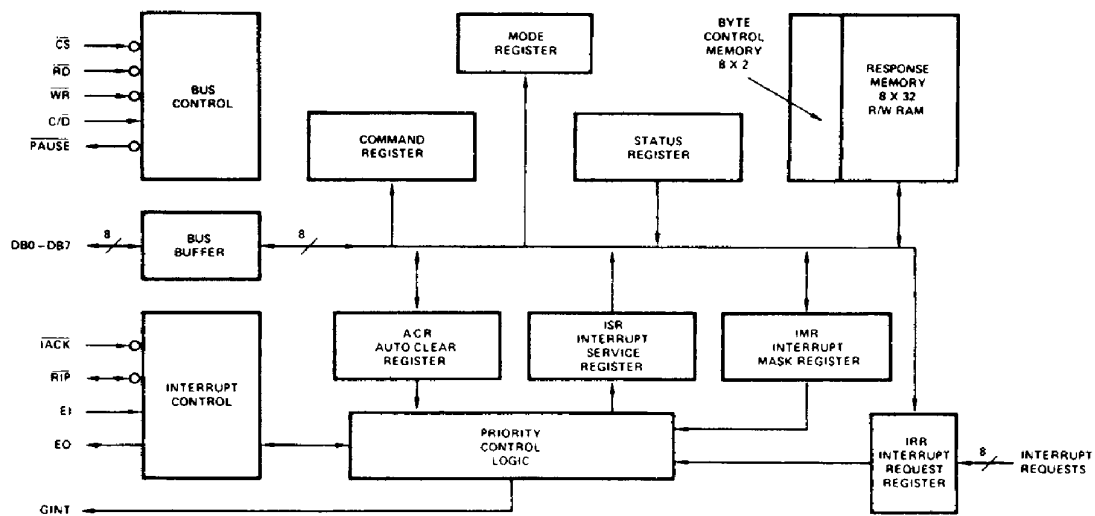
The Am9519A Universal Interrupt Controller is a processor support circuit that provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer-based systems. A single Am9519A manages up to eight maskable interrupt request inputs, resolves priorities and supplies up to four bytes of fully programmable response for each interrupt. It uses a simple expansion structure that allows many units to be cascaded for control of large numbers of interrupts. Several programmable control features are provided to enhance system flexibility and optimization.

The Universal Interrupt Controller is designed with a general purpose interface to facilitate its use with a wide

range of digital systems, including most popular 8-bit microprocessors. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the host processor may be used.

When the Am9519A controller receives an unmasked interrupt request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks and aids system diagnostic and maintenance procedures.

BLOCK DIAGRAM



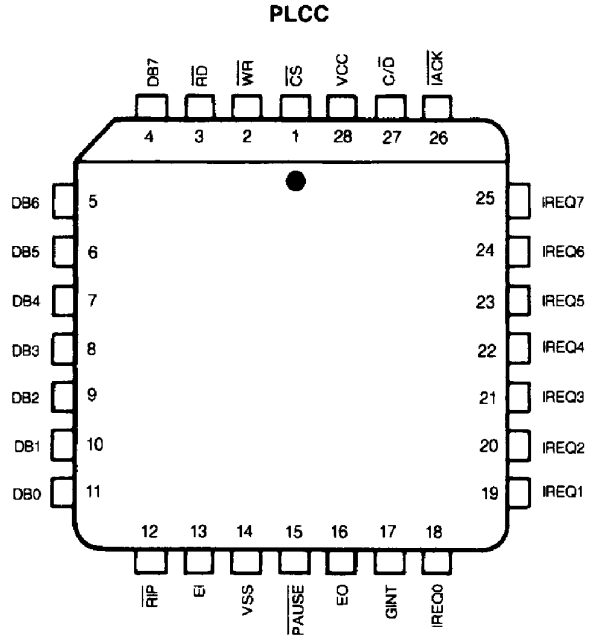
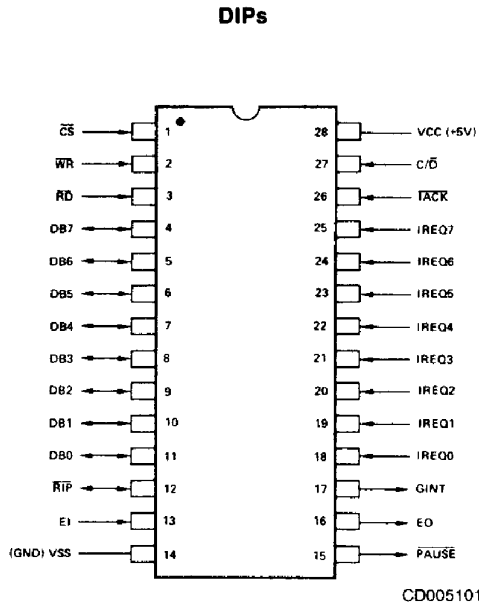
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Am9519A

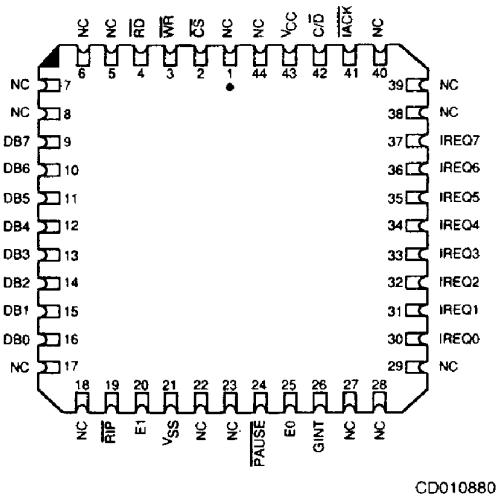
Publication #	Rev.	Amendment
00147	D	/0
Issue Date: May 1989		

CONNECTION DIAGRAMS Top View



Note: Pin 1 is marked for orientation.

LCC (Military only)



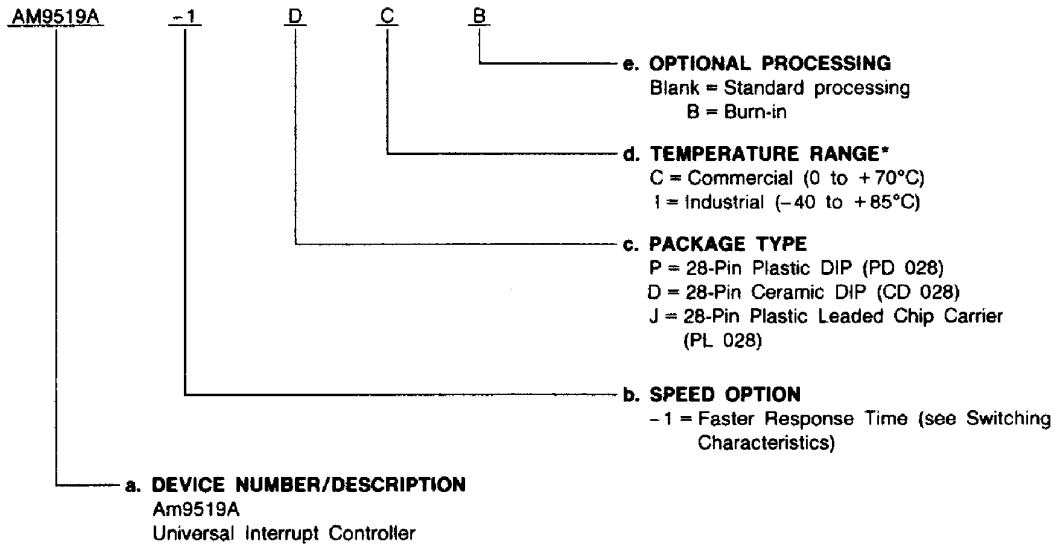
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9519A	PC, DC, DCB, DIB, JC
AM9519A-1	PC, DC, DCB, JC

*This device is also available in Military temperature range.

Valid Combinations

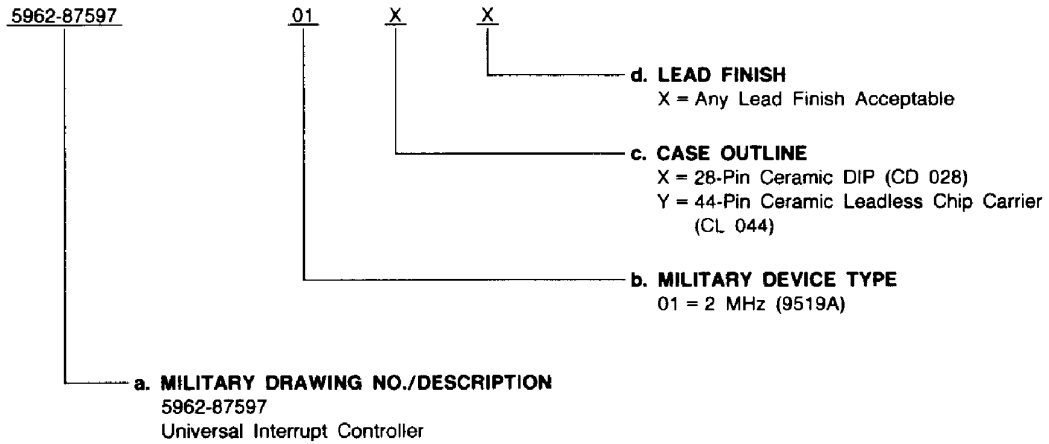
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (continued)

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:

- a. **Military Drawing Part Number**
- b. **Device Type**
- c. **Case Outline**
- d. **Lead Finish**



Valid Combinations	
5962-8759701	XX, YX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

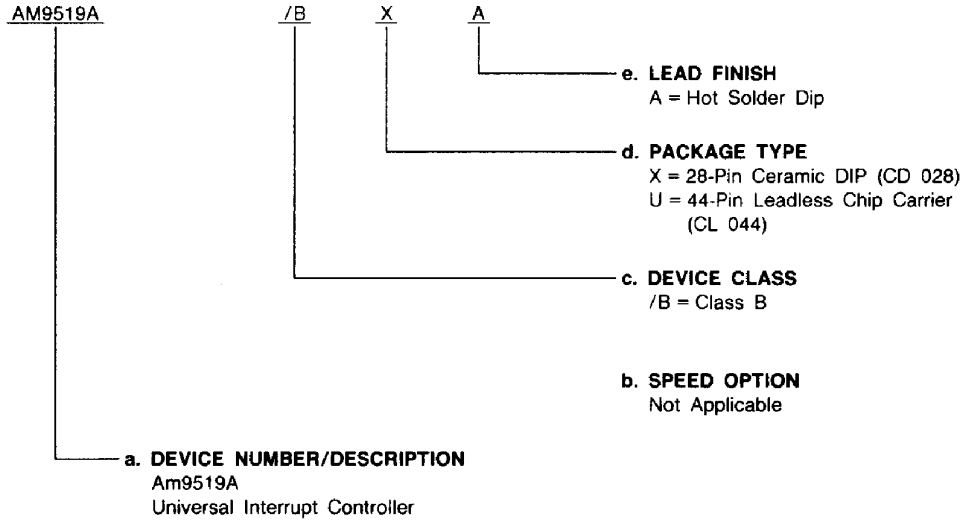
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ORDERING INFORMATION (continued)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM9519A	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
28	V _{CC}		+5 Volt Power Supply.
14	V _{SS}		Ground.
11-4	DB0-DB7	I/O	(Data Bus). The eight bidirectional data bus signals are used to transfer information between the Am9519A and the system data bus. The direction of transfer is controlled by the IACK, WR and RD input signals. Programming and control information are written into the device; status and response data are output by it.
1	CS	I	(Chip Select). The active low Chip Select input enables read and write operations on the data bus. Interrupt acknowledge responses are not conditioned by CS.
3	RD	I	(Read). The active low Read signal is conditioned by CS and indicates that information is to be transferred from the Am9519A to the data bus.
2	WR	I	(Write). The active low Write signal is conditioned by CS and indicates that data bus information is to be transferred from the data bus to a location within the Am9519A.
27	C/D	I	(Control/Data). The C/D control signal selects source and destination locations for data bus read and write operations. Data read or write transfers are made to or from preselected internal registers or memory locations. Control write operations load the command register and control read operations output the status register.
18-25	IREQ0-IREQ7	I	(Interrupt Request). The Interrupt Request signals are used by external devices to indicate that service by the host CPU is desired. IREQ inputs are accepted asynchronously and they may be programmed for either a HIGH-to-LOW or LOW-to-HIGH edge transition. Active inputs are latched internally in the Interrupt Request Register. After the IRR bit is cleared, an IREQ transition of the programmed polarity must occur to initiate another request.
12	RIP	I/O	(Response In Process). Response In Process is a bidirectional signal used when two or more Am9519A circuits are cascaded. It permits multibyte response transfers to be completed without interference from higher priority interrupts. An Am9519A that is responding to an acknowledged interrupt will treat RIP as an output and hold it LOW until the acknowledge response is finished. An Am9519A without an acknowledged interrupt will treat RIP as an input and will ignore IACK pulses as long as RIP is LOW. The RIP output is open drain and requires an external pull-up resistor to VCC.
26	IACK	I	(Interrupt Acknowledge). The active-low Interrupt Acknowledge line indicates that the external system is asking for interrupt response information. Depending on the programmed state of the Am9519A, it will accept 1, 2, 3 or 4 IACK pulses; one response byte is transferred per pulse. The first IACK pulse causes selection of the highest priority unmasked pending interrupt request and generates a RIP output signal.
15	PAUSE	O	(Pause). The active-low Pause signal is used to coordinate interrupt responses with data bus and control timing. Pause goes LOW when the first IACK is received and remains LOW until RIP goes LOW. The external system can use Pause to stretch the acknowledge cycle and allow the control timing to automatically adjust to the actual priority resolution delays in the interrupt system. Second, third and fourth response bytes do not cause Pause to go LOW. Pause is an open drain output and requires an external pull-up resistor to VCC.
16	EO	O	(Enable Out). The active-high EO signal is used to implement daisy-chained cascading of several Am9519A circuits. EO is connected to the EI input of the next lower priority chip. On receipt of an interrupt acknowledge, each EO will go inactive until it has been determined that no valid interrupt request is pending on that chip. If an active request is present, EO remains LOW. EO is also held LOW when the master mask bit is active, thus disabling all lower priority chips.
13	EI	I	(Enable in). The active-high EI signal is used to implement daisy-chained cascading of several Am9519A circuits. EI is connected to EO of the next higher priority chip. It may also be used as a hardware disable input for the interrupt system. When EI is LOW, IACK inputs will not affect ISR; however, PAUSE will go LOW until RIP goes LOW. EI is internally pulled up to VCC so that no external pull-up is needed when EI is not used.
17	GINT	O	(Group Interrupt). The Group Interrupt output signal indicates that at least one unmasked interrupt request is pending. It may be programmed for active-high or active-low polarity. When active-low, the output is open drain and requires an external pull-up resistor to VCC. Since a glitch on GINT occurs approximately 100nsec after the last IACK pulse, this pin should not be connected to edge sensitive devices.

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PRODUCT OVERVIEW

Register Description

Interrupt Request Register (IRR): The 8-bit IRR is used to store pending interrupt requests. A bit in the IRR is set whenever the corresponding IREQ input goes active. Bits may also be set under program control from the CPU, thus permitting software generated interrupts. IRR bits may be cleared under program control. An IRR bit is automatically cleared when its interrupt is acknowledged. All IRR bits are cleared by a reset function.

Interrupt Service Register (ISR): The 8-bit ISR contains one bit for each IREQ input. It is used to indicate that a pending interrupt has been acknowledged and to mask all lower priority interrupts. When a bit is set by the acknowledge logic in the ISR, the corresponding IRR bit is cleared. If an acknowledged interrupt is not programmed to be automatically cleared, its

ISR bit must be cleared by the CPU under program control when it is desired to permit interrupts from lower priority devices. When the interrupt is programmed for automatic clearing, the ISR bit is automatically reset during the acknowledge sequence. All ISR bits are cleared by a reset function.

Interrupt Mask Register (IMR): The 8-bit IMR is used to enable or disable the individual interrupt inputs. The IMR bits correspond to the IREQ inputs, and all eight may be loaded, set or cleared in parallel under program control. In addition, individual IMR bits may be set or cleared by the CPU. Care must be taken therefore when disabling a specific channel by setting its IMR bit. If that bit is causing the GINT pin to be active, a lock-up condition can occur if the CPU recognizes the interrupt and then the Am9519A removes the request. During the IACK cycle, PAUSE will go LOW and stay LOW. The solution is to disable CPU interrupts prior to writing to the IMR and then re-enable them. A reset function will set all eight

mask bits, disabling all requests. A mask bit that is set does not disable the IRR, and an IREQ that arrives while a corresponding mask bit is set will cause an interrupt later when the mask bit is cleared. Only unmasked interrupt inputs can generate a Group Interrupt output.

Response Memory: An 8 x 32 read/write response memory is included in the Am9519A. It is used to store up to four bytes of response information for each of the eight interrupt request inputs. All bits in the memory are programmable, allowing any desired vector, opcode, instruction or other data to be entered. The Am9519A transfers the interrupt response information for the highest priority unmasked interrupt from the memory to the data bus when the IACK input is active.

Auto Clear Register: The 8-bit Auto Clear register contains one bit for each IREQ input and specifies the operating mode for each of the ISR bits. When an auto clear bit is off, the corresponding ISR bit is set when that interrupt is acknowledged and is cleared by software command. When an auto clear bit is on, the corresponding ISR bit is cleared by the hardware by the rising edge of the last acknowledge pulse. A reset function clears all auto clear bits.

Status Register: The 8-bit Status register contains information concerning the internal state of the chip. It is especially useful when operating in the polled mode to identify interrupting devices. Figure 1 shows the status register bit assignments. The polarity of the GINT bit 7 is not affected by the GINT polarity control. Bits S0-S2 are set asynchronously to a status register read operation. It is recommended to read the

register twice and to compare the binary vectors for equality prior to proceeding with the device service in polled mode. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit 3). The Status register is read by executing a read operation ($\overline{CS} = 0$, $RS = 0$) with the control location selected ($C/\overline{D} = 1$).

Mode Register: The 8-bit Mode register controls the operating options of the Am9519A. Figure 2 shows the bit assignments for the Mode register. The five low order mode bits (0 through 4) are loaded in parallel by command. Bits 5, 6 and 7 are controlled by separate commands. (See Figure 4.) The Mode register cannot be read out directly to the data bus, but Mode bits 0, 2 and 7 are available as part of the Status register.

Command Register: The 8-bit Command register stores the last command entered. Depending upon the command opcode, it may initiate internal actions or precondition the part for subsequent data bus transfers. The Command register is loaded by executing a write operation ($\overline{WR} = 0$) with the control location selected ($C/\overline{D} = 1$), as shown in Figure 3.

Byte Count Register: The length in bytes of the response associated with each interrupt is independently programmed so that different interrupts may have different length responses. The byte count for each response is stored in eight 2-bit Byte Count registers. For a given interrupt, the Am9519A will expect to receive a number of IACK pulses that equal the corresponding byte count and will hold \overline{RIP} LOW until the count is satisfied.

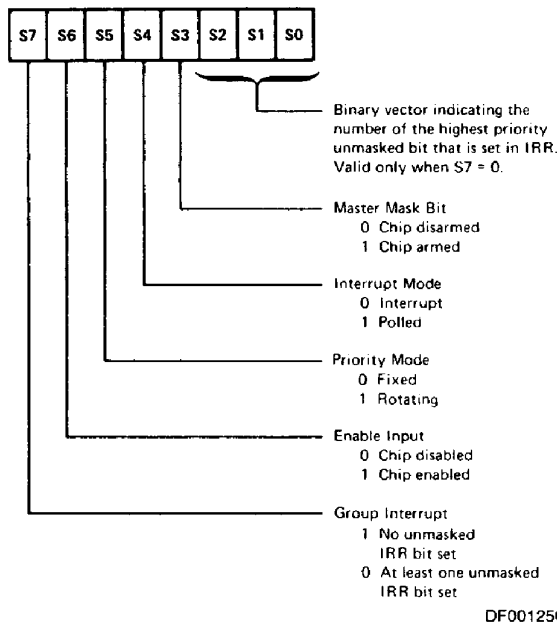


Figure 1. Status Register Bit Assignments

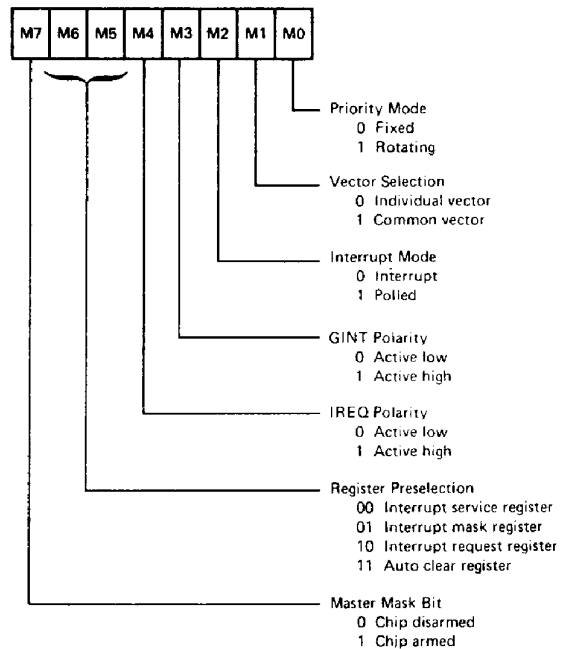


Figure 2. Mode Register Bit Assignments

DETAILED DESCRIPTION

Interrupts are used to improve system throughput and response time by eliminating heavy dependence on software polling procedures. Interrupts allow external devices to asynchronously modify the instruction sequence of a program

being executed. In systems with multiple interrupts, vectoring can further improve performance by allowing direct identification of the interrupting device and its associated service routine. The Am9519A Universal Interrupt Controller contains, on one chip, all of the circuitry necessary to detect, prioritize and manage eight vectored interrupts. It includes many

options and operating modes that permit the design of sophisticated interrupt systems.

Reset

The reset function is accomplished by software command or automatically during power-up. The reset command may be issued by the CPU at any time. Internal power-up circuitry is triggered when VCC reaches a predetermined threshold, causing a brief internal reset pulse. In both cases, the resulting internal state of the machine is that all registers are cleared except the Mask register which is set. Thus, no Group Interrupt will be generated, and no interrupt requests will be recognized. The response memory and Byte Count registers are not affected by reset. Their contents after power-up are unpredictable and must be established by the host CPU during initialization.

Operating Sequence

A brief description of a typical sequence of events in an operating interrupt system will illustrate the general interactions among the host CPU, the interrupt controller and the interrupting peripheral.

1. The Am9519A controller is initialized by the CPU to customize its configuration and operation for the application at hand. Both the controller and the CPU are then enabled to accept interrupts.
2. One (or more) of the interrupt request inputs to the controller becomes active indicating that peripheral equipment is asking for service. The controller asynchronously accepts and latches the request(s).
3. If the request is masked, no further action takes place. If the request is not masked, a Group Interrupt output is generated by the controller.
4. The GINT signal is recognized by the CPU which normally will complete the execution of the current instruction, insert an interrupt acknowledge sequence into its instruction execution stream, and disable its internal interrupt structure. The controller expects to receive one or more $\overline{\text{IACK}}$ signals from the CPU during the acknowledge sequence.
5. When the controller receives the $\overline{\text{IACK}}$ signal, it brings $\overline{\text{PAUSE}}$ low and selects the highest priority unmasked pending request. When selection is complete, the $\overline{\text{RIP}}$ output is brought low and the first byte in the response memory associated with the selected request is output on the data bus. $\overline{\text{PAUSE}}$ stays low until $\overline{\text{RIP}}$ goes low. $\overline{\text{RIP}}$ stays low until the last byte of the response has been transferred.
6. During the acknowledge sequence, the IRR bit corresponding to the selected request is automatically cleared, and the corresponding ISR bit is set by the falling edge of $\overline{\text{IACK}}$. When the ISR bit is set, the Group Interrupt output is disabled until a higher priority request arrives or the ISR bit is cleared. The ISR bit will be cleared by either hardware or software.
7. If a higher priority request arrives while the current request is being serviced, GINT will be output by the controller, but will be recognized and acknowledged only if the CPU has its interrupt input enabled. If acknowledged, the corresponding higher priority ISR bit will be set and the requests nested.

Information Transfers

Figure 3 shows the control signal configurations for all information transfer operations between the Am9519A and the data bus. The following conventions are assumed: $\overline{\text{RD}}$ and $\overline{\text{WR}}$ active are mutually exclusive; $\overline{\text{RD}}$, $\overline{\text{WR}}$ and C/D have no meaning unless $\overline{\text{CS}}$ is LOW; active $\overline{\text{IACK}}$ pulses occur only when $\overline{\text{CS}}$ is HIGH.

For reading, the Status register is selected directly by the C/D control input. Other internal registers are read by preselecting the desired register with mode bits 5 and 6, and then executing a data read. The response memory can be read only with $\overline{\text{IACK}}$ pulses. For writing, the Command register is selected directly by the C/D control input. The Mask and Auto Clear registers are loaded following specific commands to that effect. To load each level of the response memory, the response preselect command is issued to select the desired level. An appropriate number of data write operations are then executed to load that level.

CONTROL INPUT					DATA BUS OPERATION
$\overline{\text{CS}}$	C/D	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{IACK}}$	
0	0	0	1	1	Transfer contents of preselected data register to data bus
0	0	1	0	1	Transfer contents of data bus to preselected data register
0	1	0	1	1	Transfer contents of status register to data bus
0	1	1	0	1	Transfer contents of data bus to command register
1	X	X	X	0	Transfer contents of selected response memory location to data bus
1	X	X	X	1	No information transferred

Figure 3. Summary of Data Bus Transfers

The Pause output may be used by the host CPU to ensure that prototyping relationships are maintained with the Am9519A when $\overline{\text{IACK}}$ is active. The $\overline{\text{IACK}}$ pulse width required depends on several variables, including: operating temperature, internal logic delays, number of interrupt controllers chained together, and the priority level of the interrupt being acknowledged. When delays in these variables combine to delay selection of a request following the falling edge of the first $\overline{\text{IACK}}$, the Pause output may be used to extend the $\overline{\text{IACK}}$ pulse, if necessary. Pause will remain LOW until a request has been selected, as indicated by the falling edge of $\overline{\text{RIP}}$. Typically, the internal interrupt selection process is quite fast, especially for systems with a single Am9519A, and Pause will consequently remain LOW for only a very brief interval and will not cause extension of the $\overline{\text{IACK}}$ timing.

Operating Options

The Mode register specifies the various combinations of operating options that may be selected by the CPU. It is cleared by power-up or by a reset command. Mode bit 0 specifies the rotating/fixed priority mode (see Figure 2). In the fixed mode, priority is assigned to the request inputs based upon their physical location at the chip interface, with IREQ0 the highest and IREQ7 the lowest. In the rotating mode, relative priority is the same as for the fixed mode and the most recently serviced request is assigned the lowest priority. In the fixed mode, a lower priority request might never receive service if enough higher priority requests are active. In the rotating mode, any request will receive service within a maximum of seven other service cycles no matter what pattern the request inputs follow.

Mode bit 1 selects the individual/common vector option. Individual vectoring provides a unique location in the response memory for each interrupt request. The common vector option always supplies the response associated with IREQ0 no matter which request is being acknowledged.

Mode bit 2 specifies interrupt or polled operation. In the polled mode, the Group Interrupt output is disabled. The CPU may read the Status register to determine if a request is pending.

Since $\overline{\text{IACK}}$ pulses are not normally supplied in polled mode, the IRR bit is not automatically cleared, but may be cleared by command. With no $\overline{\text{IACK}}$ input, the ISR and the response memory are not used. An Am9519A in the polled mode has EI connected to EO so that in multichip interrupt systems the polled chip is functionally removed from the priority hierarchy.

Mode bit 3 specifies the sense of the GINT output. When active high polarity is selected, the output is a two-state configuration. For active low polarity, the output is open drain and requires an external pull-up resistor to provide the high logic level. The open drain output allows wired-or configurations with other similar output signals.

Mode bit 4 specifies the sense of the IREQ inputs. When active low polarity is selected, the IRR responds to falling edges on the request inputs. When active high is selected, the IRR responds to rising edges.

Mode bits 5 and 6 specify the register that will read on subsequent data read operations ($C/\overline{D} = 0, \overline{RD} = 0$). This preselection remains valid until changed by a reset or a command.

Mode bit 7 is the master mask bit that disables all request inputs. It is used to disable all interrupts without modifying the IMR so that the previous IMR contents are valid when interrupts are re-enabled. When the master mask bit is LOW, it causes the EO line to remain disabled (LOW). Thus, for multiple-chip interrupt systems, one master mask bit can disable the whole interrupt structure. Alternatively, portions of the structure may be disabled. The state of the master mask bit is available as bit S3 of the Status register.

Programming

After reset, the Am9519A must be initialized by the CPU to perform useful work. At a minimum, the master mask bit and at

least one of the IMR bits should be enabled. If vectoring is to be used, the response memory must be loaded; if not, the mode must be changed to a non-vectoring configuration. Normally, the first step will be to modify the Mode register and the Auto clear register to establish the configuration desired for the application. Then the response memory and byte count will be loaded for those request levels that will be in use. The response memory for every channel must be written even if the channel is not used. Every byte need not be written, only those specified by the byte count. Finally, the master mask bit and at least portions of the IMR will be enabled to allow interrupt processing to proceed.

Commands

The host CPU configures, changes and inspects the internal condition of the Am9519A using the set of commands shown in Figure 4. An "X" entry in the table indicates a "don't care" state. All commands are entered by directly loading the Command register as shown in Figure 3 ($C/\overline{D} = 1, \overline{WR} = 0$). Figure 5 shows the coding assignments for the Byte Count registers. (A detailed description of each command is contained in the Am9519A Application Note AMPUB-071.)

BY1	BY0	COUNT
0	0	1
0	1	2
1	0	3
1	1	4

Figure 5. Byte Count Coding

COMMAND CODE								COMMAND DESCRIPTION
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load Mode register bits 0 - 4 with specified pattern
1	0	1	0	M6	M5	0	0	Load Mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load Mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load Mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselected IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselected Auto Clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

Figure 4. Am9519A Command Summary

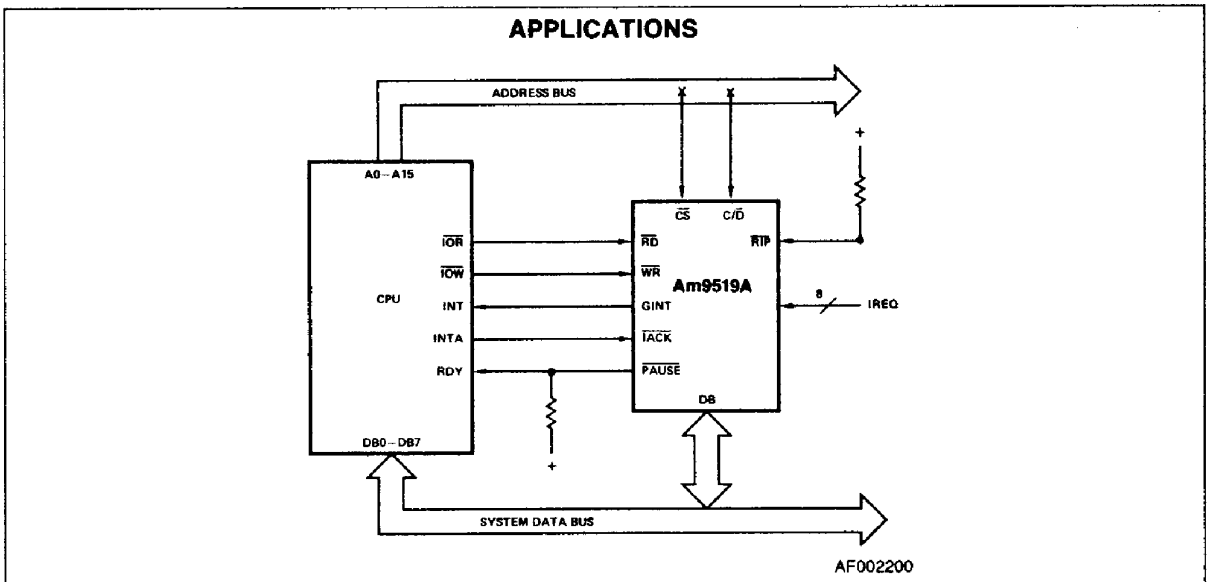


Figure 6. Base Interrupt System Configuration

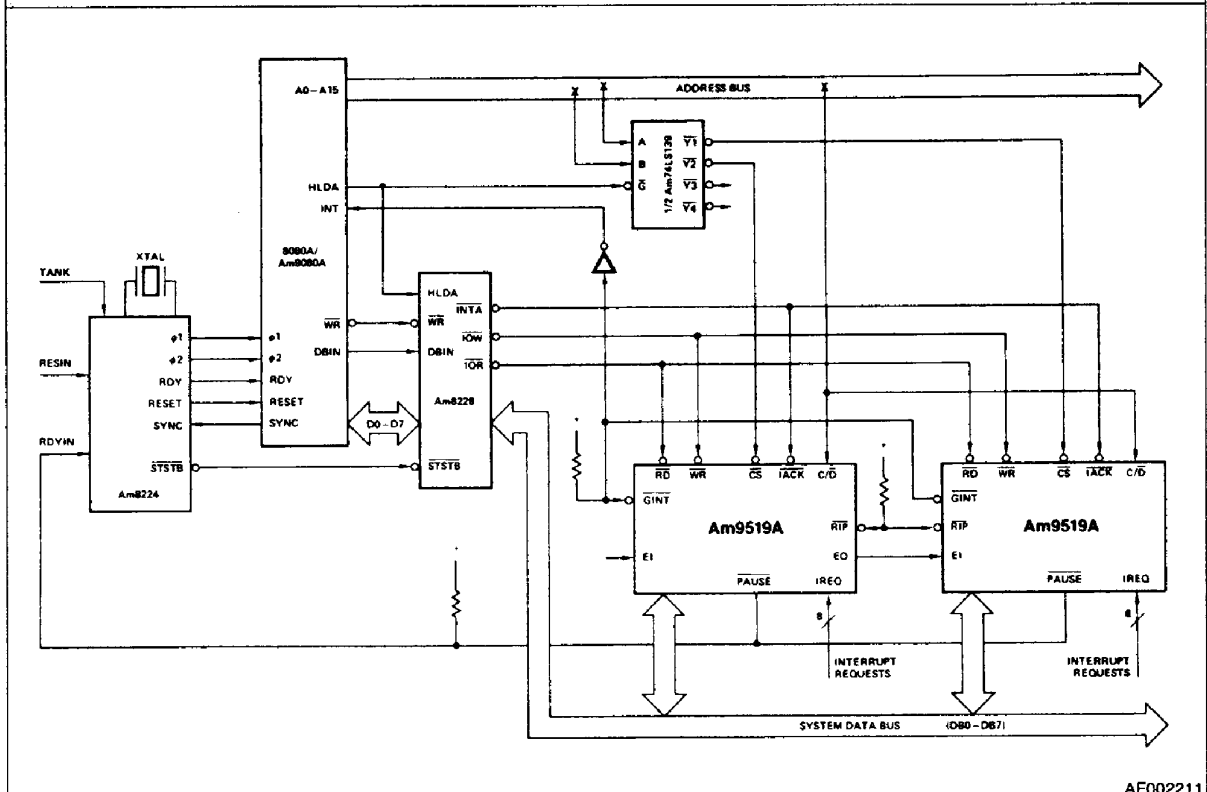


Figure 7. Expanded Interrupt System Configuration

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 VCC with Respect to VSS -0.5 V to +7.0 V
 All Signal Voltages
 with Respect to VSS -0.5 V to +7.0 V
 Power Dissipation (Package Limitation) 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
 Temperature (T_A) 0 to +70°C
 Supply Voltage (V_{CC}) 5 V ± 5%

Industrial (I) Devices
 Temperature (T_A) -40 to +85°C
 Supply Voltage (V_{CC}) 5 V ± 10%

Military (M) Devices
 Temperature (T_C) -55 to +125°C
 Supply Voltage (V_{CC}) 5 V ± 10%

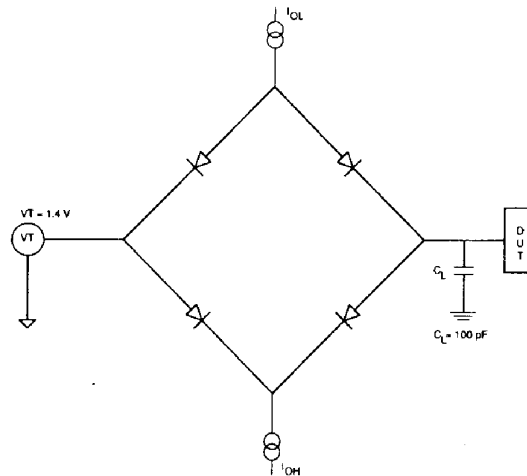
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL and SMD/DESC Products; Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameters	Description	Test Conditions	Min	Max	Units	
VOH	Output High Voltage (Note 8)	I _{OH} = -200µA	2.4		Volts	
		I _{OH} = -100µA (EO only)	2.4			
VOL	Output Low Voltage	I _{OL} = 3.2mA		0.4	Volts	
		I _{OL} = 1.0mA (EO only)		0.4		
VIH	Input High Voltage		2.0	V _{CC} *	Volts	
VIL	Input Low Voltage		-0.5*	0.8	Volts	
IIX	Input Load Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	EI Input	-60	10	µA
			Other inputs	-10	10	
IOZ	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , Output Off	COML -10	10	µA	
			MIL 150	150		
ICC	CXX Supply Current	Commercial		125	mA	
		Industrial		185		
		Military		200		
CO	Output Capacitance	f _c = 1.0 MHz		15*	pF	
CI	Input Capacitance	T _A = 25°C		10*		
CIO	I/O Capacitance	All pins at 0 V		20*		

*Guaranteed by design — not tested.

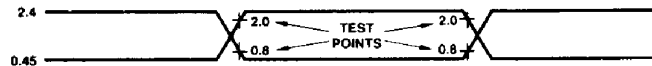
SWITCHING TEST CIRCUIT



TC004200

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Notes 1, 2)

Parameters	Description	Am9519A		Am9519A-1		Units
		Min	Max	Min	Max	
TAVRL	C/D Valid and CS LOW to Read LOW	0		0		ns
TAVWL	C/D Valid and CS LOW to Write LOW	0		0		ns
TCLPH	RIP LOW to PAUSE HIGH (Note 3)	75	375	75	375	ns
TCLQV	RIP LOW to Data Out Valid (Note 4)		50		40	ns
TDVWH	Data in Valid to Write HIGH	250		200		ns
TEHCL	Enable in HIGH to RIP LOW (Note 5)	30	300	30	300	ns
TIVGV	Interrupt Request Valid to Group Interrupt Valid	100	800		650	ns
TIVIX	Interrupt Request Valid to Interrupt Request Don't Care (IREQ Pulse Duration)	250		250		ns
TKHCH	IACK HIGH to RIP HIGH (Note 5)		450		350	ns
TKHKL	IACK HIGH to IACK LOW (IACK Recovery)	140		120		ns
TKHNL	IACK HIGH to EO HIGH (Notes 6, 7)		975		750	ns
TKHQX	IACK HIGH to Data Out Invalid	20	200	20	100	ns
TKLCL	IACK LOW to RIP LOW (Notes 5, 9)	75	600	75	450	ns
TKLKH	IACK LOW to IACK HIGH (1st IACK) (Note 9)	975		800		ns
TKLNL	IACK LOW to EO LOW (Notes 6, 7, 9)		125		100	ns
TKLPL	IACK LOW to PAUSE LOW (Note 9)	25	175	25	125	ns
TKLQV	IACK LOW to Data Out Valid (Notes 4, 9)	25	300	25	200	ns
TKLQV1	1st IACK LOW to Data Out Valid (Note 9)	75	650	75	490	ns
TPHKH	PAUSE HIGH to IACK HIGH	0		0		ns
TRHAX	Read HIGH to C/D and CS Don't Care	0		0		ns
TRHQX	Read HIGH to Data Out Invalid	20	200	20	100	ns
TRLQV	Read LOW to Data Out Valid		300		200	ns
TRLQX	Read LOW to Data Out Unknown	35		35		ns
TRLRH	Read LOW to Read HIGH (RD Pulse Duration)	300		250		ns
TWHAX	Write HIGH to C/D and CS Don't Care	25		25		ns
TWHDX	Write HIGH to Data in Don't Care	25		25		ns
TWHRW	Write HIGH to Read or Write LOW (Write Recovery)	600		400		ns
TWLWH	Write LOW to Write HIGH (WR Pulse Duration)	300		250		ns
TKHIH	IACK HIGH to GINT inactive		1000		800	ns

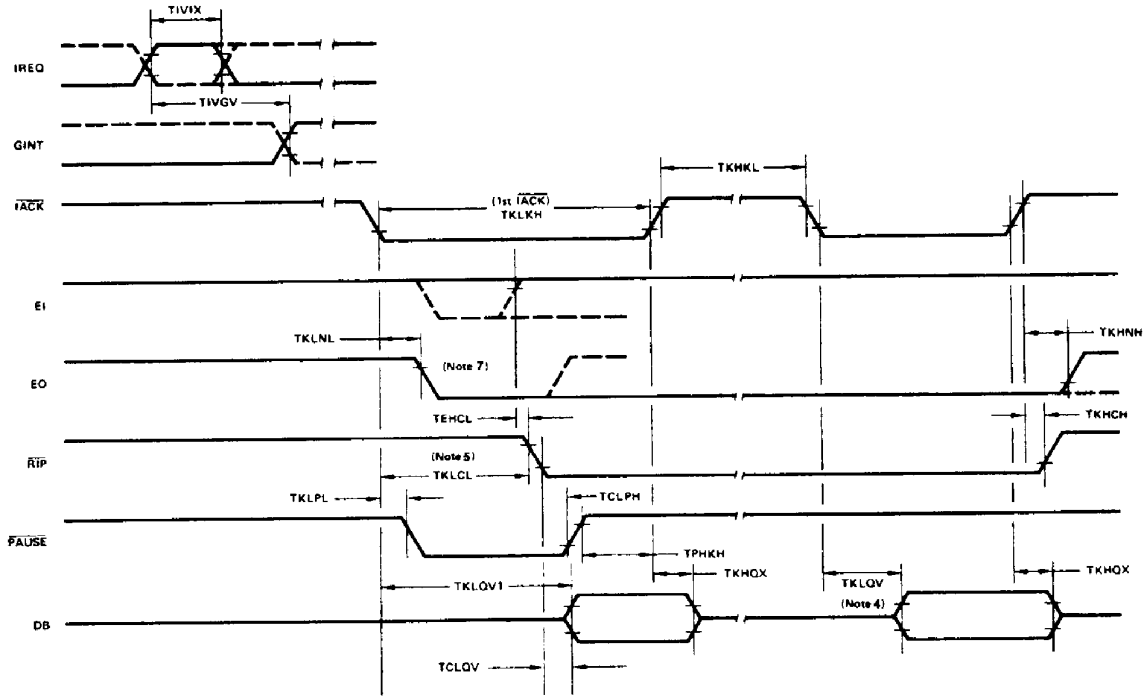
- Notes:
- Transition abbreviations used for the switching parameter symbols include: H = HIGH, L = LOW, V = Valid, X = unknown or don't care, Z = high-impedance.
 - Signal abbreviations used for the switching parameter symbols include: R = Read, W = Write, Q = Data Out, D = Data In, A = Address (CS and C/D), K = Interrupt Acknowledge, N = Enable Out, E = Enable In, P = Pause, C = RIP.
 - During the first IACK pulse, PAUSE will be LOW long enough to allow for priority resolution and will not go HIGH until after RIP goes LOW (TCLPH).
 - TKLQV applies only to second, third and fourth IACK pulses while RIP is LOW. During the first IACK pulse, Data Out will be valid following the falling edge of RIP (TCLQV).
 - RIP is pulled LOW to indicate that an interrupt request has been selected. RIP cannot be pulled LOW until EI is HIGH following an internal delay. TKLCL will govern the falling edge of RIP when EI is always HIGH or is HIGH early in the acknowledge cycle. The TEHCL will govern when EI goes HIGH later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. RIP remains LOW until after the rising edge of the IACK pulse that transfers the last response byte for the selected IREQ.
 - Test conditions for the EO line assume an output loading of IOL = 1.0 mA and IOH = -100 μA. Since EO normally only drives EI of another Am9519A, higher speed operations can be specified with this more realistic test condition.
 - The arrival of IACK will cause EO to go LOW, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return HIGH when EI is HIGH. If a pending request is selected, EO will stay LOW until after the last IACK pulse for that interrupt is complete and RIP goes HIGH.
 - VOH specifications do not apply to RIP, PAUSE, or to GINT when active-low. These outputs are open drain, and VOH levels will be determined by external circuitry.
 - CS must be HIGH for at least 100ns prior to IACK going LOW.

SWITCHING CHARACTERISTICS over **MILITARY** operating ranges (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted). (Notes 1, 2)

No.	Parameter Symbol	Parameter Description	Am9519A		Unit
			Min.	Max.	
1	TAVRL	C/D Valid and CS LOW to Read LOW	0		ns
2	TAVWL	C/D Valid and CS LOW to Write LOW	0		ns
3	TCLPH	RIP LOW to PAUSE HIGH (Note 3)	75	375	ns
4	TCLQV	RIP LOW to Data Out Valid (Note 4)		50	ns
5	TDVWH	Data in Valid to Write HIGH	250		ns
6	TEHCL	Enable in HIGH to RIP LOW (Note 5)	30	300	ns
7	TIVGV	Interrupt Request Valid to Group Interrupt Valid	100	800	ns
8	TIVIX	Interrupt Request Valid to interrupt Request Don't Care (IREQ Pulse Duration)	250		ns
9	TKHCH	IACK HIGH to RIP HIGH (Note 5)		450	ns
10	TKHKL	IACK HIGH to IACK LOW (IACK Recovery)	140		ns
11	TKHNL	IACK HIGH to EO HIGH (Notes 6, 7)		975	ns
12	TKHQX	IACK HIGH to Data Out Invalid	20	200	ns
13	TKLCL	IACK LOW to RIP LOW (Notes 5, 9)	75	650	ns
14	TKLKH	IACK LOW to IACK HIGH (1st IACK) (Note 9)	975		ns
15	TKLNL	IACK LOW to EO LOW (Notes 6, 7, 9)		125	ns
16	TKLPL	IACK LOW to PAUSE LOW (Note 9)	25	175	ns
17	TKLQV	IACK LOW to Data Out Valid (Notes 4, 9)	25	300	ns
18	TKLQV1	1st IACK LOW to Data Out Valid (Note 9)	75	650	ns
19	TPHKH	PAUSE HIGH to IACK HIGH	0		ns
20	TRHAX	Read HIGH to C/D and CS Don't Care	0		ns
21	TRHQX	Read HIGH to Data Out Invalid	20	200	ns
22	TRLQV	Read LOW to Data Out Valid		300	ns
23	TRLQX	Read LOW to Data Out Unknown	35		ns
24	TRLRH	Read LOW to Read HIGH (RD Pulse Duration)	300		ns
25	TWHAX	Write HIGH to C/D and CS Don't Care	25		ns
26	TWHDX	Write HIGH to Data in Don't Care	25		ns
27	TWHRW	Write HIGH to Read or Write LOW (Write Recovery)	600		ns
28	TWLWH	Write LOW to Write HIGH (WR Pulse Duration)	300		ns
29	TKHIH	IACK HIGH to GINT Inactive		1000	ns

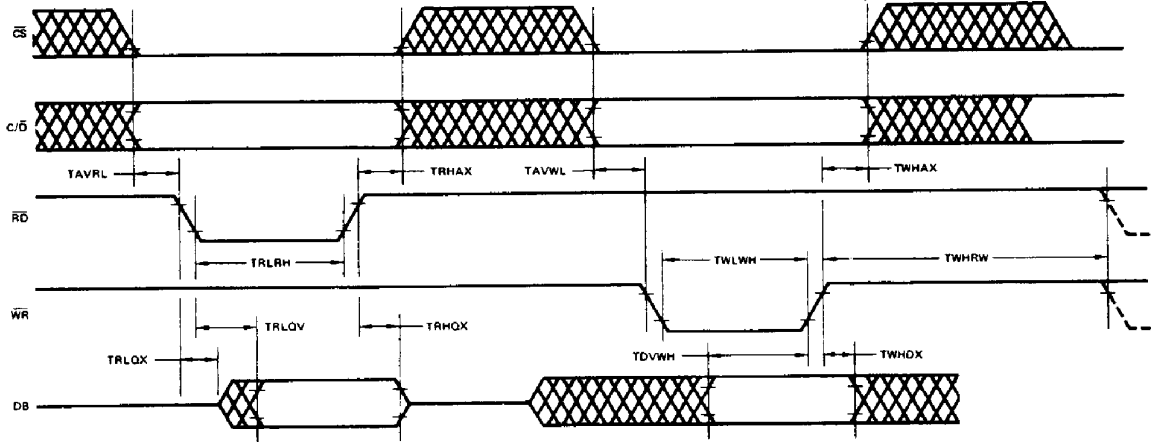
- Notes:
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 - TKLQV applies only to second, third and fourth IACK pulses while RIP is LOW. During the first IACK pulse, Data Out will be valid following the falling edge of RIP (TCLQV).
 - RIP is pulled LOW to indicate that an interrupt request has been selected. RIP cannot be pulled LOW until EI is HIGH following an internal delay. TKLCL will govern the falling edge of RIP when EI is always HIGH or is HIGH early in the acknowledge cycle. The TEHCL will govern when EI goes HIGH later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. RIP remains LOW until after the rising edge of the IACK pulse that transfers the last response byte for the selected IREQ.
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 - VOH specifications do not apply to RIP, PAUSE, or GINT when active-LOW. These outputs are open drain, and VOH levels will be determined by external circuitry.
 - CS must be HIGH for at least 100 ns prior to IACK going LOW.

SWITCHING WAVEFORMS



WF003551

Interrupt Operations



WF003560

Data Bus Transfers

Am9519A

2-225

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