Am29C818A

CMOS Pipeline Register with SSR™ Diagnostics

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed noninverting 8-bit parallel register for any data path or pipelining application**
- **WCS (Writable Control Store) pipeline register**
  - Load WCS from serial register
  - Read WCS via serial scan
- **Alternate sourced as SN74ACT818**
- **High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics**
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- **Low standby power**
- **JEDEC FCT-compatible specs**

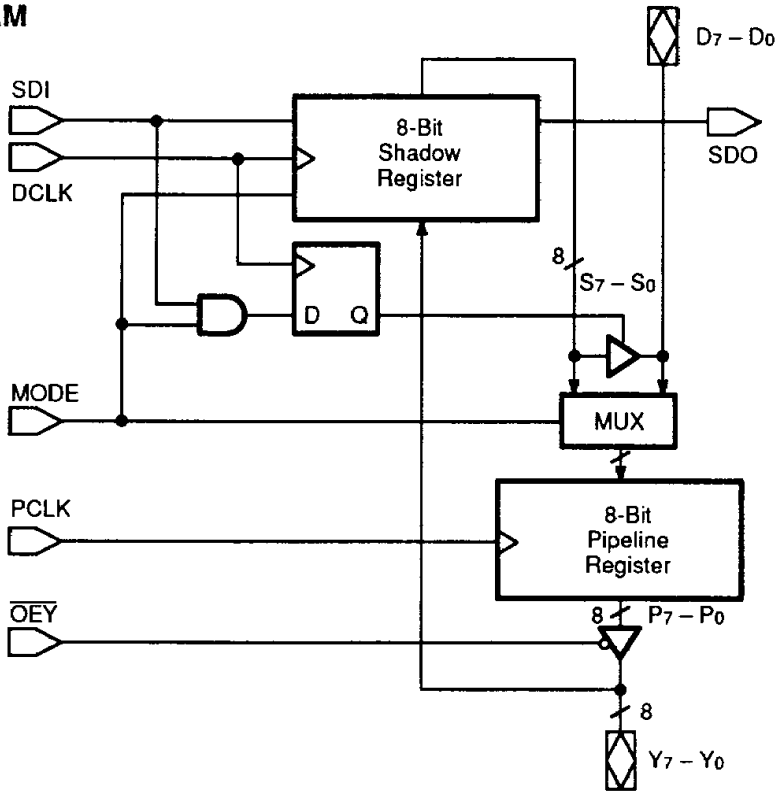
GENERAL DESCRIPTION

The Am29C818A is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a shift register. In the serial shift mode, SDI is shifted into the '0' location of the Shadow register and the contents of '7' location appear at the SDO output. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29C818A Diagnostics Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of clock cycles, the data clocked out can be compared to the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM



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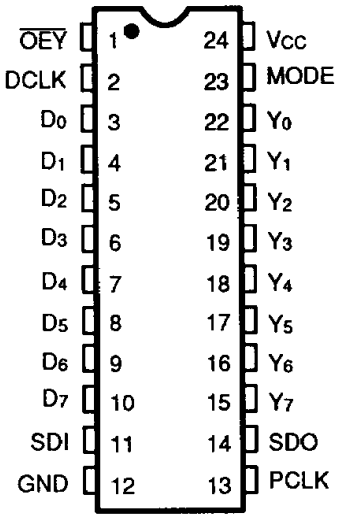
Publication# 09323 Rev. C Amendment/0
Issue Date: December 1990

CONNECTION DIAGRAMS
Top View

DIPs*



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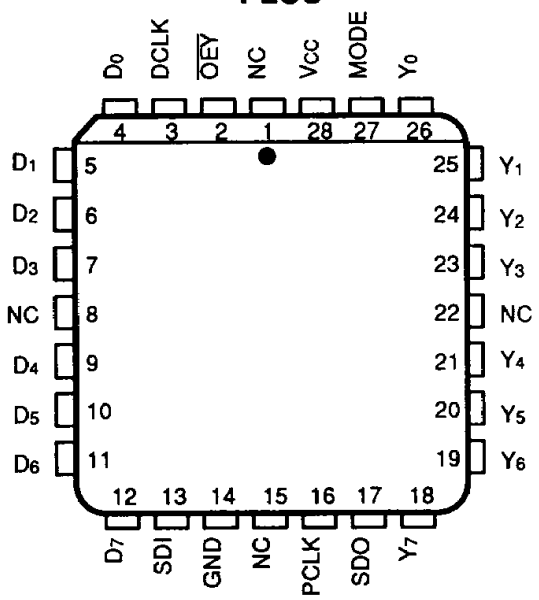
PLCC



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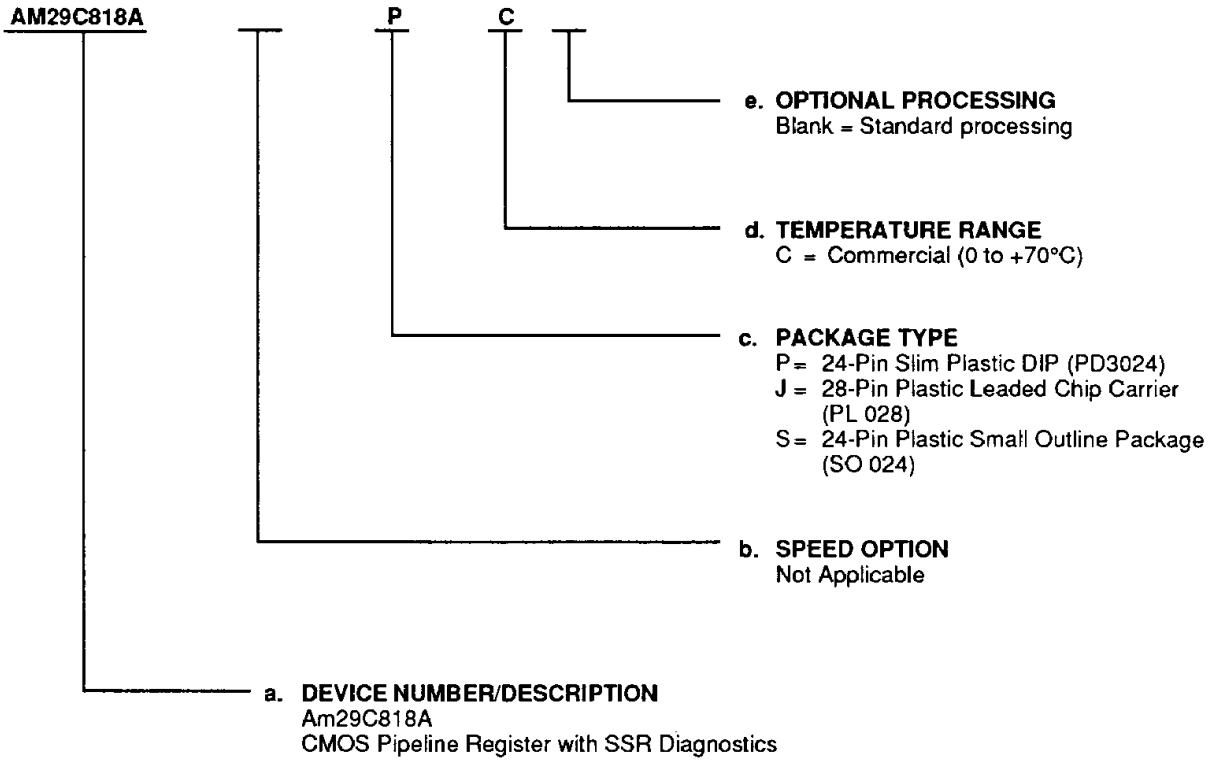
*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C818A	PC, SC, JC

Valid Combinations

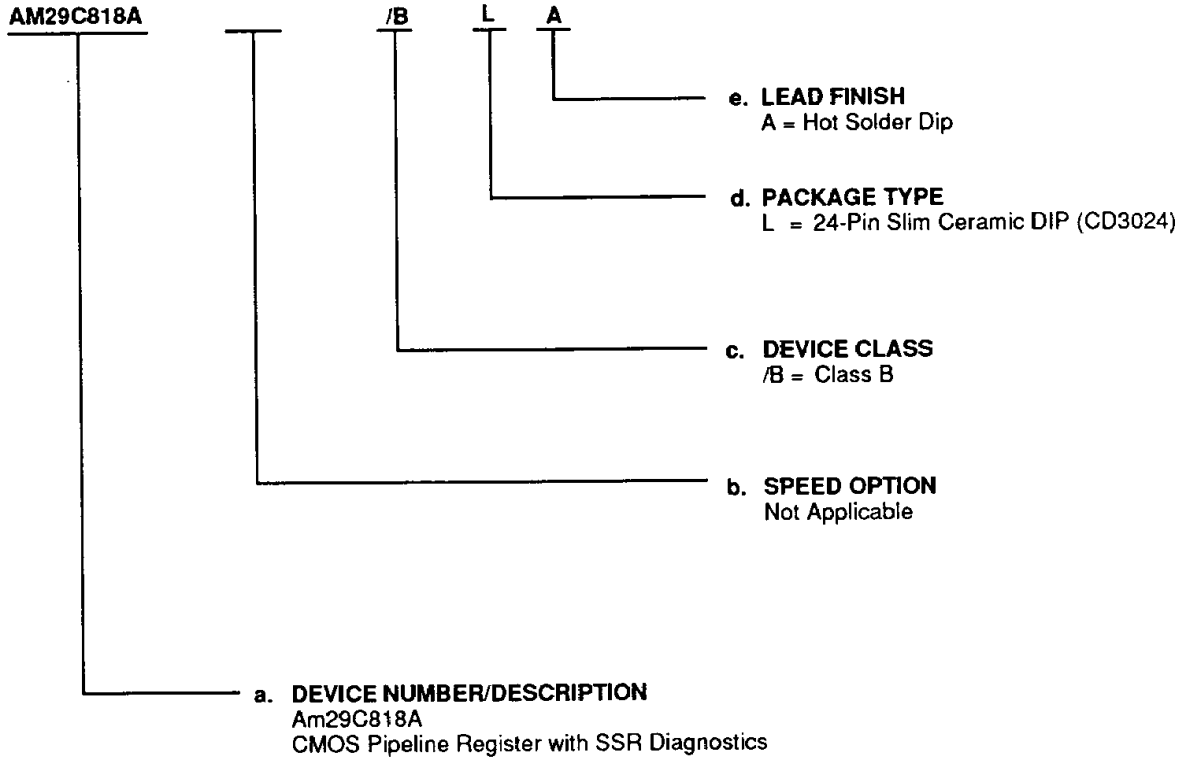
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C818A	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$D_0 - D_7$

Parallel Data Inputs (Input/Output)

Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK

Diagnostics Clock (Input)

Diagnostics/WCS clock for loading shadow register (serial or parallel modes – see Function Table).

MODE

Mode Control (Input)

Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$

Y-Port Output Enable (Input: Active LOW)

Active LOW output enable for Y-port.

PCLK

Pipeline Register Clock (Input)

Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI

Serial Data Input (Input)

Input to shadow register (see Function Table).

SDO

Serial Data Output (Output)

Output from shadow register.

$Y_0 - Y_7$

Parallel Data Outputs (Input/Output)

Data outputs from the pipeline register and parallel inputs to the shadow register.

FUNCTIONAL DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no setup or hold times are violated, this simultaneous operation is legal.

FUNCTION TABLE

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_0 \leftarrow$ SDI	NA	Serial Shift; $D_7 - D_0$ Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	SDI	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; $D_7 - D_0$ Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Reg.
H	H	↑	X	SDI	Hold*	NA	Hold Shadow Register; $D_7 - D_0$ Enabled*

*Although not shown, Hold is implemented by gating DCLK internally.

Table Definitions

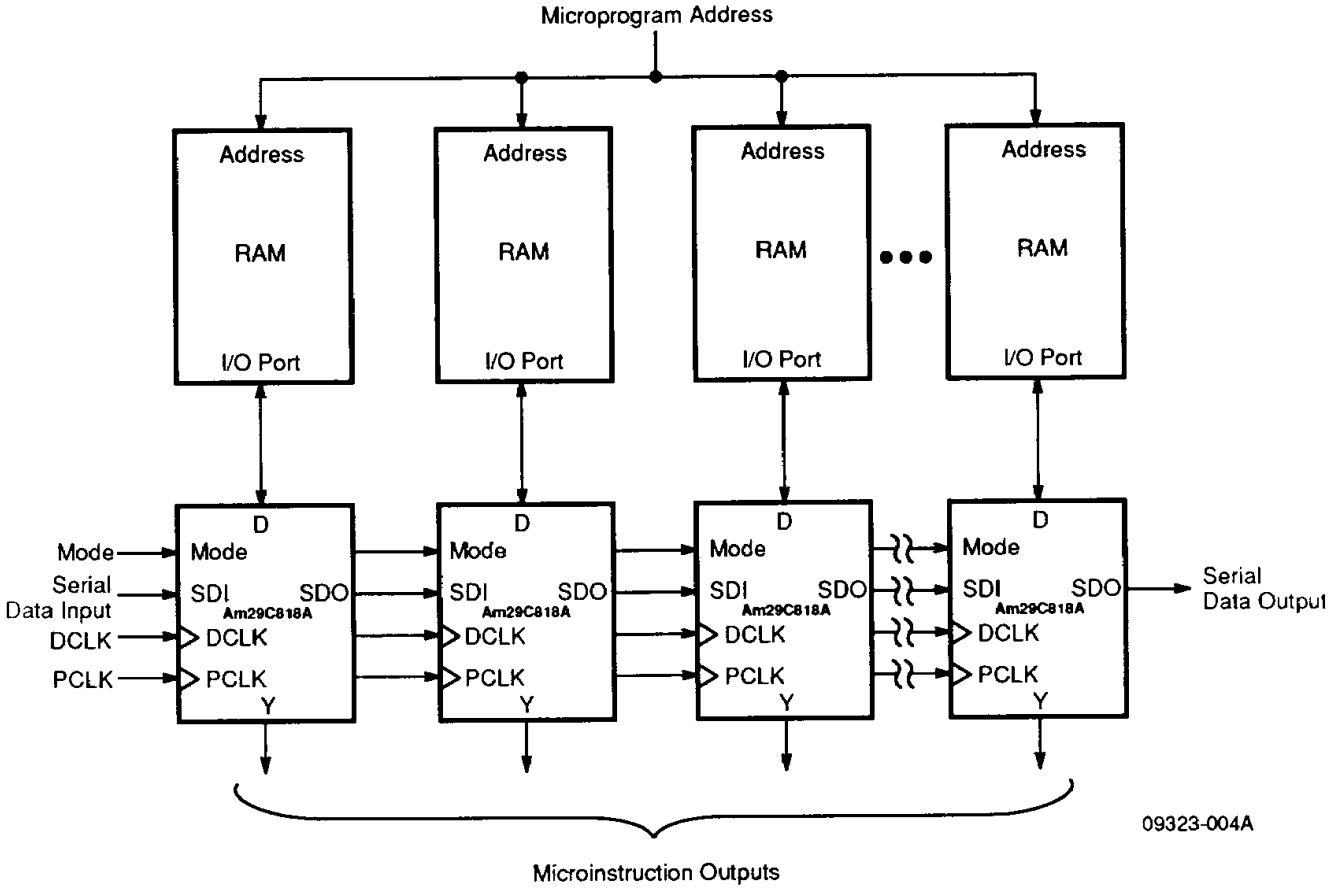
Inputs

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH Transition

Outputs

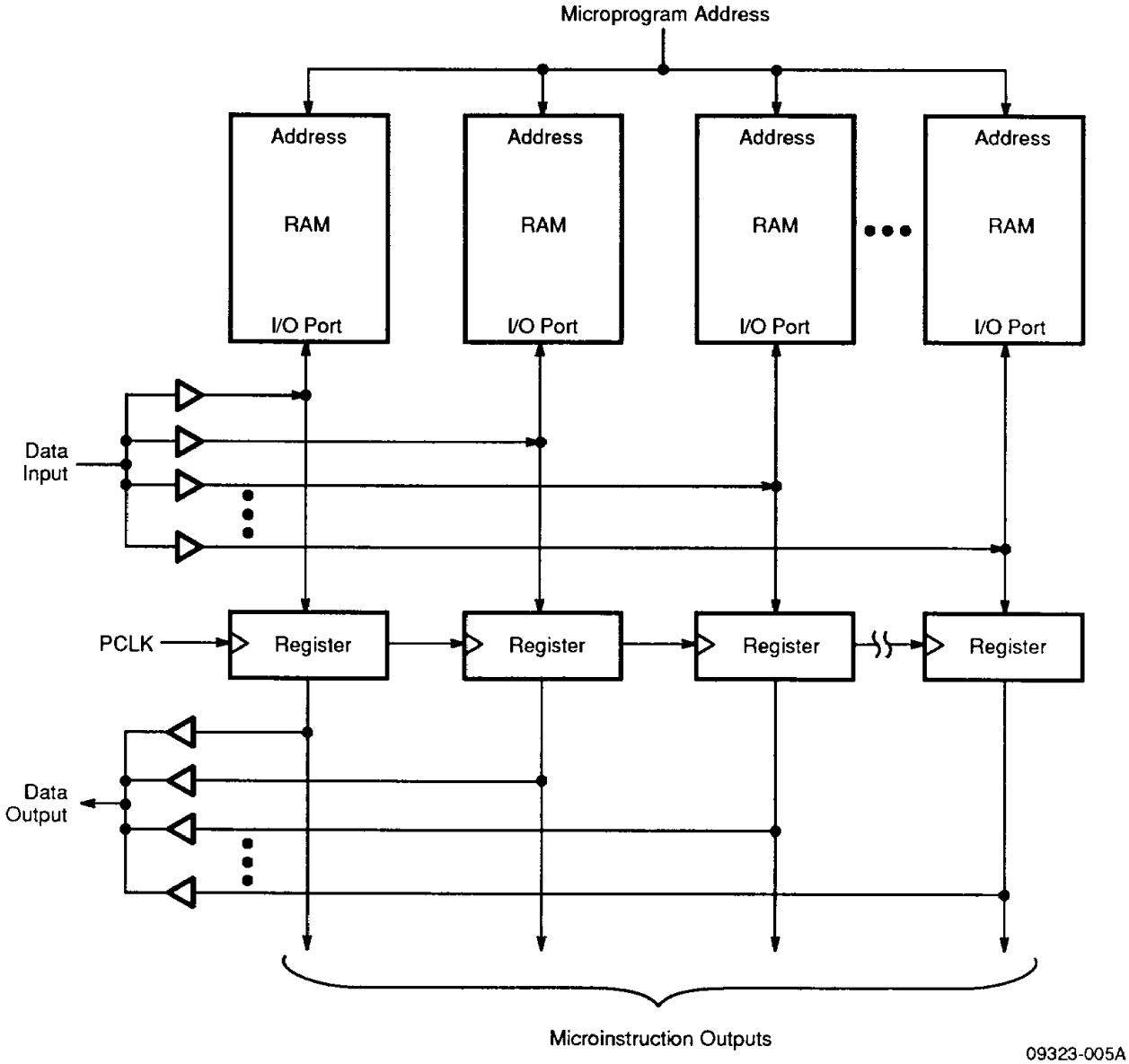
$S_7 - S_0$ = Shadow Register outputs
$P_7 - P_0$ = Pipeline Register outputs
$D_7 - D_0$ = Data I/O port
$Y_7 - Y_0$ = Y I/O port
NA = Not applicable, output is not a function of the specified input combinations.

APPLICATIONS



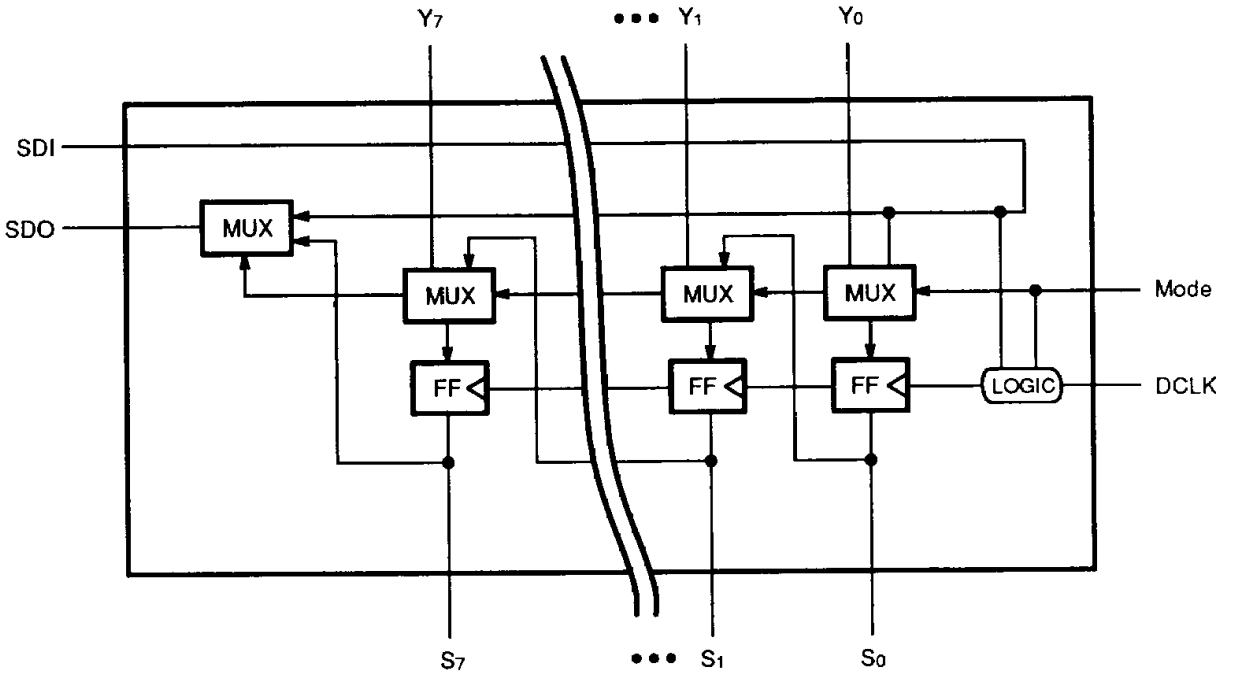
Am29C818A-Based WCS Application

APPLICATIONS (Continued)



WCS Application without Am29C818As

SHADOW REGISTER



09323-006A

An Introduction to Serial Shadow Register (SSR) Diagnostics

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware-related failures in a system. This capability must be able to both observe intermediate test points and control intermediate signals – address, data, control and status – to exercise all portions of the system under test. These two capabilities – observability and controllability – provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinatorial and Sequential Networks

The problem of testing a combinatorial logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set at test vectors will discover.

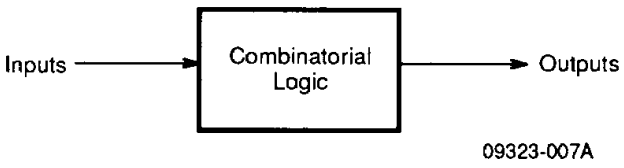


Figure 1. Combinatorial Logic Network

A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

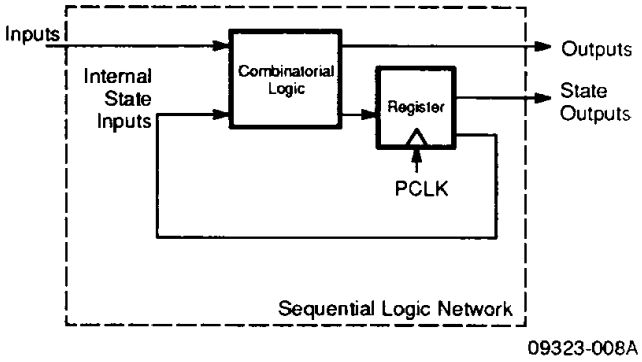


Figure 2. Sequential Network

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinatorial network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.

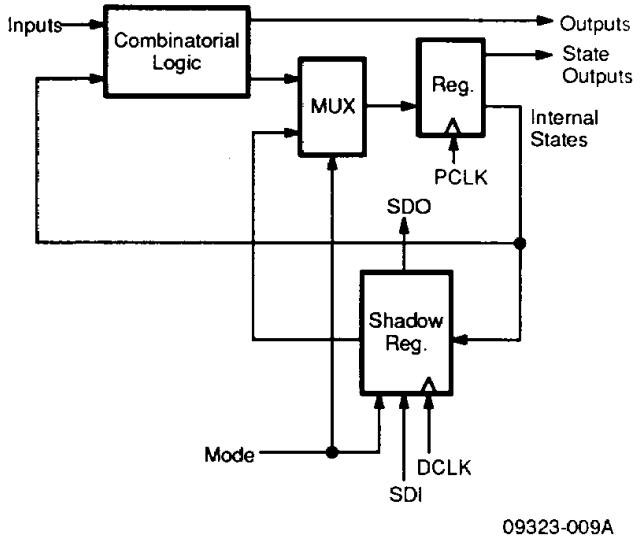


Figure 3. SSR Diagnostics Diagram

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with

PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinatorial networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

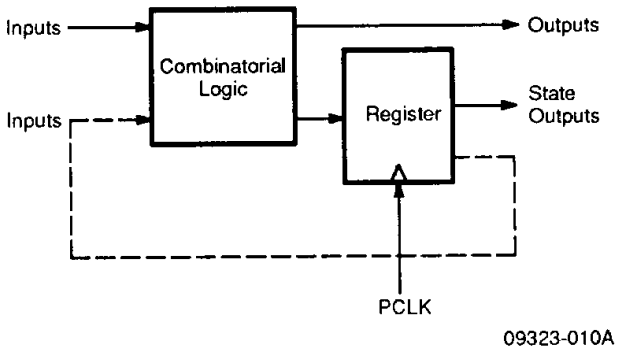


Figure 4. SSR Diagnostics Logical Path

A Typical Computer Architecture with SSR Diagnostics

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29C818A.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feedback paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29C818A's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

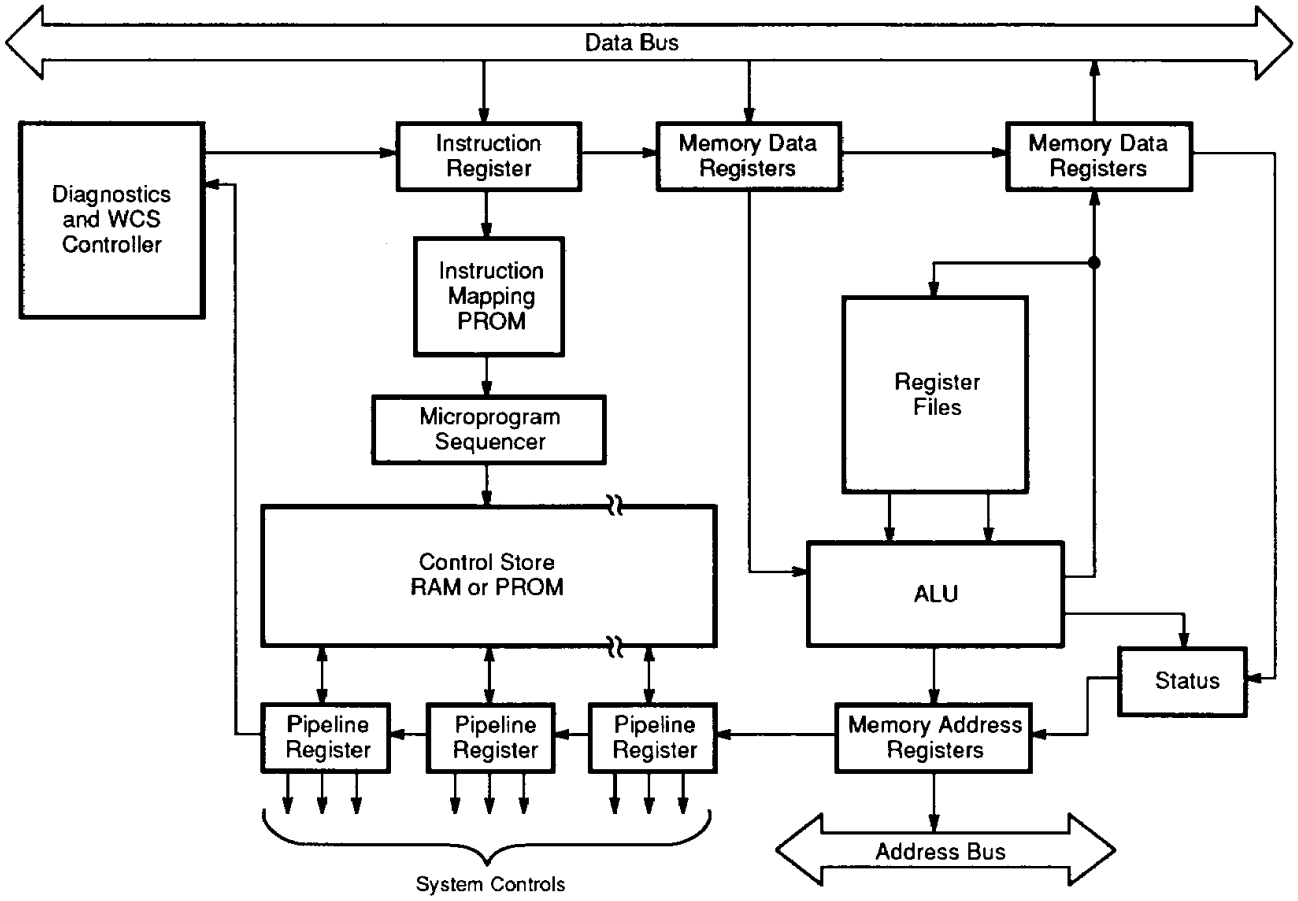


Figure 5. Typical System Configuration

Use of the Am29C818A Pipeline Register in Writable Control Store (WCS) Designs

The Am29C818A SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7, additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29C818A supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29C818A. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

Conclusion

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinatorial network. This provides a method for pin-pointing digital system hardware failures in a systematic and well-understood fashion.

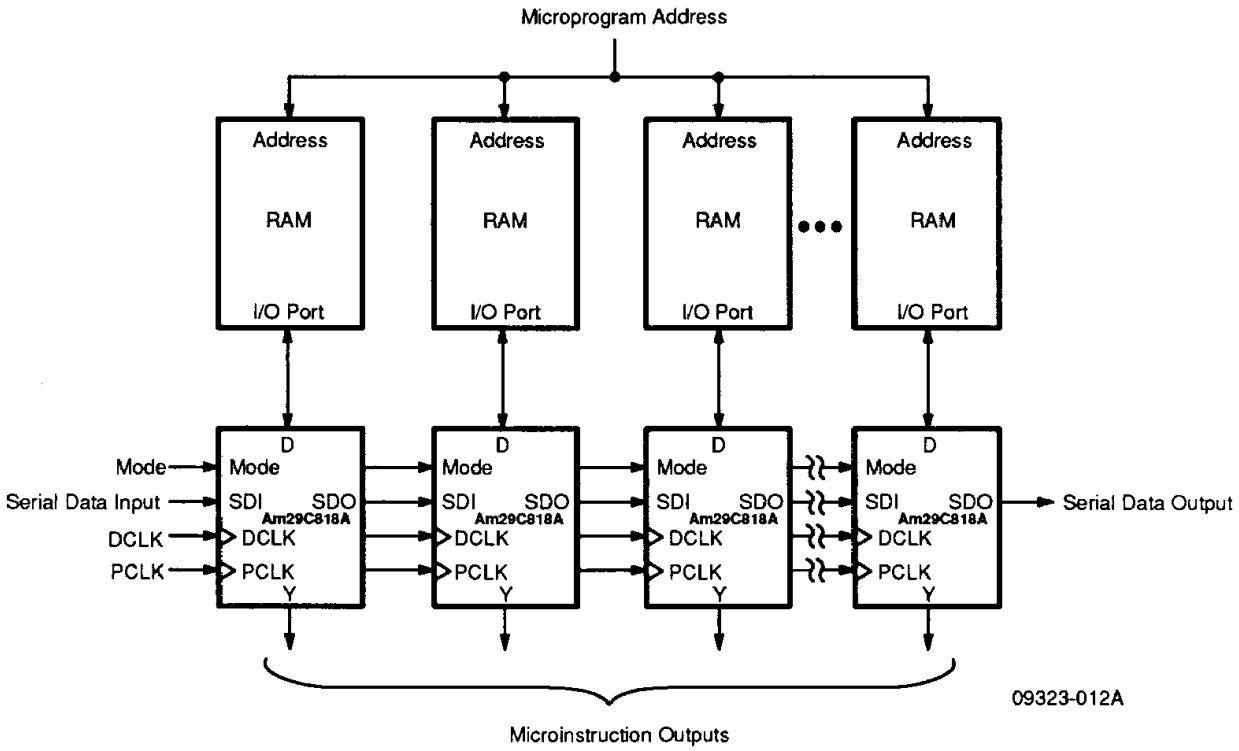


Figure 6. Am29C818A-Based WCS Application

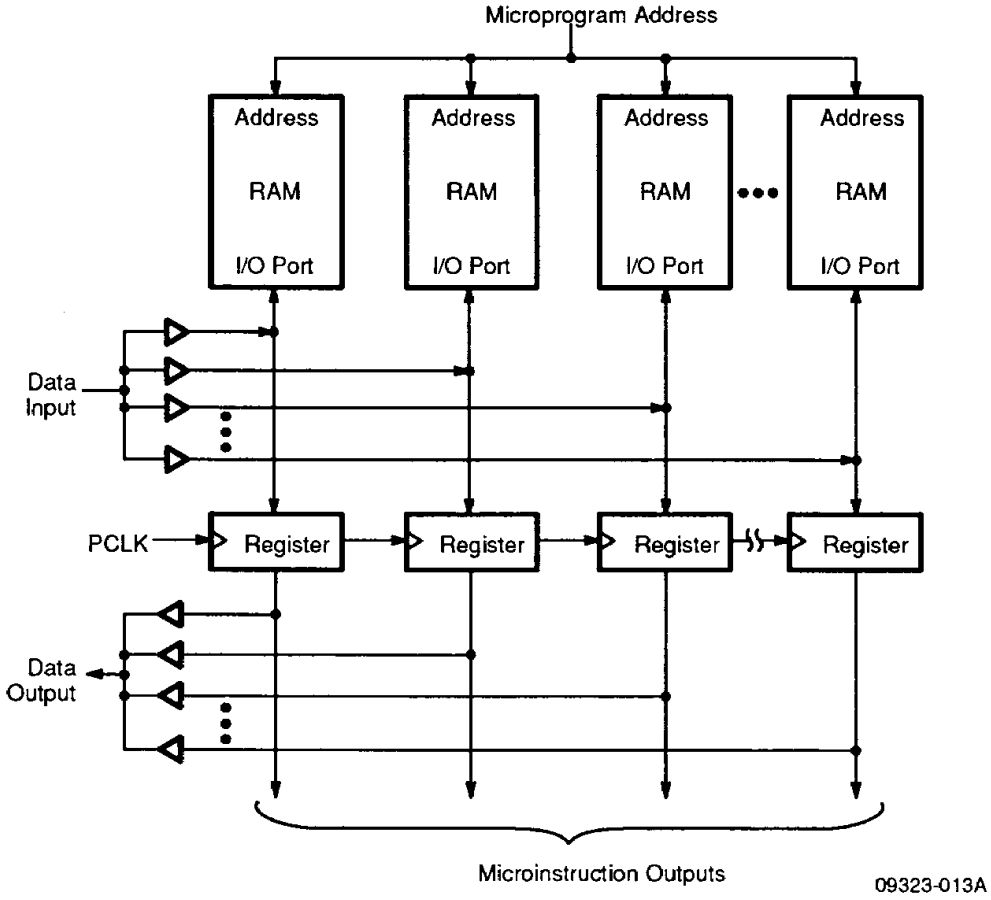


Figure 7. WCS Application without Am29C818As

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential Continuous	–0.5 V to +7.0 V
DC Output Voltage	–0.5 V to +6.0 V
DC Input Voltage	–0.5 V to +6.0 V
DC Output Diode Current:	
Into Output	+50 mA
Out of Output	–50 mA
DC Input Diode Current:	
Into Input	+20 mA
Out of Input	–20 mA
DC Output Current per Pin:	
Into Output	+48 mA (2 x I_{OL})
Out of Output	–30 mA (2 x I_{OH})
Total DC Ground Current ($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)	
Total DC V_{CC} Current ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)	

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Temperature (T_A)	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	Y_0–Y_7	I_{OH} = –15 mA	2.4		V
			D_0–D_7, SDO	I_{OH} = –3 mA	2.4		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	Y_0–Y_7	I_{OL}=24 mA		0.5	V
			D_0–D_7, SDO	I_{OL} = 8.0 mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)			2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = –18 mA				–1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = GND				–10	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V				10	µA
I_{OZH}	Output Off-State Current (High-Impedance)	V_{CC} = 5.5 V	V_O = V_{CC}			20	µA
I_{OZL}		V_{CC} = 5.5 V	V_O = GND			–20	µA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		Y_0–Y_7	–60		mA
				D_0–D_7, SDO	–20		
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	µA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Dx, Yx		1.5	mA/Bit
				$\overline{OEY}$,DCLK, SDI, MODE, PCLK		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)				400	µA/ MHz/ Bit

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

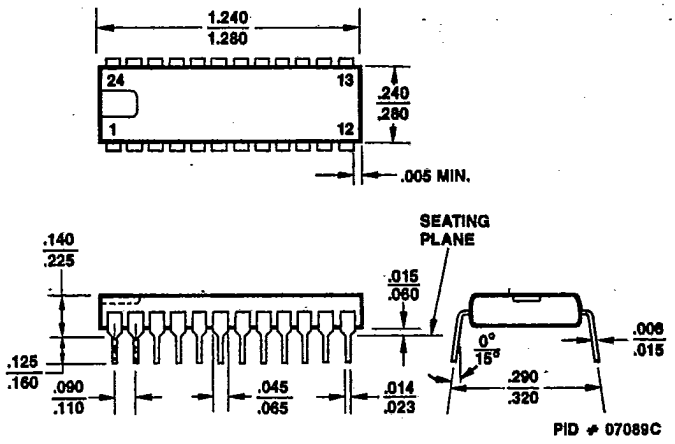
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH} & t_{PHL}	PCLK → Yx	C_L = 50 pF $R_1 = R_2$ = 500 Ω See Test Output Load Conditions		12		14	ns
	MODE → SDO			12		14	ns
	SDI → SDO			12		14	ns
	DCLK → SDO			16		18	ns
t_S	Dx → PCLK		4		6		ns
	MODE → PCLK		6		8		ns
	Yx → DCLK		6		8		ns
	MODE → DCLK		6		8		ns
	SDI → DCLK		6		8		ns
	DCLK → PCLK		20		20		ns
	PCLK → DCLK		20		20		ns
t_H	Dx → PCLK		2		2		ns
	MODE → PCLK		2		2		ns
	Yx → DCLK		2		2		ns
	MODE → DCLK		2		2		ns
	SDI → DCLK		2		2		ns
t_{LZ}	$\overline{OEY}$ → Yx			12		14	ns
	DCLK → Dx			14		16	ns
t_{HZ}	$\overline{OEY}$ → Yx			12		14	ns
	DCLK → Dx			14		16	ns
t_{ZL}	$\overline{OEY}$ → Yx			14		16	ns
	DCLK → Dx			18		20	ns
t_{ZH}	$\overline{OEY}$ → Yx			14		16	ns
	DCLK → Dx			18		20	ns
t_{PW}	PCLK (HIGH and LOW)		8		10		ns
	DCLK (HIGH and LOW)		8		10		ns

PACKAGE OUTLINES*

T-90-20

PD3024



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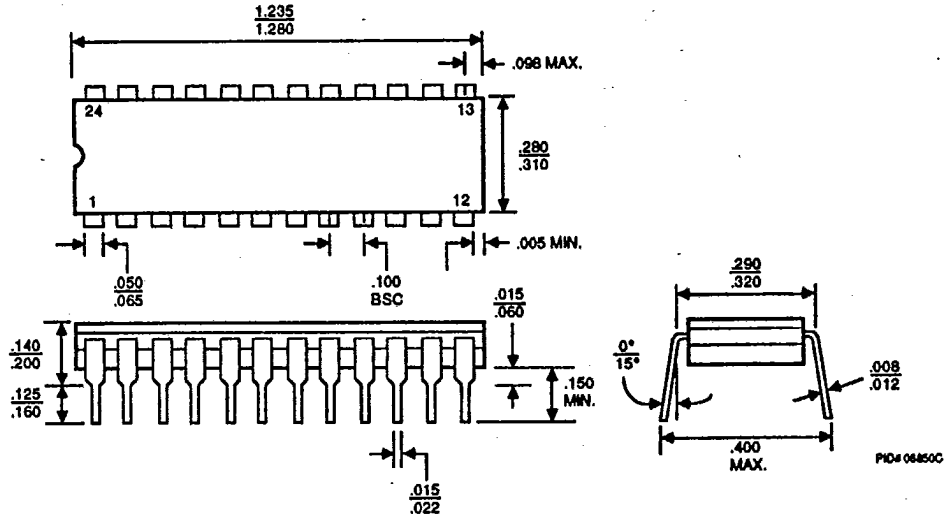
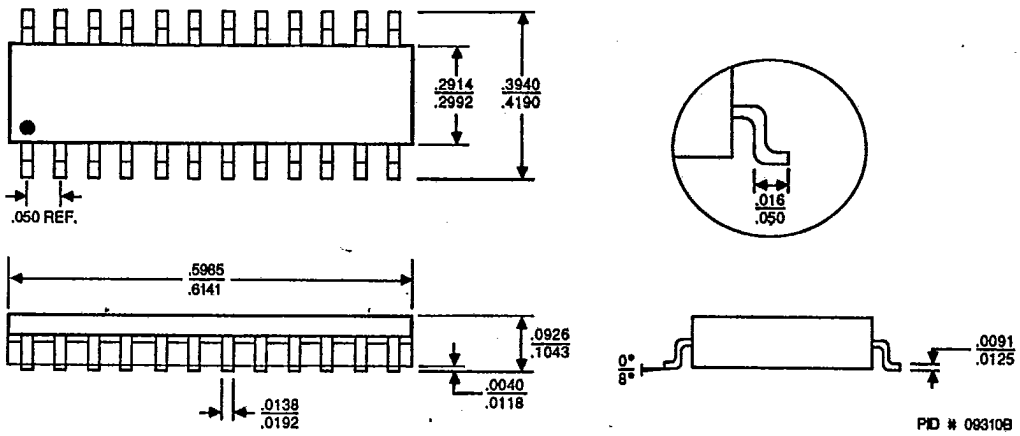


*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



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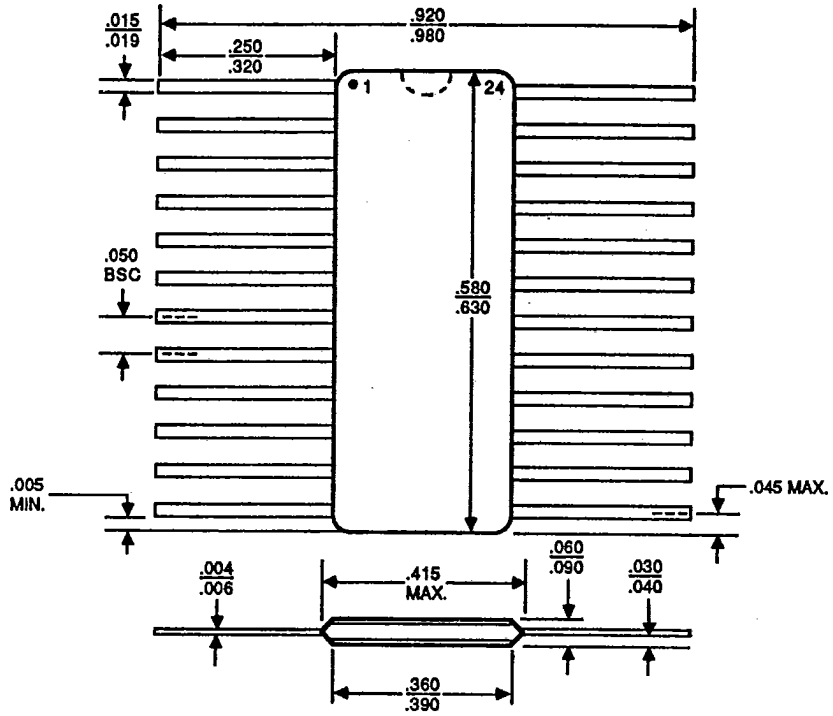

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PACKAGE OUTLINES (Cont'd.)

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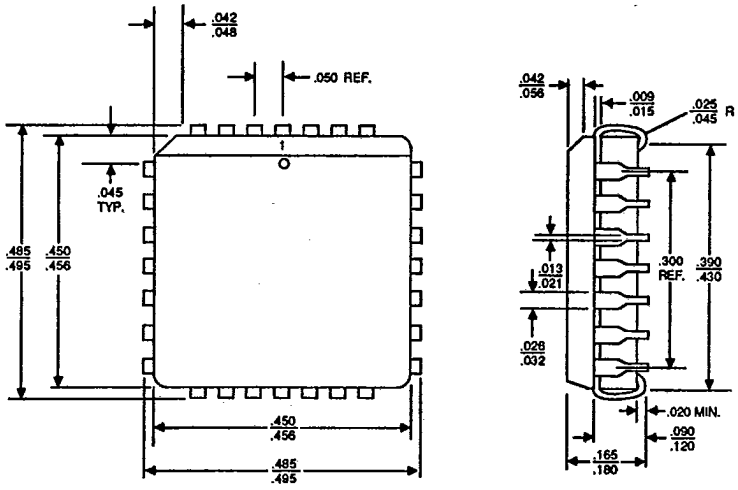
PL 028



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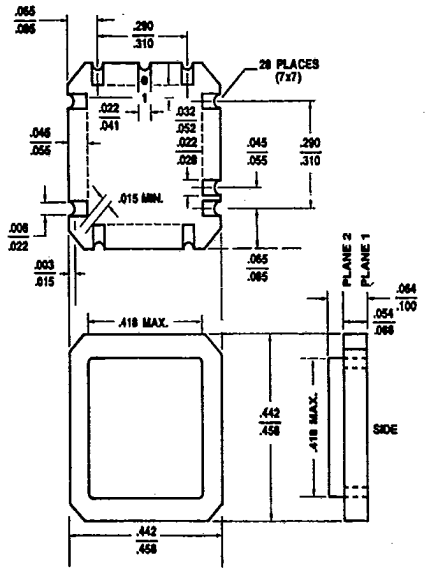

PID # 06595D

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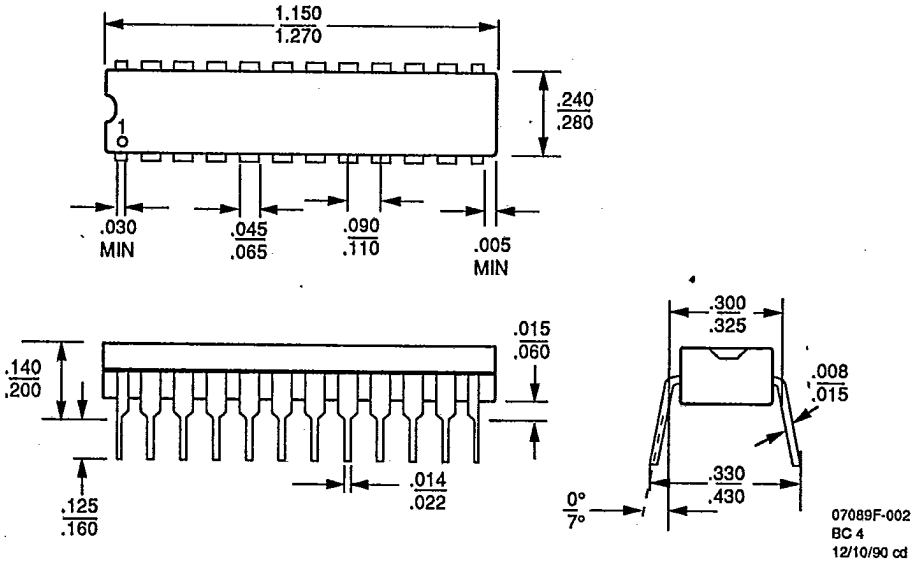
T-90-20

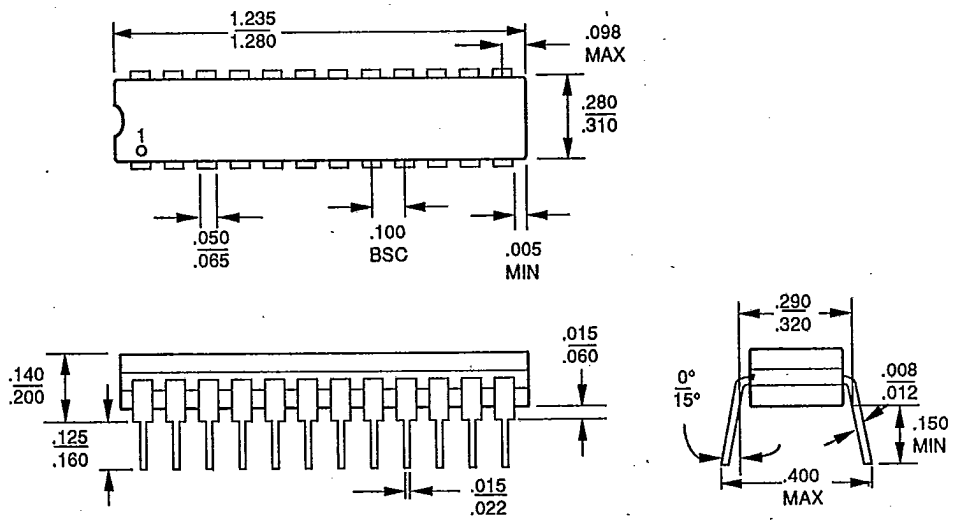
PD3024
24-Pin 300-mil Plastic SKINNYDIP



Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

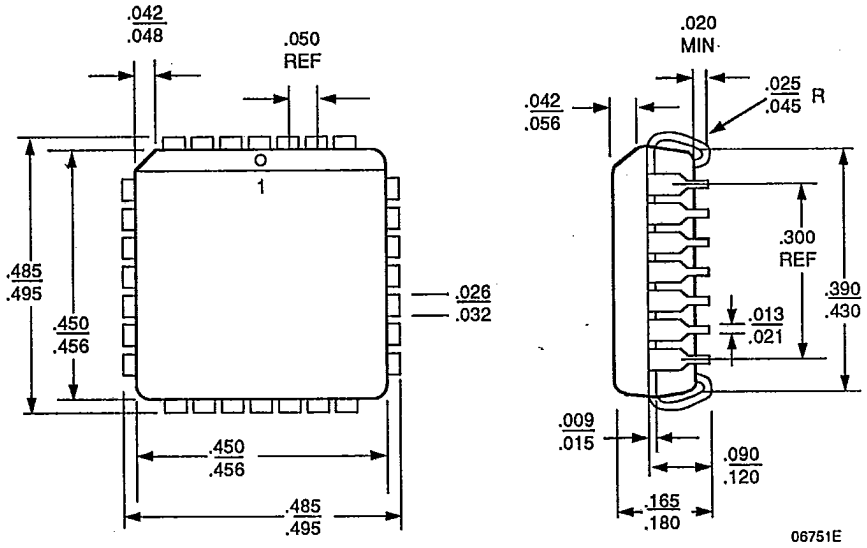
T-90-20

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



06850C

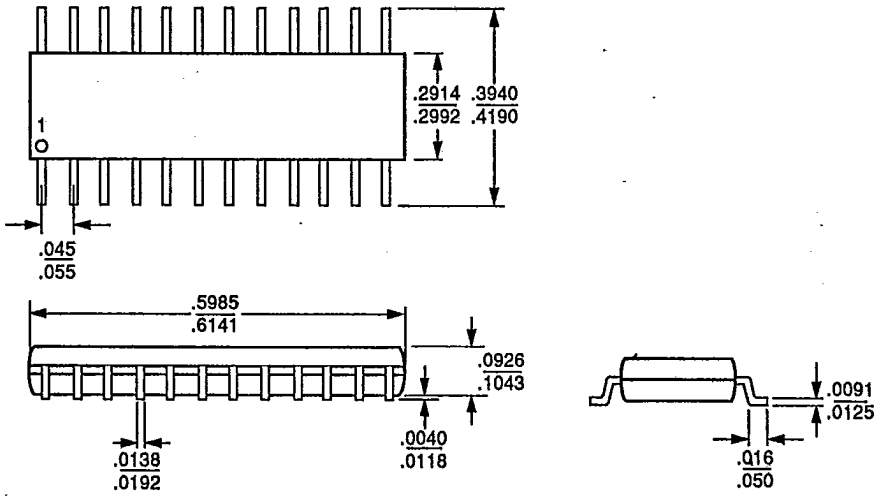
PL 028
28-Pin Plastic Leaded Chip Carrier



06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20



09310B