Integrated Digital CCIR-601 YCrCb to PAL/NTSC Video Encoder

ADV7175/ADV7176

FEATURES

CCIR-601 YCrCb to PAL/NTSC Video Encoder
Single 27 MHz Clock Required (×2 Oversampling)
Pixel Port Supports:
CCIR-656 4:2:2 8-Bit Parallel Input Format
4:2:2 16-Bit Parallel Input Format
SMPTE 170M NTSC Compatible Composite Video Output
CCIR624/CCIR601 PAL Compatible Composite Video Output
SCART/PeriTV Support
YUV Output Mode
Simultaneous Composite and S-VHS Y/C or RGB YUV Video Outputs
Programmable Luma Filters (Low-Pass/Notch)
Square Pixel Support (Slave Mode)
Allows Subcarrier Phase Locking with External Video Source
10-Bit DAC Resolution for Encoded Video Channels
8-Bit DAC Resolution for RGB Output
YUV Interpolation for Accurate Subcarrier Construction
Programmable Subcarrier Frequency and Phase
Programmable LUMA Delay
Color Signal Control/Burst Signal Control
Interlaced/Noninterlaced Operation
Complete On-Chip Video Timing Generator
Master/Slave Operation Supported
Master Mode Timing Programmability
Macrovision Antitaping Facility Rev 6.1/7.x (ADV7175 Only)*
Close Captioning Support
Teletext Support (Passthrough Mode)
On-Board Color Bar Generation
On-Board Voltage Reference
2-Wire Serial MPU Interface (I^2C Compatible)
+5 V CMOS Monolithic Construction
44-Pin PQFP Thermally Enhanced Package

APPLICATIONS

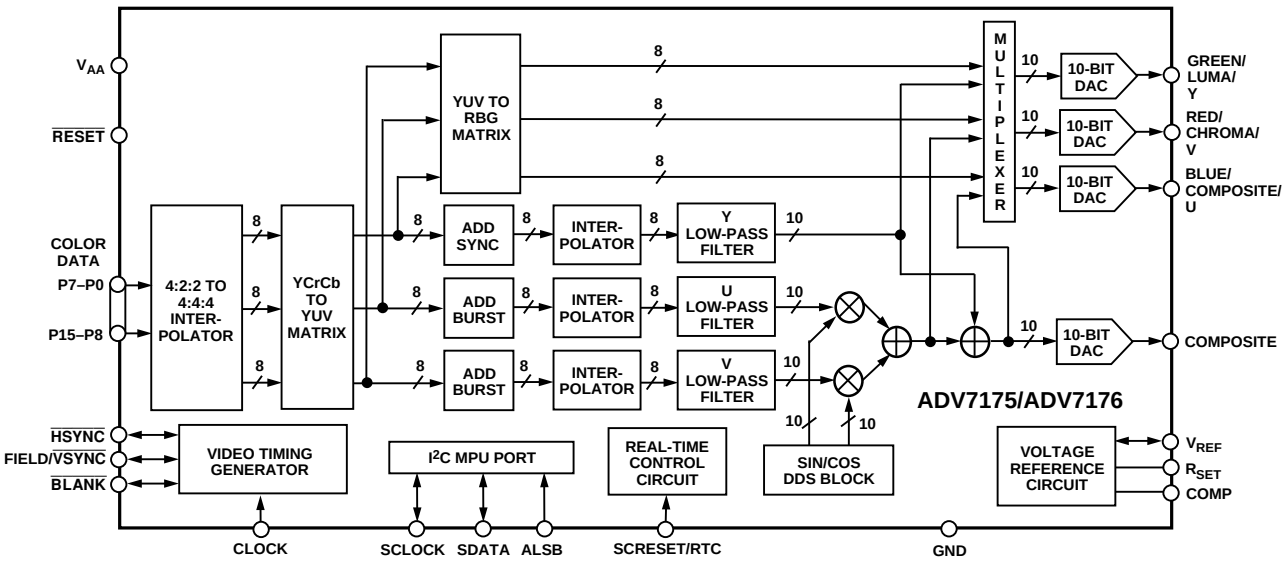
MPEG-1 and MPEG-2 Video
DVD
Digital Satellite/Cable Systems (Set Top Boxes/IRDs)
Video Games
CD Video/Karaoke
Professional Studio Quality
PC Video/Multimedia

GENERAL DESCRIPTION

The ADV7175/ADV7176 is an integrated digital video encoder that converts Digital CCIR-601 4:2:2 component video data into a standard analog baseband television signal compatible with world wide standards NTSC, PAL B/D/G/H/I, PAL M or PAL N. In addition to the composite output signal, there is the facility to output S-VHS Y/C video, YUV or RGB video. The Y/C, YUV or RGB format is simultaneously available at the analog outputs with the composite video signal. Each analog output generates a standard video-level signal into a doubly terminated 75 Ω load.

(Continued on page 6)

FUNCTIONAL BLOCK DIAGRAM



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REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

ADV7175/ADV7176–SPECIFICATIONS (V_{AA} = +5 V[1], V_{REF} = 1.235 V R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Model / Parameter	Conditions[1]	ADV7175/ADV7176 Min	Typ	Max	Units
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Floating-State Leakage Current				10	μA
Floating-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]		33	34.7	37	mA
Output Current[4]			8		mA
Full-Scale DAC Output			182.5		IRE
LSB Size			33.9		μA
DAC-to-DAC Matching			2	5	%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			15		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.112	1.235	1.359	V
POWER REQUIREMENTS[5]					
V_{AA}			5		V
I_{DAC}[6]			140	155	mA
I_{CCT}[7]			110	150	mA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.02	0.5	%/%
DYNAMIC PERFORMANCE[8]					
Luma Bandwidth[9] (Low-Pass Filter)	NTSC Mode				
Stopband Cutoff	>50 dB Attenuation			7.5	MHz
Pass Band Cutoff	<0.06 dB Attenuation			2.3	MHz
Chroma Bandwidth	NTSC Mode				
Stopband Cutoff	<40 dB Attenuation			3.6	MHz
Pass Band Cutoff	>0.1 dB Attenuation			1.0	MHz
Luma Bandwidth[9] (Low-Pass Filter)	PAL MODE				
Stopband Cutoff	>50 dB Attenuation			8.0	MHz
Pass Band Cutoff	<0.06 dB Attenuation			3.4	MHz
Chroma Bandwidth	PAL MODE				
Stopband Cutoff	<40 dB Attenuation			4.0	MHz
Pass Band Cutoff	>0.1 dB Attenuation			1.3	MHz
Differential Gain			0.8		%
Differential Phase			0.8		Degree
Differential Gain	Lower Power Mode		7		%
Differential Phase	Lower Power Mode		2		Degree
SNR	RMS		60		dB rms
SNR	Peak Periodic		56		dB p-p
Hue Accuracy			1.0		Degree
Color Saturation Accuracy			1.0		%

NOTES
[1]±5% for all versions.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Full drive into 37.5 Ω load.
[4]Minimum drive with buffered/scaled output load.
[5]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 100°C.
[6]I_{DAC} is the total current to drive all four DACs. Turning off one DAC reduces I_{DAC} correspondingly.
[7]I_{CCT} (Circuit Currrent) is the continuous currrent required to drive the device.
[8]Guaranteed by characterization.
[9]These specifications are for the low-pass filter only. For the other internal filters please see Figure 3.
Specifications subject to change without notice.

AC CHARACTERISTICS[1]

Parameter	Min	Typ	Max	Units	Condition
Chroma Nonlinear Gain		0.6		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		1		±°	NTSC
Chroma Nonlinear Phase		1.7		±°	PAL
Chroma/Luma Intermod		0.2		±%	Referenced to 714 mV (NTSC)
Chroma/Luma Intermod		0.4		±%	Referenced to 700 mV (PAL)
Chroma/Luma Gain Ineq		0.6		±%	
Chroma/Luma Delay Ineq		1		ns	
Luminance Nonlinearity		0.8		±%	
Chroma AM Noise		60		dB	
Chroma PM Noise		59		dB	

TIMING–SPECIFICATIONS[2] (V_{AA} = +5 V[3], V_{REF} = 1.235 V R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[4] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[1]					
SCLOCK Frequency	0		100	kHz	
SCLOCK High Pulse Width, t_1	4.0			µs	
SCLOCK Low Pulse Width, t_2	4.7			µs	
Hold Time (Start Condition), t_3	4.0			µs	After this period the first clock pulse is generated
Setup Time (Start Condition), t_4	4.7			µs	Relevant for repeated start condition.
Data Setup Time, t_5	250			ns	
SDATA, SCLOCK Rise Time, t_6			1	µs	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	4.7			µs	
ANALOG OUTPUTS[1, 5]					
Analog Output Delay		5		ns	
DAC Analog Output Skew		0		ns	
CLOCK CONTROL AND PIXEL PORT[6]					
F_{CLOCK}	24.52	27	29.5	MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	3.5			ns	
Data Hold Time t_{12}	1			ns	
Control Setup Time t_{11}	4			ns	
Control Hold Time t_{12}	2			ns	
Digital Output Access Time t_{13}			24	ns	
Digital Output Hold Time t_{14}		6		ns	
Pipeline Delay t_{15}		37		Clock Cycles	

NOTES

[1]Guaranteed by characterization.

[2]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog Output Load ≤ 3 pF.

[3]±5% for all versions.

[4]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following inputs:

Pixel Inputs: P15–P0

Pixel Controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$

Clock Input: CLOCK

Specifications subject to change without notice.

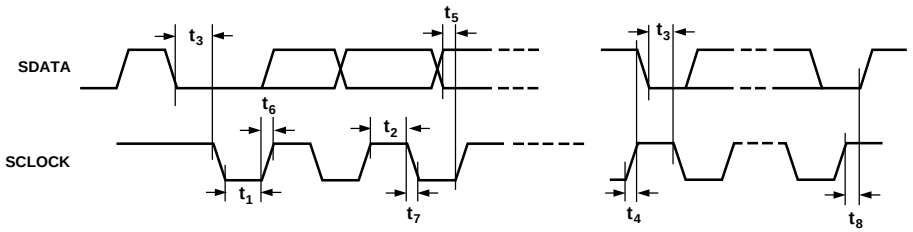


Figure 1. MPU Port Timing Diagram

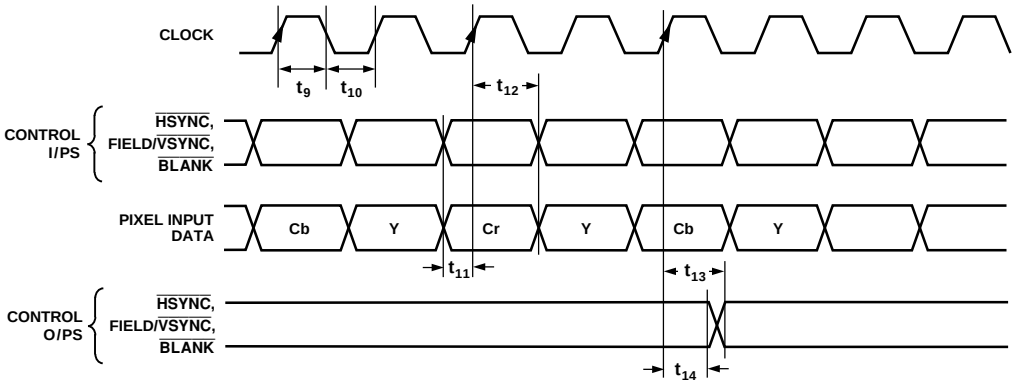


Figure 2. Pixel and Control Data Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Input Pin . GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +260°C
Analog Outputs to GND[2] . . . . . GND –0.5 to V_{AA}

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADV7175KS	0°C to +70°C	S-44
ADV7176KS	0°C to +70°C	S-44

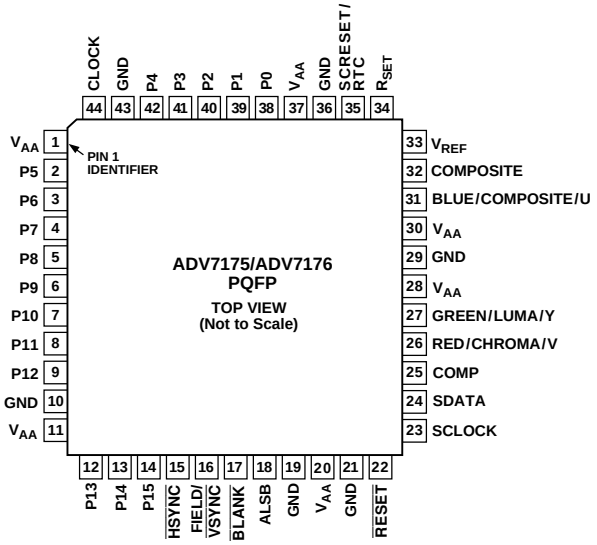
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7175/ADV7176 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

Mnemonic	Input/Output	Function
P15-P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) or 16-Bit YCrCb Pixel Port (P15–P0). P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference Clock for proper operation. Alternatively a 24.52 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 & 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) Sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or accept (Slave Mode) these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is logic level "0." This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR22 and MR21 of Mode Register 2. It can be configured as a subcarrier reset pin, in which case a high to low transition on this pin will reset the subcarrier to field 0. Alternatively it may be configured as a Real Time Control (RTC) input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.2 V).
R_{SET}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the video signals.
COMP	O	Compensation Pin. Connect a 0.1 µF capacitor from COMP to V_{AA}.
COMPOSITE	O	PAL/NTSC Composite Video Output. Full-Scale Output is 180IRE (1286 mV) for NTSC and 1300 mV for PAL.
RED/CHROMA/V	O	RED/S-VHS C/V Analog Output.
GREEN/LUMA/Y	O	GREEN/S-VHS Y/Y Analog Output.
BLUE/COMPOSITE/U	O	BLUE/Composite/U Analog Output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal set up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on chip timing generator and sets the ADV7175/ADV7176 into default mode. This is NTSC operation, Timing Slave Mode 0, 8-bit operation, 2 × composite & S VHS out.
V_{AA}	P	+5 V Supply.
GND	G	Ground Pin.

PIN CONFIGURATION



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The ADV7175/ADV7176 also supports both a PAL and NTSC square pixel mode in slave mode.

The video encoder accepts an 8-bit parallel pixel data stream in CCIR-656 format or a 16-bit parallel data stream. This 4:2:2 data stream is interpolated into 4:4:4 component video (YUV). The YUV video is interpolated to two times the pixel rate. The color-difference components (UV) are quadrature modulated using a subcarrier frequency generated by an on-chip synthesizer (also running at two times the pixel rate). The two times pixel rate sampling allows more accurate generation of the subcarrier because frequency and phase errors are reduced by the higher sampling rate. The ADV7175/ADV7176 also offers the option to output the YUV information directly.

The luminance and chrominance components are digitally combined and the resulting composite signal is output via a 10-bit DAC. Three additional 10-/8-bit DACs are provided to output S-VHS Y/C Video (10 bits), YUV or RGB Video (8 bits).

The output video frames are synchronized with the incoming data timing reference codes. Optionally the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ & FIELD timing signals. These timing signals can be adjusted to change pulse width and position while the part is in the master mode. The encoder requires a single two times pixel rate (27 MHz) clock for standard operation. Alternatively the encoder requires 24.54 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal clocks are generated on-chip. The ADV7175/ADV7176 modes are set up over a two wire serial bidirectional port (I^2C Compatible) with two slave addresses.

Additionally, the ADV7175/ADV7176 allows a subcarrier phase lock with an external video source and has a color bar generator on-board.

Functionally the ADV7175 and ADV7176 are the same with the exception that the ADV7175 can output the Macrovision (Revision 6.1/7.x) anticopy algorithm.

The ADV7175/ADV7176 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7175/ADV7176 is packaged in a 44-pin thermally enhanced PQFP package (patent pending).

The ADV7175/ADV7176 is protected by U.S. Patent Numbers 5,343,196 and 5,442,355 and other intellectual property rights.

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, M, N and NTSC M, N modes, YCrCb 4:2:2 data is input via the CCIR-656 compatible pixel port at a 13.5 MHz data rate. The pixel data is de-multiplexed to form three data paths. Y has a range of 16 to 235, Cr and Cb have a range of 128 ± 112. The ADV7175/ADV7176 supports PAL (B, D, G, H, I, N, M) and NTSC (with and without Pedestal) standards. The appropriate SYNC, BLANK and burst levels are added to the YCrCb data. Macrovision antitaping (ADV7175 only) and close-captioning levels are also added to Y and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate subcarrier sine/cosine phases and added together to make up the chrominance signal. The luma (Y) signal can be delayed 1-3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate SYNC and BLANK levels. The RGB data is in sychronization with the composite video output. Alternatively analog YUV data can be generated instead of RGB.

The four 10-bit DACs can be used to output:

1. 10-bit composite video + 8-bit RGB video.
2. 10-bit composite video + 8-bit YUV video.
3. Two 10-bit composite video signals + 10-bit LUMA & CHROMA (Y/C) signals.

Alternatively, each DAC can be individually powered off if not required.

All possible video outputs are illustrated in Appendix 3, 4 and 5.

INTERNAL FILTER RESPONSE

The Y filter supports several different frequency responses including two 4.5/5.0 MHz low-pass and PAL/NTSC subcarrier notch responses. The U and V filters have a 0.6/1 0.3 MHz low-pass response.

These filter characteristics are illustrated in Figures 3 to 11.

FILTER SELECTION			PASSBAND CUT OFF (MHz)	PASSBAND RIPPLE (dB)	STOPBAND CUT OFF (MHz)	STOPBAND ATTENUATION (dB)	F_{3dB}
	MR04	MR03					
NTSC	0	0	2.3	0.026	7.5	>50	4.2
PAL	0	0	3.4	0.098	8.0	>51.3	5.0
NTSC	0	1	1.0	0.085	3.57	>27.6	2.1
PAL	0	1	1.4	0.107	4.43	>29.3	2.7
NTSC/PAL	1	0	4.0	0.150	8.0	>40	5.65
NTSC	1	1	2.3	0.054	7.5	>54	4.2
PAL	1	1	3.4	0.106	8.0	>50.3	5.0

Figure 3. Y Filter Specifications

FILTER SELECTION	PASSBAND CUT OFF (MHz)	PASSBAND RIPPLE (dB)	STOPBAND CUT OFF (MHz)	STOPBAND ATTENUATION (dB)	ATTENUATION @ 1.3MHz (dB)	F_{3dB}
NTSC	1.0	0.085	3.6	>40	0.3	2.05
PAL	1.3	0.04	4.0	>40	0.02	2.45

Figure 4. UV Filter Specifications

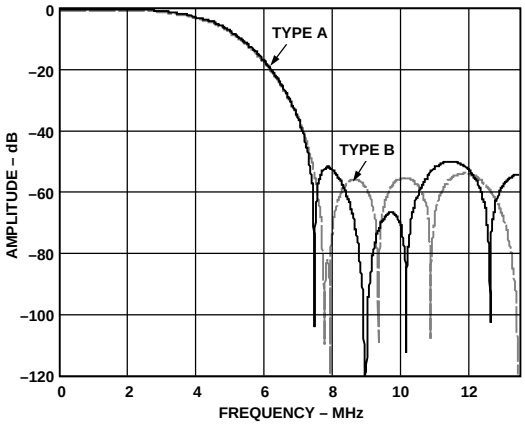


Figure 5. NTSC Low-Pass Filter

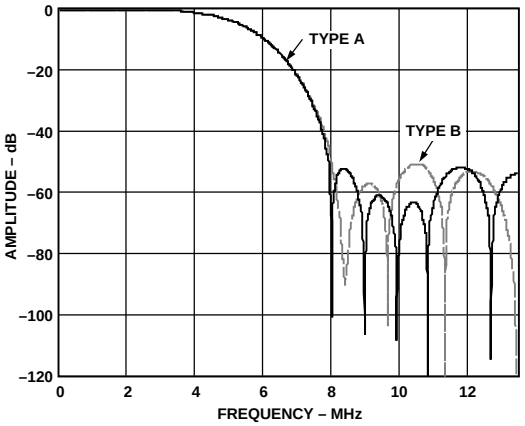


Figure 7. PAL Low-Pass Filter

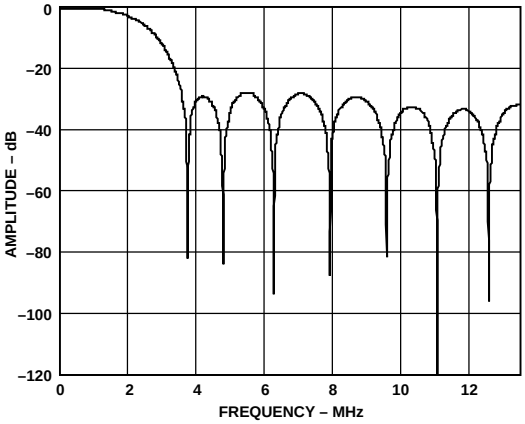


Figure 6. NTSC Notch Filter

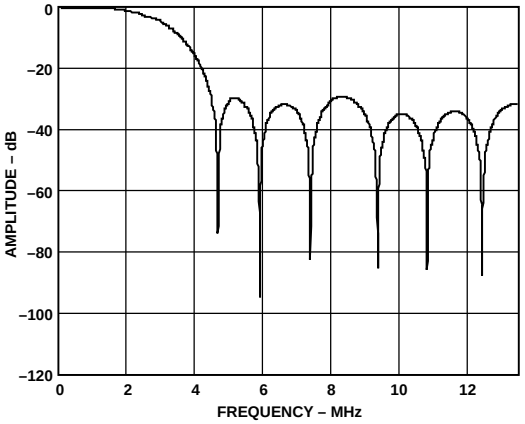


Figure 8. PAL Notch Filter

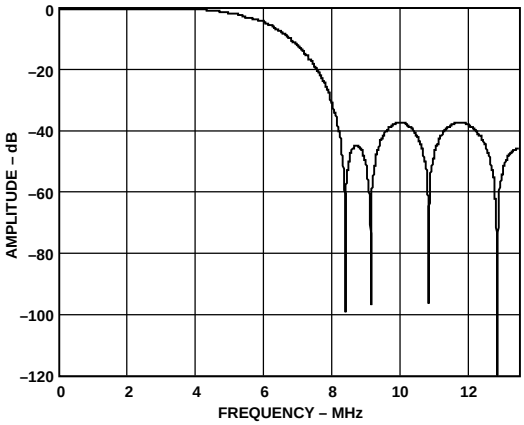


Figure 9. NTSC/PAL Extended Mode Filter

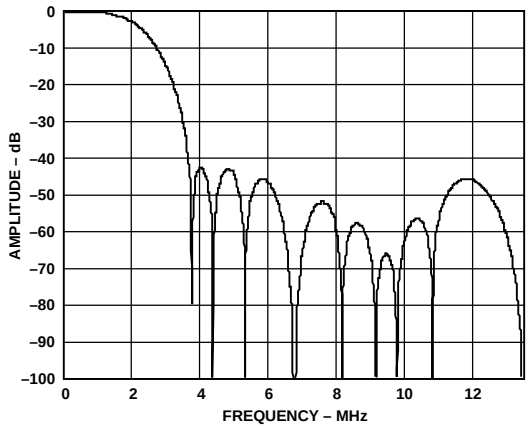


Figure 10. NTSC UV Filter

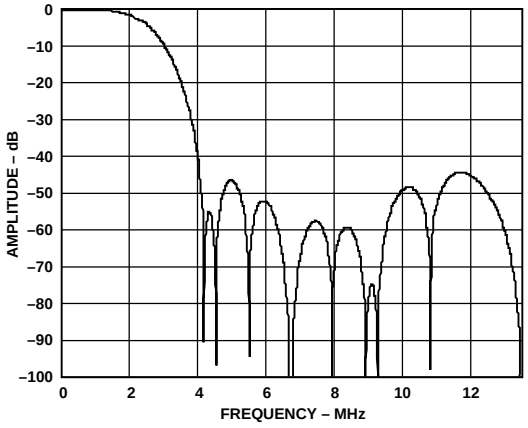


Figure 11. PAL UV Filter

COLOR BAR GENERATION
The ADV7175/ADV7176 can be configured to generate 75% amplitude, 75% saturation (75/7.5/75/7.5) for NTSC or 75% amplitude, 100% saturation (100/0/75/0) for PAL color bars. These are enabled by setting MR17 of Mode Register 1 to Logic "1."

SQUARE PIXEL MODE
The ADV7175/ADV7176 can be used to operate in square pixel mode. For NTSC operation an input clock of 24.54 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal filters scale accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL
The color information can be switched on and off the video output using Bit MR24 of Mode Register 2.

BURST SIGNAL CONTROL
The burst information can be switched on and off the video output using Bit MR25 of Mode Register 2.

NTSC PEDESTAL CONTROL
The pedestal information on both odd and even fields can be controlled on a line by line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the vertical blanking interval (Lines 10 to 25).

SUBCARRIER RESET
Together with the SCRESET/RTC PIN and Bits MR22 and MR21 of Mode Register 2, the ADV7175/ADV7176 can be used in subcarrier reset mode. The subcarrier will reset to field 0 at the start of the following field when a high to low transition occurs on this input pin.

REAL TIME CONTROL
Together with the SCRESET/RTC PIN and Bits MR22 and MR21 of Mode Register 2, the ADV7175/ADV7176 can be used to lock an external video source. The real time control mode allows the ADV7175/ADV7176 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs out a digital datastream in the RTC format (such as a Phillips SAA7110 video decoder), the part will automatically change to the compensated subcarrier frequency on a line by line basis. This digital datastream is 67 bits wide and the subcarrier is contained in bits 0 to 21. Each bit is 2 clock cycles long.

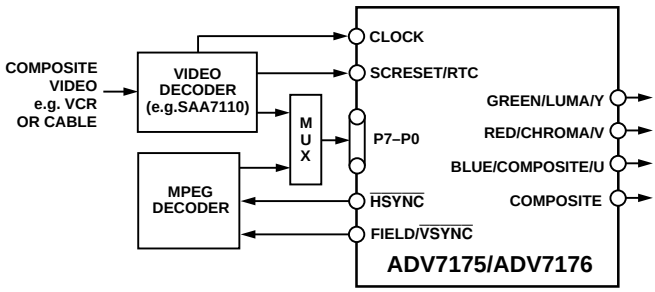


Figure 12. RTC Connections

PIXEL TIMING DESCRIPTION
The ADV7175/ADV7176 can operate in either 8-bit or 16-bit YCrCb Mode.

8-Bit YCrCb Mode
This default mode accepts multiplexed YCrCb inputs through the P7–P0 pixel inputs. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc. The Y, Cb and Cr data are input on a rising clock edge.

16-Bit YCrCb Mode
This mode accepts Y inputs through the P7-P0 pixel inputs and multiplexed CrCb inputs through the P15-P8 pixel inputs. The data is loaded on every second rising clock edge of CLOCK. The inputs follow the sequence Cb0, Y0 Cr0, Y1 Cb1, Y2, etc.

VIDEO TIMING DESCRIPTION
The ADV7175/ADV7176 is intended to interface to off the shelf MPEG1 and MPEG2 Decoders. As a consequence the ADV7175/ADV7176 accepts 4:2:2 YCrCb pixel data via a CCIR-656 pixel port and has several video timing modes of operation that allow it to be configured as either system master video timing generator or a slave to the system video timing generator. The ADV7175/ADV7176 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7175/ADV7176 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalization pulses are inserted where required.

(Continued on page 15)

Mode 0 (CCIR-656): Slave Option.
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7175/ADV7176 is controlled by the SAV (Start Active Video) and EAV (End Active Video) time codes in the pixel data.

All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 13. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ (if not used) pins should be tied high in this mode.

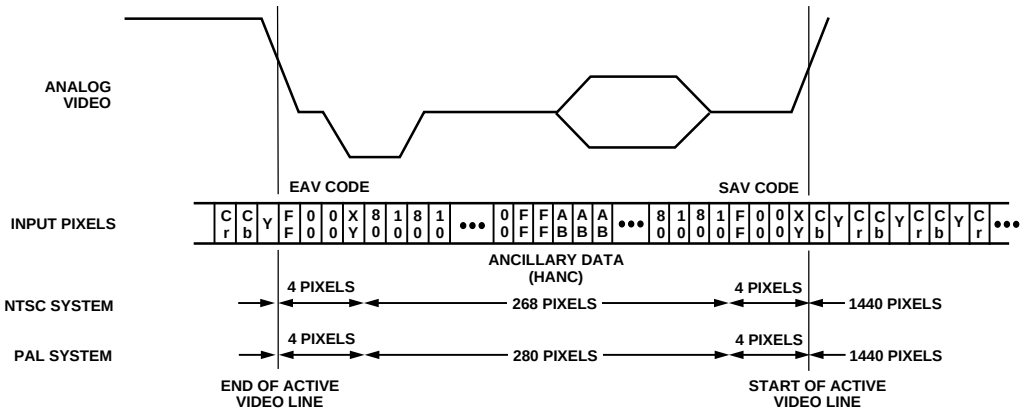


Figure 13. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR-656): Master Option.
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7175/ADV7176 generates H, V and F signals required for the SAV (start active video) and EAV (end active video) time codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 14 (NTSC) and Figure 15 (PAL). The H, V and F transitions relative to the video waveform are illustrated in Figure 16.

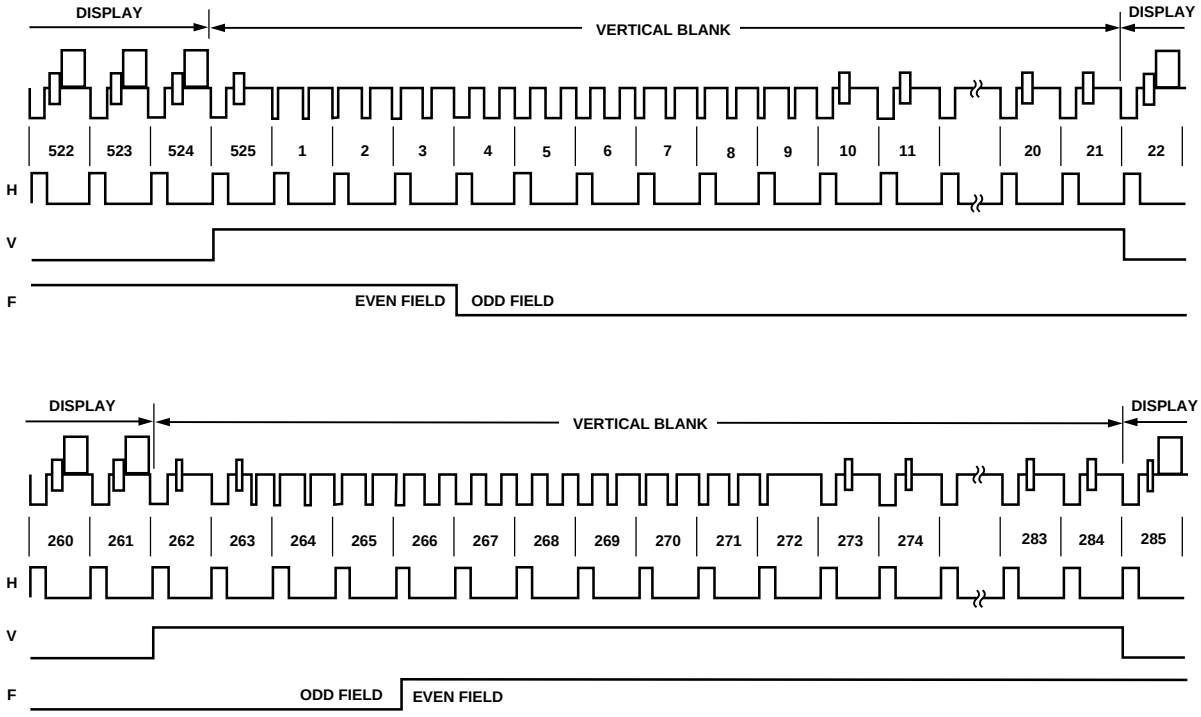


Figure 14. Timing Mode 0 (NTSC Master Mode)

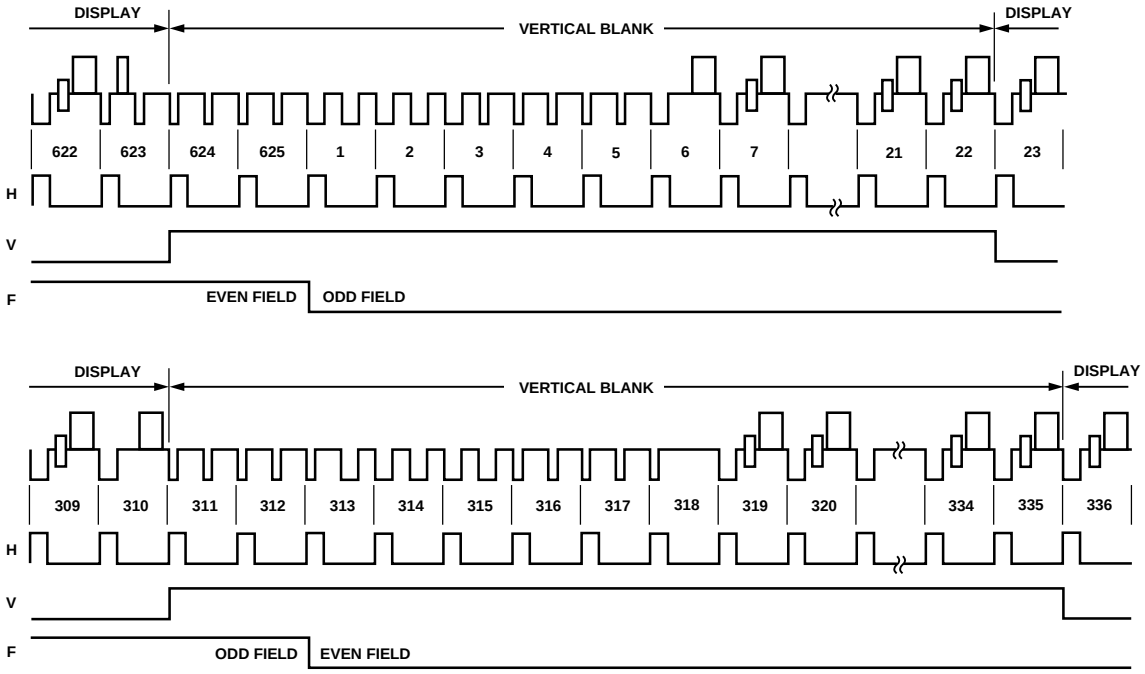


Figure 15. Timing Mode 0 (PAL Master Mode)

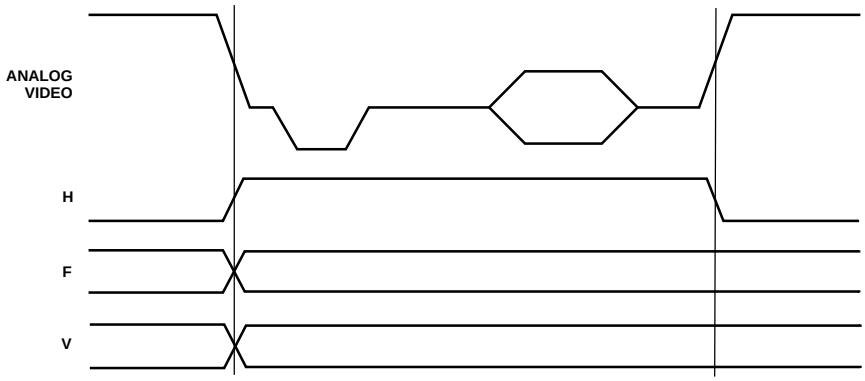


Figure 16. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD**.**
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7175/ADV7176 accepts horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7175/ADV7176 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL).

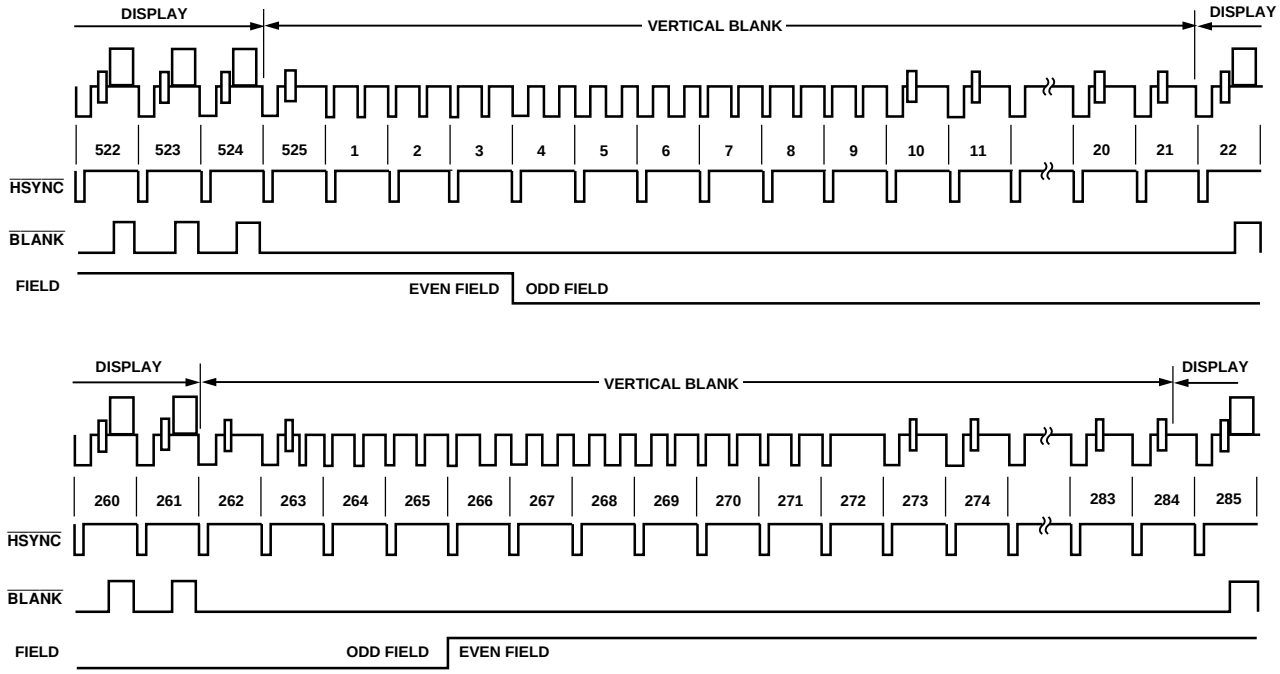


Figure 17. Timing Mode 1 (NTSC)

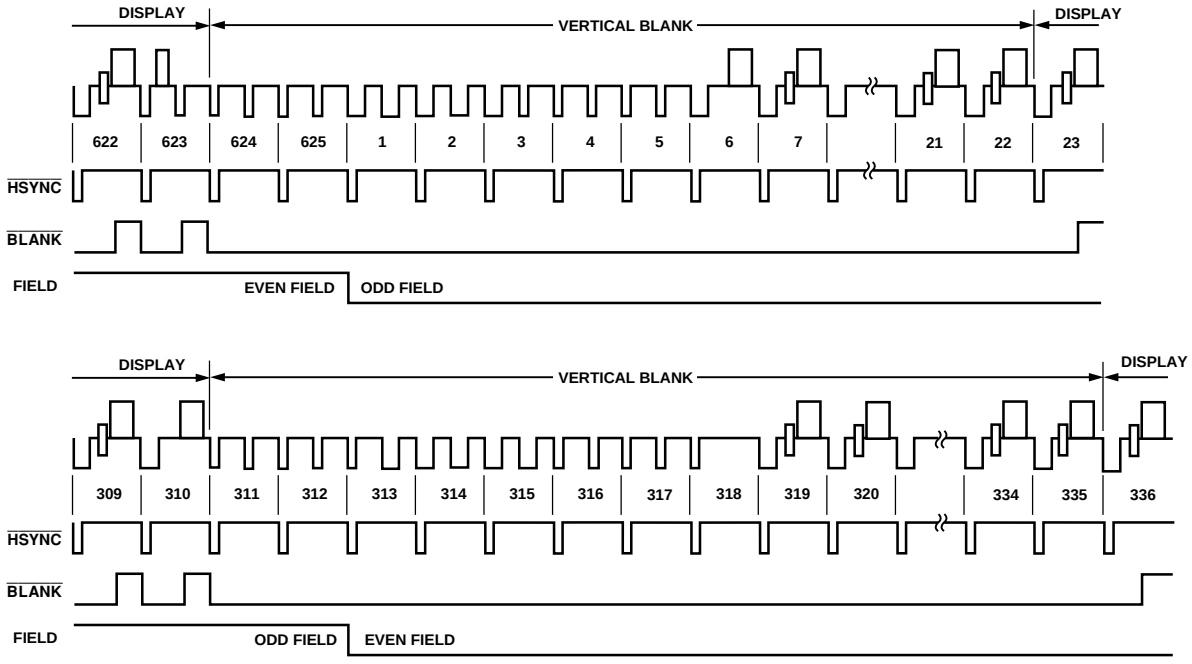


Figure 18. Timing Mode 1 (PAL)

Mode 1: Master Option. $\overline{\text{HSYNC}}$**,** $\overline{\text{BLANK}}$, FIELD**.**
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7175/ADV7176 can generate horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7175/ADV7176 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 17 (NTSC) and Figure 18 (PAL). Figure 19 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and FIELD for an odd or even field transition relative to the pixel data.

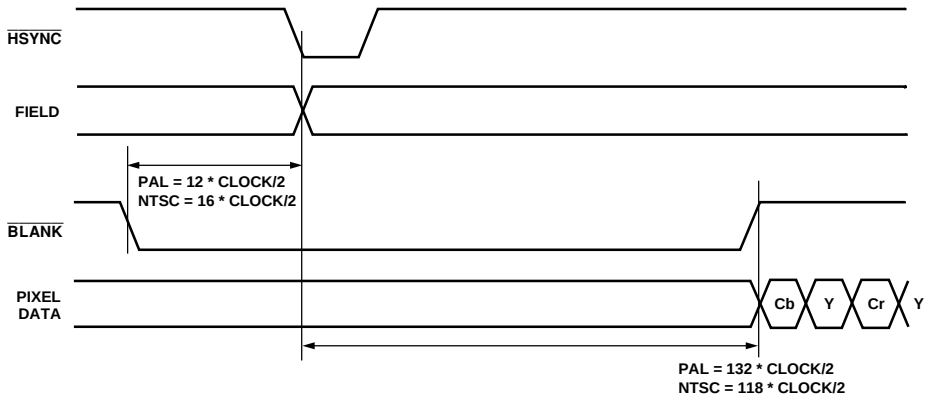


Figure 19. Timing Mode 1 Odd/Even Field Transitions

Mode 2: Slave Option. $\overline{\text{HSYNC}}$**,** $\overline{\text{VSYNC}}$**,** $\overline{\text{BLANK}}$.
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7175/ADV7176 accepts horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7175/ADV7176 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 20 (NTSC) and Figure 21 (PAL).

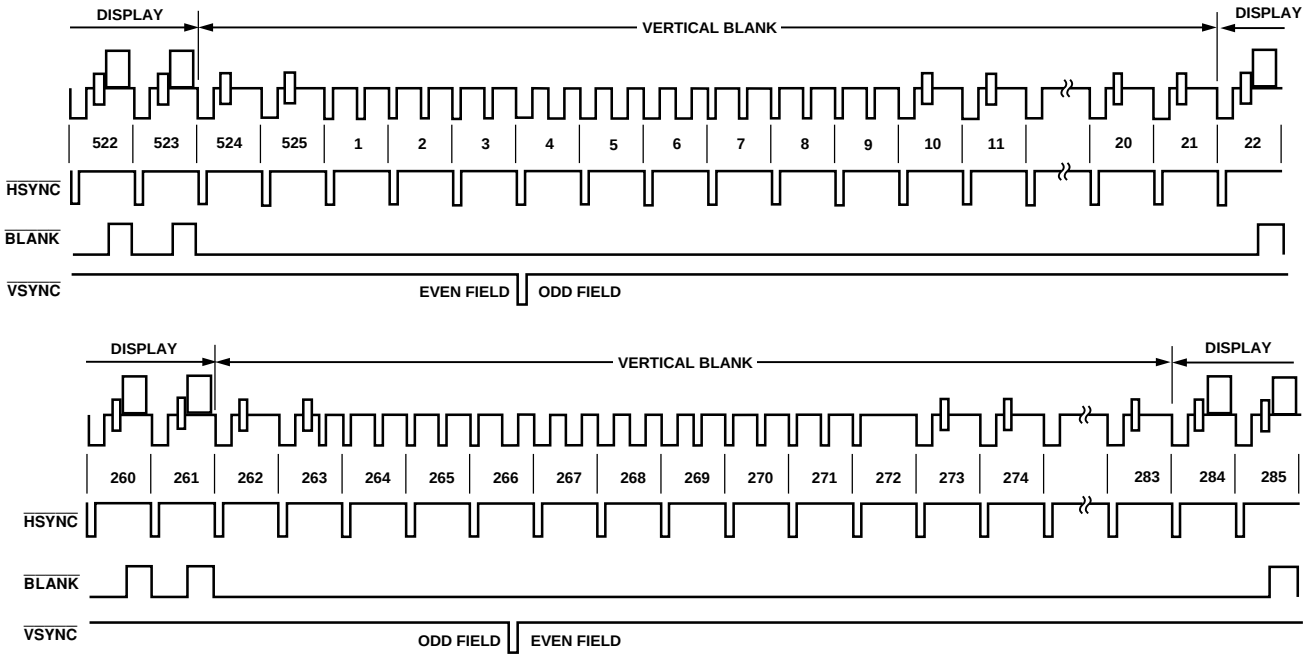


Figure 20. Timing Mode 2 (NTSC)

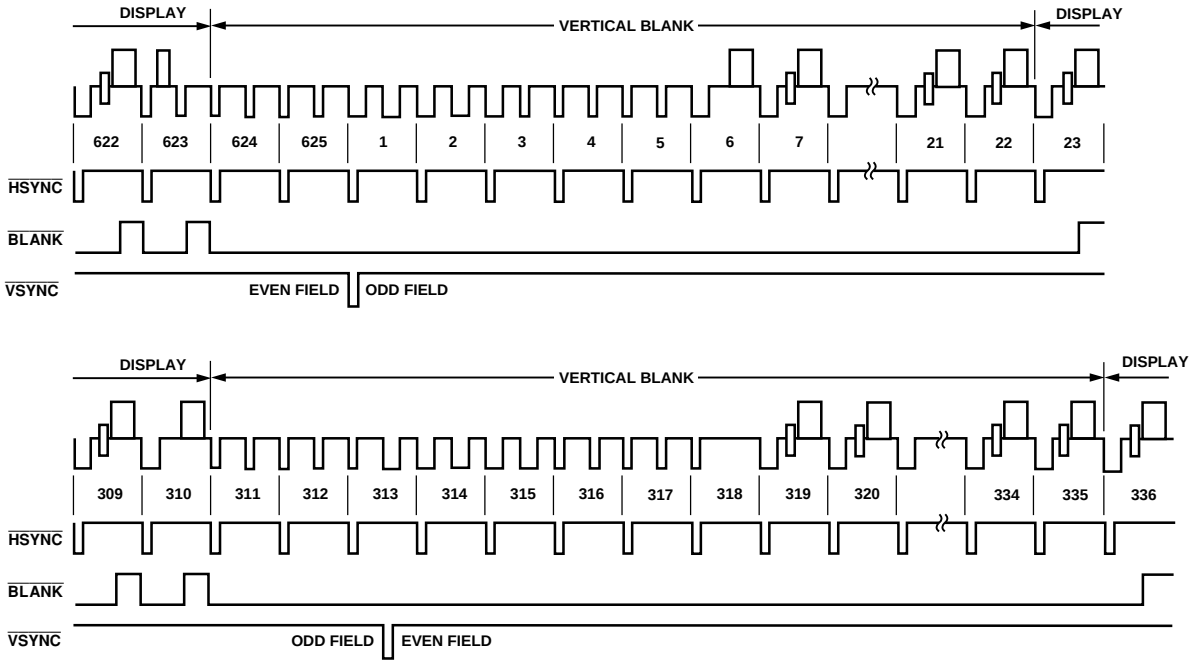


Figure 21. Timing Mode 2 (PAL)

Mode 2: Master Option. HSYNC, VSYNC, BLANK.
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7175/ADV7176 can generate horizontal and vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled the ADV7175/ADV7176 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 20 (NTSC) and Figure 21 (PAL). Figure 22 illustrates the HSYNC, BLANK and VSYNC for an even to odd field transition relative to the pixel data. Figure 23 illustrates the HSYNC, BLANK and VSYNC for an odd to even field transition relative to the pixel data.

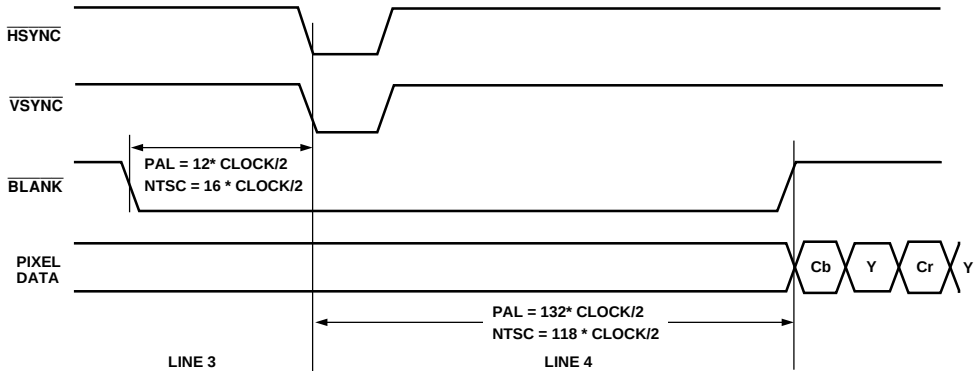


Figure 22. Timing Mode 2 Even-to-Odd Field Transition

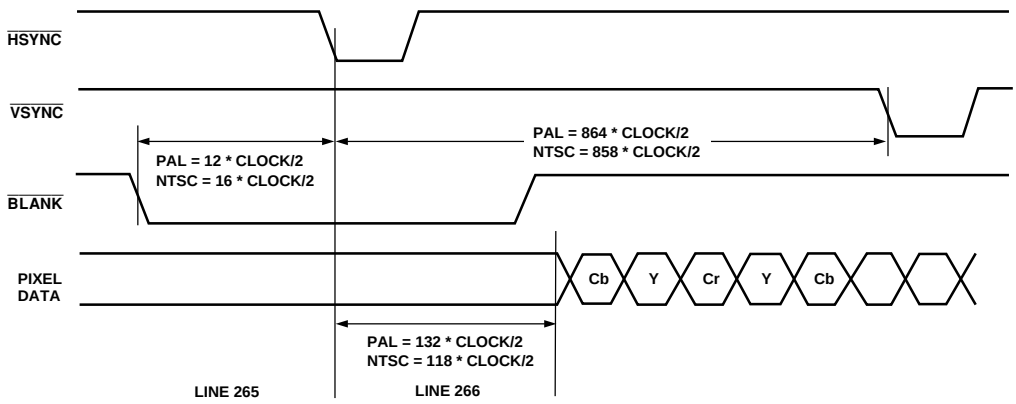


Figure 23. Timing Mode 2 Odd-to-Even Field Transition

Mode 3: Master/Slave Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7175/ADV7176 accepts or generates Horizontal SYNC and odd/even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7175/ADV7176 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL).

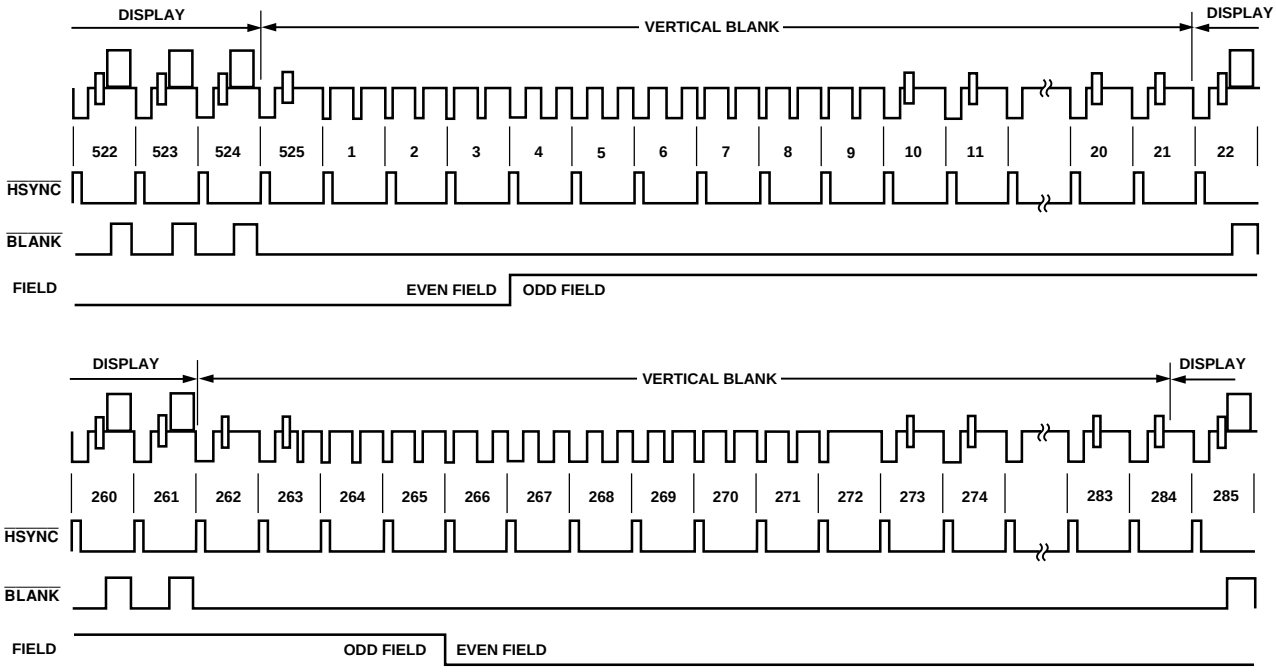


Figure 24. Timing Mode 3 (NTSC)

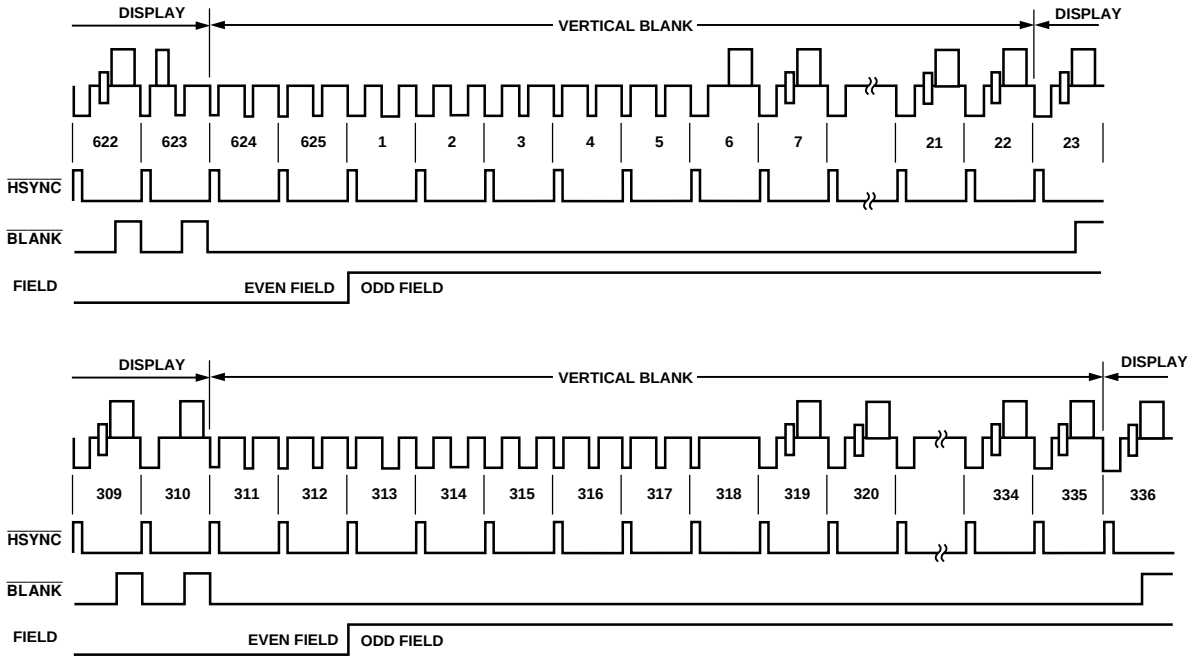


Figure 25. Timing Mode 3 (PAL)

(Continued from page 8)

In addition the ADV7175/ADV7176 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.54 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7175/ADV7176 has 8 distinct master or slave timing configurations. These are divided into 4 timing modes which operate at one discrete clock frequency (27 MHz). Timing control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulse widths and the where they occur in relation to each other.

OUTPUT VIDEO TIMING

The video timing generator generates the appropriate SYNC, BLANK and BURST sequence that controls the output analog waveforms. These sequences are summarized below. In slave modes the following sequences are synchronized with the input timing control signals. In master modes the timing generator free runs and generates the following sequences in addition to the output timing control signals.

NTSC–Interlaced: Scan lines 1–9 and 264–272 are always blanked and vertical sync pulses are included. Scan lines 525, 10–21 and 262, 263, 273–284 are also blanked and can be used for close captioning data. Burst is disabled on lines 1–6, 261–269 and 523–525.

NTSC–Noninterlaced: Scan lines 1–9 are always blanked and vertical sync pulses are included. Scan lines 10–21 are also blanked and can be used for close captioning data. Burst is disabled on lines 1–6, 261–262.

PAL–Interlaced: Scan lines 1–6, 311–318 and 624–625 are always blanked and vertical sync pulses are included in Fields 1, 2, 5 and 6. Scan lines 1–5, 311–319 and 624–625 are always blanked and vertical sync pulses are included in Fields 3, 4, 7 and 8. The remaining scan lines in the vertical interval are also blanked and can be used for close captioning data. Burst is disabled on lines 1–6, 311–318 and 623–625 in Fields 1, 2, 5 and 6. Burst is disabled on lines 1–5, 311–319 and 623–625 in Fields 3, 4, 7 and 8.

PAL–Noninterlaced: Scan lines 1–6 and 311–312 are always blanked and vertical sync pulses are included. The remaining scan lines in the vertical interval are also blanked and can be used for close captioning data. Burst is disabled on lines 1–5, 310–312.

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high to low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the pixel inputs P7–P0 are selected. After reset, the ADV7175/ADV7176 is automatically set up to operate in NTSC mode. Subcarrier frequency code 21F07C16 HEX is loaded into the subcarrier frequency registers. All other registers, with the exception of Mode Register 0, are set to 00H. All bits in Mode Register 0 are set to Logic Level “0” except Bit MR02. Bit MR02 of Mode Register 0 is set to Logic “1.” This enables the 7.5 IRE pedestal.

MPU PORT DESCRIPTION

The ADV7175 and ADV7176 support a two wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs serial data (SDATA) and serial clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7175 and ADV7176 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 26 and Figure 27. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7175/ADV7176 to Logic Level "0" or Logic Level "1."

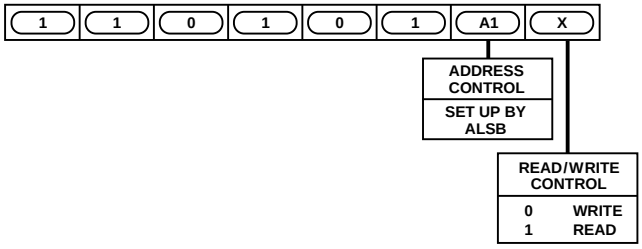


Fig 26. ADV7175 Slave Address

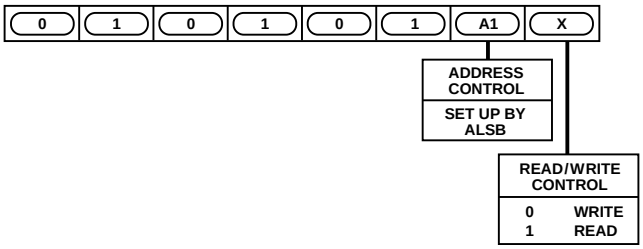


Fig 27. ADV7176 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7175/ADV7176 acts as a standard slave device on the bus. The data on the SDATA pin is 8 bits long supporting the 7-bit addresses plus the R/$\overline{W}$ bit. The ADV7175 has 33 subaddresses and the ADV7176 has 19 subaddresses to enable access to the internal registers. It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allowing data to be written to or from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers. There is one exception. The Subcarrier Frequency Registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto increment function should be then used to increment and access subcarrier frequency registers 1, 2 and 3. The subcarrier frequency registers should not be accessed independently.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period the user should only issue one start condition, one stop condition or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7175/ADV7176 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7175/ADV7176 and the part will return to the idle condition.

Figure 28 illustrates an example of data transfer for a read sequence and the start and stop conditions.

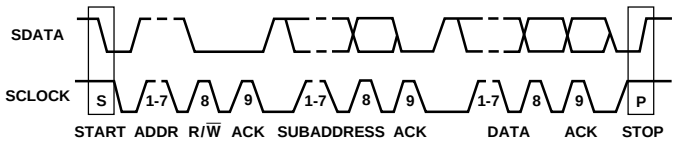


Figure 28. Bus Data Transfer

Figure 29 shows bus write and read sequences.

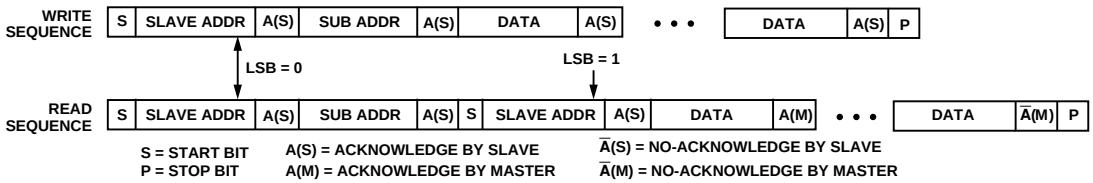


Figure 29. Write and Read Sequences

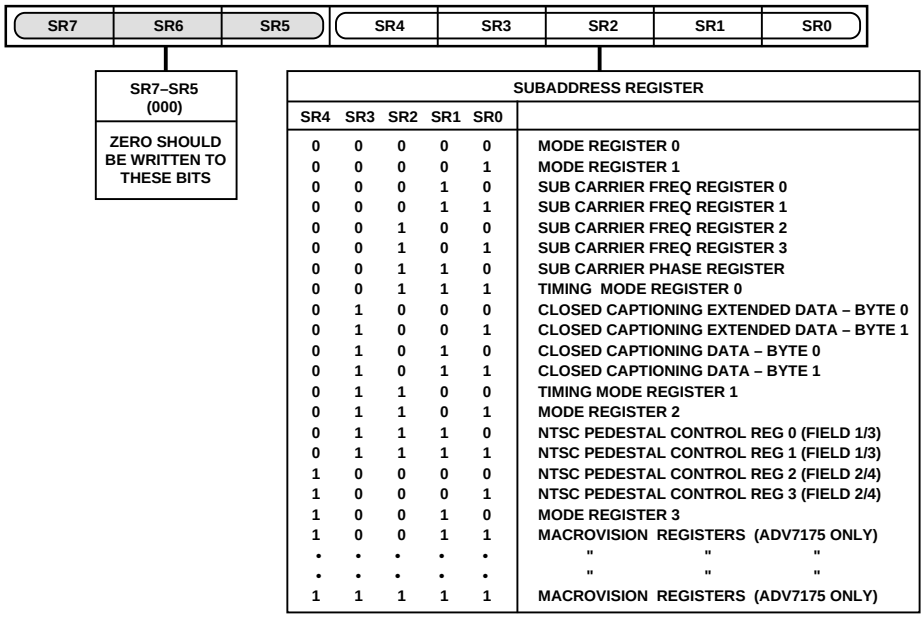


Figure 30. Subaddress Register

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7175/ADV7176 except the subaddress register which is a write only register. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Then a read/write operation is performed from/to the target address which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including subaddress register, mode registers, subcarrier frequency registers, subcarrier phase register, timing registers, closed captioning extended data registers, closed captioning data registers and NTSC pedestal control registers in terms of its configuration.

Subaddress Register (SR7–SR0)

The communications register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress set up. The subaddress register determines to/from which register the operation takes place.

Figure 30 shows the various operations under the control of the subaddress register. Zero should always be written to SR7–SR5.

Register Select (SR4–SR0):

These bits are setup to point to the required starting address.

MODE REGISTER 0 MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)

Mode Register 0 is a 8-bit wide register.

Figure 31 shows the various operations under the control of Mode Register 0. This register can be read from as well written to.

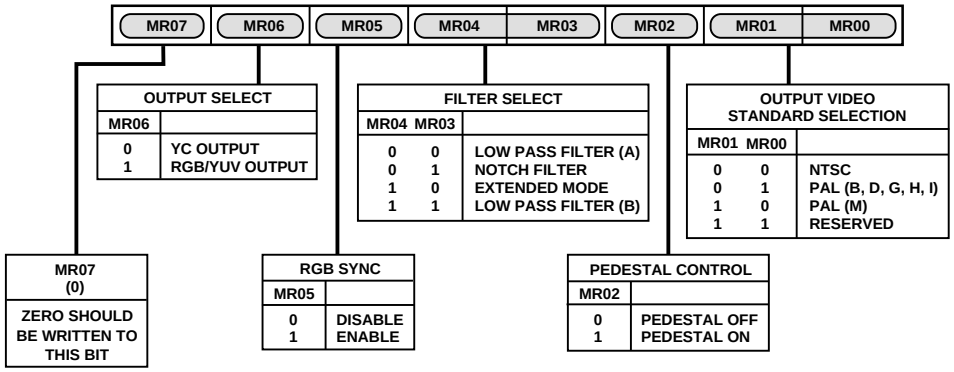


Figure 31. Mode Register 0

MODE REGISTER 0 (MR07–MR00) BIT DESCRIPTION
Encode Mode Control (MR01–MR00):
These bits are used to set up the encode mode. The ADV7175/ADV7176 can be set up to output NTSC, PAL (B, D, G, H, I), PAL (M) and PAL (N) standard video.

Pedestal Control (MR02)
This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid if the ADV7175/ADV7176 is configured in PAL mode.

Luminance Filter Control (MR04–MR03)
These bits are used for selecting between a filter for the luminance signal. These filters automatically are set to the cutoff frequency for the low-pass filters and the subcarrier frequency for the notch filter. The extended mode filter is a 5.5 MHz low-pass filter. The filters are illustrated in Figures 3 to 11.

RGB Sync (MR05)
This bit is used to set up the RGB outputs with the sync information encoded.

Output Control (MR06)
This bit specifies if the part is in composite video or RGB/YUV mode. Please note that in RGB/YUV mode the main composite signal is still available.

MODE REGISTER 1 MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)
Mode Register 1 is a 8-bit wide register.

Figure 32 shows the various operations under the control of Mode Register 1. This register can be read from as well written to.

MODE REGISTER 1 (MR17–MR10) BIT DESCRIPTION
Interlaced Mode Control (MR10):
This bit is used to setup the output to interlaced or non-interlaced mode. This mode is only relevant when the part is in composite video mode.

Closed Captioning Field Control (MR12–MR11)
These bits control the field that close captioning data is displayed on close captioning information can be displayed on an odd field, even field or both fields.

DAC Control (MR16–MR13)
These bits can be used to power down the DACs. This can be used to reduce the power consumption of the ADV7175/ADV7176 if any of the DACs are not required in the application.

Color Bar Control (MR17)
This bit can be used to generate and output an internal color bar. The color bar configuration is 75/75/75/7.5 for NTSC and 100/0/75/0 for PAL.

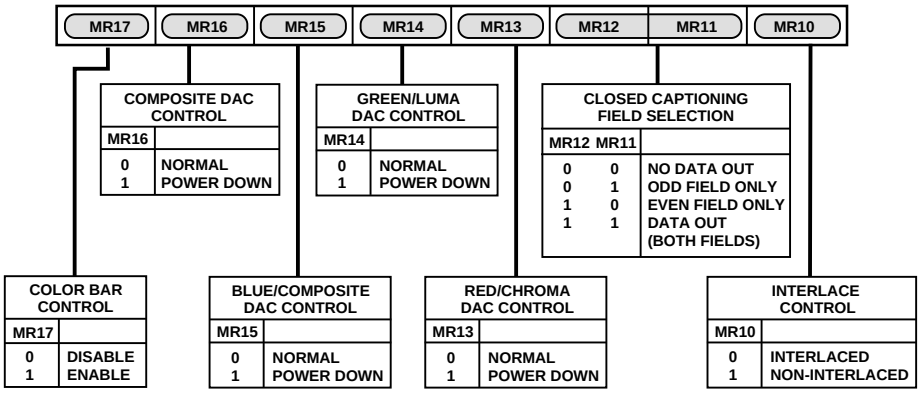


Figure 32. Mode Register 1

SUBCARRIER FREQUENCY REGISTERS 3–0 (FSC3–FSC0)
(Address (SR4–SR0) = 05H–02H)
These 8-bit wide registers are used to set up the subcarrier frequency. The value of these registers are calculated by using the following equation:

$$Subcarrier\ Frequency\ Register = \frac{2^{32}-1}{F_{CLK}} * F_{SCF}$$

i.e.: NTSC Mode, $F_{CLK} = 27\ MHz$, $F_{SCF} = 3.5796\ MHz$

$$Subcarrier\ Frequency\ Register = \frac{2^{32}-1}{27\times10^{6}} * 3.579545 \times 10^{6}$$
$$= 21F07C16\ HEX$$

Figure 33 shows how the frequency is set up by the 4 registers.

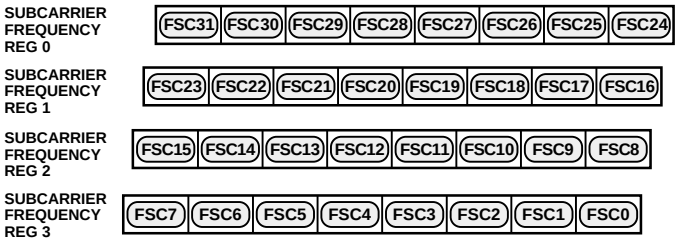


Figure 33. Subcarrier Frequency Register

SUBCARRIER PHASE REGISTER (FP7–FP0):
(Address (SR4–SR0) = 06H)
This 8-bit wide register is used to set up the subcarrier phase. Each bit represents 1.41°.

TIMING REGISTER 0 (TR07–TR00)
(Address (SR4-SR0) = 07H)
Timing Register 0 is a 8-bit wide register.

Figure 34 shows the various operations under the control of Timing Register 0. This register can be read from as well written to.

TIMING REGISTER 0 (TR07–TR00)
BIT DESCRIPTION
Master/Slave Control (TR00)
This bit controls whether the ADV7175/ADV7176 is in master or slave mode.

Timing Mode Control (TR02–TR01)
These bits control the timing mode of the ADV7175/ADV7176 These modes are described in the Timing and Control section of the data sheet.

$\overline{\text{BLANK}}$ Control (TR03)
This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode.

Luma Delay Control (TR05–TR04)
These bits control the addition of a luminance delay. Each bit represents a delay of 74 ns.

Pixel Port Select (TR06)
This bit is used to set the pixel port to accept 8-bit or 16-bit data. If an 8-bit input is selected the data will be set up on Pins P7–P0.

Timing Register Reset (TR07)
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after setting up a new timing mode.

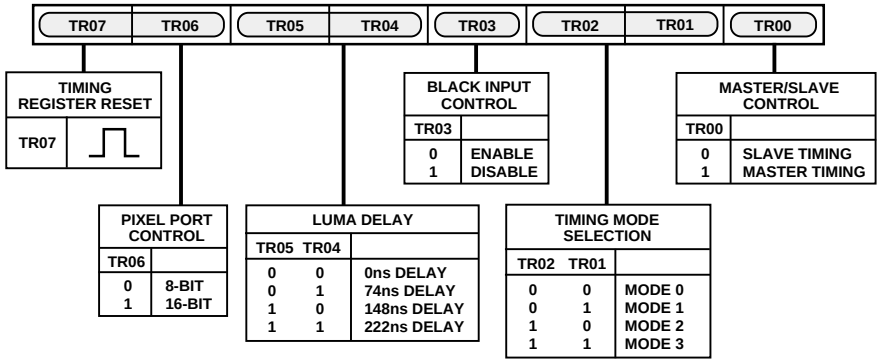


Figure 34. Timing Register 0

CLOSED CAPTIONING EXTENDED DATA REGISTERS 1–0 (CED15–CED00)
(Address (SR4–SR0) = 09–08H)
These 8-bit wide registers are used to set up the closed captioning extended data bytes. Figure 35 shows how the high and low bytes are set up in the registers.

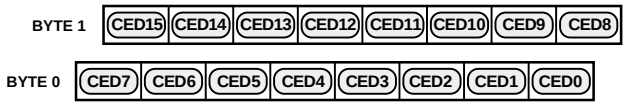


Figure 35. Closed Captioning Extended Data Register

CLOSED CAPTIONING DATA REGISTERS 1–0 (CCD15–CCD00)
(Subaddress (SR4–SR0) = 0B–0AH)
These 8-bit wide registers are used to set up the closed captioning data bytes. Figure 36 shows how the high and low bytes are set up in the registers.

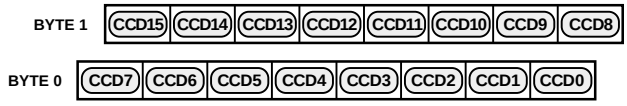


Figure 36. Closed Captioning Data Register

TIMING REGISTER 1 (TR17–TR10)
(Address (SR4–SR0) = 0CH)
Timing Register 1 is an 8-bit wide register.

Figure 37 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

TIMING REGISTER 1 (TR17–TR10) BIT DESCRIPTION
$\overline{\text{HSYNC}}$ Width (TR11–TR10)
These bits adjust the $\overline{\text{HSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$/FIELD Delay Control (TR13–TR12)
These bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD/$\overline{\text{VSYNC}}$ output.

$\overline{\text{HSYNC}}$ to FIELD Delay Control (TR15–TR14)
When the ADV7175/ADV7176 is in Timing Mode 1, these bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD output rising edge.

$\overline{\text{VSYNC}}$ Width (TR15–TR14)
When the ADV7175/ADV7176 is in Timing Mode 2, these bits adjust the $\overline{\text{VSYNC}}$ pulse width.

$\overline{\text{HSYNC}}$ to Pixel Data Adjust (TR17–TR16)
This enables the $\overline{\text{HSYNC}}$ to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.

MODE REGISTER 2 MR2 (MR27–MR20)
(Address (SR4-SR0) = 0DH)
Mode Register 2 is an 8-bit wide register.

Figure 38 shows the various operations under the control of Mode Register 2. This register can be read from as well written to.

MODE REGISTER 2 (MR27–MR20) BIT DESCRIPTION
Square Pixel Mode Control (MR20)
This bit is used to setup square pixel mode. This is available in slave mode only. For NTSC, a 24.54 MHz clock must be supplied. For PAL, a 29.5 MHz clock must be supplied.

Genlock Control (MR22–MR21)
These bits control the genlock feature of the ADV7175/ADV7176 Setting MR21 to a Logic "1" configures the SCRESET/RTC pin as an input. Setting MR22 to logic level "0" configures the SCRESET/RTC pin as a subcarrier reset input. Therefore, the subcarrier will reset to Field 0 following a low to high transition on the SCRESET/RTC pin. Setting MR22 to Logic Level "1" configures the SCRESET/RTC pin as a real time control input.

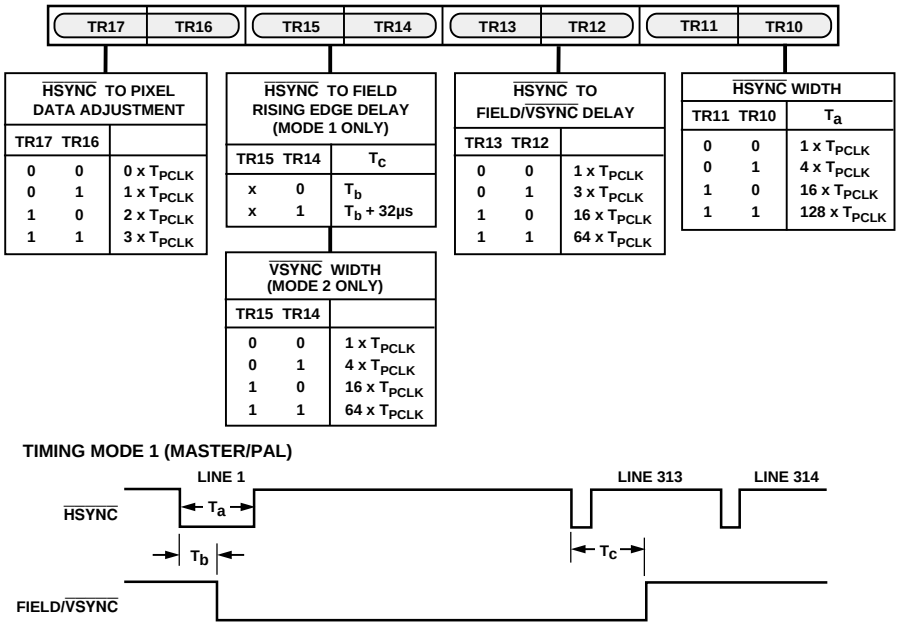


Figure 37. Timing Register 1

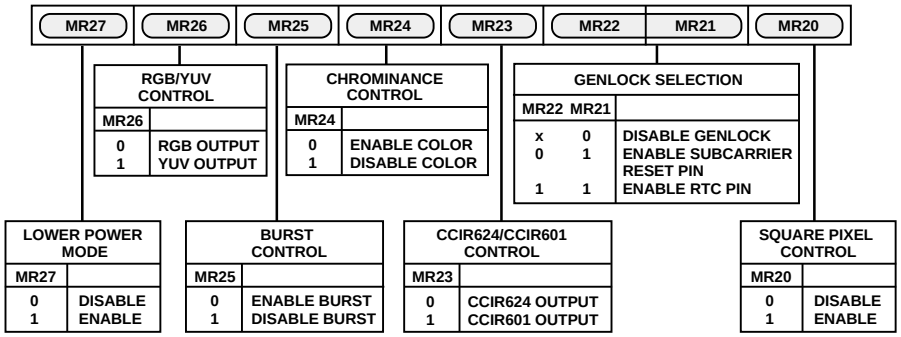


Figure 38. Mode Register 2

CCIR624/CCIR601 Control (MR23)
This bit switches the video output between CCIR624 and CCIR601 video standard.

Chrominance Control (MR24)
This bit enables the color information to be switched on and off the video output.

Burst Control (MR25)
This bit enables the burst information to be switched on and off the video output.

RGB/YUV Control (MR26)
This bit enables the output from the RGB DACs to be set to YUV output video standard. Bit MR06 of Mode Register 0 must be set to Logic Level "1" before MR26 is set.

Lower Power Control (MR27)
This bit enables the lower power mode of the ADV7175/ ADV7176.

NTSC PEDESTAL CONTROL REGISTERS 3–0 (PCE15–0, PCO15–0)

(Subaddress (SR4–SR0) = 11-0EH)
These 8-bit wide registers are used to set up the NTSC pedestal on a line by line basis in the vertical blanking interval for both odd and even fields. Figure 39 shows the four control registers. A Logic "1" in any of the bits of these registers has the effect of turning the pedestal off on the equivalent line.

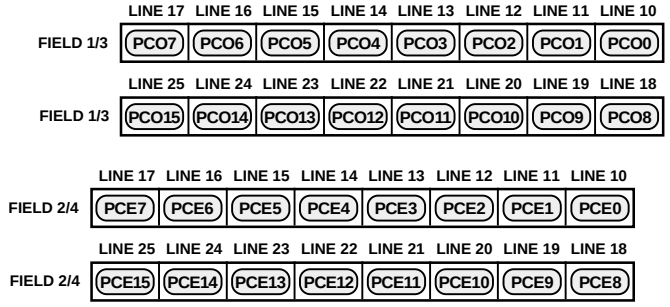


Figure 39. Pedestal Control Registers

MODE REGISTER 3 MR3 (MR37–30) (Address (SR4–SR0) = 12H)
Mode Register 3 is an 8-bit wide register.

Figure 34 shows the various operations under the control of Mode Register 3. Bits MR36–MR30 are reserved and Logic "0" should be written to them.

MODE REGISTER 3 (MR37–MR30) DESCRIPTION
DAC Switching Control (MR37)
This bit is used to switch the luminance signal onto the composite DAC. Figure 40 illustrates the DAC outputs and how they switch when MR 37 is set to Logic "1".

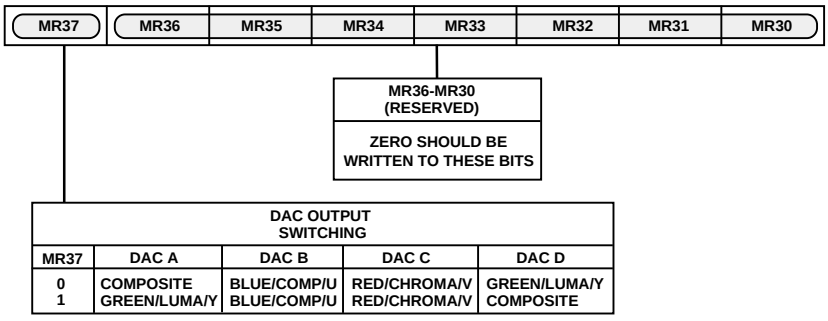


Figure 40. Mode Register 3

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7175/ADV7176 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7175/ADV7176 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes
The ground plane should encompass all ADV7175/ADV7176 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7175/ADV7176, the analog output traces, and all the digital signal traces leading up to the ADV7175/ADV7176. The ground plane is the board's common ground plane.

Power Planes
The ADV7175/ADV7176 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7175/ADV7176.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7175/ADV7176 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling
For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7175/ADV7176 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7175/ADV7176 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect
The digital inputs to the ADV7175/ADV7176 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7175/ADV7176 should be avoided to reduce noise pickup. Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect
The ADV7175/ADV7176 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital inputs, especially pixel data inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7175/ADV7176 so as to minimize reflections.

The ADV7175/ADV7176 should have no inputs left floating. Any inputs that are not required should be tied to ground.

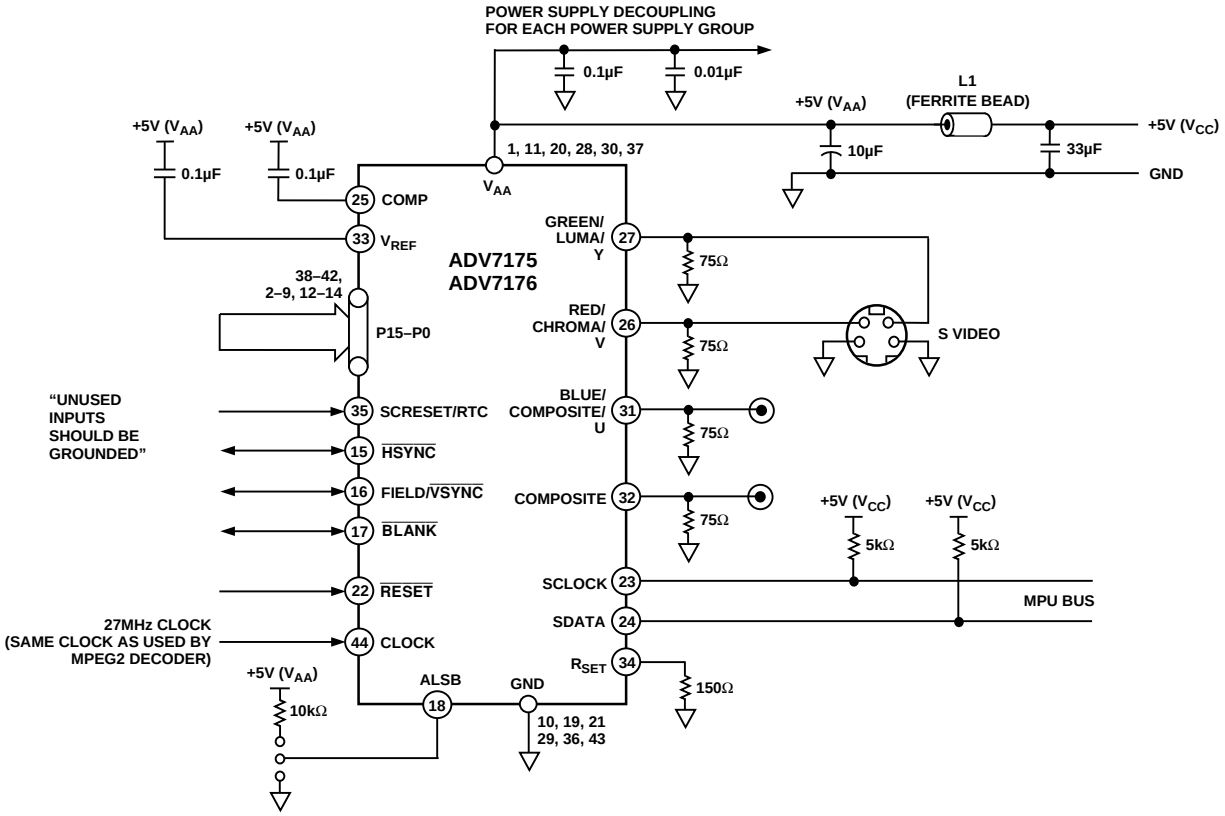


Figure 41. Recommended Analog Circuit Layout

The circuit below can be used to generate a 13.5 MHz waveform using the 27 MHz clock and the $\overline{\text{HSYNC}}$ pulse. This waveform is guaranteed to produce the 13.5 MHz clock in synchronization with the 27 MHz clock. This 13.5 MHz clock can be used if 13.5 MHz clock is required by the MPEG decoder. This will guarantee that the Cr and Cb pixel information is input to the ADV7175/ADV7176 in the correct sequence.

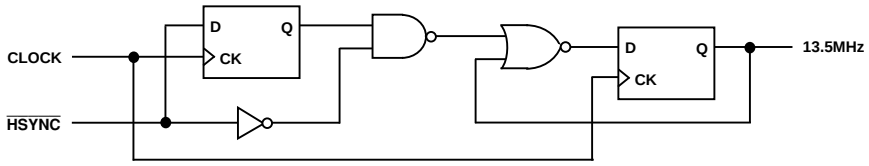


Figure 42. Circuit to Generate 13.5 MHz

APPENDIX 2

CLOSED CAPTIONING

The ADV7175/ADV7176 supports closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of line 21 of the odd fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run in signal, the blanking level is held for two data bits and is followed by a Logic Level "1" start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes. The data for these bytes is stored in closed captioning data registers 0 and 1.

The ADV7175/ADV7176 also supports the extended closed captioning operation which is active during even fields and is encoded on scan line 284. The data for this operation is stored in closed captioning extended data registers 0 and 1.

All clock run-in signals and timing to support closed captioning on lines 21 and 282 are generated automatically by the ADV7175/ADV7176. All pixels inputs are ignored during lines 21 and 282.

FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA208 describe the closed captioning information for lines 21 and 284.

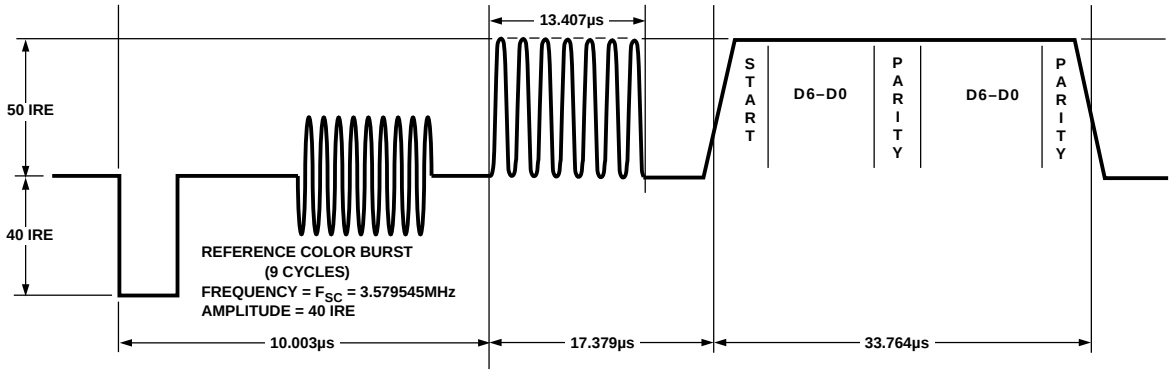


Figure 43. Closed Captioning Waveform (NTSC)

APPENDIX 3

NTSC WAVEFORMS (With Pedestal)

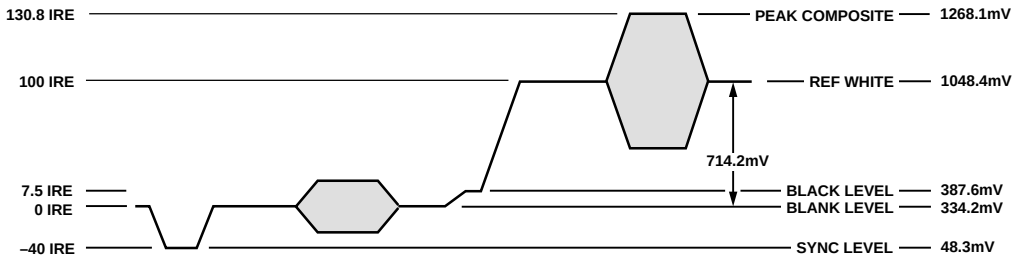


Figure 44. NTSC Composite Video Levels

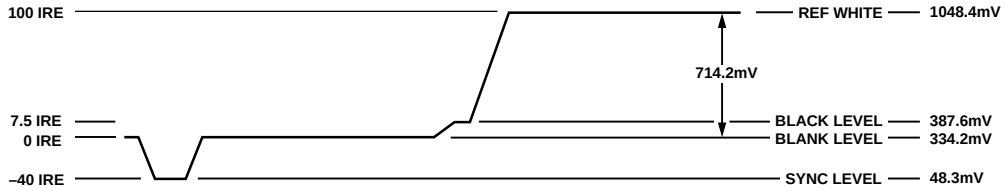


Figure 45. NTSC Luma Video Levels

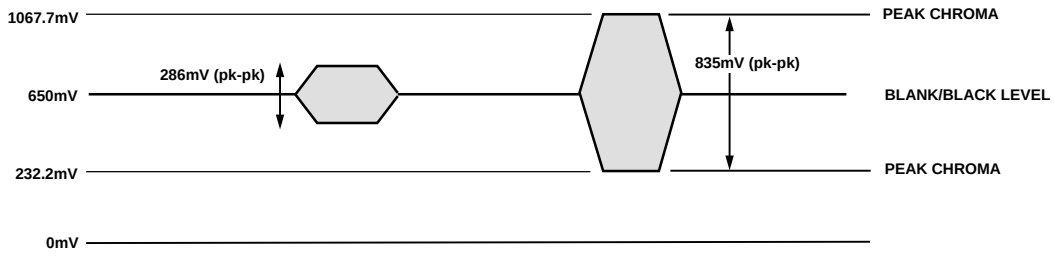


Figure 46. NTSC Chroma Video Levels

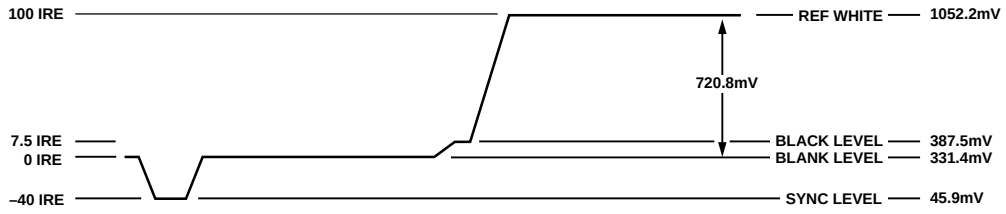


Figure 47. NTSC RGB Video Levels

NTSC WAVEFORMS (Without Pedestal)

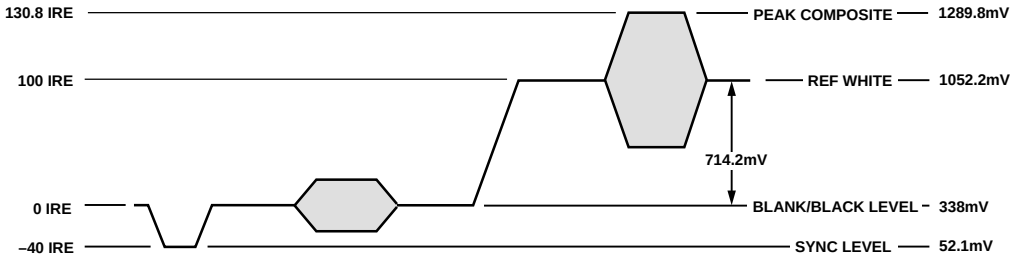


Figure 48. NTSC Composite Video Levels

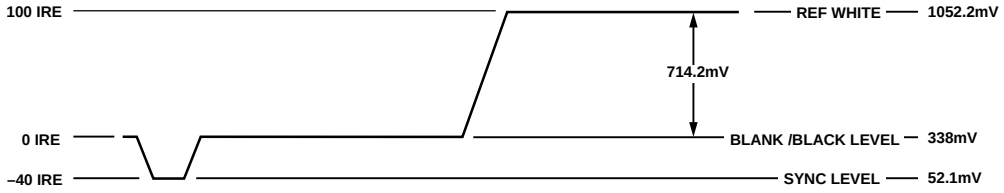


Figure 49. NTSC Luma Video Levels

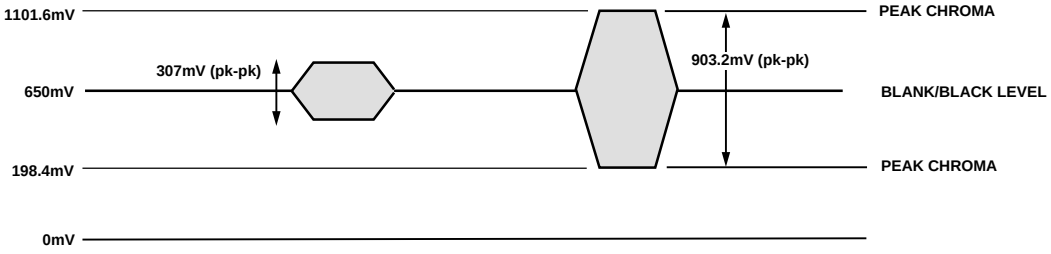


Figure 50. NTSC Chroma Video Levels

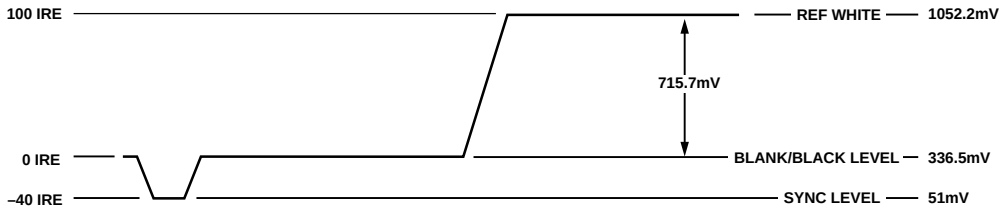


Figure 51. NTSC RGB Video Levels

PAL WAVEFORMS

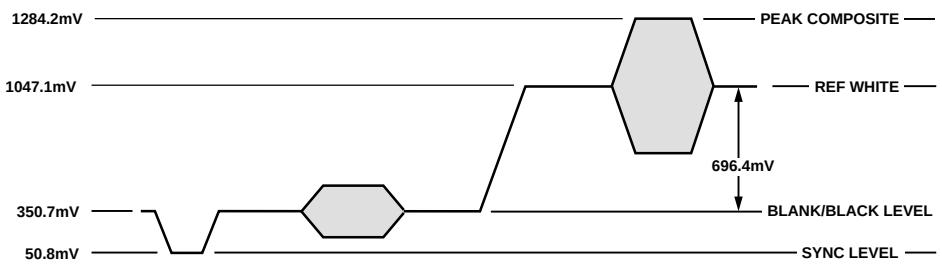


Figure 52. PAL Composite Video Levels

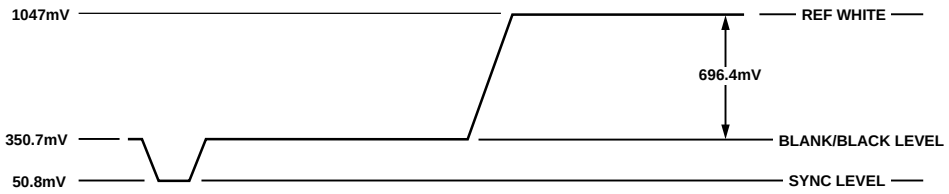


Figure 53. PAL Luma Video Levels

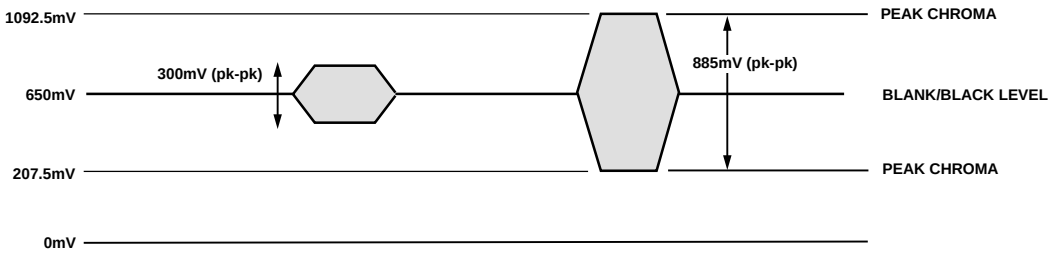


Figure 54. PAL Chroma Video Levels

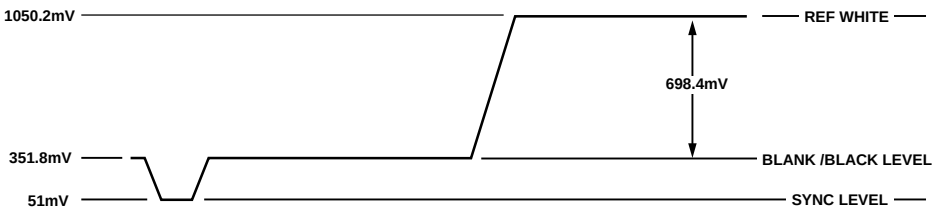


Figure 55. PAL RGB Video Levels

APPENDIX 4

REGISTER VALUES

The ADV7175/ADV7176 registers can be set depending on the user standard required.

The following examples give the various register formats for several video standards.

In each case the output is set to composite o/p with all DACs powered up and with the $\overline{\text{BLANK}}$ input control disabled. Additionally, the burst and color information are enabled on the output and the internal color bar generator is switched off. In the examples shown the timing mode is set to Mode 0 in slave format. TR02–TR00 of the timing register 0 control the timing modes. For a detailed explanation of each bit in the command registers, please turn to the register programming section of the data sheet. TR07 should be toggled after setting up a new timing mode. Timing Register 1 provides additional control over the position and duration of the timing signals. In the examples this register is programmed in default mode.

NTSC

Mode Register 0	04 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	16 Hex
Subcarrier Frequency Register 1	7C Hex
Subcarrier Frequency Register 2	F0 Hex
Subcarrier Frequency Register 3	21 Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

PAL (B, D, G, H, I)

Mode Register 0	01 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	CB Hex
Subcarrier Frequency Register 1	8A Hex
Subcarrier Frequency Register 2	09 Hex
Subcarrier Frequency Register 3	2A Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

PAL (M)

Mode Register 0	06 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	A3 Hex
Subcarrier Frequency Register 1	EF Hex
Subcarrier Frequency Register 2	E6 Hex
Subcarrier Frequency Register 3	21 Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

PAL (N)

Mode Register 0	05 Hex
Mode Register 1	00 Hex
Subcarrier Frequency Register 0	CB Hex
Subcarrier Frequency Register 1	8A Hex
Subcarrier Frequency Register 2	09 Hex
Subcarrier Frequency Register 3	2A Hex
Subcarrier Phase Register	00 Hex
Timing Register 0	08 Hex
Closed Captioning Ext Register 0	00 Hex
Closed Captioning Ext Register 1	00 Hex
Closed Captioning Register 0	00 Hex
Closed Captioning Register 1	00 Hex
Timing Register 1	00 Hex
Mode Register 2	00 Hex
Pedestal Control Register 0	00 Hex
Pedestal Control Register 1	00 Hex
Pedestal Control Register 2	00 Hex
Pedestal Control Register 3	00 Hex
Mode Register 3	00 Hex

APPENDIX 5

OUTPUT FILTER

If an output filter is required for the composite output of the ADV7175/ADV7176. The following filter can be used. Plots of the filter characteristics can be produced on request.

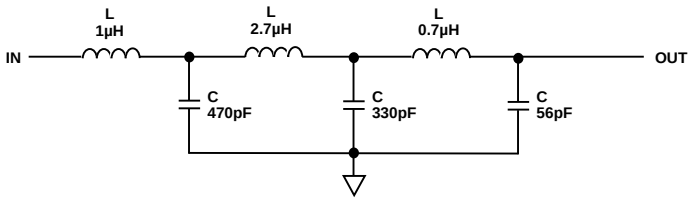


Figure 56. Output Filter

APPENDIX 6

OUTPUT WAVEFORMS

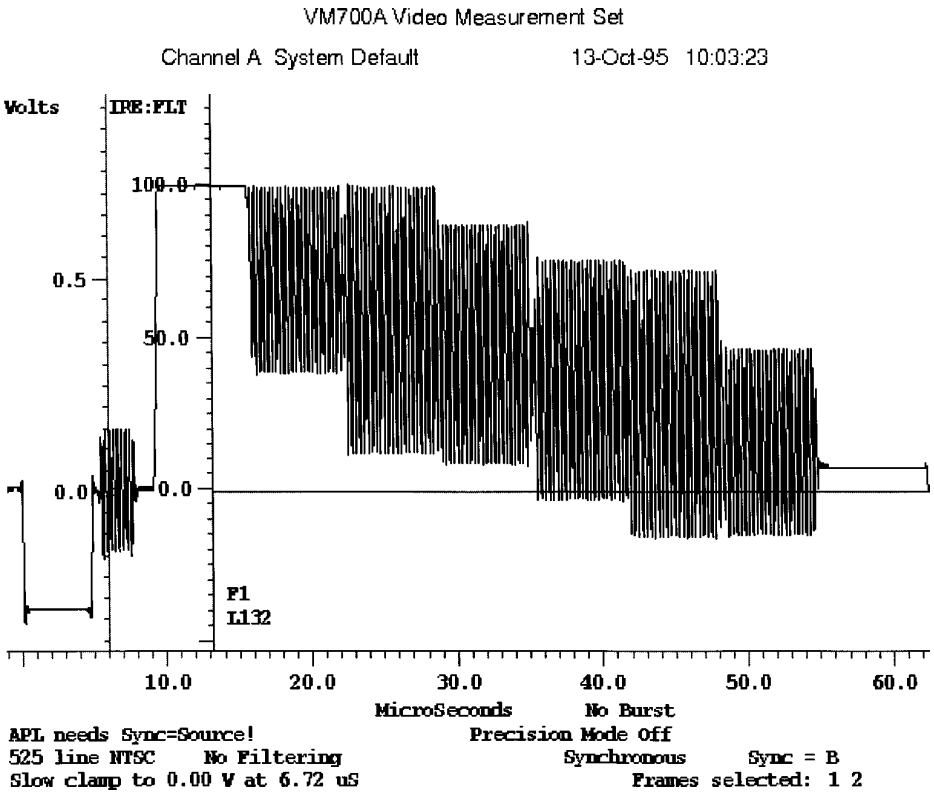


Figure 57. 100/75% Color Bars NTSC

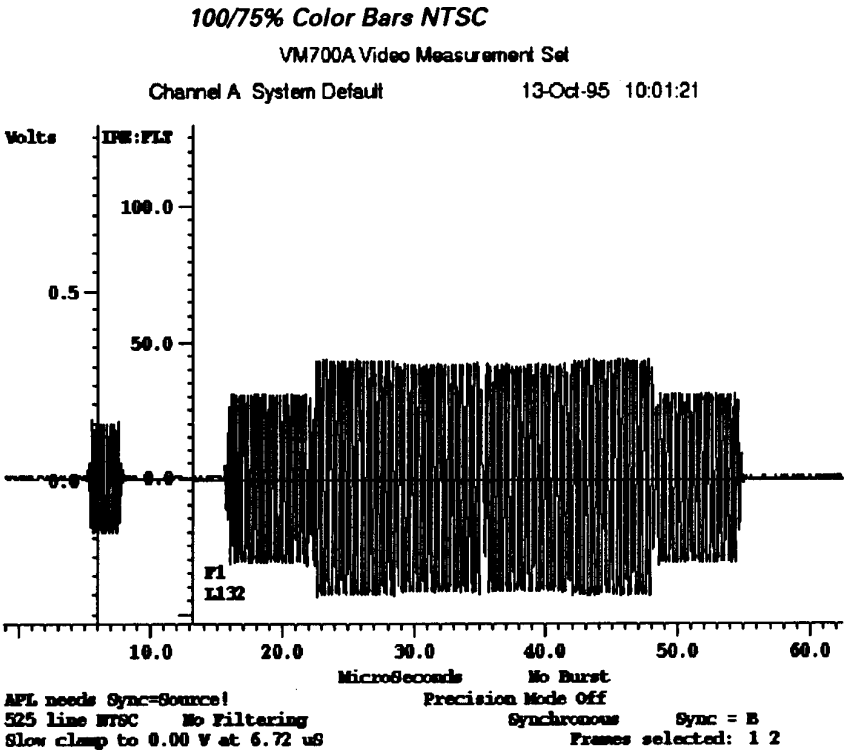


Figure 58. 100/75% Color Bars NTSC (Chrominance Only)

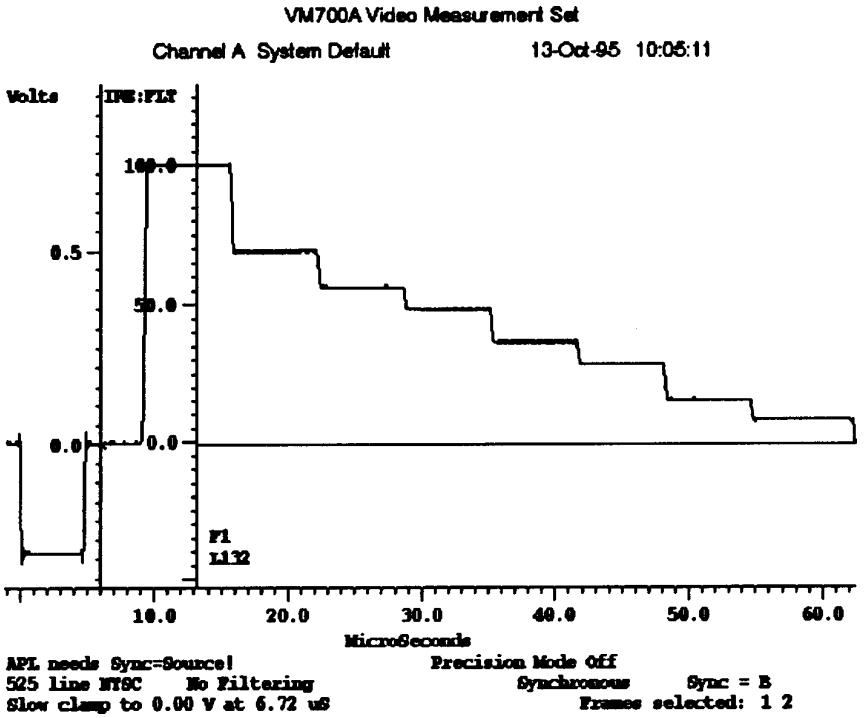


Figure 59. 100/75% Color Bars NTSC (Luminance Only)

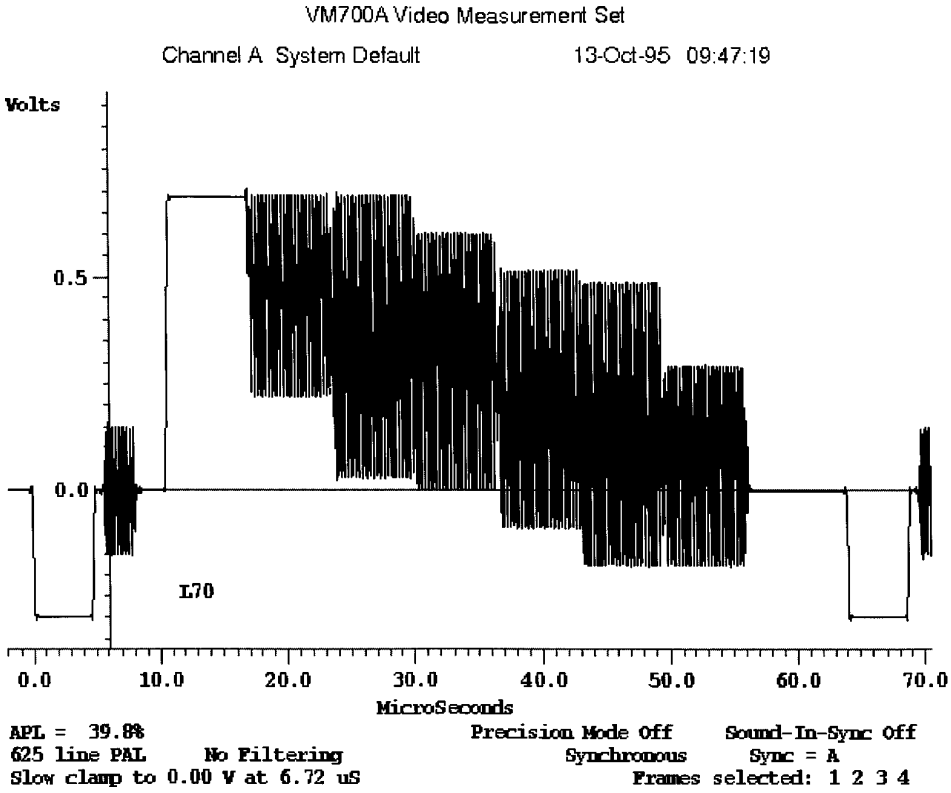


Figure 60. 100/75% Color Bars PAL

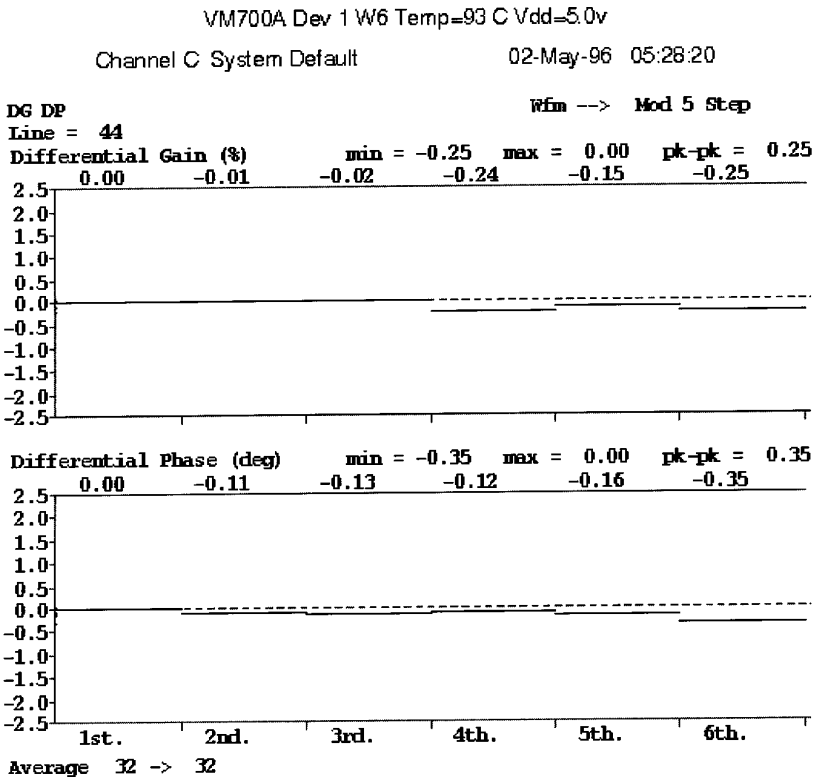


Figure 61. Differential Phase and Gain Measurements (PAL)

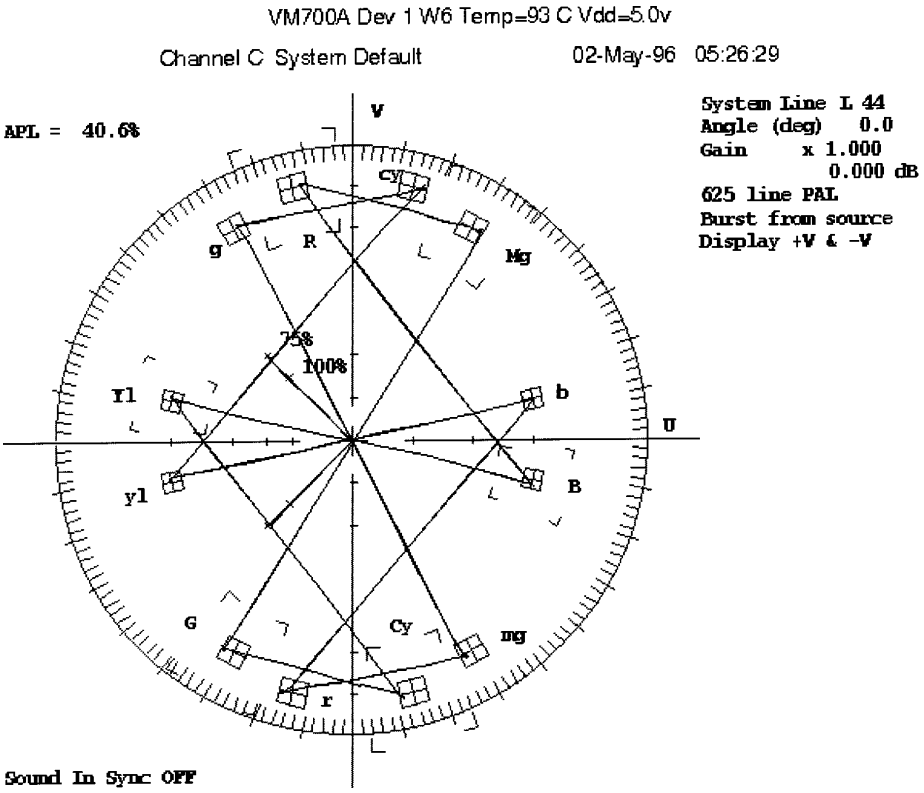


Figure 62. Vectorscope Measurements (PAL)

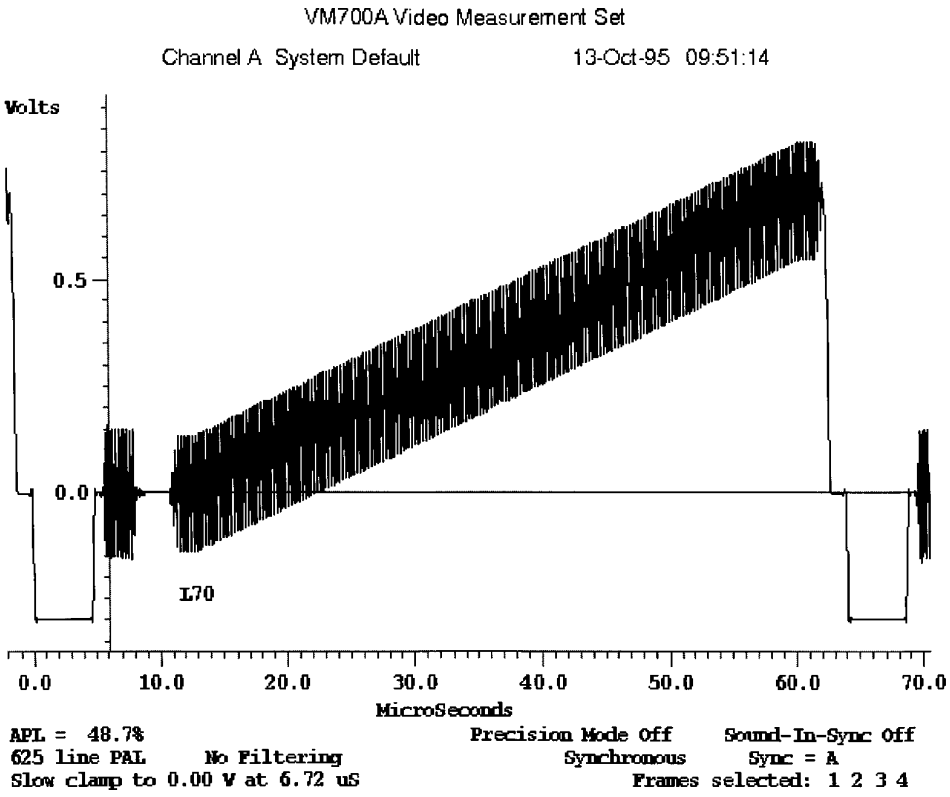


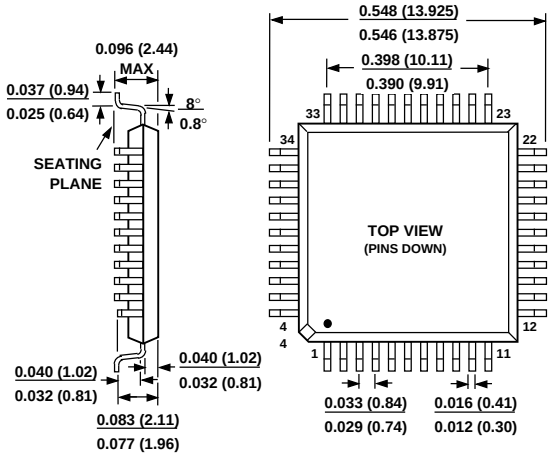
Figure 63. Modulated Ramp Measurements (PAL)

INDEX

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Quad Flatpack
(S-44)



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