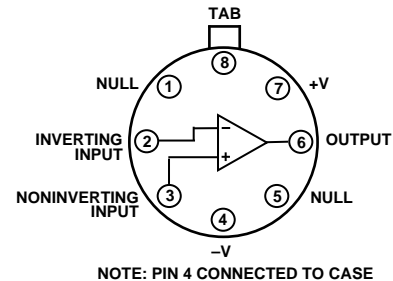


AD542/AD544/AD547

FEATURES

Ultralow Drift: 1 $\mu\text{V}/^\circ\text{C}$ (AD547L)
Low Offset Voltage: 0.25 mV (AD547L)
Low Input Bias Currents: 25 pA max
Low Quiescent Current: 1.5 mA
Low Noise: 2 μV p-p
High Open Loop Gain: 110 dB
High Slew Rate: 13 V/ μs
Fast Settling to $\pm 0.01\%$: 3 μs
Low Total Harmonic Distortion: 0.0025%
Available in Hermetic Metal Can and Die Form
MIL-STD-883B Versions Available
Dual Versions Available: AD642, AD644, AD647

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The BiFET series of precision, monolithic FET-input op amps are fabricated with the most advanced BiFET and laser trimming technologies. The AD542, AD544, AD547 series offers bias currents significantly lower than currently available BiFET devices, 25 pA max, warmed up.

In addition, the offset voltage is laser trimmed to less than 0.25 mV on the AD547L, which is achieved by utilizing Analog Devices' exclusive laser wafer trimming (LWT) process. When combined with the AD547's low offset drift (1 $\mu\text{V}/^\circ\text{C}$), these features offer the user performance superior to existing BiFET op amps at low BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate cost. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common-mode rejection (80 dB, min on the "K" and "L" grades) and high open-loop gain, even under heavy loading, ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is recommended for any op amp applications requiring excellent ac and dc performance at low cost. The 2 MHz bandwidth and low offset of the AD544 make it the first choice as an output amplifier for current output D/A converters, such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four grades: the "J," "K," and "L" grades are specified over the 0°C to +70°C temperature range and the "S" grade over the -55°C to +125°C operating temperature range. All devices are offered in the hermetically sealed, TO-99 metal can package.

REV. B

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PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage drift to 1 $\mu\text{V}/^\circ\text{C}$ max and offset voltage to only 0.25 mV max on the AD547L.
4. Low voltage noise (2 μV p-p) and low offset voltage drift enhance performance as a precision op amp.
5. High slew rate (13 V/ μs) and fast settling time to 0.01% (3 μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0025%) make the AD544 an ideal choice in audio applications.
7. Bare die are available for use in hybrid circuit applications.

AD542/AD544/AD547—SPECIFICATIONS ($V_S = \pm 15\text{ V}$ @ $T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	AD542			AD544			AD547			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN-LOOP GAIN ¹ $V_{OUT} = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$										
J Grade	100			30			100			V/mV
K, L, S Grades	250			50			250			V/mV
$T_A = T_{MIN}$ to T_{MAX}										
J Grade	100			20			100			V/mV
S Grade	100			20			100			V/mV
K, L Grades	250			40			250			V/mV
OUTPUT CHARACTERISTICS										
$R_L = 2\text{ k}\Omega$										
$T_A = T_{MIN}$ to T_{MAX}	± 10	± 12		± 10	± 12		± 10	± 12		V
$R_L = 10\text{ k}\Omega$										
$T_A = T_{MIN}$ to T_{MAX}	± 12	± 13		± 12	± 13		± 12	± 13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	2.0	3.0		8.0	13.0		2.0	3.0		V/ μs
Total Harmonic Distortion					0.0025					%
INPUT OFFSET VOLTAGE ²										
J Grade			2.0			2.0			1.0	mV
K Grade			1.0			1.0			0.5	mV
L Grade			0.5			0.5			0.25	mV
S Grade			1.0			1.0			0.5	mV
vs. Temperature ³										
J Grade		20			20			5		$\mu\text{V}/^\circ\text{C}$
K Grade		10			10			2		$\mu\text{V}/^\circ\text{C}$
L Grade		5			5			1		$\mu\text{V}/^\circ\text{C}$
S Grade		15			15			5		$\mu\text{V}/^\circ\text{C}$
vs. Supply, $T_A = T_{MIN}$ to T_{MAX}										
J Grade			200			200			200	$\mu\text{V}/\text{V}$
K, L, S Grades			100			100			100	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT ⁴										
Either Input										
J Grade			50			50			50	pA
K, L, S Grades		10	25		10	25		10	25	pA
Input Offset Current										
J Grade		5	15		5	15		5	15	pA
K, L, S Grades		2	15		2	15		2	15	pA
INPUT IMPEDANCE										
Differential		$10^{12} \parallel 6$			$10^{12} \parallel 6$			$10^{12} \parallel 6$		$\Omega \parallel \text{pF}$
Common Mode		$10^{12} \parallel 3$			$10^{12} \parallel 3$			$10^{12} \parallel 3$		$\Omega \parallel \text{pF}$
INPUT VOLTAGE ⁵										
Differential		± 20			± 20			± 20		V
Common Mode	± 10	± 12		± 10	± 12		± 10	± 12		V
Common-Mode Rejection										
$V_{IN} = \pm 10\text{ V}$										
J Grade		76			76			76		dB
K, L, S Grades		80			80			80		dB

Parameter	AD542			AD544			AD547			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.1	1.5		1.8	2.5		1.1	1.5	mA
VOLTAGE NOISE										
0.1 Hz to 10 Hz										
J Grade		2.0			2.0			2.0		μV p-p
K, L, S Grades		2.0			2.0			4.0		μV p-p
10 Hz		70			35			70		nV/√Hz
100 Hz		45			22			45		nV/√Hz
1 kHz		30			18			30		nV/√Hz
10 kHz		25			16			25		nV/√Hz
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L Grades		0 to +70			0 to +70			0 to +70		°C
S Grade		-55 to +125			-55 to +125			-55 to +125		°C
Storage		-65 to +150			-65 to +150			-65 to +150		°C
TRANSISTOR COUNT										
	29			29			29			

NOTES

¹Open-Loop Gain is specified with V_{OS} both nulled and unnullled.

²Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

³Input Offset Voltage Drift is specified with the offset voltage unnullled. Nulling will induce an additional 3 μV/°C/mV of nulled offset.

⁴Bias Current specifications are guaranteed at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

⁵Defined as the maximum safe voltage between inputs, such that neither exceeds ±10 V from ground.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for a 10 V Step	Package Description	Package Option
AD542JCHIPS	2.0 mV	20 μV/°C	5 μs	Bare Die	
AD542JH	2.0 mV	20 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542KH	1.0 mV	10 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542LH	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542SH	1.0 mV	15 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542SH/883B	1.0 mV	15 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD544JH	2.0 mV	20 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544KH	1.0 mV	10 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544LH	0.5 mV	5 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544SH	1.0 mV	15 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544SH/883B	1.0 mV	15 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD547JH	1.0 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547KH	0.5 mV	2 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547LH	0.25 mV	1 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547SCHIPS	0.5 mV	5 μV/°C	5 μs	Bare Die	
AD547SH/883B	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A

AD542/AD544/AD547—Typical Characteristics

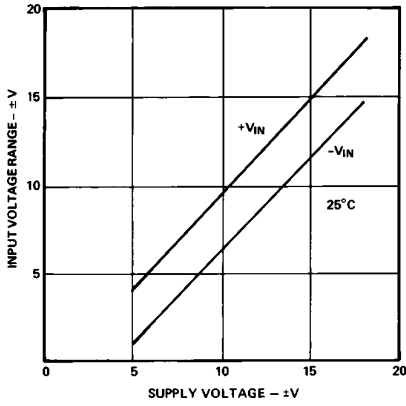


Figure 1. Input Voltage Range vs. Supply Voltage

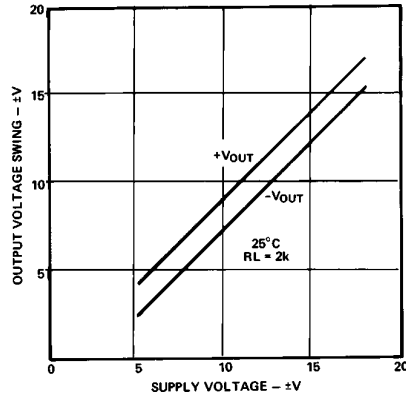


Figure 2. Output Voltage Swing vs. Supply Voltage

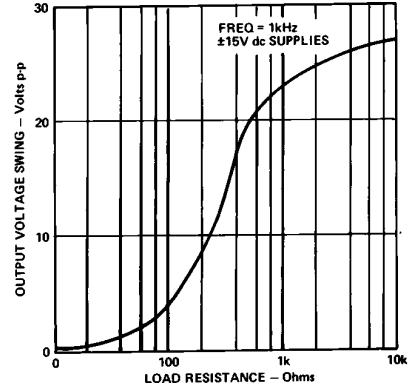


Figure 3. Output Voltage Swing vs. Load Resistance

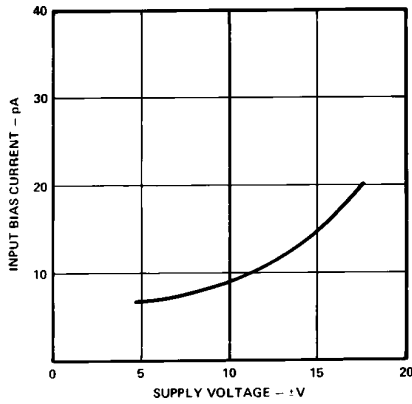


Figure 4. Input Bias Current vs. Supply Voltage

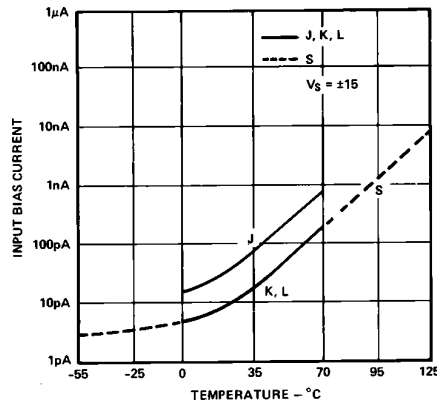


Figure 5. Input Bias Current vs. Temperature

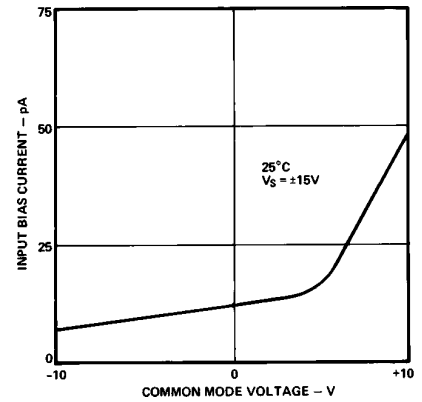


Figure 6. Input Bias Current vs. CMV

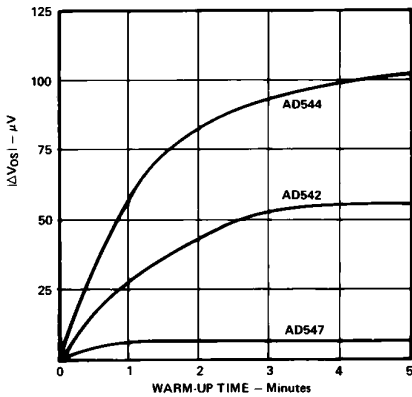


Figure 7. Change in Offset Voltage vs. Warm-Up Time

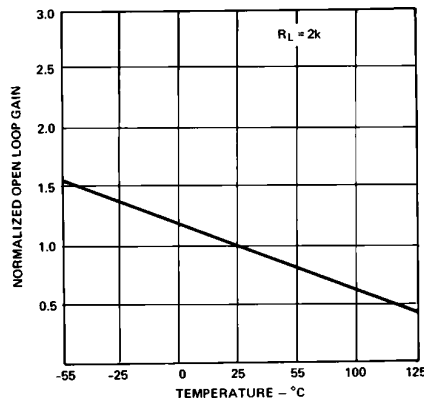


Figure 8. Open Loop Gain vs. Temperature

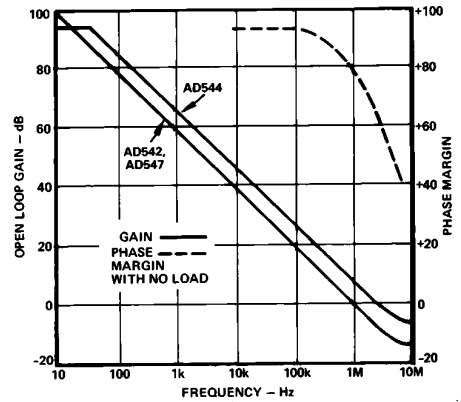


Figure 9. Open Loop Frequency Response

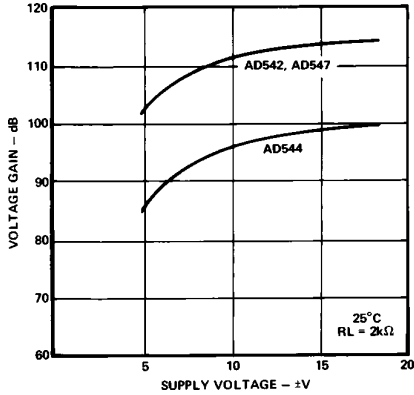


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

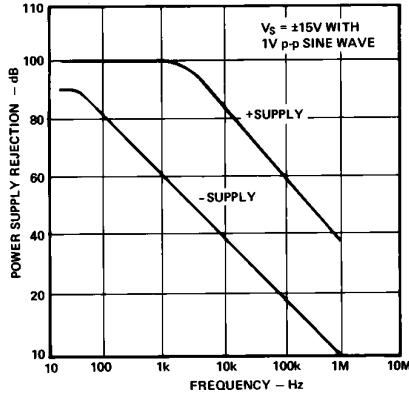


Figure 11. Power Supply Rejection vs. Frequency

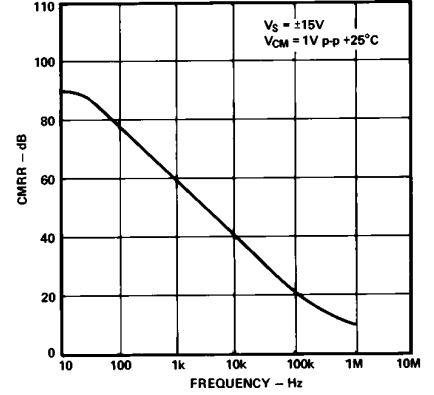


Figure 12. Common-Mode Rejection Ratio vs. Frequency

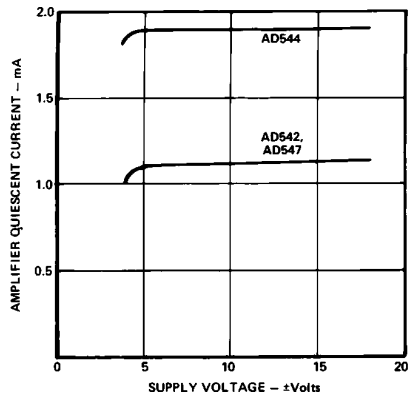


Figure 13. Quiescent Current vs. Supply Voltage

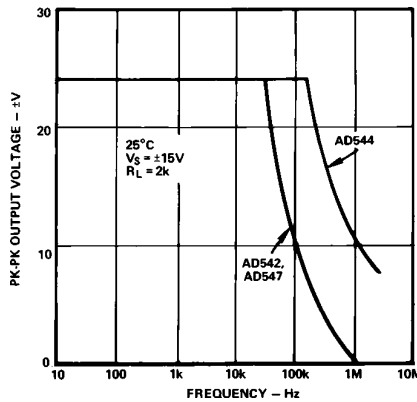


Figure 14. Large Signal Frequency Response

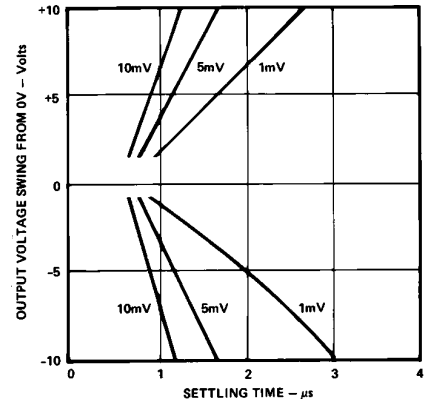


Figure 15. AD544 Output Swing and Error vs. Settling Time

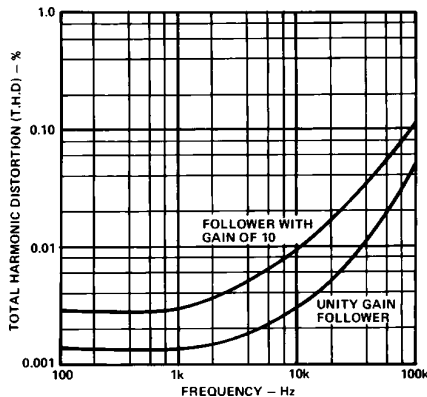


Figure 16. AD544 Total Harmonic Distortion vs. Frequency

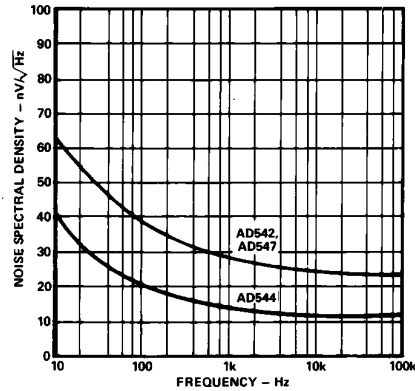


Figure 17. Input Noise Voltage Spectral Density

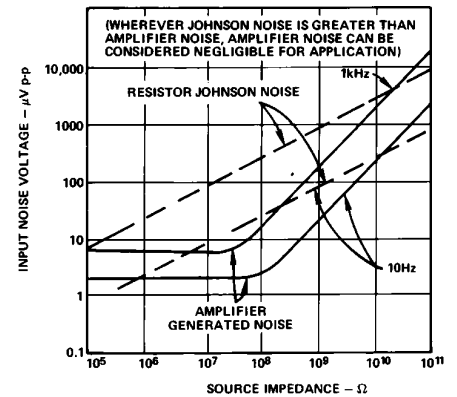


Figure 18. Total RMS Noise vs. Source Resistance

AD542/AD544/AD547

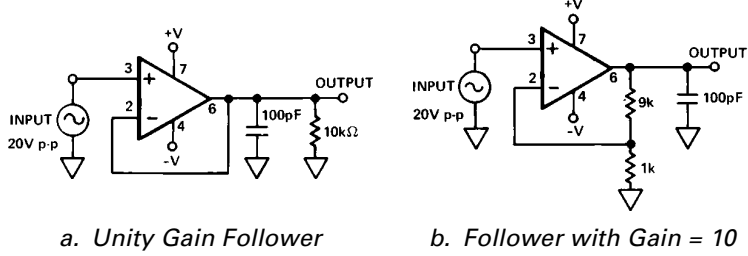


Figure 19. THD Test Circuits

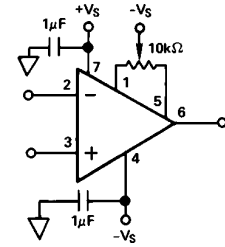


Figure 20. Standard Null Circuit

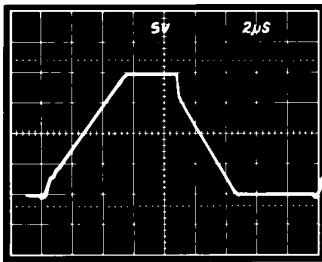


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

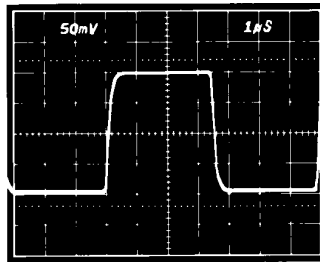


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

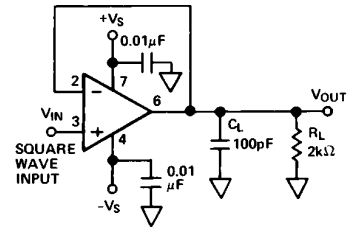


Figure 21c. Unity Gain Follower—AD542/AD547

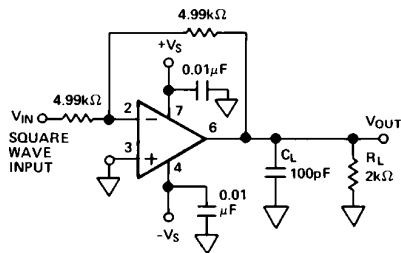


Figure 22a. Unity Gain Inverter AD542/AD547

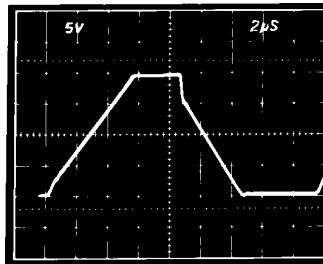


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

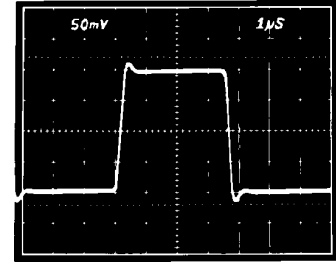


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

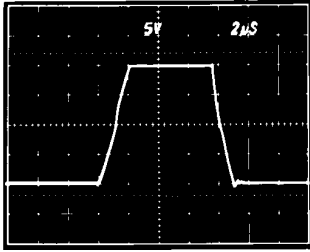


Figure 23a. Unity Gain Follower Pulse Response (Large Signal)

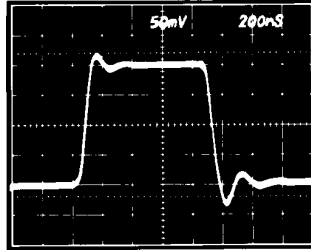


Figure 23b. Unity Gain Follower Pulse Response (Small Signal)

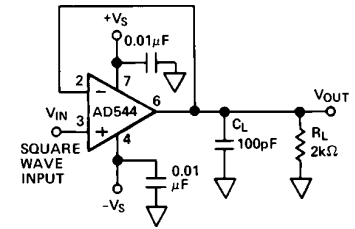


Figure 23c. Unity Gain Follower

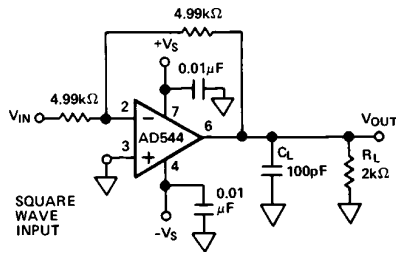


Figure 24a. Unity Gain Inverter

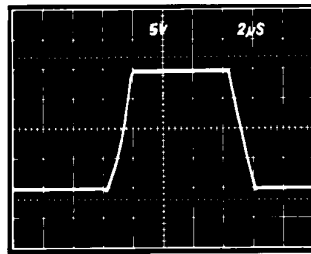


Figure 24b. Unity Gain Inverter Pulse Response (Large Signal)

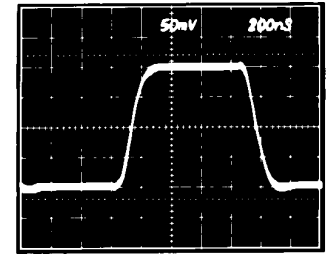


Figure 24c. Unity Gain Inverter Pulse Response (Small Signal)

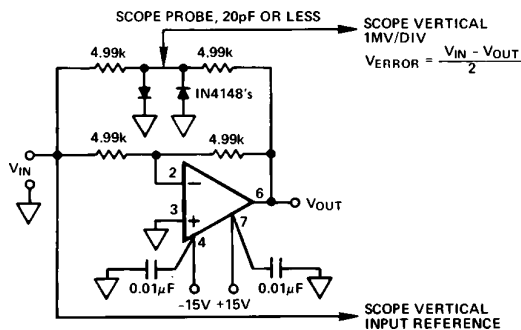


Figure 25. Settling Time Test Circuit

The upper trace of the oscilloscope photograph of Figure 26 shows the settling characteristic of the AD544. The lower trace represents the input to Figure 27. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.

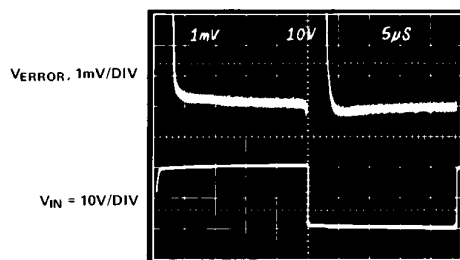


Figure 26. Settling Characteristic Detail—AD544

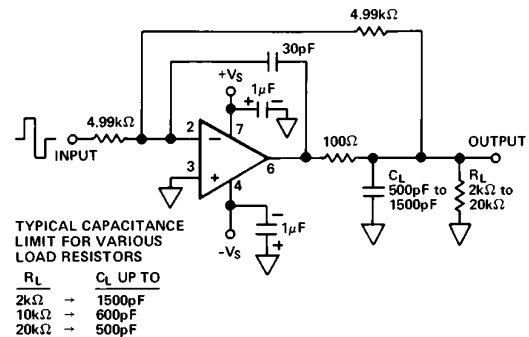


Figure 27. Circuit for Driving a Large Capacitance Load

The circuit in Figure 27 employs a 100 Ω isolation resistor which enables the amplifier to drive capacitance loads exceeding 500 pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low-pass filter formed by the 100 Ω series resistor and the load capacitance, C_L .

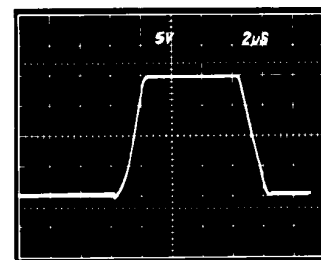


Figure 28. Transient Response $R_L = 2\text{ k}\Omega$
 $C_L = 500\text{ pF}$ —AD544

AD542/AD544/AD547

BiFET Application Hints

APPLICATION NOTES

The BiFET series was designed for high performance op amp applications that require true dc precision. To capitalize on all of the performance available from the BiFETs there are some practical error sources that should be considered.

The bias currents of JFET input amplifiers double with every 10°C increase in chip temperature. Therefore, minimizing the junction temperature of the chip will result in extending the performance limits of the device.

1. Heat dissipation due to power consumption is the main contributor to self-heating and can be minimized by reducing the power supplies to the lowest level allowed by the application.
2. The effects of output loading should be carefully considered. Greater power dissipation increases bias currents and decreases open loop gain.

GUARDING

The low input bias current (25 pA) and low noise characteristics of the high performance BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from these amplifiers. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit.

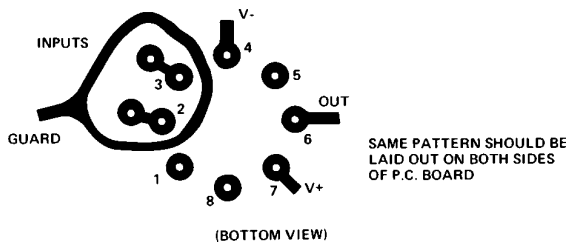


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The BiFET series is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ± 1 volt while maintaining the full differential input resistance of $10^{12} \Omega$. This makes the BiFET series suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the

current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate Zener protection schemes which often compromise overall performance. The BiFET series requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0 mA (for example, 100 k Ω for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

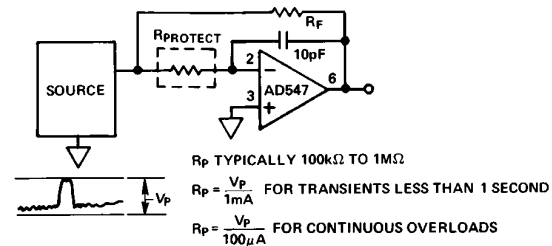


Figure 30. Input Protection

D/A CONVERTER APPLICATIONS

The BiFET series of operational amplifiers can be used with CMOS DACs to perform both 2-quadrant and 4-quadrant operation. The output impedance of a CMOS DAC varies with the digital word, thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The BiFET series with trimmed offset will minimize this effect. Additionally, the Schottky protection diodes recommended for use with many older CMOS DACs are not required when using one of the BiFET series amplifiers.

Figure 31a shows the AD547 and AD7541 configured for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit operates as a unipolar converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

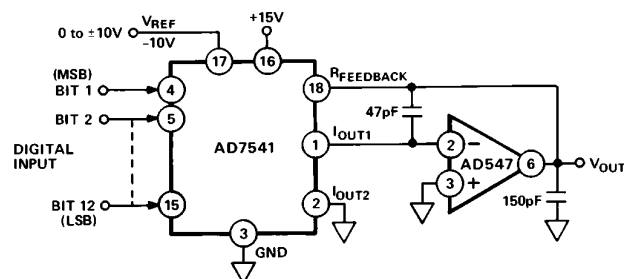


Figure 31a. AD547 Used as DAC Output Amplifier

AD542/AD544/AD547

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3 dB bandwidth is 50 kHz over the top 3 decades, 100 nA to 100 μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100 pF of shunt capacitance. For larger input capacitances a 20 pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply $V_1 = V_2 = -10.00$ V and adjust "Balance" for $V_{OUT} = 0.00$ V. Next apply $V_1 = -10.00$ V, $V_2 = -1.00$ V and adjust gain for $V_{OUT} = +1.00$ V. Repeat this procedure until gain and balance readings are within 2 mV of ideal values.

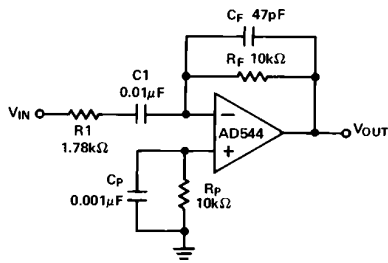


Figure 34. Differentiator

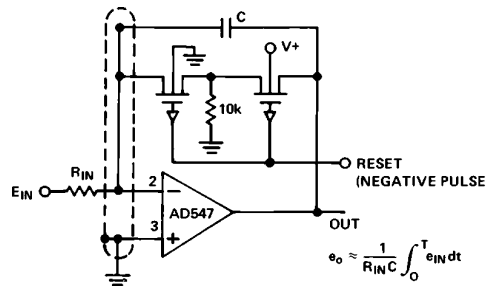


Figure 35. Low Drift Integrator and Low Leakage Guarded Reset

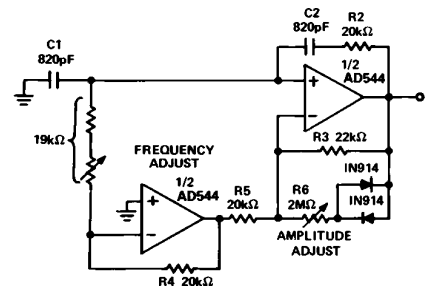


Figure 36. Wien-Bridge Oscillator- $f_0 = 10$ kHz

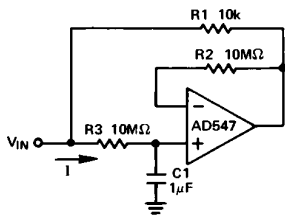


Figure 37. Capacitance Multiplier

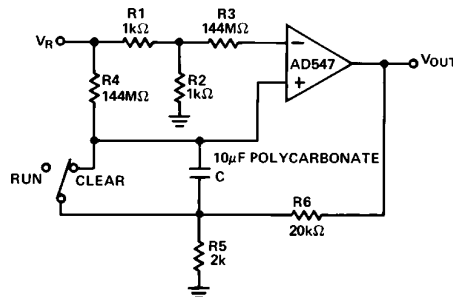


Figure 38. Long Interval Timer-1,000 Seconds

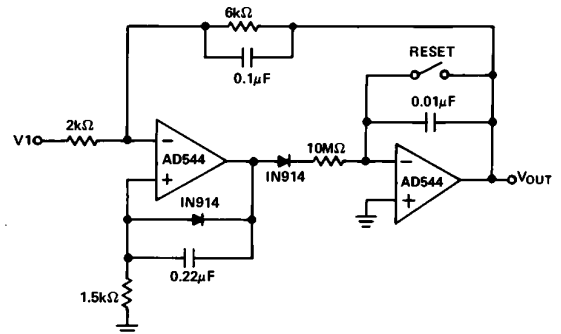


Figure 39. Positive Peak Detector

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO-99 (H-08A)

