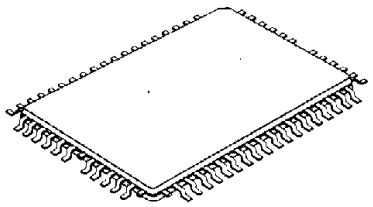
40-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

The KS0065B is a LCD driver LSI which is fabricated by low power CMOS technology. Bascially this LSI consists of 20 x 2bit bidirectional shift register, 20 x 2bit data latch ad 20 x 2 bit driver. (refer to Fig 1) This LSI can be used a common or segment driver.

60 QFP



FUNCTION

- **Dot matrix LCD driver with 40 channel output.**
- **Selectable function to use common/segment drivers simultaneously.**
- **Input/Output signal**
  - **— output; 20 × 2 channel waveform for LCD driving**
  - **— input ; - Serial display data and control pulse from the controller LSI.**
    - Bias voltage (V_1-V_6)

FEATURES

- **Display driving bias; static-1/5**
- **Power supply voltage; +5V ±10%**
- **Supply voltage for display: 0~-5V(V_{EE})**
- **interface**

driver (cascade connection)	controller
Other KS0065B, KS0063	KS0066

- **CMOS Process**
- **60QFP and bare chip available**

BLOCK DIAGRAM

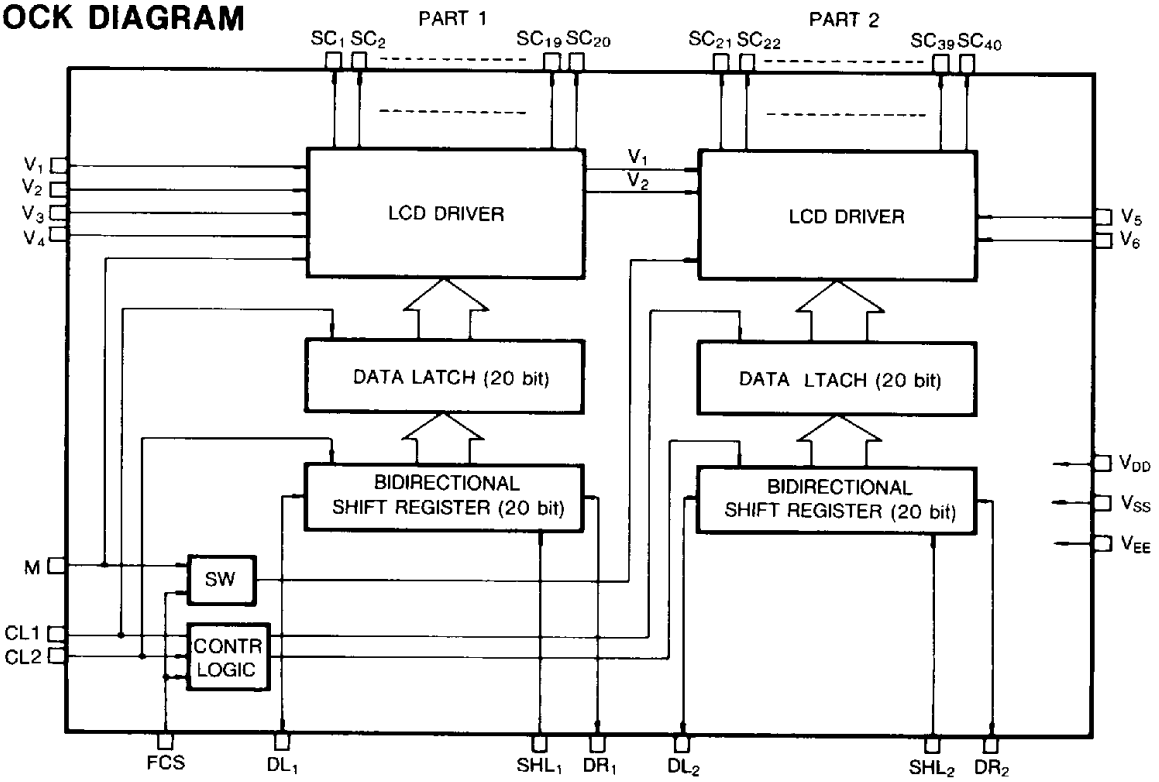


Fig. 1. KS0065B functional block diagram.

PIN CONFIGURATION

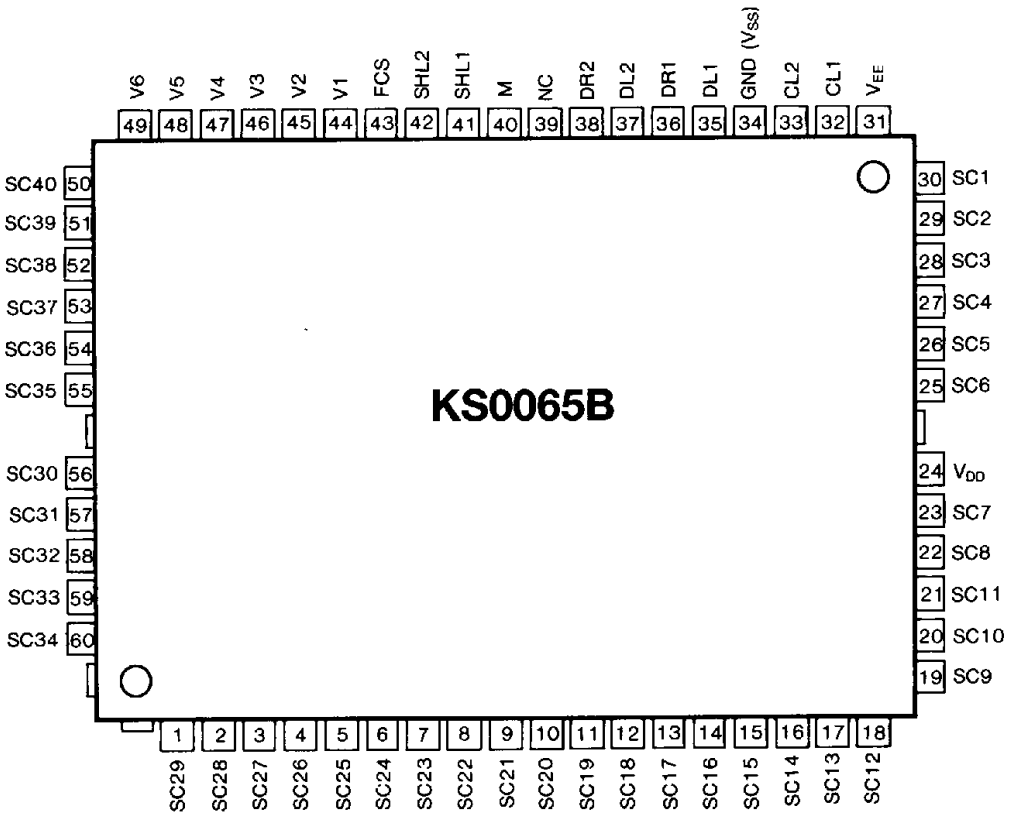


Fig. 2. 60 QFP Top View

<table>
<tr><th>PIN(No.)</th><th>INPUT/ OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(24)</td><td rowspan="3"></td><td colspan="2" rowspan="3">Power Supply</td><td>For logical circuit (+5V±10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(34)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td>For LCD driver circuit (−5V)</td></tr>
<tr><td>V_1 V_2 (44, 45)</td><td>Input</td><td colspan="2">Bias Vtg</td><td>Bias voltage level for LCD drive (select level)</td><td>power</td></tr>
<tr><td>SC_1~SC_{20}</td><td>Output</td><td rowspan="4">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V_3 V_4 (46, 47)</td><td>Input</td><td>Bias Vtg</td><td>Bias voltage level for LCD drive (nonselect level)</td><td>power</td></tr>
<tr><td>SHL1 (41)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1 (35, 36)</td><td>Input Output</td><td>Data input/output of Part 1 shift register</td><td>Controller or KS0065B</td></tr>
<tr><td>SC_{21}~SC_{40}</td><td>Output</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V5 V6 (48, 49)</td><td>Input</td><td>Bias Vtg</td><td>Bias voltage level for LCD drive (non select level)</td><td>power</td></tr>
<tr><td>SHL2 (42)</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2 (37, 38)</td><td>Input Output</td><td rowspan="4"></td><td rowspan="4"></td><td>Data input/output of Part 2 shift register</td><td>Controller or KS0065B Controller</td></tr>
<tr><td>M (40)</td><td>Input</td><td>Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr><tr><td rowspan="2">1</td><td>VSS</td><td rowspan="2">latch clock (⌐¬)</td><td rowspan="2">shift clock (⌐¬)</td><td rowspan="2">M</td></tr><tr><td>VDD</td></tr><tr><td rowspan="2">2</td><td>VSS</td><td rowspan="2">shift clock (¬⌐)</td><td rowspan="2">latch clock (¬⌐)</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>VDD</td></tr></table>Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td></tr>
<tr><td>CL1,CL2 (32, 33)</td><td>Input</td><td>Data shift /latch clock</td></tr>
<tr><td>FCS(43)</td><td>Input</td><td>Mode selection</td></tr>
<tr><td>NC (39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>N.C</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	−0.3∼+7.0	V
Driver supply voltage	V_{LCD}	V_{DD}−13.5∼V_{DD}+0.3	V
Input voltage 1	V_{IN1}	−0.3∼V_{DD}+0.3	V
Input voltage 2 (V_1-V_6)	V_{IN2}	V_{DD}+0.3∼V_{EE}−0.3	V
Operating temperature	T_{opr}	−20∼+75	°C
Storage temperature	T_{stg}	−55∼+125	°C

* Voltage greater than above may damage to the circuit
* V_{EE}: connect a protection resistor (220Ω ±5%)

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD}=+5V±10%, V_{EE}=−5V±10%, V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Supply current*	I_{DD}	f_{CL2}=400KHz	—	1	mA	—
	I_{EE}	f_{CL1}=1kHz	—	10	μA	
Input voltage	V_{IH}	—	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2 DR1, DR2, SHL1, SHL2, M, FCS
	V_{IL}		0	0.3 V_{DD}		
Input leakage current	I_{IL}	V_{IN}=0-V_{DD}	−5	5	μA	
Output Voltage	V_{OH}	I_{OH}=−0.4mA	V_{DD}−0.4	—	V	DL1, DL2, DR1, DR2
	V_{OL}	I_{OL}=+0.4mA	—	0.4		
Voltage descending	V_{d1}	I_{ON}=0.1mA for one of SC1-SC40	—	1.1		V(V_1-V_6)-SC(SC1-SC40)
	V_{d2}	I_{ON}=0.05mA for each SC1-SC40	—	1.5		
Leakage current	I_{v1}	V_{IN}=V_{DD}∼V_{EE} (Output SC1-SC40: floating)	−10	10	μA	V_1-V_6

AC CHARACTERISTICS (V_{DD}=+5V±10%, V_{EE}=−5V±10%, V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f_{CL}	—	—	400	KHz	CL2
Clock high level width	t_{CWH}	—	800	—	ns	CL1, CL2
Clock low level width	t_{CWL}	—	800	—		CL2
Clock set-up time	t_{SL}	from CL2 to CL1	500	—		CL1, CL2
	t_{LS}	from CL1 to CL2	500	—		
Clock rise/fall time	t_{CT}	—	—	200		
Data set-up time	t_{SU}	—	300	—		DL1, DL2, DR1, DR2, FLM
Data hold time	t_{DH}	—	300	—		
Data delay time	t_{PD}	CL=15pF	—	500		DL1, DL2, DR1, DR2

* Input/output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".

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TIMING CHARACTERISTICS

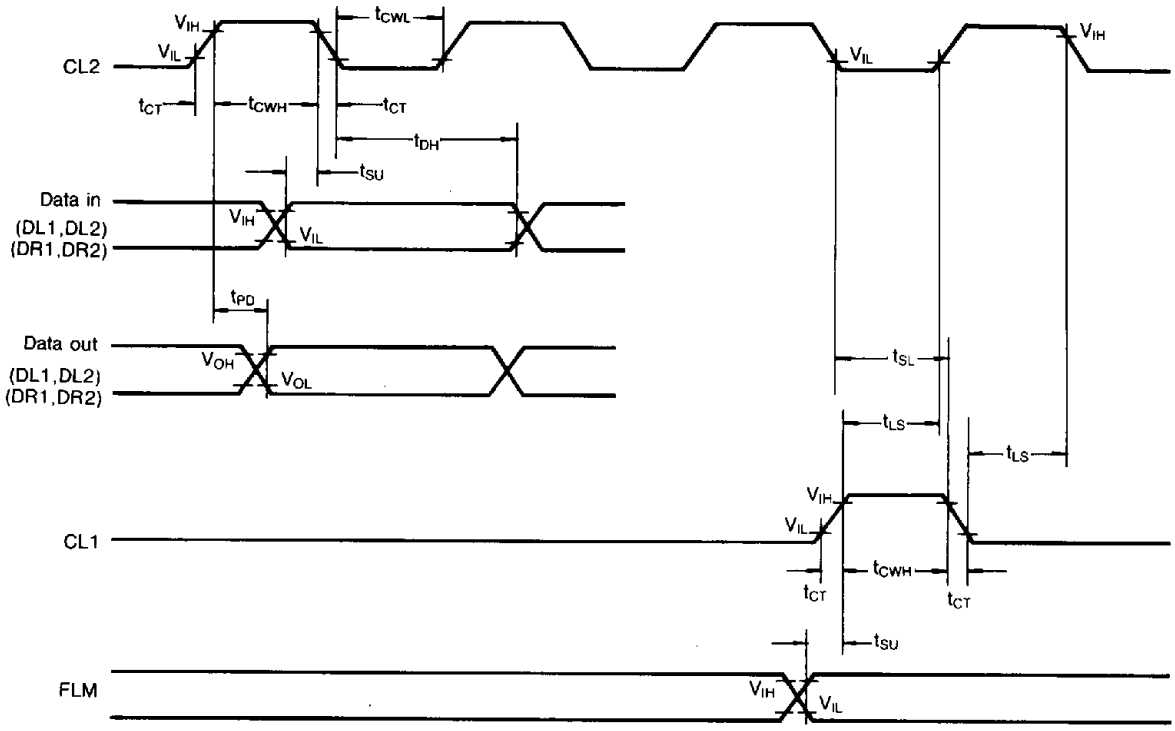

Fig. 3. AC characteristics

FUNCTIONAL DESCRIPTION

1) To drive segment type

When the FCS is connected to Vss, KS0065B(SC1-SC40) is operated as segment driver.(refer to fig 4)

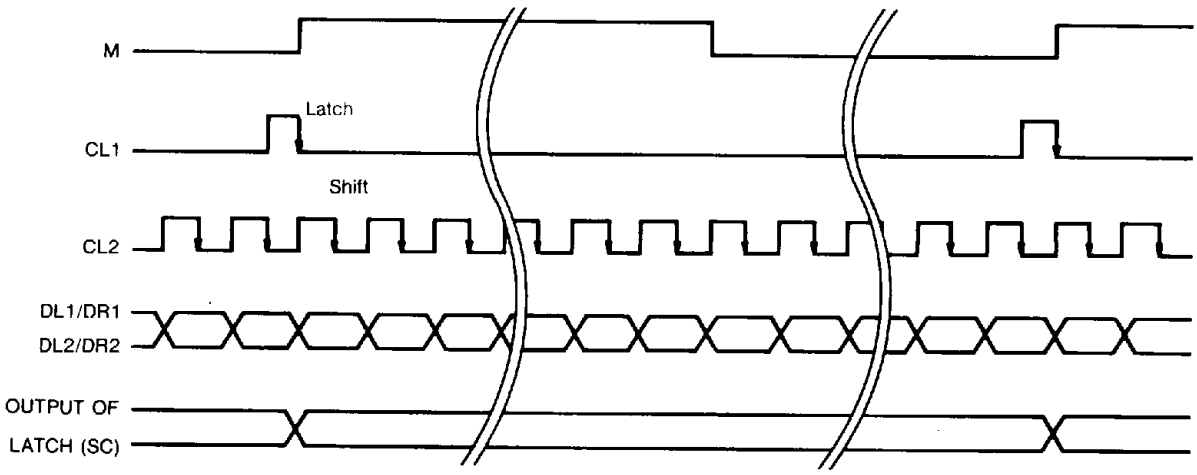

Fig. 4. Segment Data Waveforms

2) To drive common type

When the FCS is connected to VDD, only part2(SC21-SC40)of KS0065B is operated as common driver.(refer to Fig 5).

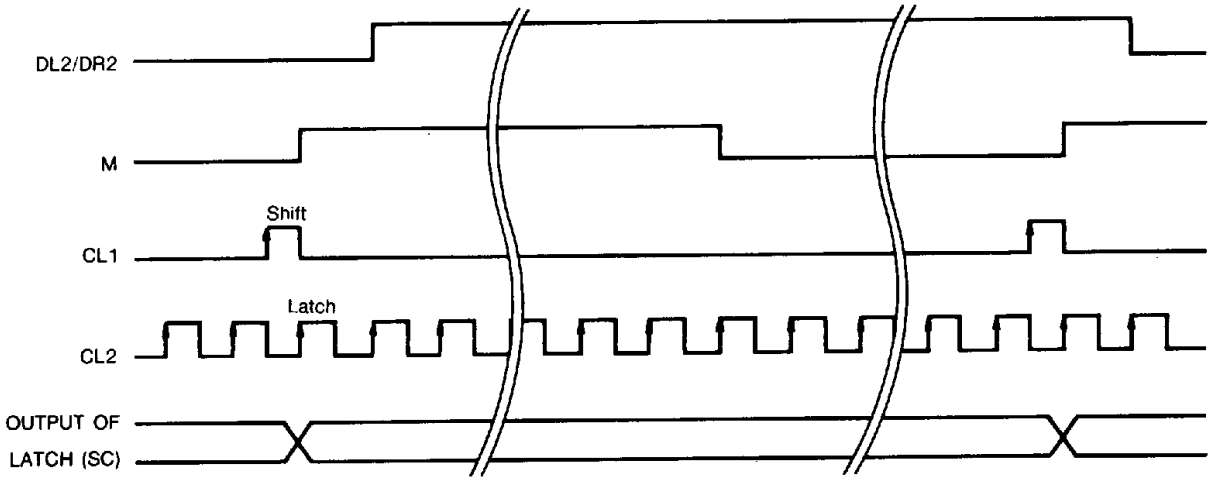

Fig. 5. Common Data Waveforms

LCD OUTPUT WAVEFORMS

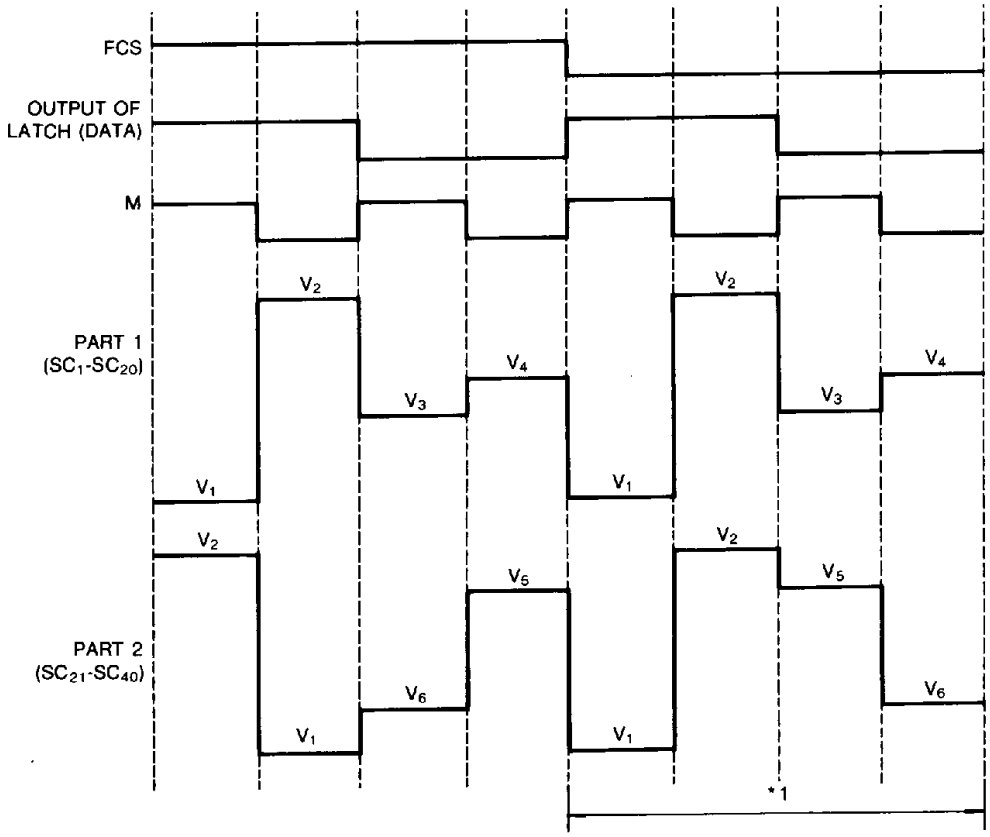

Fig. 6. Output waveform

***1: To use for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.**

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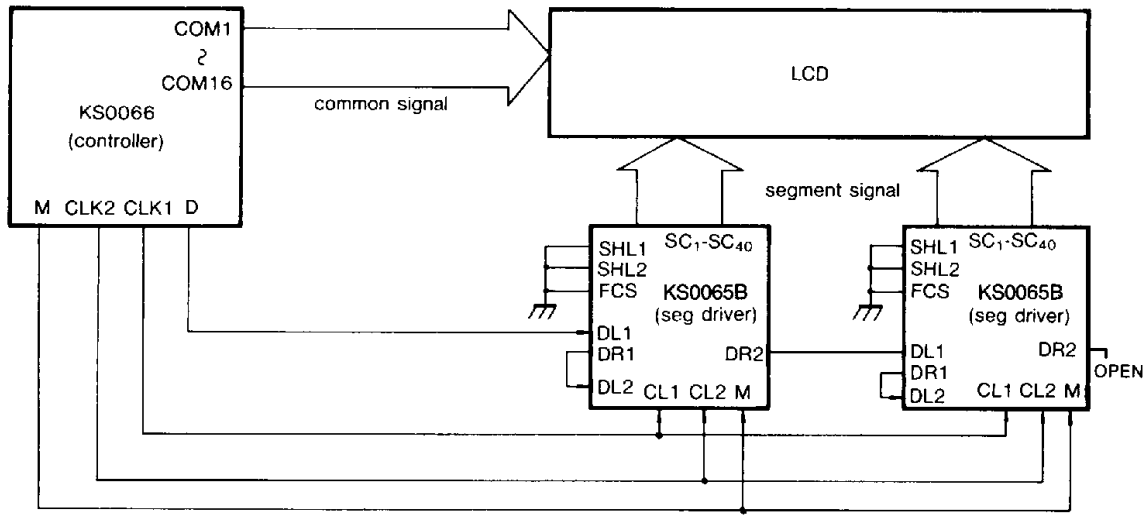
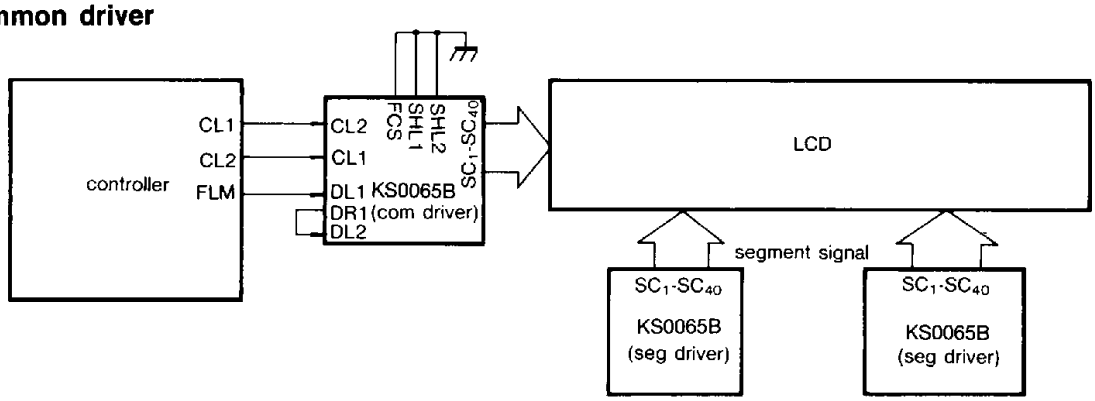
APPLICATION CIRCUIT

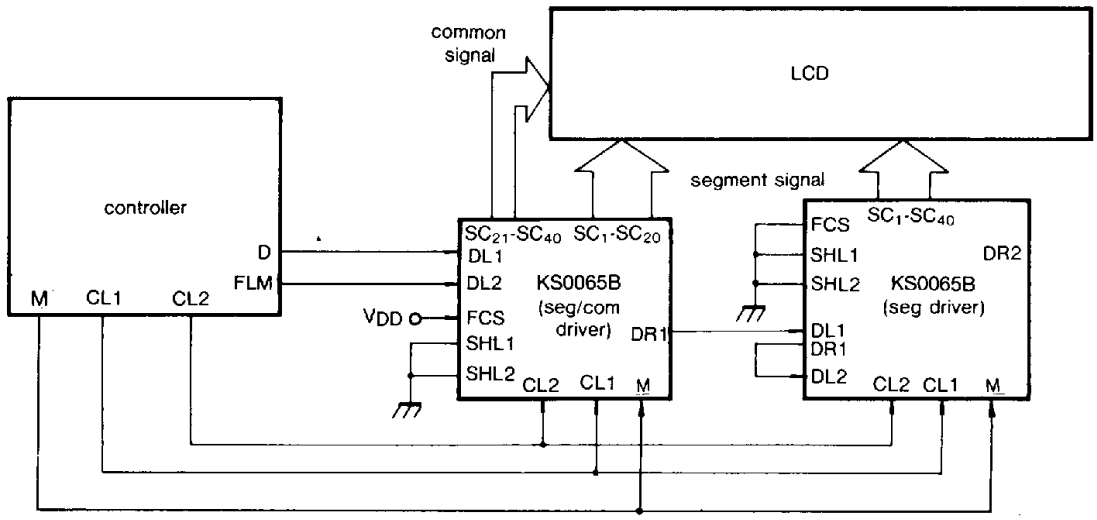
1) Segment driver



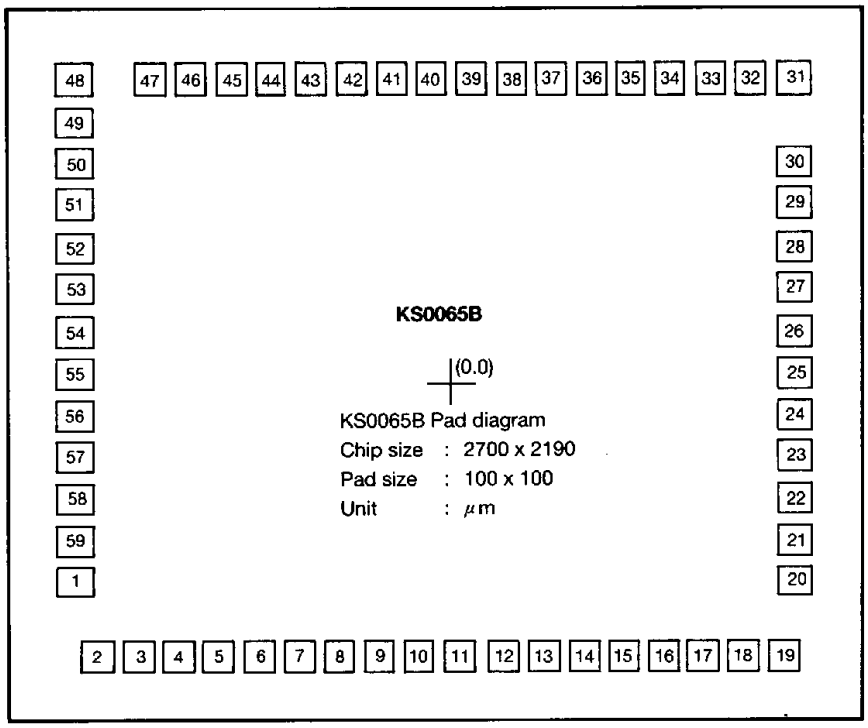
2) Common driver



3) Segment/common driver



PAD DIAGRAM



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PAD LOCATION

UNIT [um]

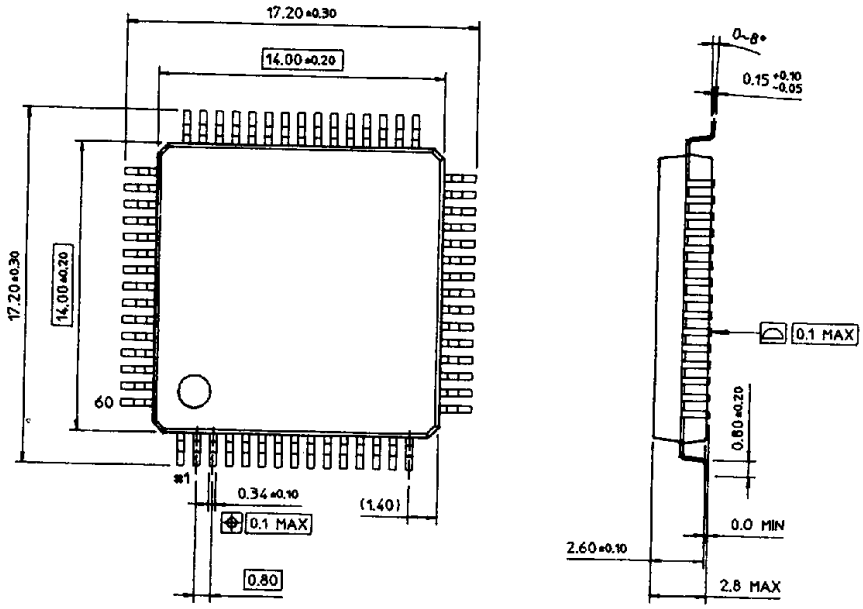
PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y
1	V_{EE}	-1120.2	-642.5	31	SC_{28}	1117.5	865.2
2	CL_1	-1062.5	-865.2	32	SC_{27}	992.5	865.2
3	CL_2	-937.5	-865.2	33	SC_{26}	867.5	865.2
4	V_{SS}	-812.5	-865.2	34	SC_{25}	742.5	865.2
5	DL_1	-687.5	-865.2	35	SC_{24}	617.5	865.2
6	DR_1	-562.5	-865.2	36	SC_{23}	492.5	865.2
7	DL_2	-437.5	-865.2	37	SC_{22}	367.5	865.2
8	DR_2	-312.5	-865.2	38	SC_{21}	242.5	865.2
9	M	-187.5	-642.5	39	SC_{20}	117.5	865.2
10	SHL_1	-62.5	-865.2	40	SC_{19}	-7.5	865.2
11	SHL_2	62.5	-865.2	41	SC_{18}	-132.5	865.2
12	FCS	187.5	-865.2	42	SC_{17}	-257.5	865.2
13	V_1	332.5	-865.2	43	SC_{16}	-382.5	865.2
14	V_2	457.5	-865.2	44	SC_{15}	-507.5	865.2
15	V_3	582.5	-865.2	45	SC_{14}	-632.5	865.2
16	V_4	707.5	-865.2	46	SC_{13}	-757.5	865.2
17	V_5	832.5	-865.2	47	SC_{12}	-882.5	865.2
18	V_6	957.5	-865.2	48	SC_9	-1120.2	857.5
19	SC_{40}	1082.5	-865.2	49	SC_{10}	-1120.2	732.5
20	SC_{39}	1120.2	-627.5	50	SC_{11}	-1120.2	607.5
21	SC_{38}	1120.2	-502.5	51	SC_8	-1120.2	482.5
22	SC_{37}	1120.2	-377.5	52	SC_7	-1120.2	357.5
23	SC_{36}	1120.2	-252.5	53	V_{DD}	-1120.2	232.5
24	SC_{35}	1120.2	-127.5	54	SC_6	-1120.2	107.5
25	SC_{30}	1120.2	-2.5	55	SC_5	-1120.2	-17.5
26	SC_{31}	1120.2	122.5	56	SC_4	-1120.2	-142.5
27	SC_{32}	1120.2	247.5	57	SC_3	-1120.2	-267.5
28	SC_{33}	1120.2	372.5	58	SC_2	-1120.2	-392.5
29	SC_{34}	1120.2	497.5	59	SC_1	-1120.2	-517.5
30	SC_{29}	1120.2	622.5				

Note : (0.0) is center in the chip

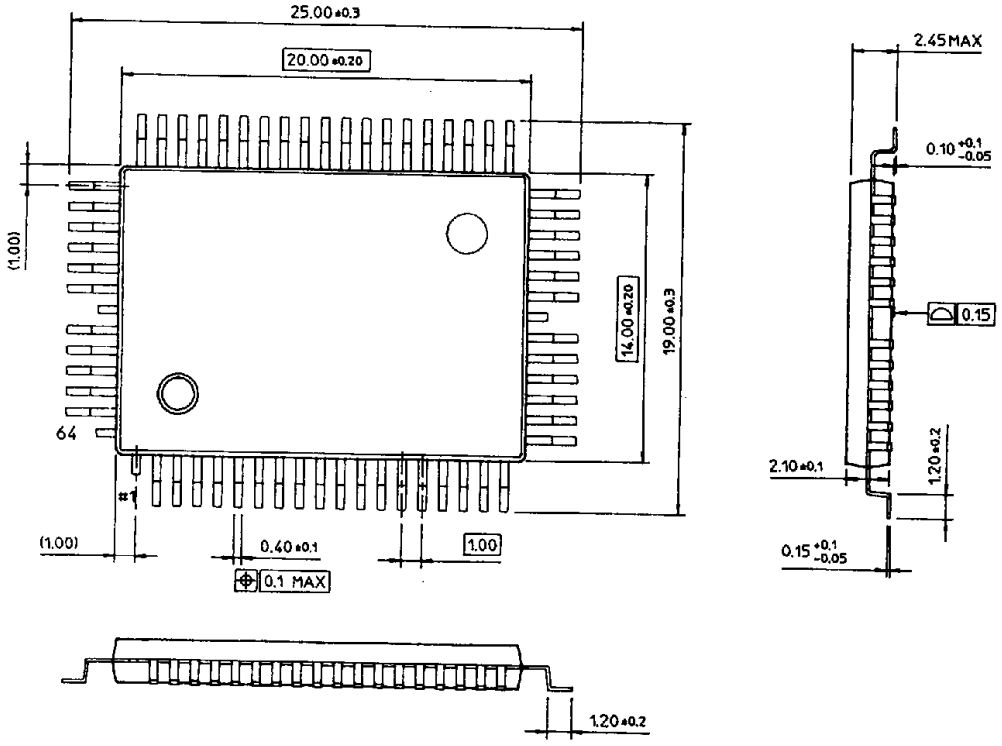
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



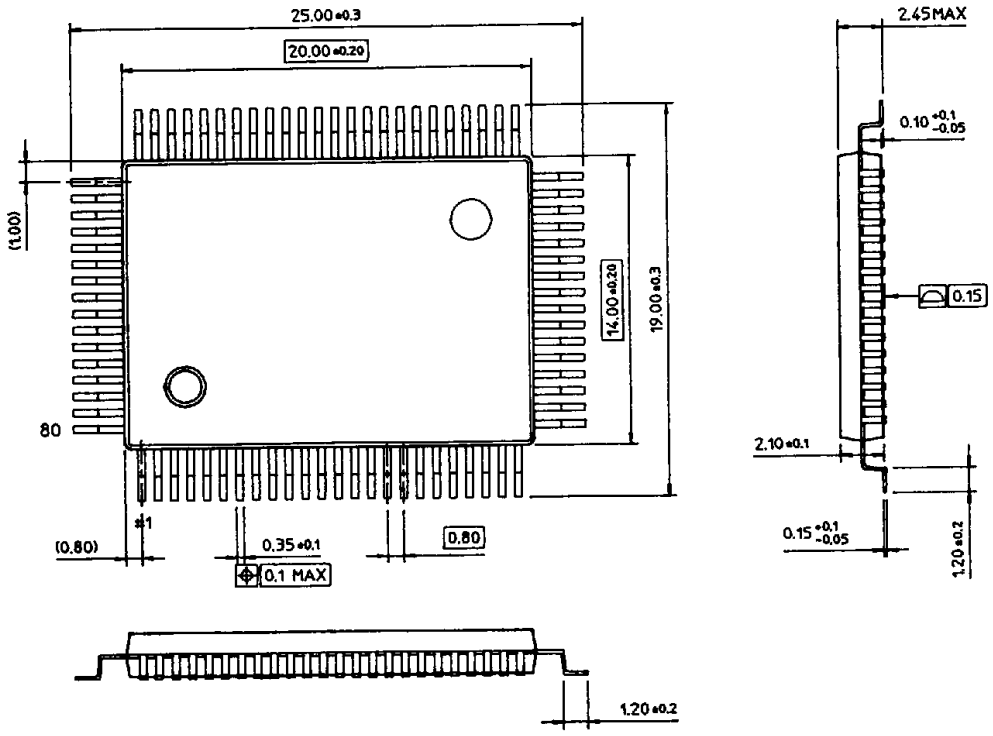
64-QFP-1420D



PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



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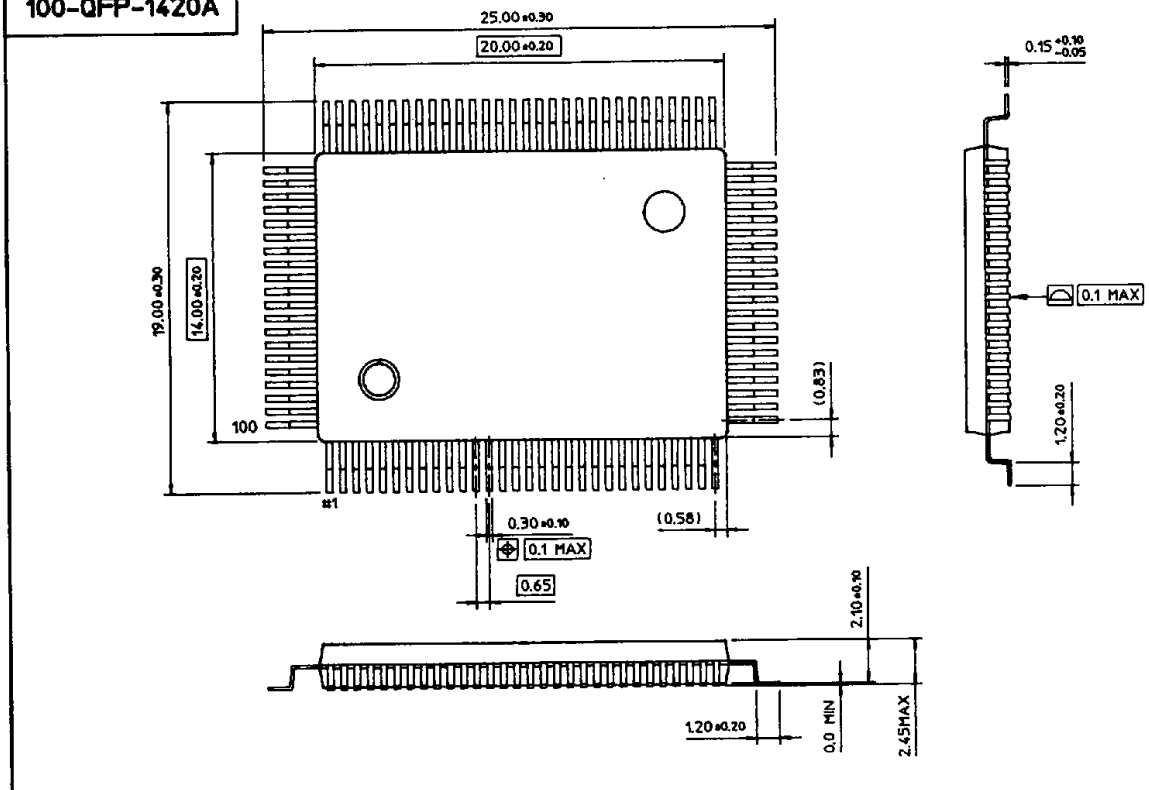

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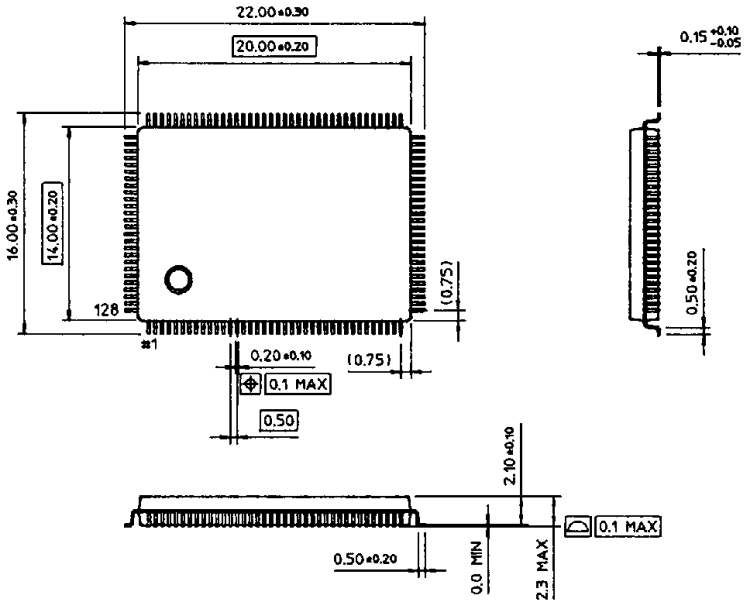
7964142 0022067 5T3

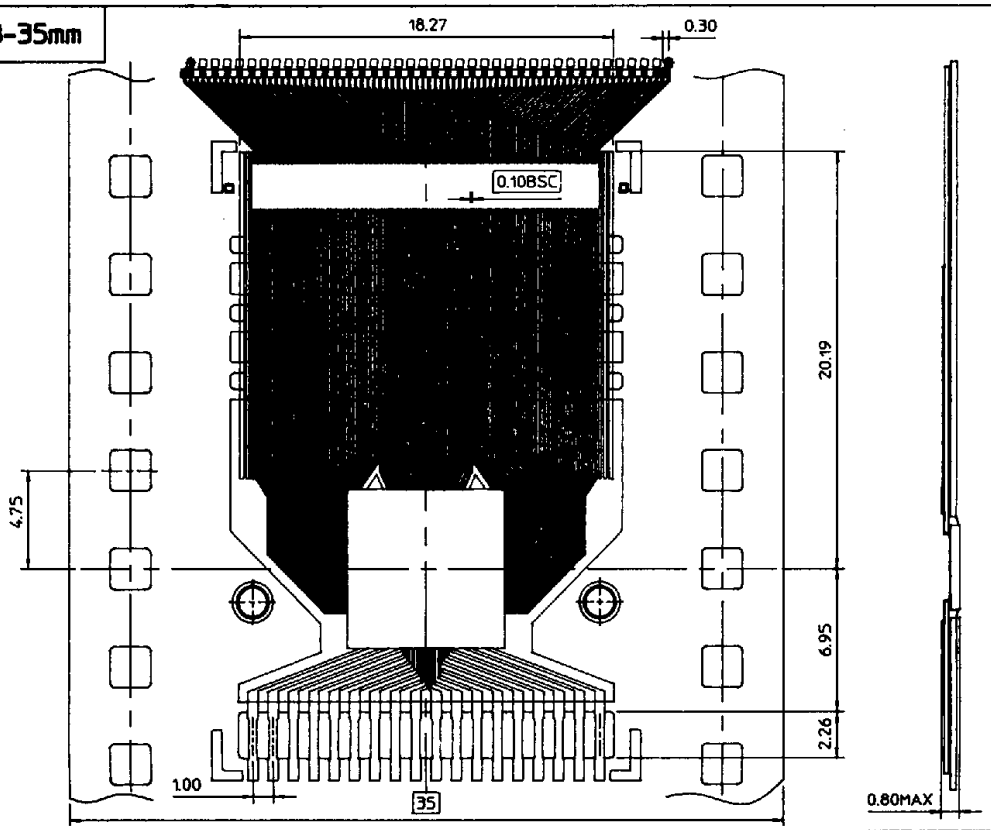
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm



3

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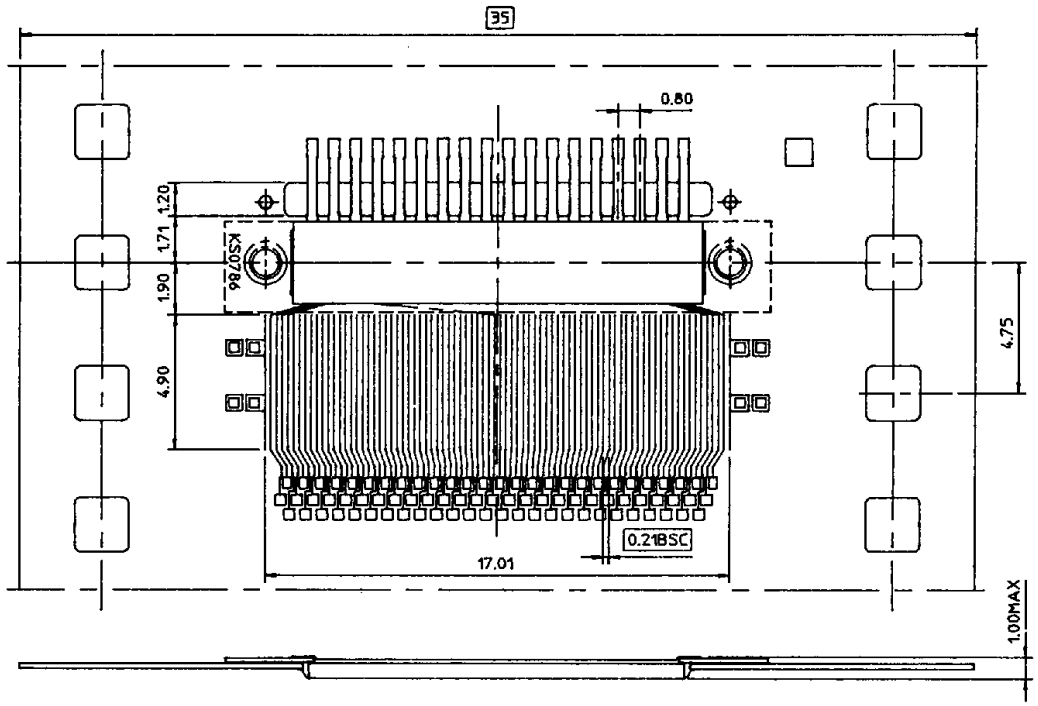
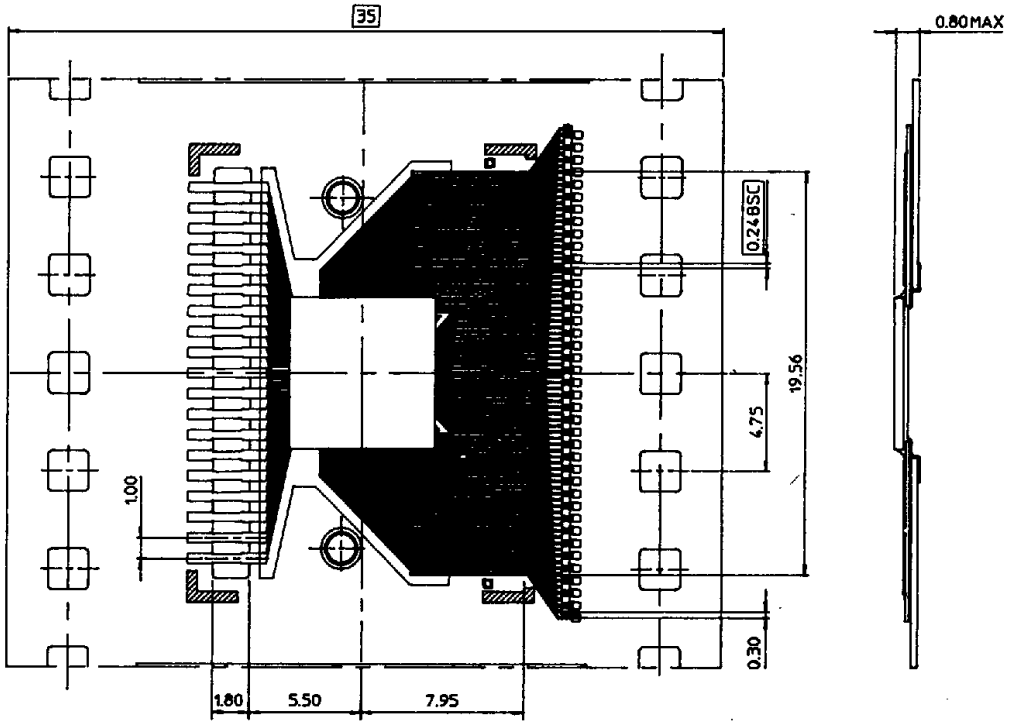
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



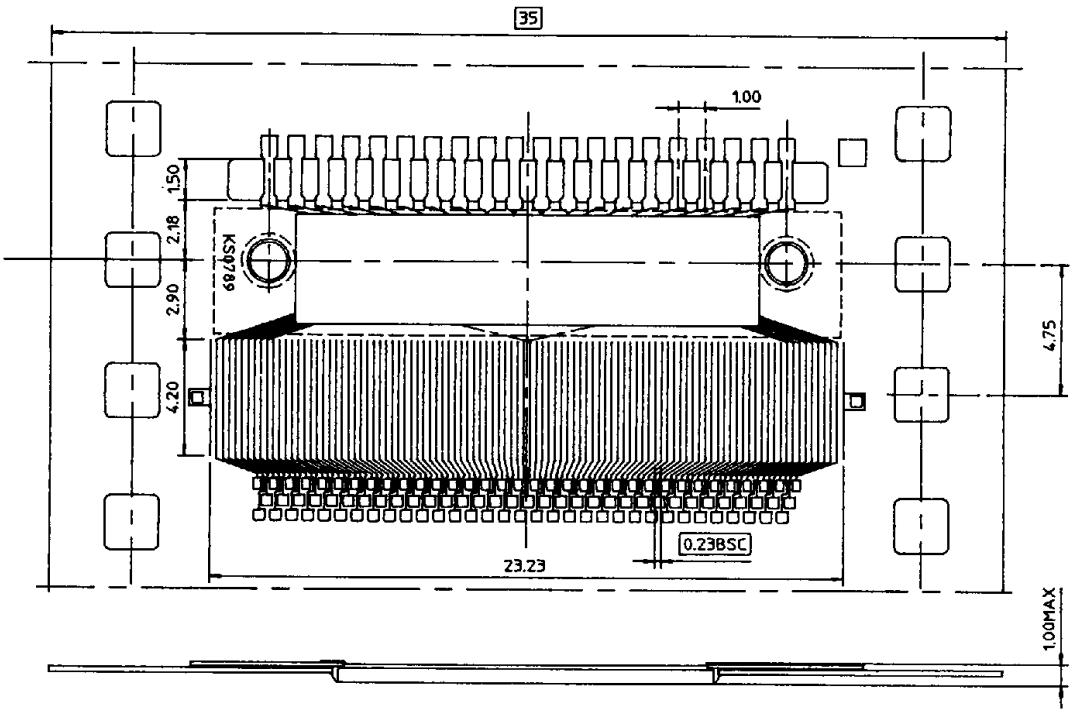
99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm



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