

Features

• ENHANCEMENTS

- ispLSI 2032A is Fully Form and Function Compatible to the ispLSI 2032, with Identical Timing Specifications and Packaging
- ispLSI 2032A is Built on an Advanced 0.35 Micron E²CMOS[®] Technology

• HIGH DENSITY PROGRAMMABLE LOGIC

- 1000 PLD Gates
- 32 I/O Pins, Two Dedicated Inputs
- 32 Registers
- High Speed Global Interconnect
- Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
- Small Logic Block Size for Random Logic

• HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY

- $f_{max} = 180$ MHz Maximum Operating Frequency
- $t_{pd} = 5.0$ ns Propagation Delay
- TTL Compatible Inputs and Outputs
- Electrically Erasable and Reprogrammable
- Non-Volatile
- 100% Tested at Time of Manufacture
- Unused Product Term Shutdown Saves Power

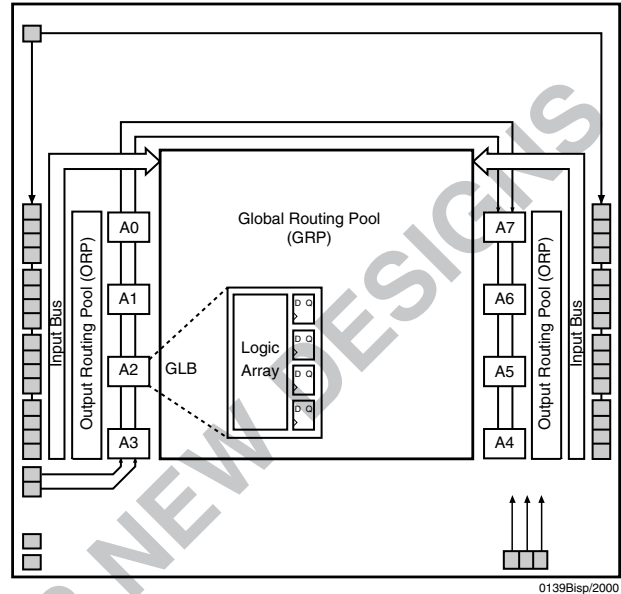
• IN-SYSTEM PROGRAMMABLE

- In-System Programmable (ISP[™]) 5V Only
- Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
- Reprogram Soldered Devices for Faster Prototyping

• OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS

- Complete Programmable Device Can Combine Glue Logic and Structured Designs
- Enhanced Pin Locking Capability
- Three Dedicated Clock Input Pins
- Synchronous and Asynchronous Clocks
- Programmable Output Slew Rate Control to Minimize Switching Noise
- Flexible Pin Placement
- Optimized Global Routing Pool Provides Global Interconnectivity
- Lead-Free Package Options

Functional Block Diagram



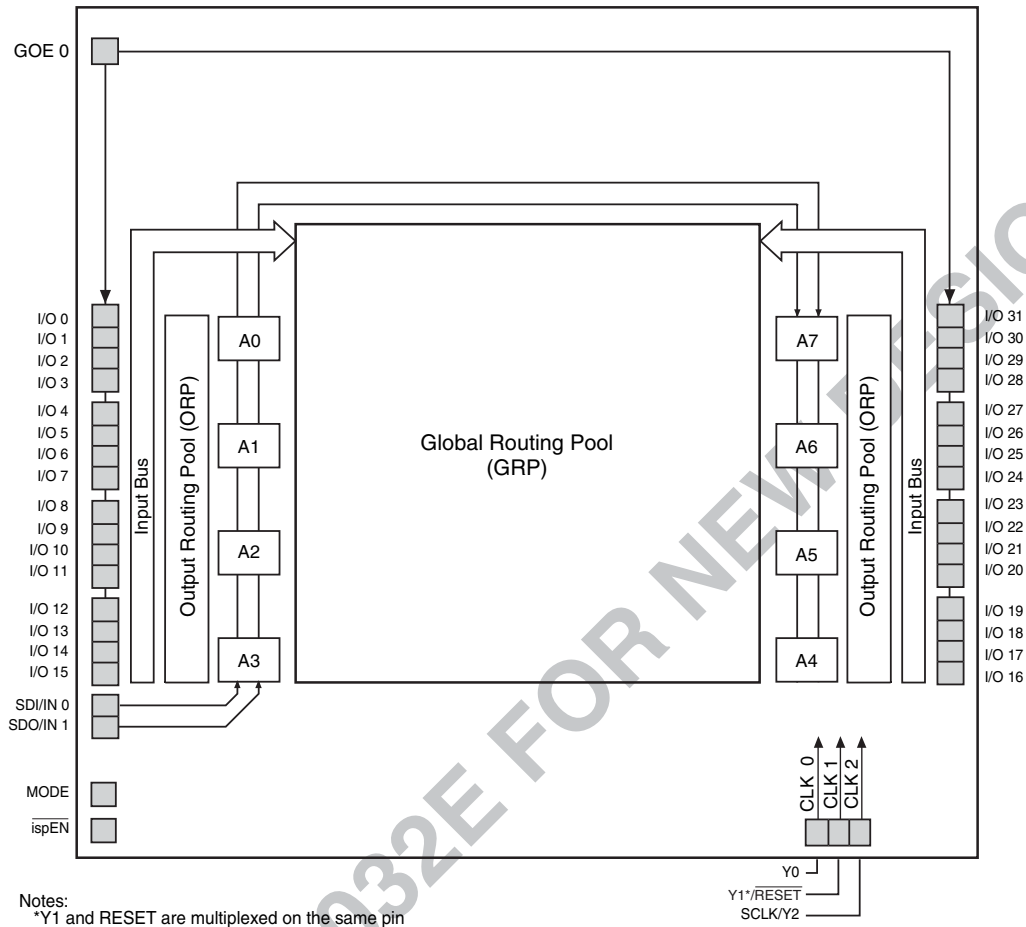
Description

The ispLSI 2032 and 2032A are High Density Programmable Logic Devices. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 and 2032A feature 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 and 2032A offer non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on these devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (Figure 1). There are a total of eight GLBs in the ispLSI 2032 and 2032A devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 2032/A Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI 2032 and 2032A device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells.

All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2032 and 2032A devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings ¹

Supply Voltage V_{CC} -0.5 to +7.0V
 Input Voltage Applied..... -2.5 to $V_{CC} + 1.0V$
 Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

| SYMBOL | PARAMETER | | MIN. | MAX. | UNITS |
|----------|--------------------|--|------|--------------|-------|
| V_{CC} | Supply Voltage | Commercial $T_A = 0^\circ C$ to $+ 70^\circ C$ | 4.75 | 5.25 | V |
| | | Industrial $T_A = -40^\circ C$ to $+ 85^\circ C$ | 4.5 | 5.5 | V |
| V_{IL} | Input Low Voltage | | 0 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | $V_{CC} + 1$ | V |

Table 2 - 0005/2032

Capacitance ($T_A = 25^\circ C$, $f = 1.0$ MHz)

| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|--------|-----------------------------|---------|-------|-----------------------------------|
| C_1 | Dedicated Input Capacitance | 6 | pf | $V_{CC} = 5.0V$, $V_{IN} = 2.0V$ |
| C_2 | I/O Capacitance | 7 | pf | $V_{CC} = 5.0V$, $V_{IO} = 2.0V$ |
| C_3 | Clock Capacitance | 10 | pf | $V_{CC} = 5.0V$, $V_Y = 2.0V$ |

Table 2-0006/2032

Data Retention Specifications

| PARAMETER | MINIMUM | MAXIMUM | UNITS |
|------------------------|---------|---------|--------|
| Data Retention | 20 | – | Years |
| Erase/Reprogram Cycles | 10000 | – | Cycles |

Table 2-0008A-isp

Switching Test Conditions

| | | |
|--|------------------|----------|
| Input Pulse Levels | GND to 3.0V | |
| Input Rise and Fall Time 10% to 90% | -135, -150, -180 | ≤ 1.5 ns |
| | -80, -110 | ≤ 3 ns |
| Input Timing Reference Levels | 1.5V | |
| Output Timing Reference Levels | 1.5V | |
| Output Load | See Figure 2 | |

3-state levels are measured 0.5V from steady-state active level.

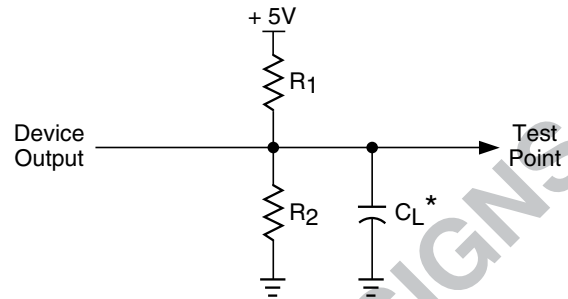
Table 2-0003/2032

Output Load Conditions (see Figure 2)

| TEST CONDITION | | R1 | R2 | CL |
|----------------|--------------------------------------|------|------|------|
| A | | 470Ω | 390Ω | 35pF |
| B | Active High | ∞ | 390Ω | 35pF |
| | Active Low | 470Ω | 390Ω | 35pF |
| C | Active High to Z at $V_{OH}-0.5V$ | ∞ | 390Ω | 5pF |
| | Active Low to Z at $V_{OL}+0.5V$ | 470Ω | 390Ω | 5pF |

Table 2 - 0004A

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. ³ | MAX. | UNITS | |
|----------------|---|--|------------|-------------------|------|---------------|----|
| V_{OL} | Output Low Voltage | $I_{OL} = 8 \text{ mA}$ | - | - | 0.4 | V | |
| V_{OH} | Output High Voltage | $I_{OH} = -4 \text{ mA}$ | 2.4 | - | - | V | |
| I_{IL} | Input or I/O Low Leakage Current | $0V \leq V_{IN} \leq V_{IL} (\text{Max.})$ | - | - | -10 | μA | |
| I_{IH} | Input or I/O High Leakage Current | $3.5V \leq V_{IN} \leq V_{CC}$ | - | - | 10 | μA | |
| I_{IL-isp} | $\overline{\text{ispEN}}$ Input Low Leakage Current | $0V \leq V_{IN} \leq V_{IL}$ | - | - | -150 | μA | |
| I_{IL-PU} | I/O Active Pull-Up Current | $0V \leq V_{IN} \leq V_{IL}$ | - | - | -150 | μA | |
| I_{OS}^1 | Output Short Circuit Current | $V_{CC} = 5V, V_{OUT} = 0.5V$ | - | - | -200 | mA | |
| $I_{CC}^{2,4}$ | Operating Power Supply Current | $V_{IL} = 0.0V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$ | Comm. | -180, -150 | - | 60 | mA |
| | | | | Others | - | 40 | mA |
| | | | Industrial | - | 40 | mA | |

Table 2-0007/2032

- One output at a time for a maximum duration of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using two 16-bit counters.
- Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$.
- Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

| PARAMETER | TEST COND. ⁴ | # ² | DESCRIPTION ¹ | -180 | | -150 | | -135 | | UNITS |
|-------------------------|-------------------------|----------------|--|------|------|------|------|------|------|-------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t _{pd1} | A | 1 | Data Prop. Delay, 4PT Bypass, ORP Bypass | – | 5.0 | – | 5.5 | – | 7.5 | ns |
| t _{pd2} | A | 2 | Data Prop. Delay | – | 7.5 | – | 8.0 | – | 10.0 | ns |
| f _{max} | A | 3 | Clk Frequency with Internal Feedback ³ | 180 | – | 154 | – | 137 | – | MHz |
| f _{max} (Ext.) | – | 4 | Clk Frequency with Ext. Feedback ($\frac{1}{t_{su2} + t_{co1}}$) | 125 | – | 111 | – | 100 | – | MHz |
| f _{max} (Tog.) | – | 5 | Clk Frequency, Max. Toggle | 200 | – | 167 | – | 167 | – | MHz |
| t _{su1} | – | 6 | GLB Reg Setup Time before Clk, 4 PT Bypass | 3.0 | – | 3.0 | – | 4.0 | – | ns |
| t _{co1} | A | 7 | GLB Reg. Clk to Output Delay, ORP Bypass | – | 4.0 | – | 4.5 | – | 4.5 | ns |
| t _{h1} | – | 8 | GLB Reg. Hold Time after Clk, 4 PT Bypass | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| t _{su2} | – | 9 | GLB Reg. Setup Time before Clk | 4.0 | – | 4.5 | – | 5.5 | – | ns |
| t _{co2} | – | 10 | GLB Reg. Clk to Output Delay | – | 4.5 | – | 5.0 | – | 5.5 | ns |
| t _{h2} | – | 11 | GLB Reg. Hold Time after Clk | 0.0 | – | 0.0 | – | 0.0 | – | ns |
| t _{r1} | A | 12 | Ext. Reset Pin to Output Delay | – | 7.0 | – | 8.0 | – | 10.0 | ns |
| t _{rw1} | – | 13 | Ext. Reset Pulse Duration | 4.0 | – | 4.5 | – | 5.0 | – | ns |
| t _{ptoen} | B | 14 | Input to Output Enable | – | 10.0 | – | 11.0 | – | 12.0 | ns |
| t _{ptoedis} | C | 15 | Input to Output Disable | – | 10.0 | – | 11.0 | – | 12.0 | ns |
| t _{goeen} | B | 16 | Global OE Output Enable | – | 5.0 | – | 5.0 | – | 6.0 | ns |
| t _{goedis} | C | 17 | Global OE Output Disable | – | 5.0 | – | 5.0 | – | 6.0 | ns |
| t _{wh} | – | 18 | Ext. Synchronous Clk Pulse Duration, High | 2.5 | – | 3.0 | – | 3.0 | – | ns |
| t _{wl} | – | 19 | Ext. Synchronous Clk Pulse Duration, Low | 2.5 | – | 3.0 | – | 3.0 | – | ns |

Table 2-0030B-180/2032

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

| PARAMETER | TEST COND. ⁴ | # ² | DESCRIPTION ¹ | -110 | | -80 | | UNITS |
|-------------------------|-------------------------|----------------|--|------|------|------|------|-------|
| | | | | MIN. | MAX. | MIN. | MAX. | |
| t _{pd1} | A | 1 | Data Propagation Delay, 4PT Bypass, ORP Bypass | – | 10.0 | – | 15.0 | ns |
| t _{pd2} | A | 2 | Data Propagation Delay | – | 13.0 | – | 18.5 | ns |
| f _{max} | A | 3 | Clock Frequency with Internal Feedback ³ | 111 | – | 84.0 | – | MHz |
| f _{max} (Ext.) | – | 4 | Clock Frequency with External Feedback ($\frac{1}{t_{su2} + t_{co1}}$) | 77.0 | – | 57.0 | – | MHz |
| f _{max} (Tog.) | – | 5 | Clock Frequency, Max. Toggle | 125 | – | 83.0 | – | MHz |
| t _{su1} | – | 6 | GLB Reg. Setup Time before Clock, 4 PT Bypass | 5.5 | – | 7.5 | – | ns |
| t _{co1} | A | 7 | GLB Reg. Clock to Output Delay, ORP Bypass | – | 5.5 | – | 8.0 | ns |
| t _{h1} | – | 8 | GLB Reg. Hold Time after Clock, 4 PT Bypass | 0.0 | – | 0.0 | – | ns |
| t _{su2} | – | 9 | GLB Reg. Setup Time before Clock | 7.5 | – | 9.5 | – | ns |
| t _{co2} | – | 10 | GLB Reg. Clock to Output Delay | – | 6.5 | – | 9.5 | ns |
| t _{h2} | – | 11 | GLB Reg. Hold Time after Clock | 0.0 | – | 0.0 | – | ns |
| t _{r1} | A | 12 | Ext. Reset Pin to Output Delay | – | 13.5 | – | 19.5 | ns |
| t _{rw1} | – | 13 | Ext. Reset Pulse Duration | 6.5 | – | 10.0 | – | ns |
| t _{ptoen} | B | 14 | Input to Output Enable | – | 14.5 | – | 24.0 | ns |
| t _{ptoedis} | C | 15 | Input to Output Disable | – | 14.5 | – | 24.0 | ns |
| t _{goeen} | B | 16 | Global OE Output Enable | – | 7.0 | – | 12.0 | ns |
| t _{goedis} | C | 17 | Global OE Output Disable | – | 7.0 | – | 12.0 | ns |
| t _{wh} | – | 18 | External Synchronous Clock Pulse Duration, High | 4.0 | – | 6.0 | – | ns |
| t _{wl} | – | 19 | External Synchronous Clock Pulse Duration, Low | 4.0 | – | 6.0 | – | ns |

Table 2-0030B-110/2032

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters¹

Over Recommended Operating Conditions

| PARAMETER | # ² | DESCRIPTION | -180 | | -150 | | -135 | | UNITS |
|----------------------------|----------------|---|------|------|------|------|------|------|-------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Inputs | | | | | | | | | |
| t_{io} | 20 | Input Buffer Delay | – | 0.6 | – | 0.6 | – | 1.1 | ns |
| t_{din} | 21 | Dedicated Input Delay | – | 1.1 | – | 1.3 | – | 2.4 | ns |
| GRP | | | | | | | | | |
| t_{grp} | 22 | GRP Delay | – | 0.7 | – | 0.7 | – | 1.3 | ns |
| GLB | | | | | | | | | |
| t_{4ptbpc} | 23 | 4 Product Term Bypass Path Delay (Combinatorial) | – | 2.3 | – | 2.6 | – | 3.6 | ns |
| t_{4ptbpr} | 24 | 4 Product Term Bypass Path Delay (Registered) | – | 3.1 | – | 3.1 | – | 3.6 | ns |
| t_{1ptxor} | 25 | 1 Product Term/XOR Path Delay | – | 3.6 | – | 4.3 | – | 5.0 | ns |
| t_{20ptxor} | 26 | 20 Product Term/XOR Path Delay | – | 4.1 | – | 4.6 | – | 5.1 | ns |
| t_{xoradj} | 27 | XOR Adjacent Path Delay ³ | – | 4.8 | – | 5.0 | – | 5.6 | ns |
| t_{gbp} | 28 | GLB Register Bypass Delay | – | 0.2 | – | 0.0 | – | 0.0 | ns |
| t_{gsu} | 29 | GLB Register Setup Time before Clock | 0.5 | – | 0.7 | – | 0.3 | – | ns |
| t_{gh} | 30 | GLB Register Hold Time after Clock | 1.8 | – | 1.8 | – | 3.0 | – | ns |
| t_{gco} | 31 | GLB Register Clock to Output Delay | – | 0.7 | – | 0.8 | – | 0.7 | ns |
| t_{gro} | 32 | GLB Register Reset to Output Delay | – | 1.0 | – | 1.2 | – | 1.1 | ns |
| t_{ptre} | 33 | GLB Product Term Reset to Register Delay | – | 2.8 | – | 2.9 | – | 4.4 | ns |
| t_{ptoe} | 34 | GLB Product Term Output Enable to I/O Cell Delay | – | 5.9 | – | 6.9 | – | 6.4 | ns |
| t_{ptck} | 35 | GLB Product Term Clock Delay | 2.5 | 3.8 | 2.5 | 4.1 | 2.9 | 5.2 | ns |
| ORP | | | | | | | | | |
| t_{orp} | 36 | ORP Delay | – | 0.7 | – | 0.8 | – | 1.3 | ns |
| t_{orpbp} | 37 | ORP Bypass Delay | – | 0.2 | – | 0.3 | – | 0.3 | ns |
| Outputs | | | | | | | | | |
| t_{ob} | 38 | Output Buffer Delay | – | 1.2 | – | 1.3 | – | 1.2 | ns |
| t_{sl} | 39 | Output Slew Limited Delay Adder | – | 10.0 | – | 10.0 | – | 10.0 | ns |
| t_{oen} | 40 | I/O Cell OE to Output Enabled | – | 2.8 | – | 2.8 | – | 3.2 | ns |
| t_{odis} | 41 | I/O Cell OE to Output Disabled | – | 2.8 | – | 2.8 | – | 3.2 | ns |
| t_{goe} | 42 | Global Output Enable | – | 2.2 | – | 2.2 | – | 2.8 | ns |
| Clocks | | | | | | | | | |
| t_{gy0} | 43 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 1.9 | 1.9 | 2.1 | 2.1 | 2.3 | 2.3 | ns |
| t_{gy1/2} | 44 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 1.9 | 1.9 | 2.1 | 2.1 | 2.3 | 2.3 | ns |
| Global Reset | | | | | | | | | |
| t_{gr} | 45 | Global Reset to GLB | – | 4.1 | – | 4.7 | – | 6.4 | ns |

Table 2-0036C-180/2032

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters¹

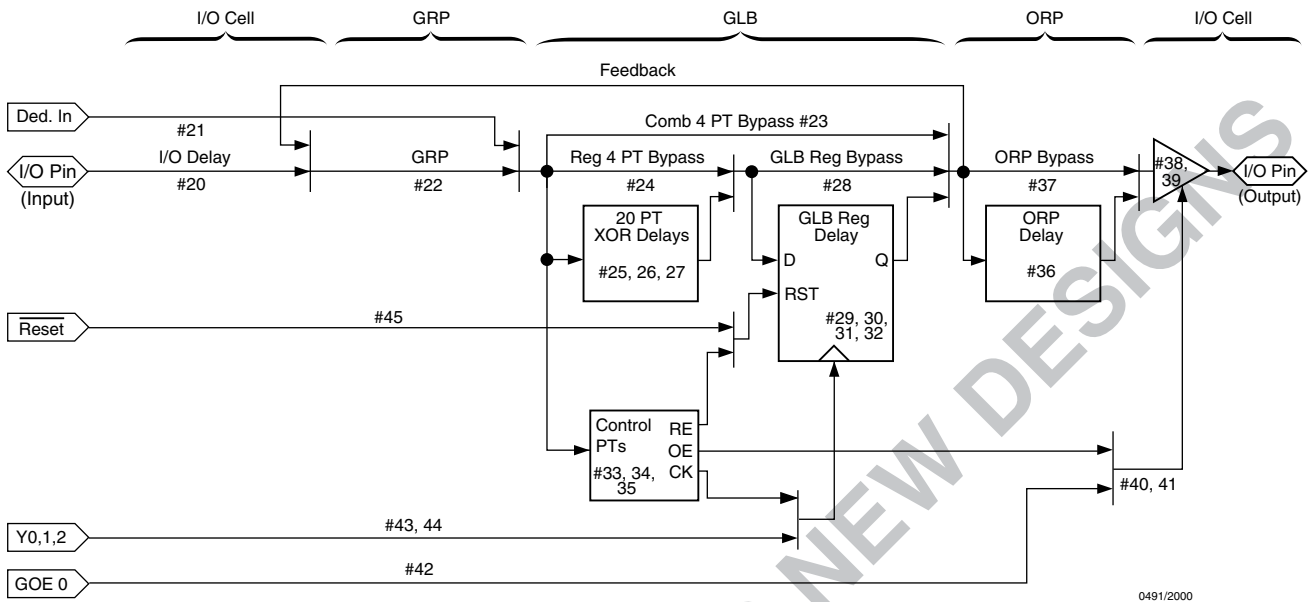
Over Recommended Operating Conditions

| PARAMETER | # ² | DESCRIPTION | -110 | | -80 | | UNITS |
|----------------------------|----------------|---|------|------|------|------|-------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Inputs | | | | | | | |
| t_{io} | 20 | Input Buffer Delay | – | 1.7 | – | 2.2 | ns |
| t_{din} | 21 | Dedicated Input Delay | – | 3.4 | – | 4.8 | ns |
| GRP | | | | | | | |
| t_{grp} | 22 | GRP Delay | – | 1.7 | – | 2.6 | ns |
| GLB | | | | | | | |
| t_{4ptbpc} | 23 | 4 Product Term Bypass Path Delay (Combinatorial) | – | 4.9 | – | 7.2 | ns |
| t_{4ptbpr} | 24 | 4 Product Term Bypass Path Delay (Registered) | – | 4.8 | – | 7.2 | ns |
| t_{1ptxor} | 25 | 1 Product Term/XOR Path Delay | – | 6.2 | – | 8.8 | ns |
| t_{20ptxor} | 26 | 20 Product Term/XOR Path Delay | – | 6.8 | – | 9.2 | ns |
| t_{xoradj} | 27 | XOR Adjacent Path Delay ³ | – | 7.5 | – | 10.2 | ns |
| t_{gbp} | 28 | GLB Register Bypass Delay | – | 0.1 | – | 0.0 | ns |
| t_{gsu} | 29 | GLB Register Setup Time before Clock | 0.5 | – | 0.1 | – | ns |
| t_{gh} | 30 | GLB Register Hold Time after Clock | 4.0 | – | 6.0 | – | ns |
| t_{gco} | 31 | GLB Register Clock to Output Delay | – | 0.6 | – | 0.4 | ns |
| t_{gro} | 32 | GLB Register Reset to Output Delay | – | 1.8 | – | 2.2 | ns |
| t_{ptre} | 33 | GLB Product Term Reset to Register Delay | – | 5.9 | – | 8.8 | ns |
| t_{ptoe} | 34 | GLB Product Term Output Enable to I/O Cell Delay | – | 7.1 | – | 12.8 | ns |
| t_{ptck} | 35 | GLB Product Term Clock Delay | 4.0 | 7.0 | 5.5 | 9.5 | ns |
| ORP | | | | | | | |
| t_{orp} | 36 | ORP Delay | – | 1.5 | – | 2.1 | ns |
| t_{orpbp} | 37 | ORP Bypass Delay | – | 0.5 | – | 0.6 | ns |
| Outputs | | | | | | | |
| t_{ob} | 38 | Output Buffer Delay | – | 1.2 | – | 2.4 | ns |
| t_{sl} | 39 | Output Slew Limited Delay Adder | – | 10.0 | – | 10.0 | ns |
| t_{oen} | 40 | I/O Cell OE to Output Enabled | – | 4.0 | – | 6.4 | ns |
| t_{odis} | 41 | I/O Cell OE to Output Disabled | – | 4.0 | – | 6.4 | ns |
| t_{goe} | 42 | Global Output Enable | – | 3.0 | – | 5.6 | ns |
| Clocks | | | | | | | |
| t_{gy0} | 43 | Clock Delay, Y0 to Global GLB Clock Line (Ref. clock) | 3.2 | 3.2 | 4.6 | 4.6 | ns |
| t_{gy1/2} | 44 | Clock Delay, Y1 or Y2 to Global GLB Clock Line | 3.2 | 3.2 | 4.6 | 4.6 | ns |
| Global Reset | | | | | | | |
| t_{gr} | 45 | Global Reset to GLB | – | 9.0 | – | 12.8 | ns |

Table 2-0036C-110/2032

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI 2032/A Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 2.1 \text{ ns} &= (0.6 + 0.7 + 4.1) + (0.5) - (0.6 + 0.7 + 2.5) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 1.5 \text{ ns} &= (0.6 + 0.7 + 3.8) + (1.8) - (0.6 + 0.7 + 4.1) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 7.7 \text{ ns} &= (0.6 + 0.7 + 3.8) + (0.7) + (0.7 + 1.2)
 \end{aligned}$$

Note: Calculations are based upon timing specifications for the ispLSI 2032/A-180L

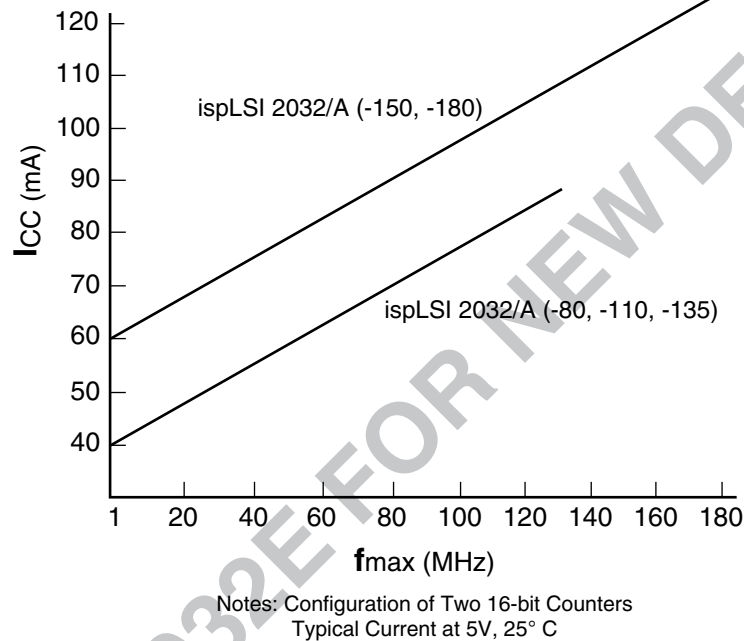
Table 2- 0042-16/2032

Power Consumption

Power consumption in the ispLSI 2032 and 2032A devices depends on two primary factors: the speed at which the device is operating and the number of Product Terms

used. Figure 4 shows the relationship between power and operating speed.

Figure 4. Typical Device Power Consumption vs fmax



ICC can be estimated for the ispLSI 2032/A using the following equation:

For 2032/A -150, -180: $I_{CC}(mA) = 30 + (\# \text{ of PTs} * 0.46) + (\# \text{ of nets} * \text{Max freq} * 0.012)$

For 2032/A -135, -110, -80: $I_{CC}(mA) = 21 + (\# \text{ of PTs} * 0.30) + (\# \text{ of nets} * \text{Max freq} * 0.012)$

Where:

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max freq = Highest Clock Frequency to the device (in MHz)

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A/2032A

Pin Description

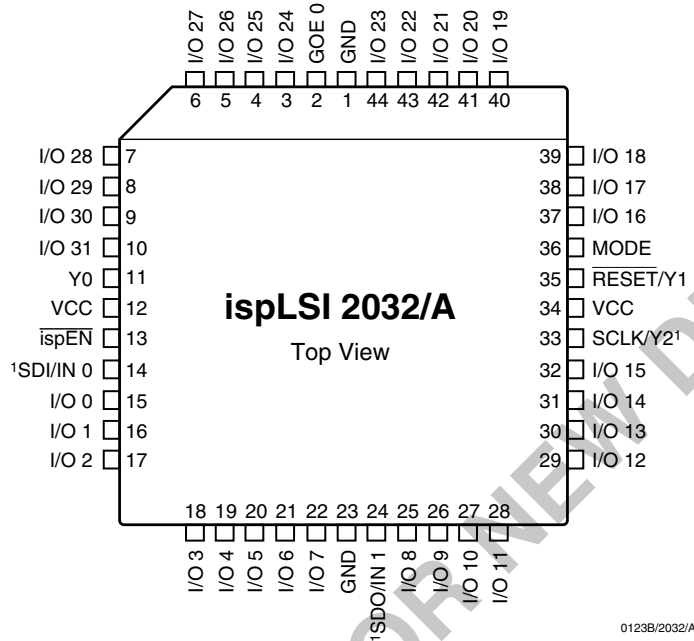
| NAME | 44-PIN PLCC PIN NUMBERS | 44-PIN TQFP PIN NUMBERS | 48-PIN TQFP PIN NUMBERS | DESCRIPTION |
|---|--|--|--|---|
| I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 | 15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10 | 9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4 | 9, 10, 11, 13, 14, 15, 16, 17, 20, 21, 22, 23, 25, 26, 27, 28, 33, 34, 35, 37, 38, 39, 40, 41, 44, 45, 46, 47, 1, 2, 3, 4 | Input/Output Pins — These are the general purpose I/O pins used by the logic array. |
| GOE 0 | 2 | 40 | 43 | Global Output Enable input pin. |
| Y0 RESET/Y1 | 11 35 | 5 29 | 5 31 | Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device. This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. |
| $\overline{\text{ispEN}}$ SDI/IN 0 ² MODE SDO/IN 1 ² SCLK/Y2 ² | 13 14 36 24 33 | 7 8 30 18 27 | 7 8 32 19 29 | Input — Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active. Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin. Input — When in ISP Mode, controls operation of ISP state machine. Output/Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin. Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated clock input. This clock input is brought into the Clock Distribution Network and can be routed to any GLB and/or I/O cell on the device. |
| GND VCC NC ¹ | 1, 23 12, 34 | 17, 39 6, 28 | 18, 42 6, 30 12, 24, 36, 48 | Ground (GND) VCC No Connect. |

Table 2-0002A-08isp/2032

1. NC pins are not to be connected to any active signals, VCC or GND.
2. Pins have dual function capability.

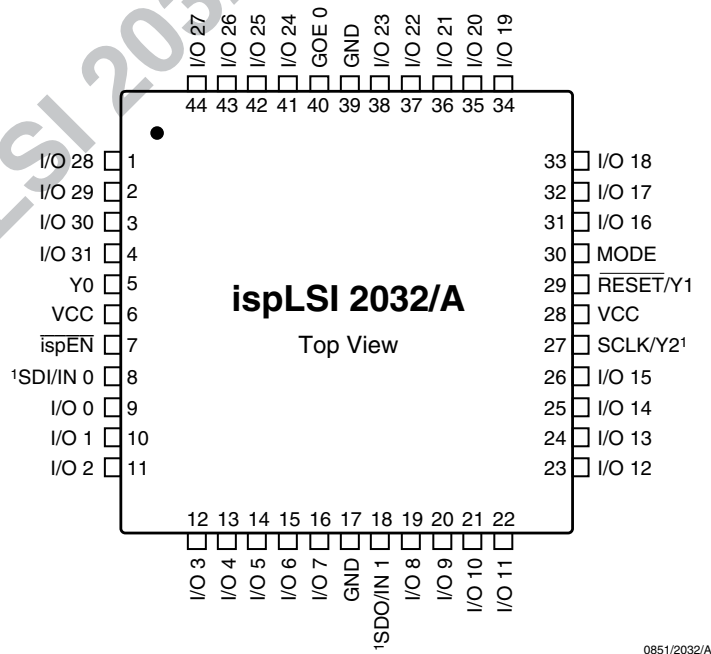
Pin Configuration

ispLSI 2032/A 44-Pin PLCC Pinout Diagram



1. Pins have dual function capability.

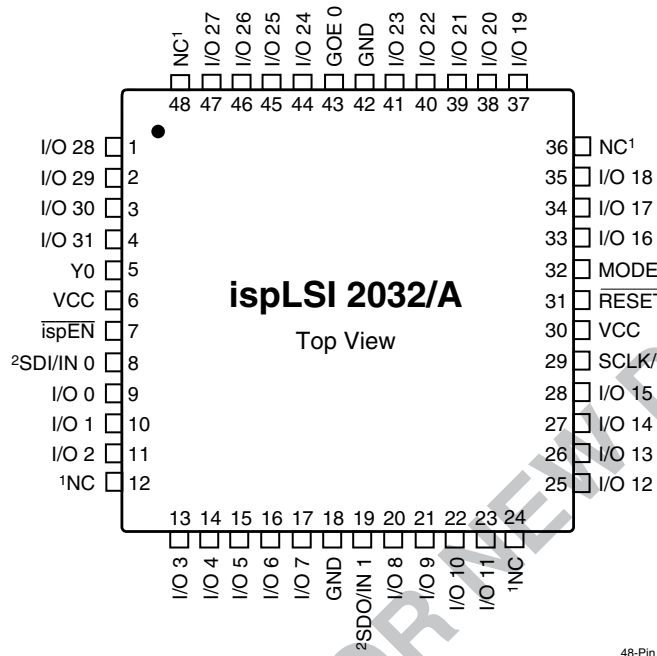
ispLSI 2032/A 44-Pin TQFP Pinout Diagram



1. Pins have dual function capability.

Pin Configuration

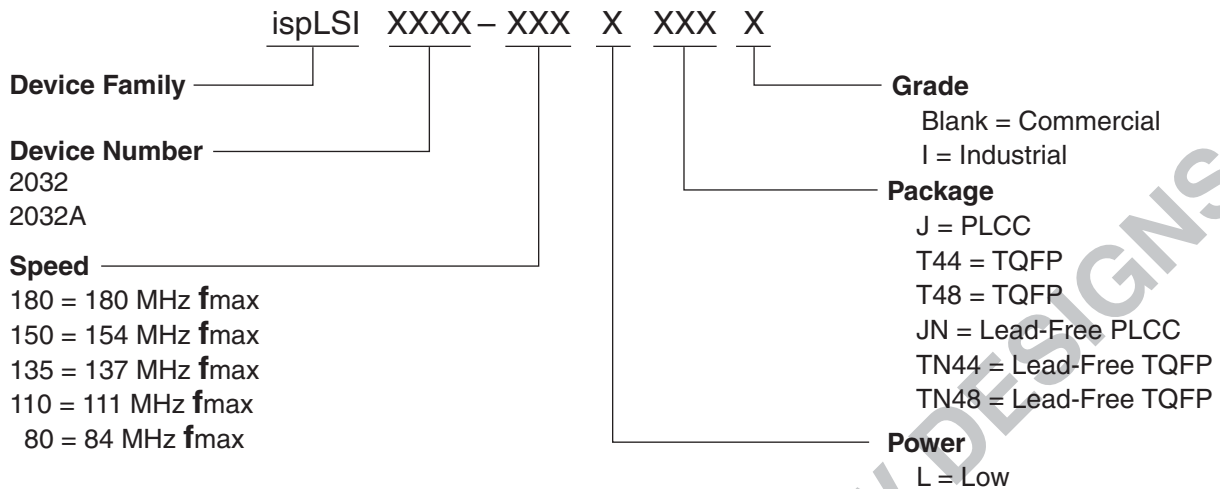
ispLSI 2032/A 48-Pin TQFP Pinout Diagram



48-Pin TQFP-2032/A

1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

Part Number Description



ispLSI 2032/A Ordering Information

Conventional Packaging

COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|---------------------|----------------------|-------------|
| ispLSI | 180 | 5.0 | ispLSI 2032A-180LJ44 | 44-Pin PLCC |
| | 180 | 5.0 | ispLSI 2032A-180LT44 | 44-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032A-180LT48 | 48-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032A-150LJ44 | 44-Pin PLCC |
| | 154 | 5.5 | ispLSI 2032A-150LT44 | 44-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032A-150LT48 | 48-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032A-135LJ44 | 44-Pin PLCC |
| | 137 | 7.5 | ispLSI 2032A-135LT44 | 44-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032A-135LT48 | 48-Pin TQFP |
| | 111 | 10 | ispLSI 2032A-110LJ44 | 44-Pin PLCC |
| | 111 | 10 | ispLSI 2032A-110LT44 | 44-Pin TQFP |
| | 111 | 10 | ispLSI 2032A-110LT48 | 48-Pin TQFP |
| | 84 | 15 | ispLSI 2032A-80LJ44 | 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032A-80LT44 | 44-Pin TQFP |
| 84 | 15 | ispLSI 2032A-80LT48 | 48-Pin TQFP | |

Table 2-0041A/2032A

INDUSTRIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|----------------------|-------------|
| ispLSI | 84 | 15 | ispLSI 2032A-80LJ44I | 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032A-80LT44I | 44-Pin TQFP |
| | 84 | 15 | ispLSI 2032A-80LT48I | 48-Pin TQFP |

Table 2-0041B/2032A

ispLSI 2032/A Ordering Information (Cont.)

Conventional Packaging

COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|---------------------|-------------|
| ispLSI | 180 | 5.0 | ispLSI 2032-180LJ | 44-Pin PLCC |
| | 180 | 5.0 | ispLSI 2032-180LT44 | 44-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032-180LT48 | 48-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032-150LJ | 44-Pin PLCC |
| | 154 | 5.5 | ispLSI 2032-150LT44 | 44-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032-150LT48 | 48-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032-135LJ | 44-Pin PLCC |
| | 137 | 7.5 | ispLSI 2032-135LT44 | 44-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032-135LT48 | 48-Pin TQFP |
| | 111 | 10 | ispLSI 2032-110LJ | 44-Pin PLCC |
| | 111 | 10 | ispLSI 2032-110LT44 | 44-Pin TQFP |
| | 111 | 10 | ispLSI 2032-110LT48 | 48-Pin TQFP |
| | 84 | 15 | ispLSI 2032-80LJ | 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032-80LT44 | 44-Pin TQFP |
| | 84 | 15 | ispLSI 2032-80LT48 | 48-Pin TQFP |

Table 2-0041A/2032

INDUSTRIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|---------------------|-------------|
| ispLSI | 84 | 15 | ispLSI 2032-80LJI | 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032-80LT44I | 44-Pin TQFP |
| | 84 | 15 | ispLSI 2032-80LT48I | 48-Pin TQFP |

Table 2-0041C/2032

Lead-Free Packaging

COMMERCIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|-----------------------|-----------------------|
| ispLSI | 180 | 5.0 | ispLSI 2032A-180LJN44 | Lead-Free 44-Pin PLCC |
| | 180 | 5.0 | ispLSI 2032A-180LTN44 | Lead-Free 44-Pin TQFP |
| | 180 | 5.0 | ispLSI 2032A-180LTN48 | Lead-Free 48-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032A-150LJN44 | Lead-Free 44-Pin PLCC |
| | 154 | 5.5 | ispLSI 2032A-150LTN44 | Lead-Free 44-Pin TQFP |
| | 154 | 5.5 | ispLSI 2032A-150LTN48 | Lead-Free 48-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032A-135LJN44 | Lead-Free 44-Pin PLCC |
| | 137 | 7.5 | ispLSI 2032A-135LTN44 | Lead-Free 44-Pin TQFP |
| | 137 | 7.5 | ispLSI 2032A-135LTN48 | Lead-Free 48-Pin TQFP |
| | 111 | 10 | ispLSI 2032A-110LJN44 | Lead-Free 44-Pin PLCC |
| | 111 | 10 | ispLSI 2032A-110LTN44 | Lead-Free 44-Pin TQFP |
| | 111 | 10 | ispLSI 2032A-110LTN48 | Lead-Free 48-Pin TQFP |
| | 84 | 15 | ispLSI 2032A-80LJN44 | Lead-Free 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032A-80LTN44 | Lead-Free 44-Pin TQFP |
| | 84 | 15 | ispLSI 2032A-80LTN48 | Lead-Free 48-Pin TQFP |

ispLSI 2032/A Ordering Information (Cont.)

Lead-Free Packaging

INDUSTRIAL

| FAMILY | fmax (MHz) | tpd (ns) | ORDERING NUMBER | PACKAGE |
|--------|------------|----------|-----------------------|-----------------------|
| ispLSI | 84 | 15 | ispLSI 2032A-80LJN44I | Lead-Free 44-Pin PLCC |
| | 84 | 15 | ispLSI 2032A-80LTN44I | Lead-Free 44-Pin TQFP |
| | 84 | 15 | ispLSI 2032A-80LTN48I | Lead-Free 48-Pin TQFP |

Revision History

| Date | Version | Change Summary |
|-------------|---------|--|
| — | 10 | Previous Lattice release. |
| August 2006 | 11 | Updated for lead-free package options. |

USE ispLSI 2032E FOR NEW DESIGN