Data Sheet, V1.1, April 2003

HYB25L256160AC

256-Mbit Mobile-RAM

2.5V V_{DD}

Memory Products

Infineon technologies

Never stop thinking.

Revision History:	**2003-04-16**	V1.1
Previous Version:	2001-11-23	V1.0

Page	Subjects (major changes since last version)
all	applied new data sheet template Din-A4
Page 13f	Temperature Compensated Self Refresh with On-Chip Temperature Sensor
Page 15	Table Operation Definition extended by two rows “Clock Suspend Entry” and “Clock Suspend Exit”; Note 5 extended by “When this command is asserted during a burst cycle the device …”
Page 18	“Self Refresh” description improved
Page 19	“Simplified State Diagram” added
Page 20	relaxed Absolute Maximum Ratings (+0.5/–0.7 V instead of ±0.3 V relative to V_{DD}/V_{SS})
Page 20	Note 4: relaxed over-/underswing delta to 2.0 V
Page 20ff	deleted V_{DD} and V_{DDQ} range above tables and partly replaced by note “(Recommended Operating Conditions unless otherwise noted)“
Page 22	PC133 replaced by –7.5
Page 23f	table operating currents updated, symbols changed from I_{CC} to I_{DD}, value type “max.” added, I_{DD6} named “self refresh current”, I_{DD1} description (“Single bank access cycles”) updated t_{CK} defined by Note 3 or set to infinity; Note 4: “assumed” replaced by “used”
Page 41	revised timing diagram SPT03919-4
Page 54	TFBGA package outline moved to end , added “tolerance ±0.1mm for length and width”

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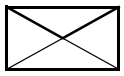

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1 Overview

1.1 Features

- 16 Mbits × 16 organisation
- Fully synchronous to positive clock edge
- Four internal banks for concurrent operation
- Data mask (DM) for byte control with write and read data
- Programmable CAS latency: 2 or 3
- Programmable burst length: 1, 2, 4, 8, or full page
- Programmable wrap sequence: sequential or interleaved
- Random column address every clock cycle (1-N rule)
- Deep power down mode
- Extended mode register for Mobile-RAM features
- Temperature compensated self refresh with on-die temperature sensor
- Partial array self refresh
- Power down and clock suspend mode
- Automatic and controlled precharge command
- Auto refresh mode (CBR)
- 8192 refresh cycles / 64 ms
- Self-refresh with programmble refresh period
- Programmable power reduction feature by partial array activation during self-refresh
- V_{DDQ} = 1.8V or 2.5 V
- V_{DD} = 2.5 V
- P-TFBGA-54 package 9-by-6-ball array with 3 depopulated rows (12 x 8 mm^2)
- Operating temperature range: commerical (0 °C to 70 °C)

Table 1 Performance [1)]

Part Number Speed Code			–7.5	–8	Unit
max. Clock Frequency	@CL3	f_{CK3}	133	125	MHz
min. Clock Period	@CL3	t_{CK3}	7.5	8.0	ns
min. Access Time from Clock	@CL3	t_{AC3}	6.0	6.0	ns
min. Clock Period	@CL2	t_{CK2}	9.5	9.5	ns
min. Access Time from Clock	@CL2	t_{AC2}	6.0	6.0	ns

1) for VDDQ = 2.5 V; see **Table 10** for VDDQ dependent performance

1.2 Description

The 256-Mbit Mobile-RAM is a new generation of low power, four bank synchronous DRAM organized as 4 banks x 4 Mbit x 16 with additional features for mobile applications. The synchronous Mobile-RAM achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The device adds new features to the industry standards set for synchronous DRAM products. Parts of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is programmable in 4 steps which drastically reduces the self refresh current, depending on the case temperature of the components in the system application. In addition a “Deep Power Down Mode” is available. Operating the four memory banks in an

interleave fashion allows random access operation to occur at higher rate. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

The Mobile-RAM is housed in a FBGA “chip-size” package. The Mobile-RAM is available in the commerical (0 °C to 70 °C) temperature range.

Table 2 Ordering Information

Part Number[1)]	Function Code	Case Temperature Range	Package
HYB25L256160AC–7.5	PC133–333–522	commerical (0 °C to 70 °C)	P-TFBGA-54
HYB25L256160AC–8	PC100–222–620		

1) HYB/E: designator for memory components for commercial/extended temperature range
25L: Mobile-RAM at V_{DD} = 2.5 V
256: 256-Mbit density
160: Product variation x16
A: Die revision A
C: Package type FBGA
–7.5/8: speed grade - see **Table 1**

2 Pin Configuration

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
A12	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10/AP
VSS	A5	A4	J	A3	A2	VDD

< Top-view >

Figure 1 Pin Configuration P-TFBGA-54 (16 Mb × 16)

Table 3 Input/Output Signals

Pin	Symbol	Type	Polarity	Function
F2	CLK	Input	Positive Edge	**Clock** The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
F3	CKE	Input	Active High	**Clock Enable** CKE activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
G9	$\overline{CS}$	Input	Active Low	**Chip Select** $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
F8	$\overline{RAS}$	Input	Active Low	**Command Inputs** Sampled at the rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the command to be executed by the SDRAM.
F7	$\overline{CAS}$			
F9	$\overline{WE}$			
G8	BA1	Input	Active High	**Bank Address Inputs** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determine if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
G7	BA0			
G1	A12	Input	Active High	**Address Inputs** During a Bank Activate command cycle, A12 - A0 define the row address (RA12 - RA0) when sampled at the rising clock edge. During a Read or Write command cycle, A8-A0 define the column address (CA8 - CA0) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA1, BA0 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA1 and BA0 to control which bank(s) to precharge. If AP is high, all four banks will be precharged regardless of the state of BA0 and BA1. If AP is low, then BA1 and BA0 are used to define which bank to precharge.
G2	A11			
H9	A10/AP			
G3	A9			
H1	A8			
H2	A7			
H3	A6			
J2	A5			
J3	A4			
J7	A3			
J8	A2			
H8	A1			
H7	A0			

Table 3 Input/Output Signals (cont'd)

Pin	Symbol	Type	Polarity	Function
A2	DQ15	Input/ Output	Active High	**Data Input/Output** Data bus operates in the same manner as on conventional DRAMs.
B1	DQ14			
B2	DQ13			
C1	DQ12			
C2	DQ11			
D1	DQ10			
D2	DQ9			
E1	DQ8			
E9	DQ7			
D8	DQ6			
D9	DQ5			
C8	DQ4			
C9	DQ3			
B8	DQ2			
B9	DQ1			
A8	DQ0			
F1	UDQM	Input	Active High	**Data Input/Output Mask** UDQM and LDQM are output disable signals during read mode and input mask signals for write data. In Read mode, U/LDQM have a latency of two clock cycles and control the output buffers like low active output enable signals. In Write mode, U/LDQM have a latency of zero and operate as a word mask by allowing input data to be written if it is low but blocks the write operation if the respective DQM is high. UDQM controls the upper byte and LDQM controls the lower byte.
E8	LDQM			
E2	NC	–	–	**Not Connected** No internal electrical connection is present.
A7, B3, C7, D3	V_{DDQ}	Supply	–	**DQ Power Supply**
A3 B7 C3 D7	V_{SSQ}	Supply	–	**DQ Ground**
A9 E4 J9	V_{DD}	Supply	–	**Power Supply**
A1 E3 J1	V_{SS}	Supply	–	**Ground**

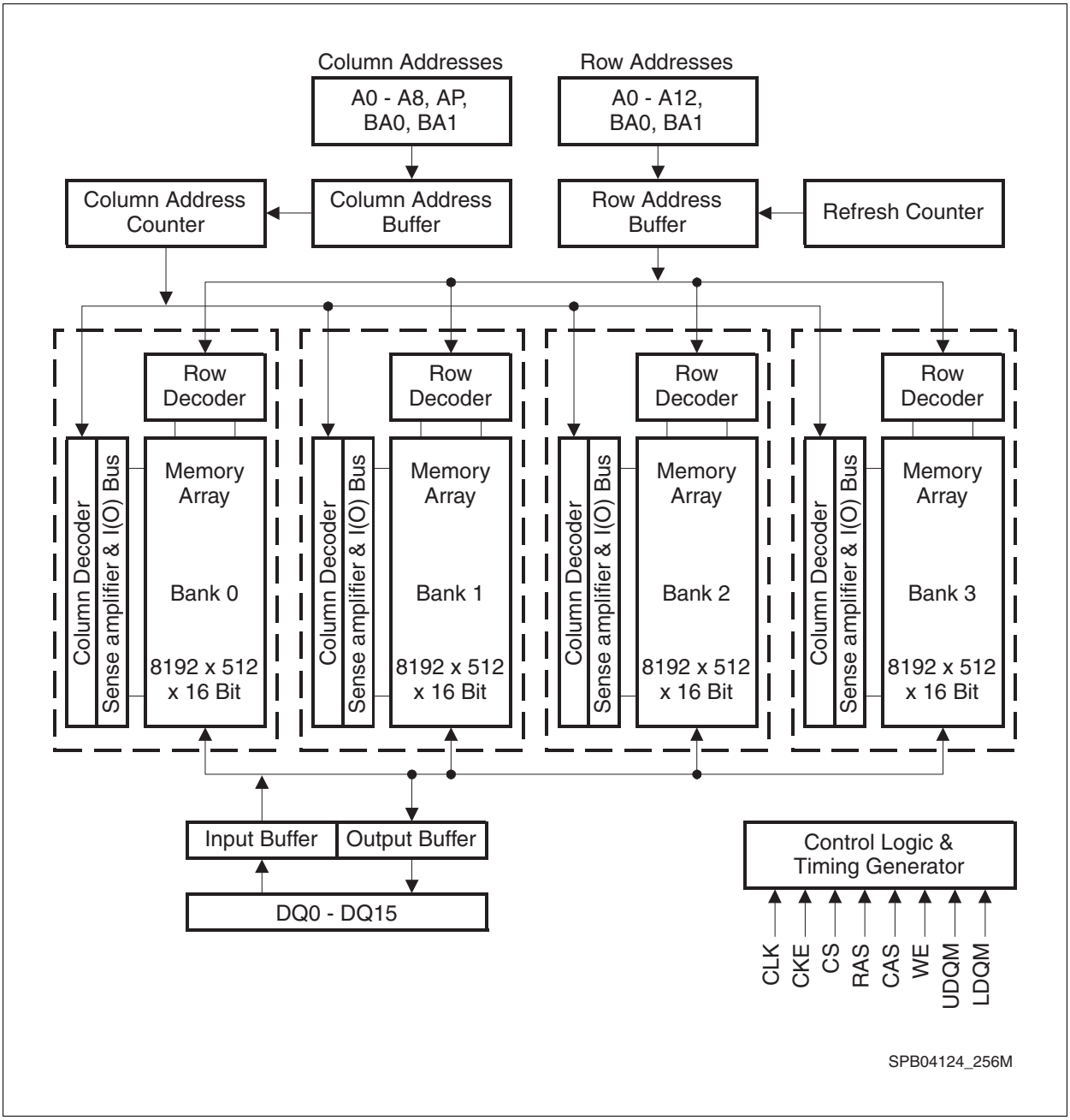


Figure 2 Block Diagram (16 Mbit × 16, 13 / 9 / 2 Addressing)

Note:

1. *This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.*
2. *DQM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ signals.*

3 Functional Description

The 256-Mbit Mobile-RAM is a new generation of low power, four bank synchronous DRAM organized as 4 banks × 4 Mbit × 16 with additional features for mobile applications. The synchronous Mobile-RAM achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The device adds new features to the industry standards set for synchronous DRAM products. Parts of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is programmable in 4 steps which drastically reduces the self refresh current, depending on the case temperature of the components in the system application. In addition a “Deep Power Down Mode” is available. Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Prior to normal operation, the 256-Mbit Mobile-RAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

3.1 Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the 256-Mbit Mobile-RAM must be powered up and initialized in a predefined manner. V_{DD} must be applied before or at the same time as V_{DDQ} to the specified voltage when the input signals are held in the “NOP” or “DESELECT” state. The power on voltage must not exceed V_{DD} + 0.3 V on any of the input pins or V_{DDQ} supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 ms is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.Mode Register Definition

3.2 Mode Register

The Mode Register designates the operation mode at the read or write cycle. This register is divided into four fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), and a CAS Latency Field to set the access time at clock cycle, an The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table. BA0 and BA1 have to be set to “0” to enter the Mode Register.

MR
Mode Register Definition **(BA[1:0] = 00_B)**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**MODE**						**CL**			**BT**	**BL**		
reg. addr		w						w			w	w		

Field	Bits	Type	Description
BL	[2:0]	w	**Burst Length** Number of sequential bits per DQ related to one read/write command; see **Chapter 3.2.1**. *Note: All other bit combinations are RESERVED.* 000 1 001 2 010 4 011 8 111 full page (sequential burst type only)
BT	3	w	**Burst Type** See **Table 4** for internal address sequence of low order address bits; see **Chapter 3.2.2**. 0 Sequential 1 Interleaved
CL	[6:4]	w	**CAS Latency** Number of full clocks from read command to first data valid window; see **Chapter 3.2.3**. *Note: All other bit combinations are RESERVED.* 010 2 011 3
MODE	[12:7]	w	**Operating Mode** See **Chapter 3.2.4**. *Note: All other bit combinations are RESERVED.* 000000 Burst Read/Burst Write 000100 Burst Read/Single Write

3.2.1 Burst Length

Read and write accesses to the 256-Mbit Mobile-RAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by Ai-A1 when the burst length is set to two, by Ai-A2 when the burst length is set to four and by Ai-A3 when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies always to Read bursts and depending on A9 in Operating Mode also on Write bursts.

3.2.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 4**.

Table 4 Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Note:

1. *For a burst length of two, Ai-A1 selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, Ai-A2 selects the four-data-element block; A1-A0 selects the first access within the block.*
3. *For a burst length of eight, Ai-A3 selects the eight-data- element block; A2-A0 selects the first access within the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

3.2.3 Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 and 3 clocks.

If a Read command is registered at rising clock edge n, and the latency is *m* clocks, the data is available nominally coincident with rising clock edge *n + m*.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

3.2.4 Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A12-A7 set to zero, and bits A6-A0 set to the desired values. Burst Length for Write bursts is fixed to one by issuing a Mode Register Set command with bits A12-A10 and A8-A7 each set to zero, bit A9 set to one, and bits A0-A6 set to the desired values.

All other combinations of values for A12-A7 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

3.3 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register. These additional functions are unique to Mobile RAMs and includes a refresh period field (TCSR) for Temperature Compensated Self Rrefresh and a Partial Array Self Refresh field (PASR).

The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 1) and retains the stored information until it is programmed again or the device looses power. The Extended mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either these requirements result in unspecified operation. Unused bit A12 to A5 have to be programmed to “0”.

3.3.1 Partial Array Self Refresh

The PASR field is a power saving feature specific to Mobile-RAMs and is used to specify whether only one quarter or half of bank 0, one bank (bank 0), two banks (banks 0 + 1) or all four banks (default) of the SDRAM array are enabled for Self Refresh. Disabled banks will not be refreshed in Self Refresh mode and written data will get lost after a period defined by t_{REF}.

3.3.2 Temperature Compensated Self Refresh with On-Chip Temperature Sensor

DRAM devices store data as electrical charge in tiny capacitors that require a periodic refresh in order to retain the stored information. This refresh requirment heavily depends on the die temperatur: high temperature corresponds to short refresh period, and low temperature to long refresh period.

The Mobile-RAM is equipped with an on-chip temperature sensor which continuously monitors the current die temperature and adjusts the refresh period in self refresh mode accordingly. By default the on-chip temperature sensor is enabled (TCSR = 00, see **Table "EMR" on Page 14**); the other three TCSR settings use defined temperature values to adjust the self refresh period to with the on-chip temperature sensor being disabled.

EMR
Extended Mode Register Definition (BA[1:0] = 10_B)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	**0**	**MODE**								**TCSR**		**PASR**		
reg. addr		w								w		w		

Field	Bits	Type	Description[1)]
PASR	[2:0]	w	**Partial Array Self Refresh** See **Chapter 3.3.1** 000 banks to be self refreshed: all 4 of 4 001 banks to be self refreshed: 2 of 4, BA[1:0] = 00_B or 01_B 010 banks to be self refreshed: 1 of 4, BA[1:0] = 00_B 101 banks to be self refreshed: 0.5 of 4, BA[1:0] = 00_B & RA12 = 0_B 110 banks to be self refreshed: 0.25 of 4, BA[1:0] = 00_B & RA[12:11] = 00_B
TCSR	[4:3]	w	**Temperature Compensated Self Refresh** See **Chapter 3.3.2**. 00 on-chip temperature sensor enabled 01 Maximum case temperature: 45°C, on-chip temperature sensor disabled 10 Maximum case temperature: 15°C, on-chip temperature sensor disabled
MODE	[12:5]	w	**Operating Mode** 00h Normal operation

1) All other bit combinations are RESERVED.

3.4 Commands

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Table 5 Operation Definition[1)]

Operation	Device State	CKE n-1[2)]	CKE n[2)]	DQM	BA1 BA0	AP= A10	Addr	CS	RAS	CAS	WE
Bank Active	Idle[3)]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3)]	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active[3)]	H	X	X	V	H	V	L	H	L	L
Read	Active[3)]	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active[3)]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Entry	Active[4)]	H	L	X	X	X	X	X	X	X	X
Clock Suspend Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active[4)]							L	H	H	H
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X
Deep Power Down Entry	Idle	H	L	X	X	X	X	L	H	H	L
Deep Power Down Exit	Deep Power Down[5)]	L	H	X	X	X	X	X	X	X	X

1) V = Valid, x = Don't Care, L = Low Level, H = High Level.

2) CKE_n signal is input level when commands are provided, CKE_{n-1} signal is input level one clock before the commands are provided.

3) This is the state of the banks designated by BA0, BA1 signals.

4) Power Down Mode can not be entered during a burst cycle. When this command is asserted during a burst cycle the device enters Clock Suspend Mode.

5) After Deep Power Down mode exit a full new initialisation of the memory device is mandatory.

Deselect

The Deselect function prevents new commands from being executed by the 256-Mbit Mobile-RAM. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a 256-Mbit Mobile-RAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A12-A0, BA1 and BA0. See mode register descriptions in **Chapter 3.2**. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. This is called the start of a RAS cycle and occures when $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock. The value on the BA1 and BA0 inputs selects the bank, and the address provided on inputs A12-A0 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read and Write

A CAS cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 133 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, which is one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation does not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM’s, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages. When the partial array activation is set, data will get lost when self-refresh is used in all non activated banks.

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA1 and BA0 inputs selects the bank, and the address provided on inputs A9-A0 for x16 selects the starting column location. The value on input A10/AP determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA1 and BA0 inputs selects the bank, and the address provided on inputs A9-A0 for x16 selects the starting column location. The value on input A10/AP determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered low, the corresponding data is written to memory; if the DQM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the Precharge command is issued. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock edge, it triggers the precharge operation. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care” (see **Table 6**). Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2 and two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay t_{WR} from the last data out to apply the precharge command.

Table 6 Bank Selection by Address Bits with Precharge

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	x	x	all Banks

Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10/AP to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit Precharge command was issued at the earliest possible time. The 256-Mbit Mobile-RAM automatically enters the precharge operation after t_{WR} (Write recovery time) following the last data in.

Burst Terminate

Once a burst read or write operation has been initiated, there are several methods used to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, using a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Auto Refresh

Auto Refresh is used during normal operation of the 256-Mbit Mobile-RAM and is analogous to CAS Before RAS (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses. This makes the address bits “Don’t Care” during an Auto Refresh command.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock edge. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

In Auto-Refresh mode all banks are refreshed, independendly of the fact that the partial array self-refresh has been set or not.

Self Refresh

The chip has an on-chip timer that is used when the Self Refresh mode is entered. The self-refresh command is asserted with $\overline{RAS}$, $\overline{CAS}$, and CKE low and $\overline{WE}$ high at a clock edge. All external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command. The use of self refresh mode introduces the possibility that an iternally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh an extra auto refresh command is recommended.

Low Power SDRAMs have the possibility to program the refresh period of the on-chip timer with the use of an appropriate extended MRS command, depending on the maximum operation case temperature in the application. In partial array self refresh mode only the selected banks will be refreshed. Data written to the non activated banks will get lost after a period defined by tref.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock edge, data outputs are disabled and become high impedance after two clock periods (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged before the Mobile-RAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all receiver circuits except for CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for power down mode entry and exit.

Deep Power Down Mode

The Deep Power Down Mode is an unique function on Mobile RAMs with very low standby currents.

All internal voltage generators inside the Mobile RAMs are stopped and all memory data is lost in this mode. To enter the Deep Power Down mode all banks must be precharged.

3.5 Simplified State Diagram

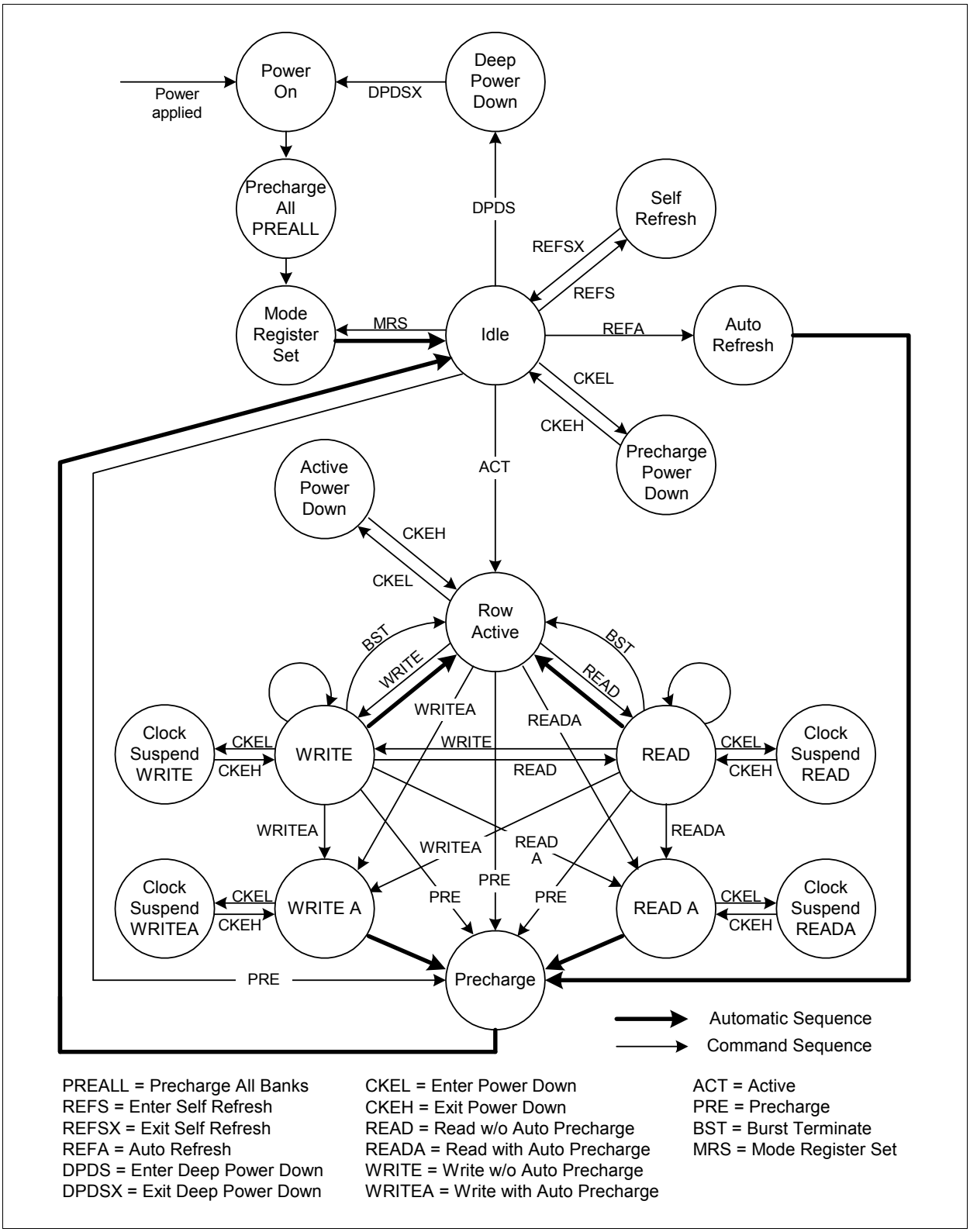


Figure 3 Simplified State Diagram

4 Electrical Characteristics

4.1 Operating Conditions

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.7	—	V_{DD} + 0.5	V	—
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.7	—	+3.6	V	—
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–0.7	—	+3.6	V	—
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–0.7	—	+3.6	V	—
Operating Case Temperature (commercial)	T_{CASE}	0	—	+70	°C	—
Storage Temperature (Plastic)	T_{STG}	–55	—	+150	°C	—
Power Dissipation	P_D	—	—	0.7	W	—
Short Circuit Output Current	I_{OUT}	—	50	—	mA	—

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 8 Recommended Operating Conditions and DC Characteristics[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		min.	max.		
Supply Voltage	V_{DD}	+2.3	+2.9	V	—
I/O Supply Voltage	V_{DDQ}	+1.65	+2.9	V	2)
Supply Voltage	V_{SS}	0	0	V	—
I/O Supply Voltage	V_{SSQ}	0	0	V	—
Input High (Logic 1) Voltage	V_{IH}	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	3)4)
Input Low (Logic 0) Voltage	V_{IL}	–0.3	+0.3	V	3)4)
Output High (Logic 1) Voltage	V_{OH}	V_{DDQ} – 0.2	—	V	I_{OH} = –0.1 mA
Output Low (Logic 0) Voltage	V_{OL}	—	+0.2	V	I_{OH} = +0.1 mA
Input Leakage Current	I_{IL}	–5	+5	µA	Any input 0 V ≤V_{IN} ≤V_{DD}; all other pins not under test V_{IN} = 0 V
Output Leakage Current	I_{OZ}	–5	+5	µA	DQ is disabled; 0 V ≤V_{OUT} ≤V_{DDQ}

1) 0 °C ≤T_{CASE} ≤+70 °C

2) V_{DDQ} < V_{DD} + 0.3 V

3) All voltages referenced to V_{SS}

4) V_{IH} may overshoot to V_{DDQ} + 2.0 V for pulse width of < 4 ns.
V_{IL} may undershoot to – 2.0 V for pulse width < 4 ns.
Pulse width measured at 50% points with amplitude measured peak to DC reference

Table 9 Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Input Capacitance: CLK	C_{I1}	–	–	3.5	pF	1)
Input Capacitance: All other input-only pins	C_{I2}	–	–	3.8	pF	1)
Input/Output Capacitance: DQ	C_{IO}	4.0	–	5.0	pF	1)

1) These values are guaranteed by design and are tested on a sample base only. V_{DDQ} = V_{DD} = 2.5 V ±0.2 V, f = 1 MHz, T_{CASE} = 25 °C, $V_{OUT(DC)}$ = V_{DDQ}/2, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.

4.2 Timing Characteristics

Table 10 AC Timing Characteristics[1)2)]

Parameter	Symbol	–8		–7.5		Unit	Note/ Test Condition
		min.	max.	min.	max.		
Clock							
DQ output access time from CLK	t_{AC3}	–	7.5	–	7.5	ns	V_{DDQ} < 2.3 V 3)4)5)8)
		–	6	–	6	ns	V_{DDQ} ≥ 2.3 V 3)4)5)8)
	t_{AC2}	–	7.5	–	7.5	ns	V_{DDQ} < 2.3 V 3)4)5)8)
		–	6	–	6	ns	V_{DDQ} ≥ 2.3 V 3)4)5)8)
CK high-level width	t_{CH}	3	–	2.5	–	ns	–
CK low-level width	t_{CL}	3	–	2.5	–	ns	–
Clock cycle time	t_{CK3}	8	–	7.5	–	ns	V_{DDQ} ≥ 2.3 V 3)
		8	–	8	–	ns	V_{DDQ} < 2.3 V 3)
	t_{CK2}	9.5	–	9.5	–	ns	3)
Clock frequency	f_{CK3}	–	125	–	133	MHz	V_{DDQ} ≥ 2.3 V 3)
		–	125	–	125	MHz	V_{DDQ} < 2.3 V 3)
	f_{CK2}	–	105	–	105	MHz	3)
Transition time	t_T	0.5	1.5	0.3	1.2	ns	–
Setup and Hold Times							
Input setup time	t_{IS}	2	–	1.5	–	ns	6)
Input hold time	t_{IH}	1	–	0.8	–	ns	6)
CKE setup time	t_{CKS}	2	–	1.5	–	ns	6)
CKE hold time	t_{CKH}	1	–	0.8	–	ns	6)
Mode register setup time	t_{RSC}	2	–	2	–	t_{CK}	–
Power down moder entry time	t_{SB}	0	8	0	7.5	ns	–
Common Parameters							
Active to Read or Write delay	t_{RCD}	19	–	19	–	ns	7)
Precharge command period	t_{RP}	19	–	19	–	ns	7)
Active to Precharge command	t_{RAS}	48	100000	45	100000	ns	7)
Active bank A to Active bank A period	t_{RC}	70	–	67	–	ns	7)
Active bank A to Active bank B delay	t_{RRD}	16	–	15	–	ns	7)
CAS to CAS command delay	t_{CCD}	1	–	1	–	t_{CK}	–

Table 10 AC Timing Characteristics[1)2)] (cont'd)

Parameter	Symbol	–8		–7.5		Unit	Note/ Test Condition
		min.	max.	min.	max.		
Refresh Cycle							
Refresh period	t_{REF}	–	64	–	64	ms	–
Self refresh exit time	t_{SREX}	1	–	1	–	t_{CK}	–
Read Cycle							
Data output hold time	t_{OH}	3	–	3	–	ns	4)7)8)
Data output from high to low impedance	t_{LZ}	0	–	1	–	ns	–
Data output from low to high impedance	t_{HZ}	3	8	3	7	ns	–
DQM data output disable latency	t_{DQZ}	–	2	–	2	t_{CK}	–
Write Cycle							
Write recovery time	t_{WR}	14	–	14	–	ns	9)
DQM write data mask latency	t_{DQW}	0	–	0	–	t_{CK}	–

1) 0 °C ≤T_{CASE} ≤+70 °C; recommended operating conditions unless otherwise noted

2) For proper power-up see the operation section of this data sheet.

3) Symbol index 2 and 3 refer to CL = 2 and CL = 3.

4) AC timing tests are referenced to the 0.9 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit (details will be defined later). Specified t_{AC} and t_{OH} parameters are measured with a 30 pF only, without any resistive termination and with a input signal of 1 $^V/_{ns}$ edge rate (see **Figure 4**).

5) If clock rising time is longer than 1 ns, a time (t_T/2 - 0.5) ns has to be added to this parameter.

6) If t_T is longer than 1 ns, a time (t_T - 1) ns has to be added to this parameter.

7) These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows: *the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*

8) Access time from clock t_{AC} is 4.6 ns for –7.5 components with no termination and 0 pF load,
Data out hold time t_{OH} is 1.8 ns for –7.5 components with no termination and 0 pF load.

9) The write recovery time of t_{WR} = 14 ns allows the use of one clock cycle for the write recovery time when the memory operation frequency is equal or less than 72MHz. For all memory operation frequencies higher than 72MHz two clock cycles for t_{WR} are mandatory. INFINEON recommends to use two clock cylces for the write recovery time in all applications.

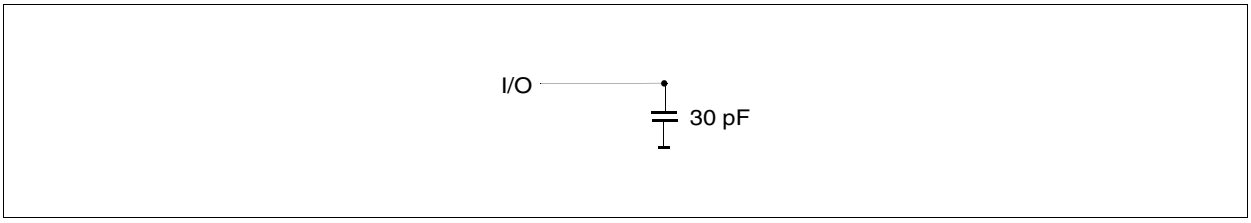


Figure 4 Measurement Conditions for t_{AC} and t_{OH}

4.3 Current Specification

Table 11 I_{DD} Specification and Conditions[1)2)]

Parameter	Symbol	–8		–7.5		Unit	Note/ Test Condition
		typ.	max.	typ.	max.		
Operating current Single bank access cycles	I_{DD1}		60		65	mA	$t_{RC} = t_{RC,MIN}$ [3)]
Precharge standby current Power down mode	I_{DD2P}		0.5		0.6	mA	$\overline{CS} = V_{IH,MIN}$, CKE $\leq V_{IL,MAX}$ [3)]
Precharge standby current Non power down mode	I_{DD2N}		18		20	mA	$\overline{CS} = V_{IH,MIN}$, CKE $\geq V_{IH,MIN}$ [3)]
Non operating current Active state of 1 upto 4 banks, power down	I_{DD3P}		3.5		3.5	mA	$\overline{CS} = V_{IH,MIN}$, CKE $\leq V_{IL,MAX}$ [3)]
Non operating current Active state of 1 upto 4 banks, non power down	I_{DD3N}		20		25	mA	$\overline{CS} = V_{IH,MIN}$, CKE $\geq V_{IH,MIN}$ [3)]
Burst operating current Read command cycling	I_{DD4}		60		80	mA	[3)4)]
Auto refresh current Auto refresh command cycling	I_{DD5}		140		155	mA	$t_{RC} = t_{RC,MIN}$
Self refresh current	I_{DD6}	see Table 12				µA	t_{CK} =infinity, CKE = 0.2 V
Deep power down mode current	I_{DD7}		5		5	µA	

1) 0 °C $\leq T_{CASE} \leq$ +70 °C; recommended operating conditions unless otherwise noted

2) For proper power-up see the operation section of this data sheet.

3) These parameters depend on the frequency. These values are measured at 133 MHz for –7.5 and at 100 MHz for –8 parts. Input signals are changed once during t_{CK}. If the devices are operating at a frequency less than the maximum operation frequency, these current values are reduced.

4) These parameters are measured with continuous data stream during read access and all DQs toggling. CL = 3 and BL = 4 is used and the V_{DDQ} current is excluded.

Table 12 I_{DD6} Programmable Self Refresh Current[1)2)]

Parameter	Symbol	–8, –7.5	Unit	T_{CASE}	Note/ Test Condition
		max.		TCSR[3)]	
Self refresh current Self refresh mode, full array activations = all banks	I_{DD6}	t.b.d.	µA	max. 15°C	t_{CK} =infinity, CKE = 0.2 V [4)]
		250	µA	max. 45°C	
		475	µA	max. 70°C	
Self refresh current Self refresh mode, half array activations = bank 0 + 1	I_{DD6}	t.b.d.	µA	max. 15°C	t_{CK} =infinity, CKE = 0.2 V [4)]
		150	µA	max. 45°C	
		250	µA	max. 70°C	
Self refresh current Self refresh mode, quarter array activations = bank 0	I_{DD6}	t.b.d.	µA	max. 15°C	t_{CK} =infinity, CKE = 0.2 V [4)]
		100	µA	max. 45°C	
		150	µA	max. 70°C	

1) Recommended operating conditions unless otherwise noted

2) For proper power-up see the operation section of this data sheet.

3) Extended Mode Register A4-A3, see **"Temperature Compensated Self Refresh with On-Chip Temperature Sensor" on Page 13**

4) Target values to be verified on final product and may change.

5 Timing Diagrams

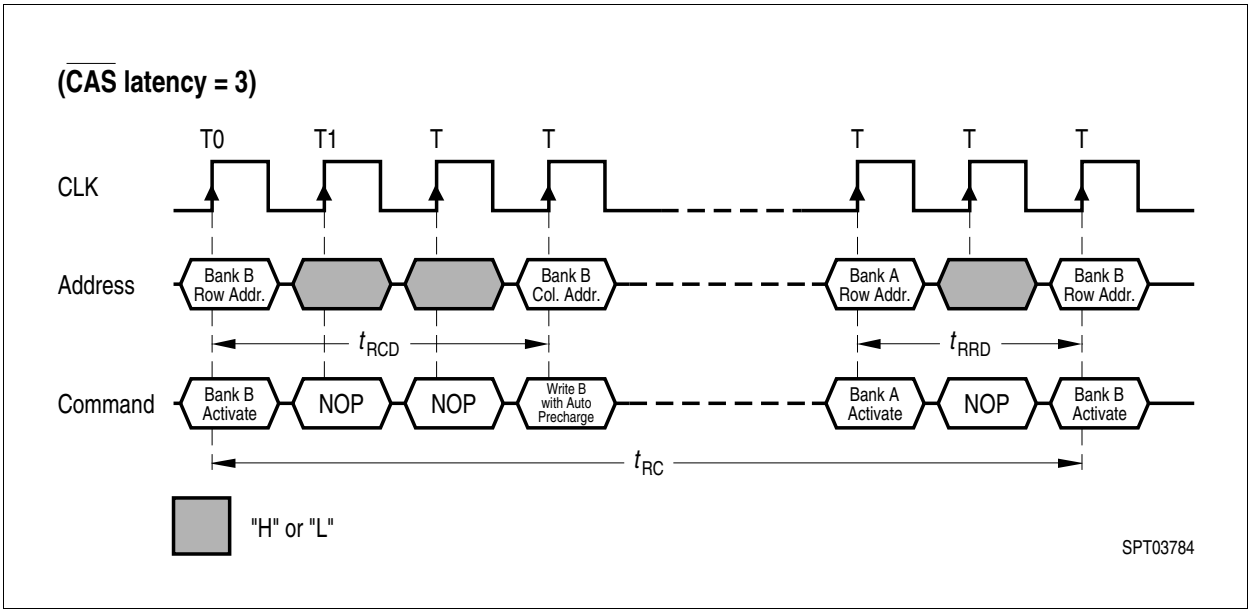


Figure 5 Bank Activate Command Cycle

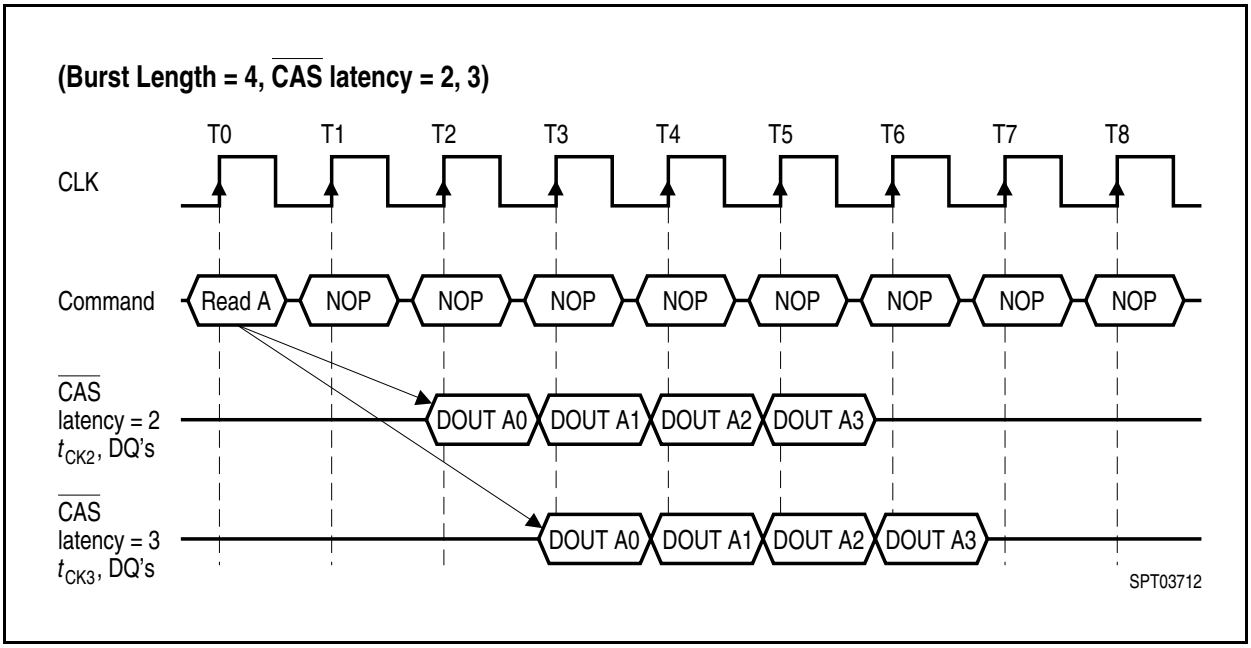


Figure 6 Burst Read Operation

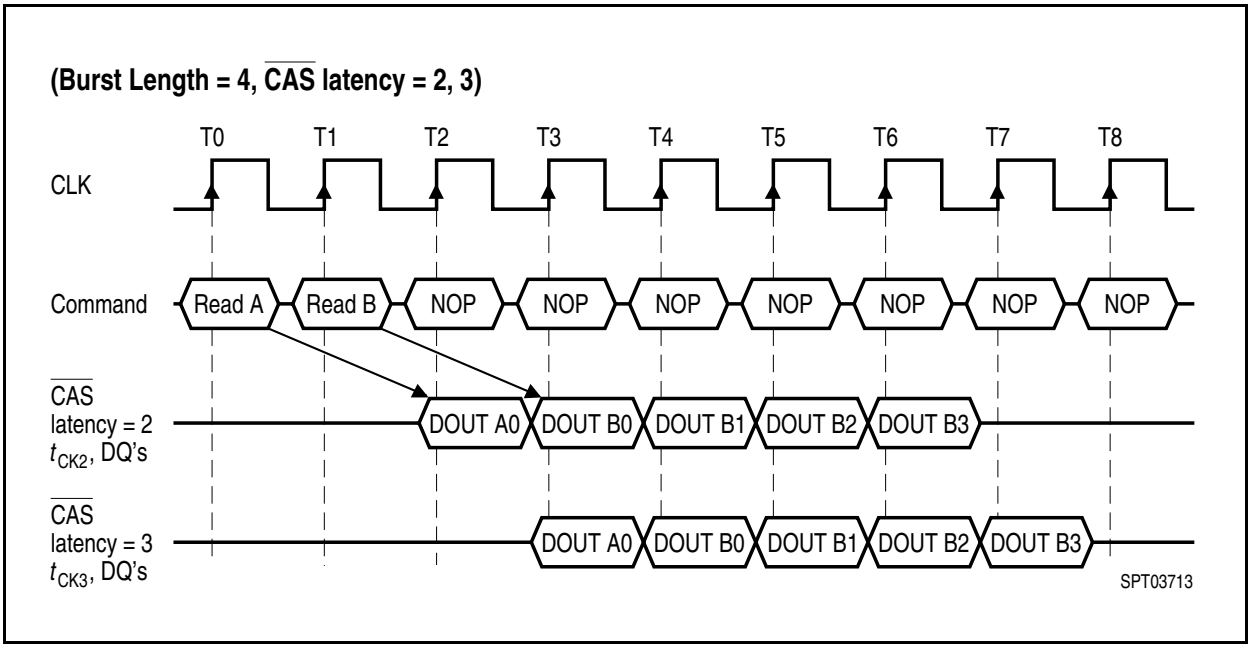


Figure 7 Read Interrupted by a Read

Read to Write Interval

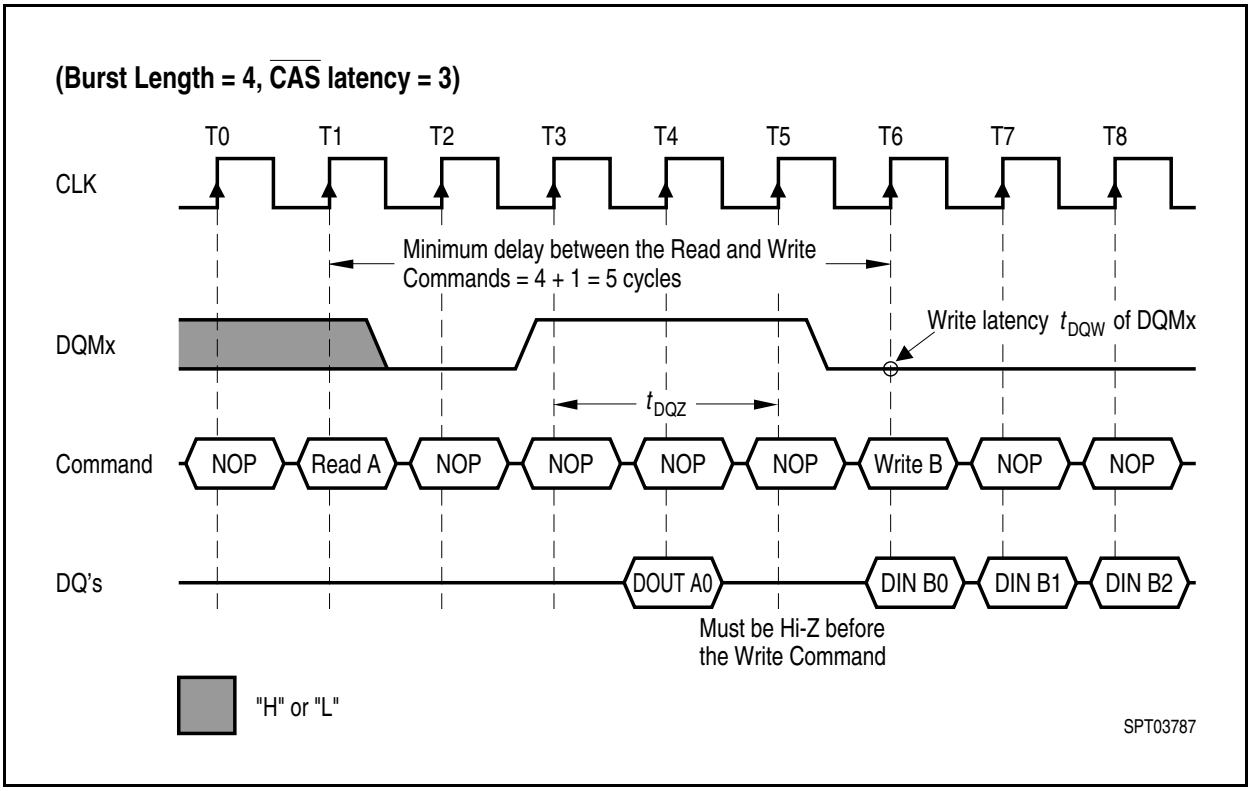


Figure 8 Read to Write Interval

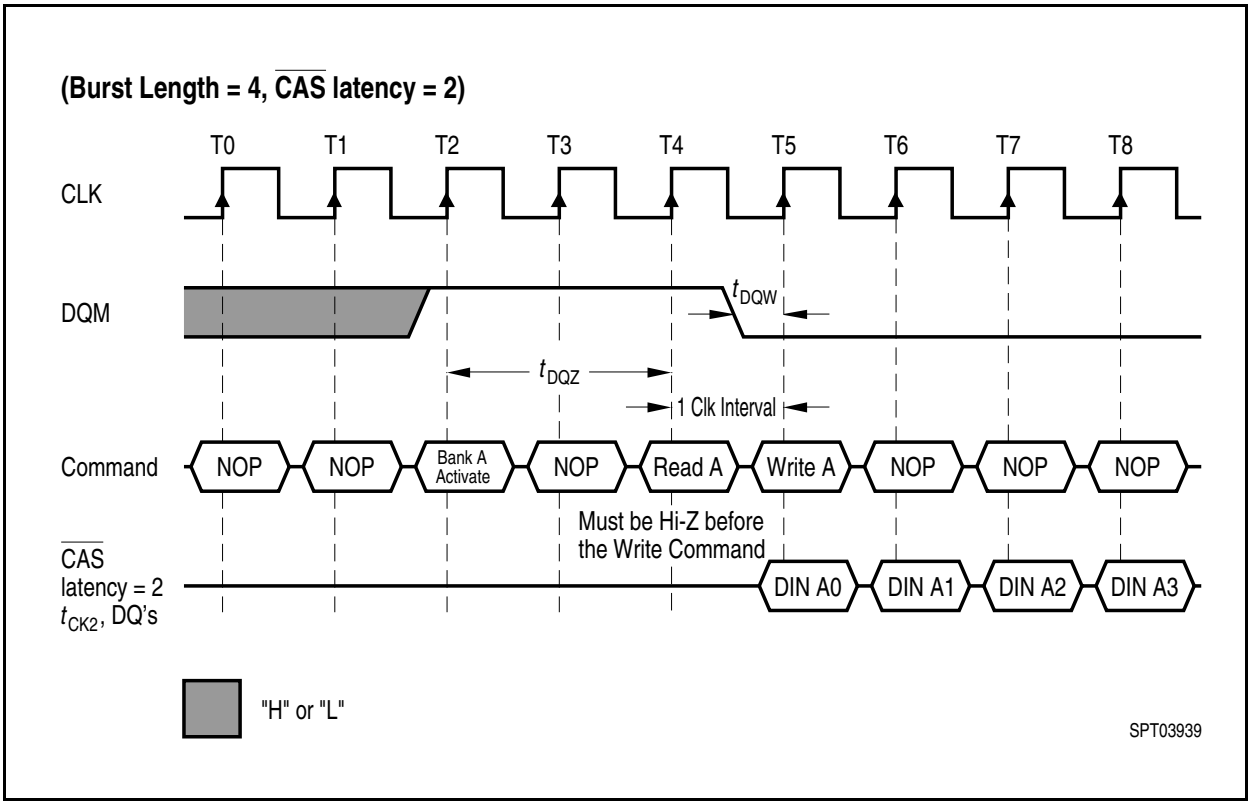


Figure 9 Minimum Read to Write Interval

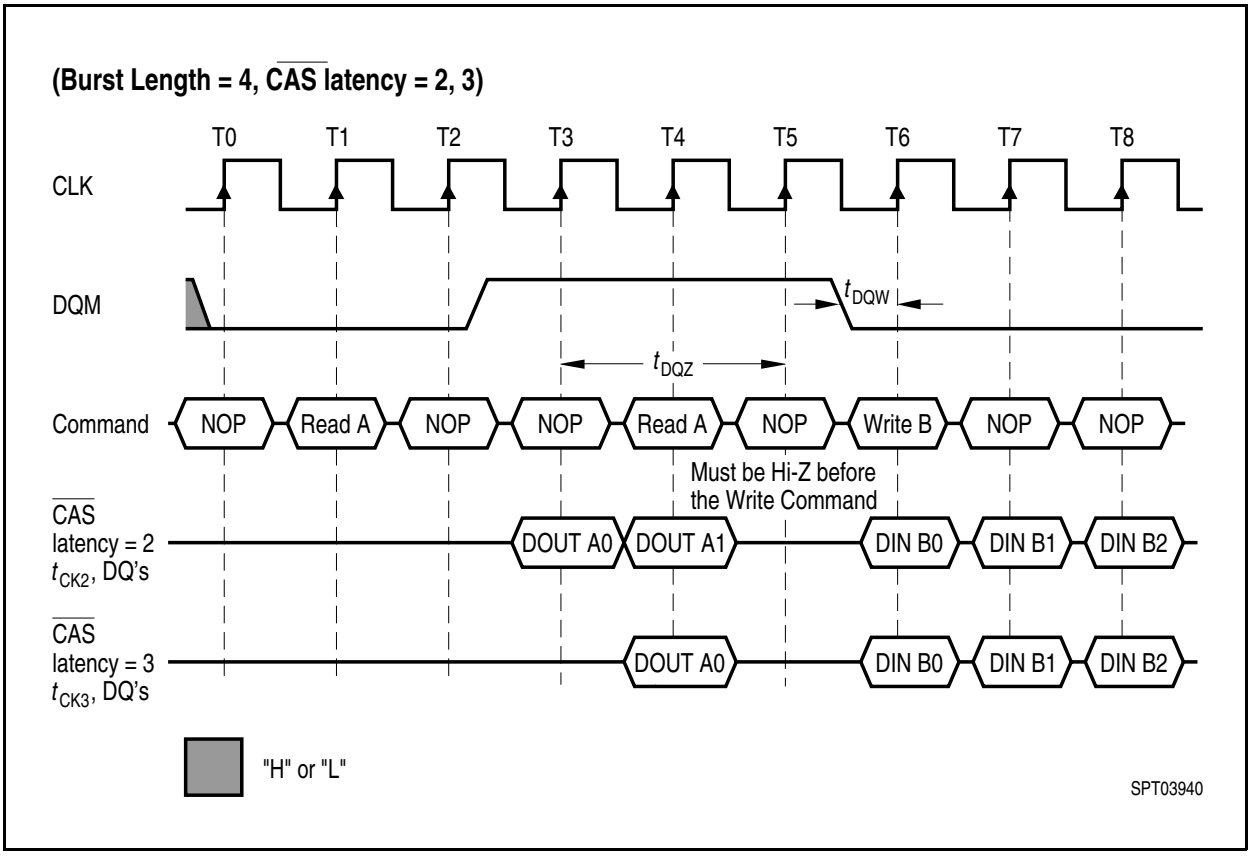


Figure 10 Non-Minimum Read to Write Interval

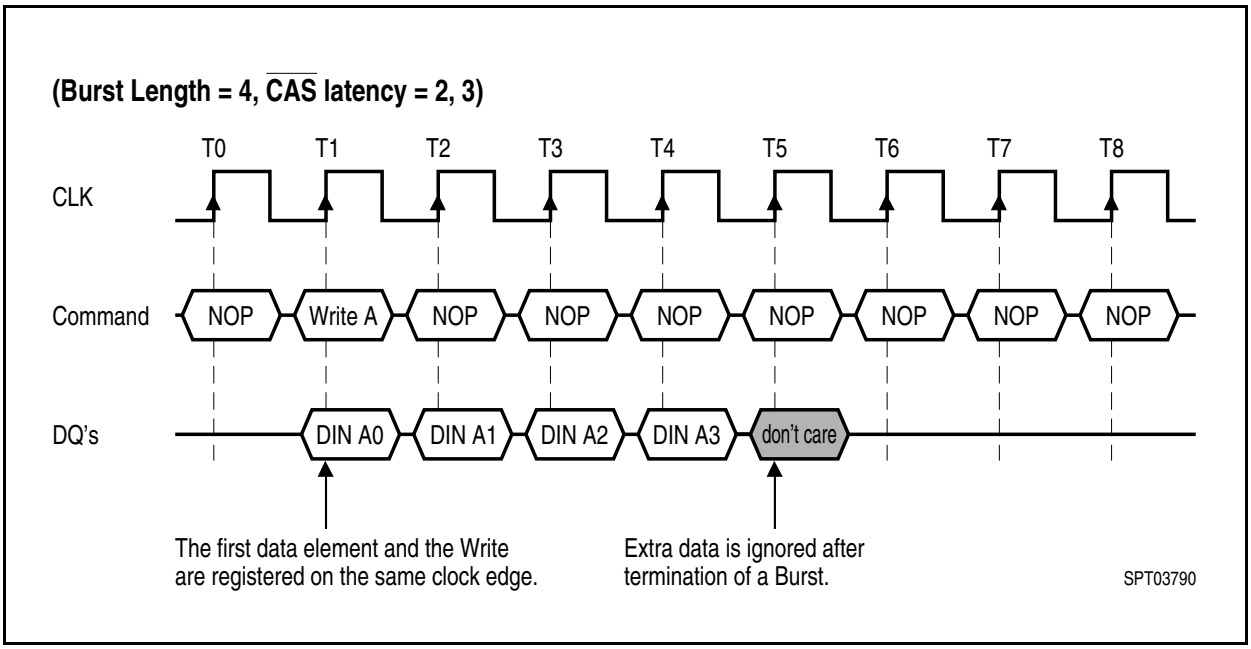


Figure 11 Burst Write Operation

Write and Read Interrupt

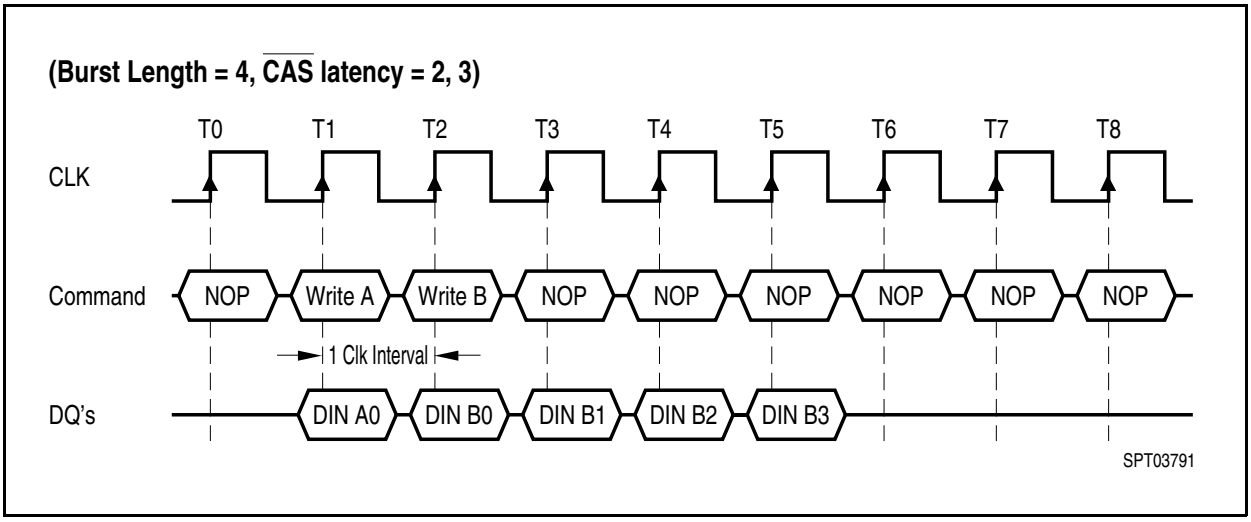


Figure 12 Write Interrupted by a Write

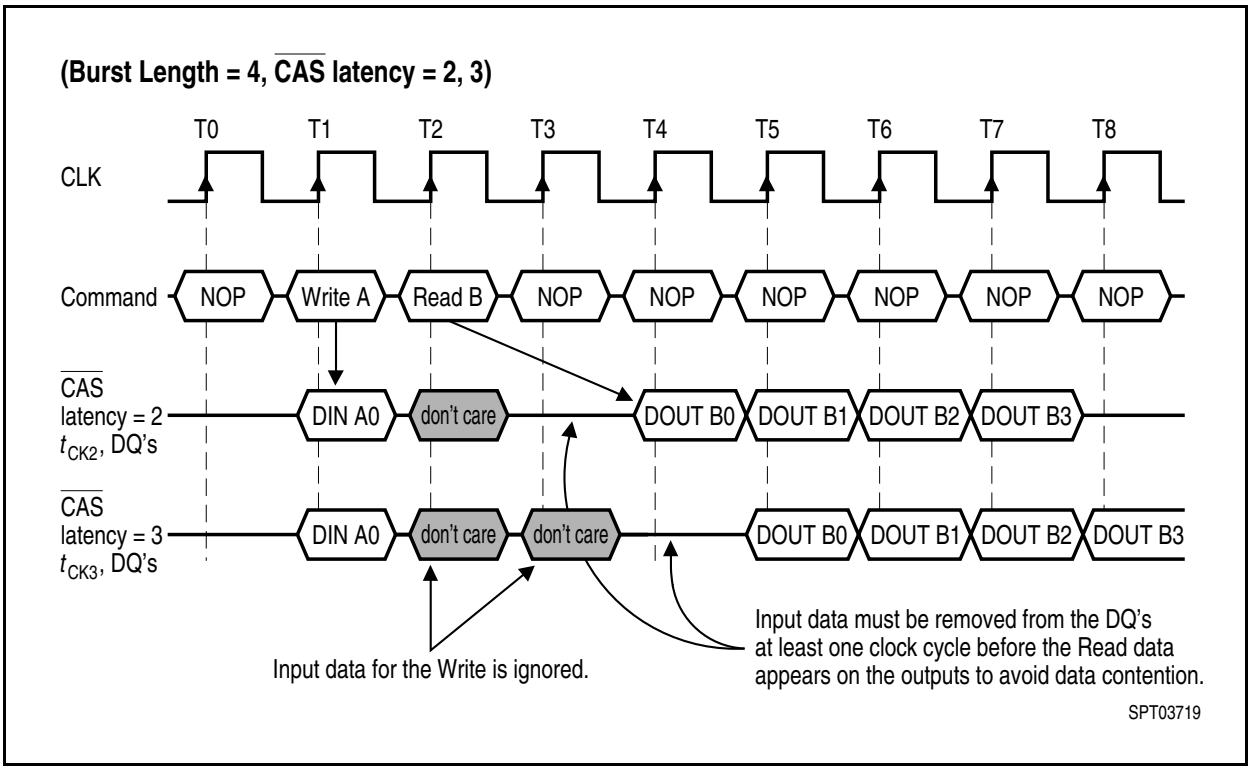


Figure 13 Write Interrupted by a Read

Burst Write and Read with Auto Precharge

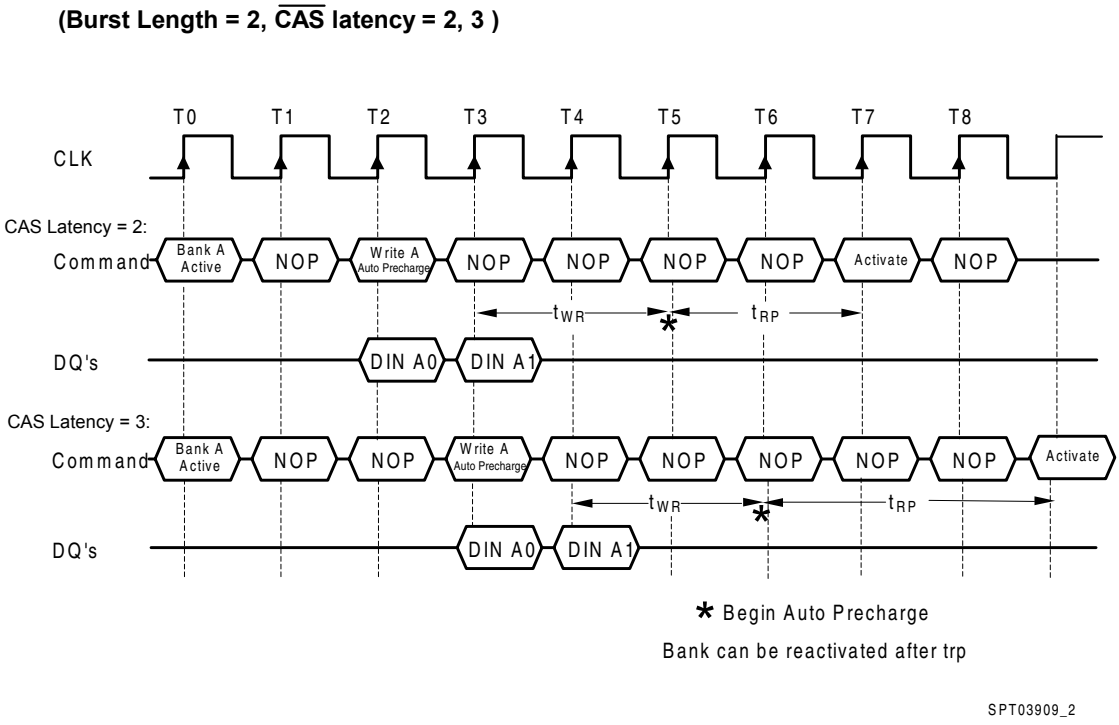


Figure 14 Burst Write with Auto-Precharge

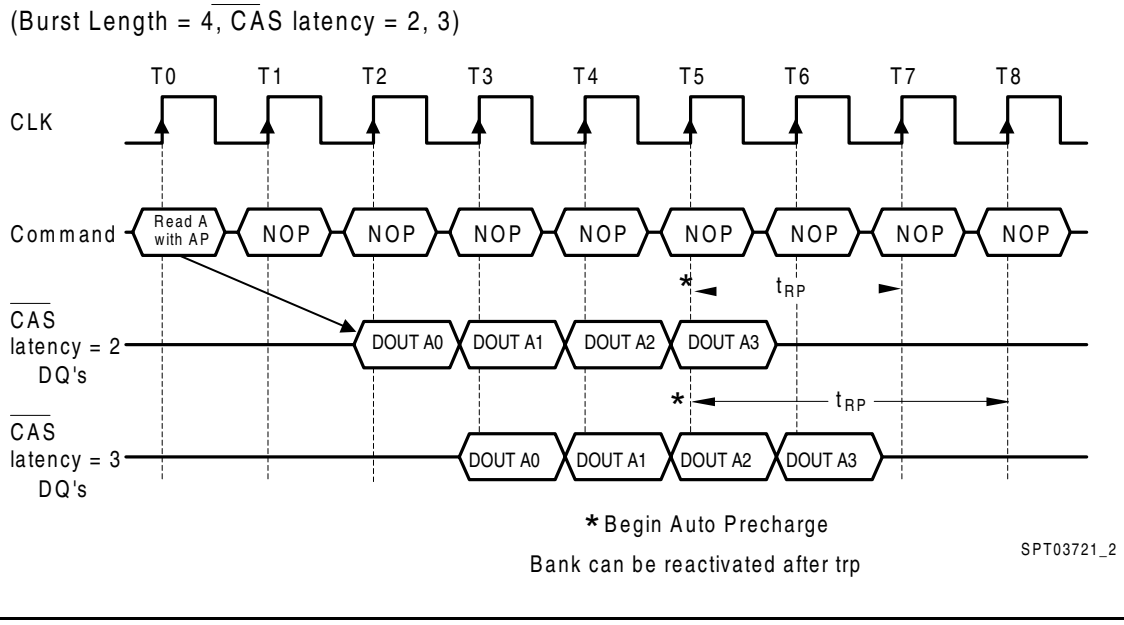


Figure 15 Burst Read with Auto-Precharge

AC Parameters

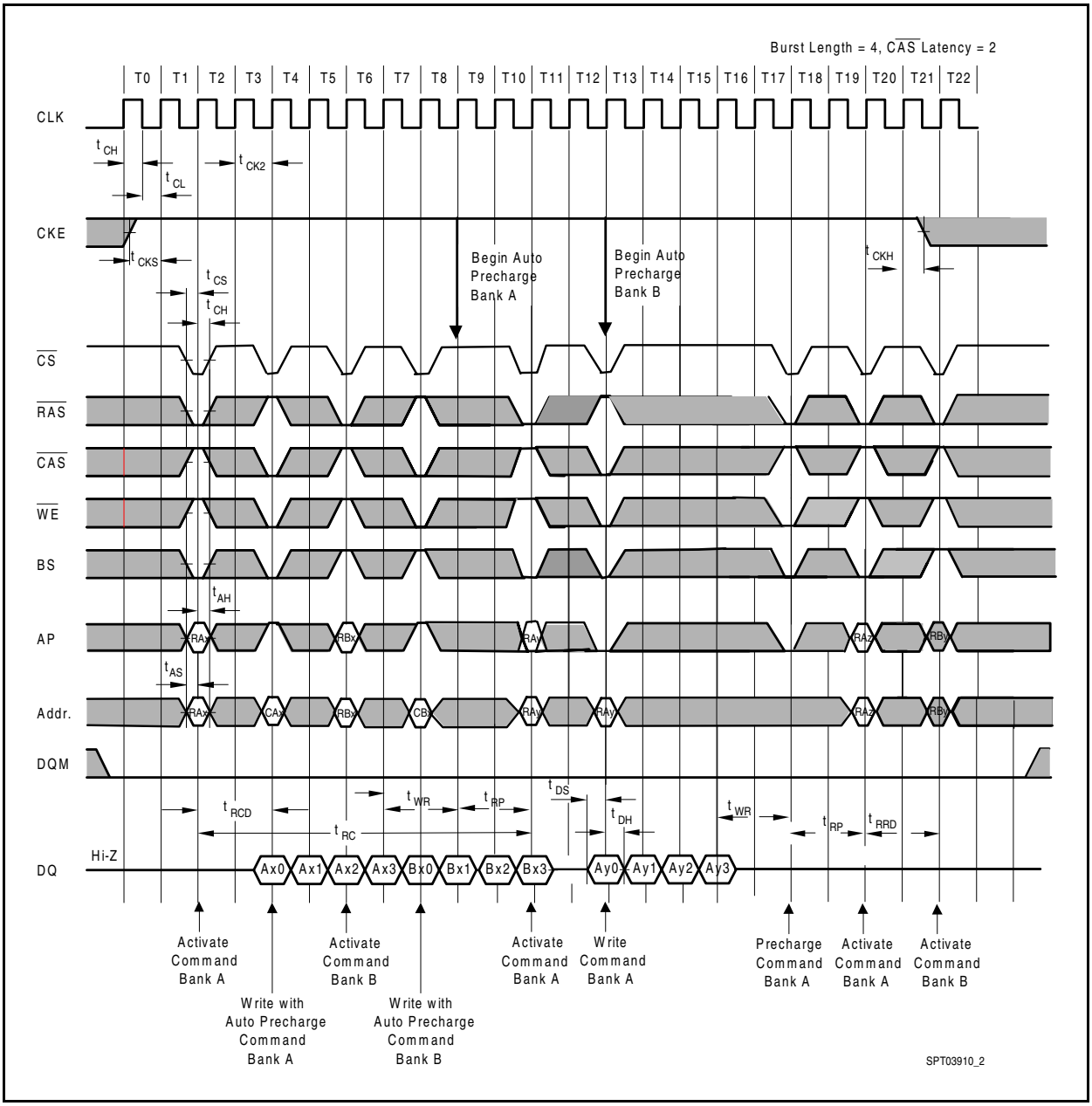


Figure 16 AC Parameters for a Write Timing

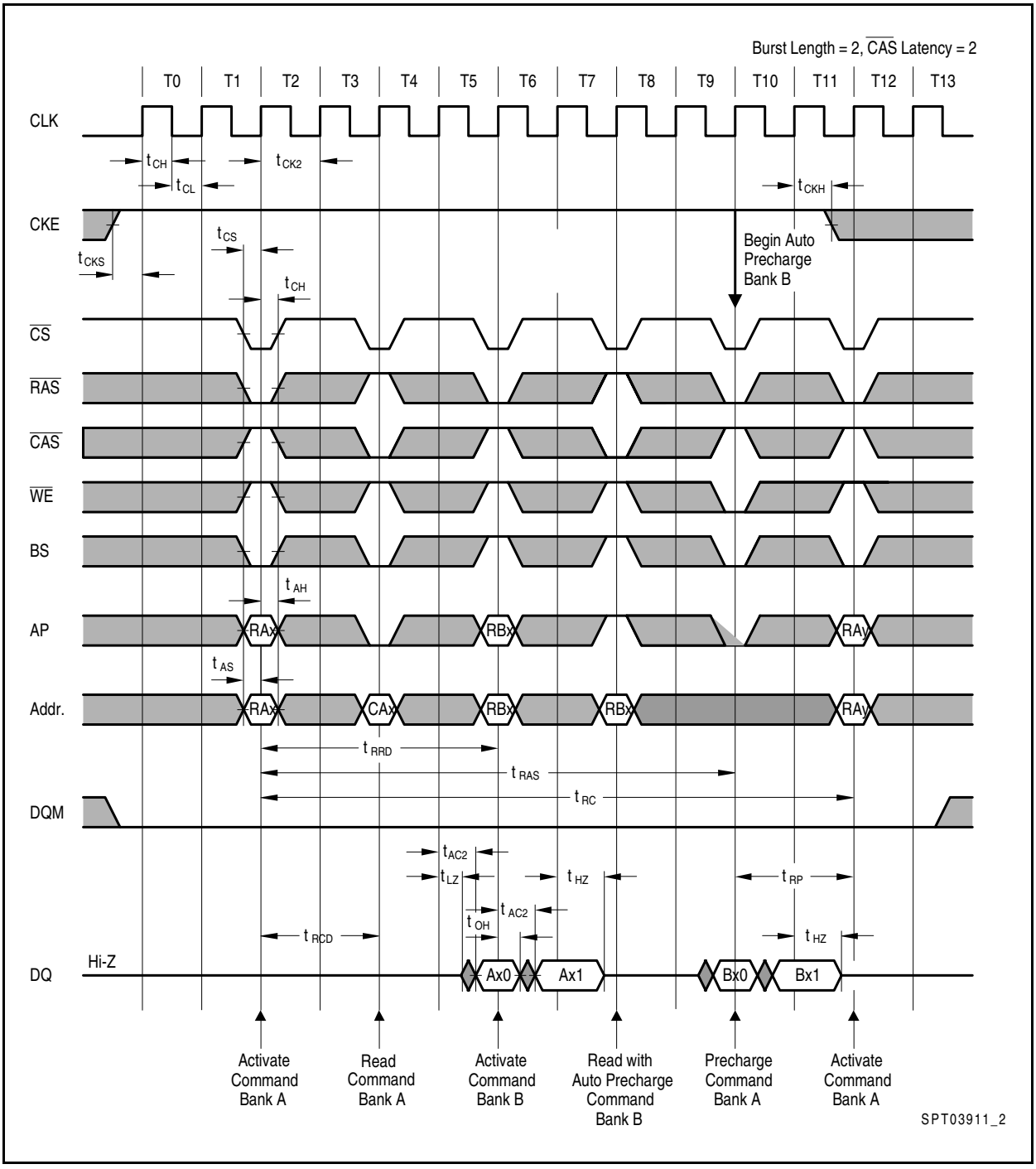


Figure 17 AC Parameters for a Read Timing

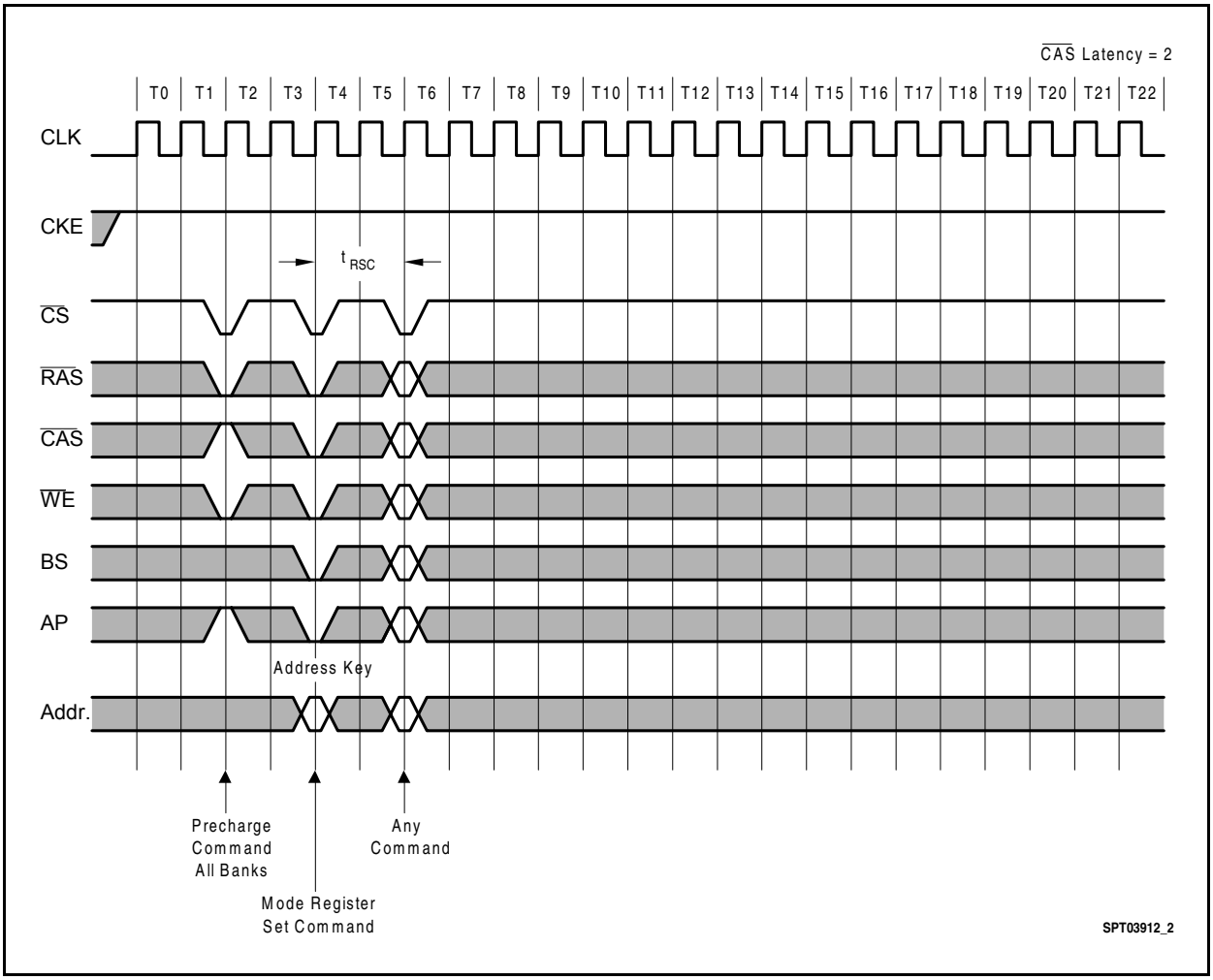


Figure 18 Mode Register Set

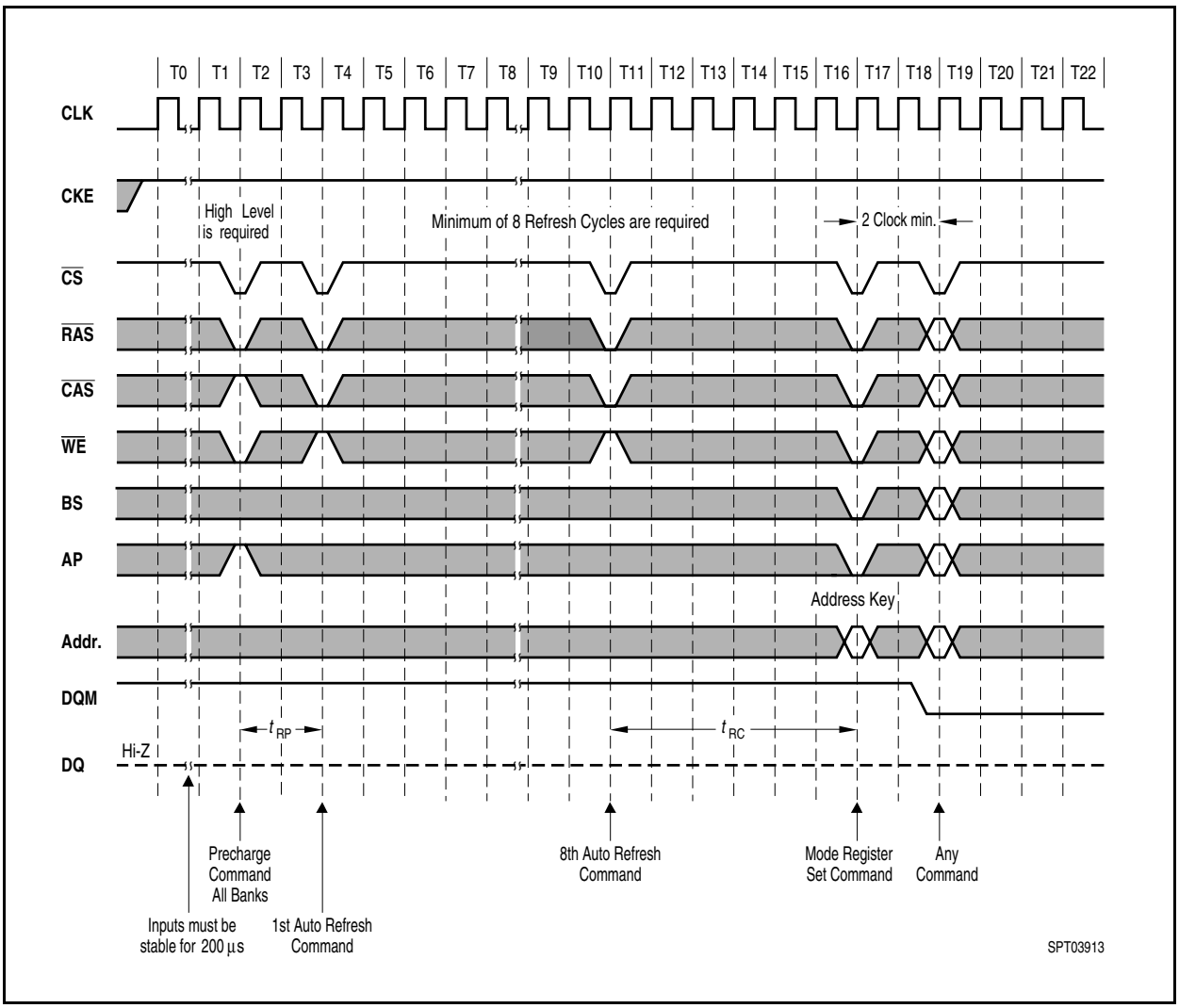


Figure 19 Power on Sequence and Auto Refresh (CBR)

Clock Suspension (Using CKE)

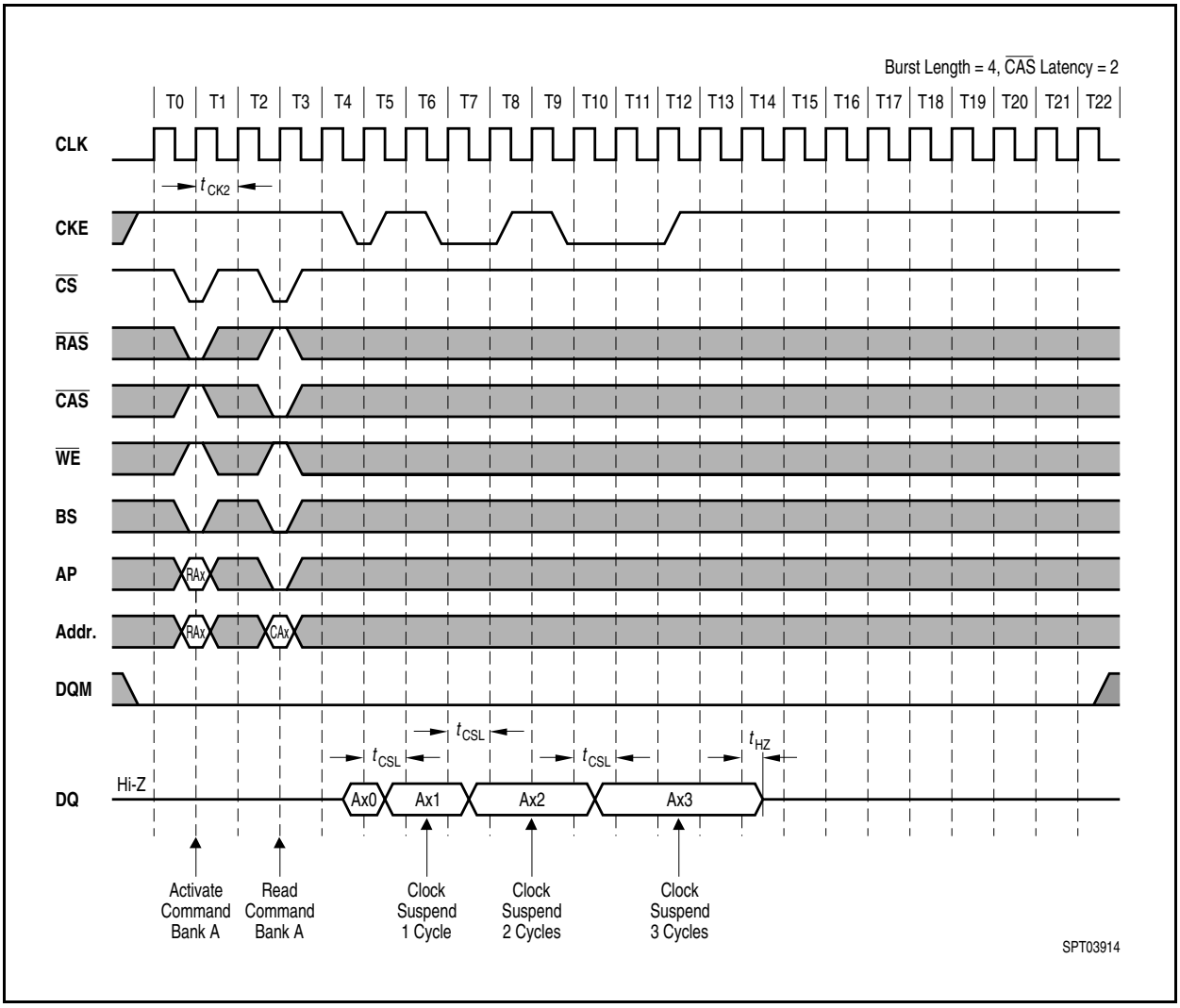


Figure 20 Clock Suspension During Burst Read CAS Latency = 2

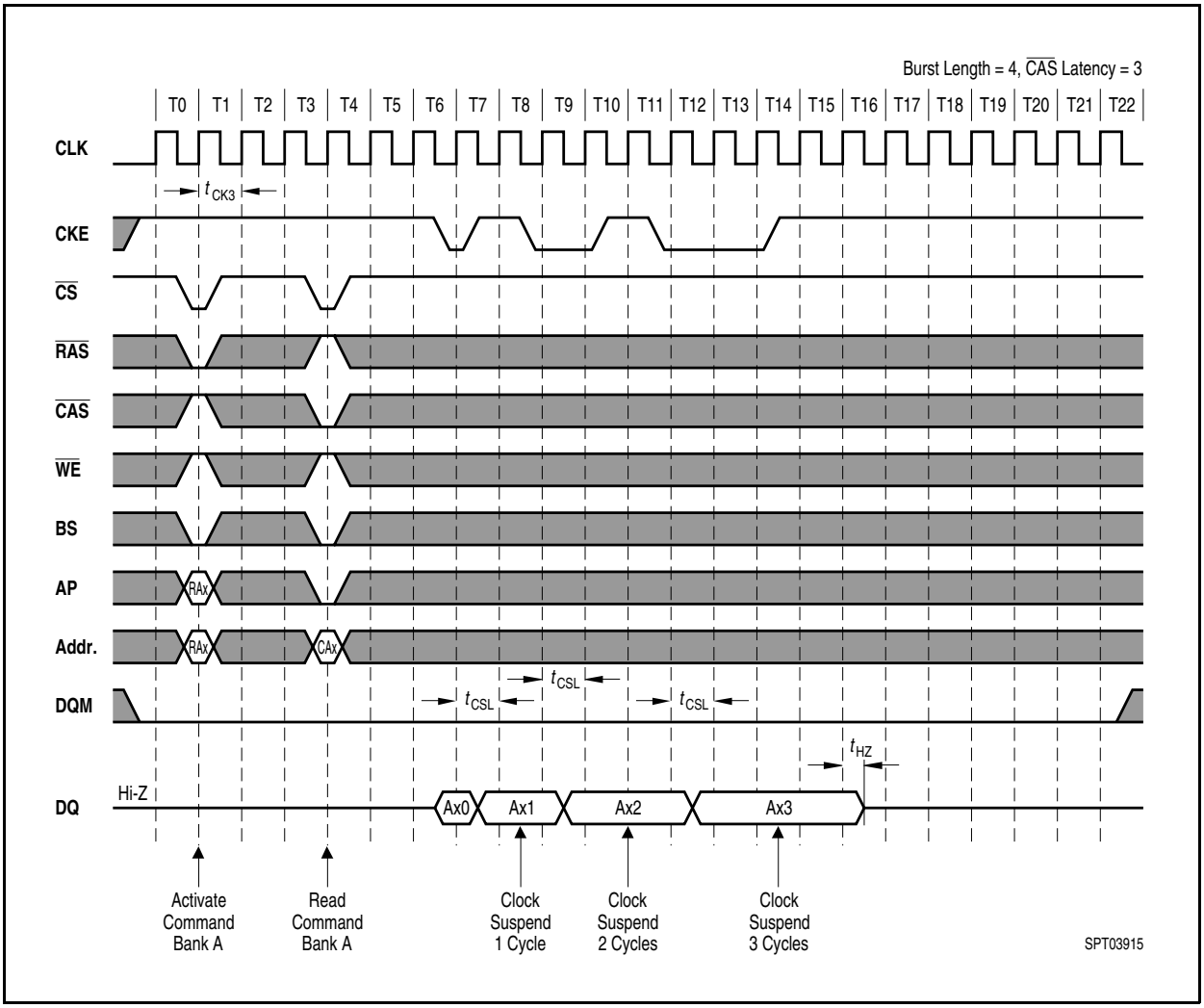


Figure 21 Clock Suspension During Burst Read CAS Latency = 3

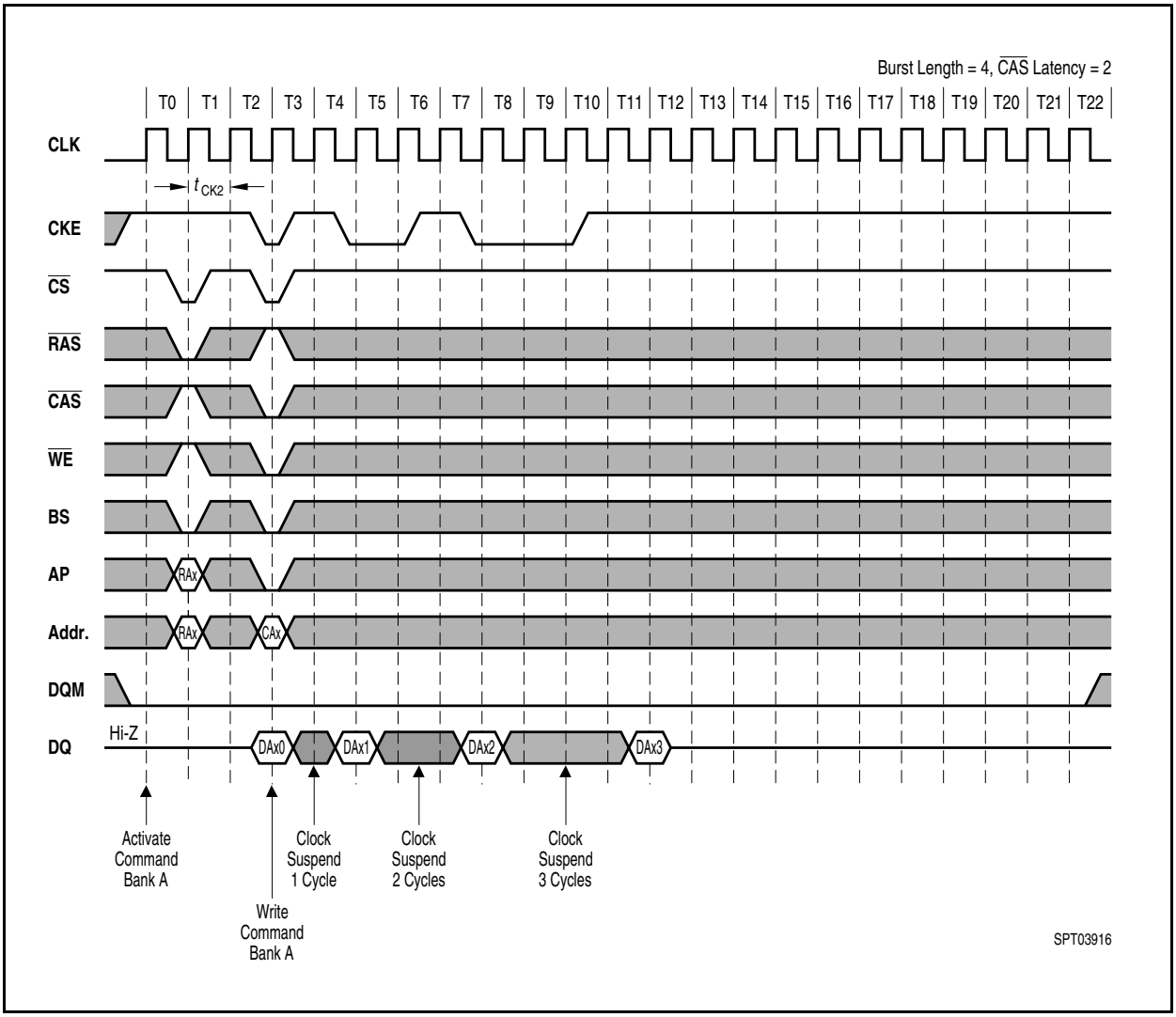


Figure 22 Clock Suspension During Burst Write CAS Latency = 2

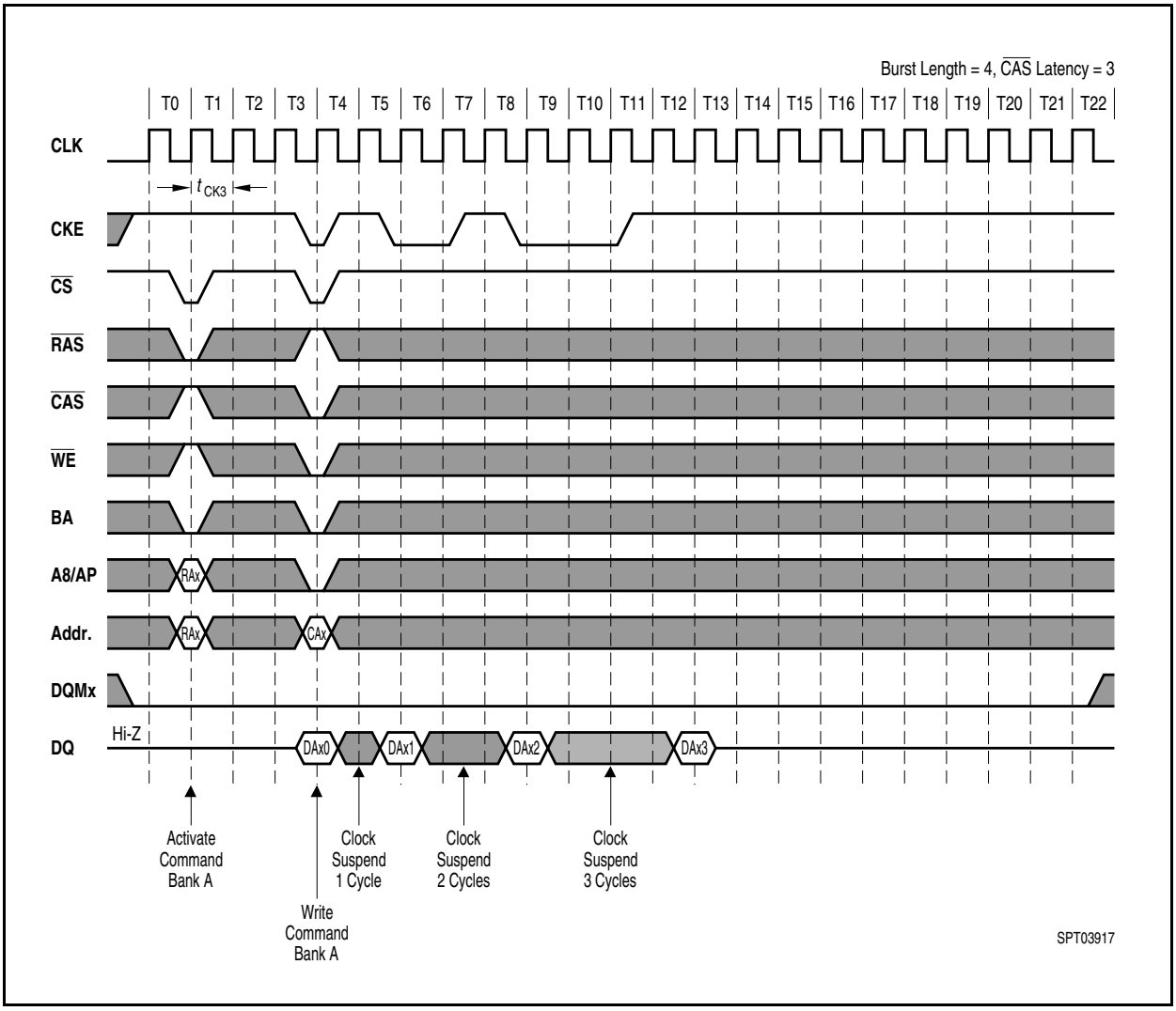


Figure 23 Clock Suspension During Burst Write CAS Latency = 3

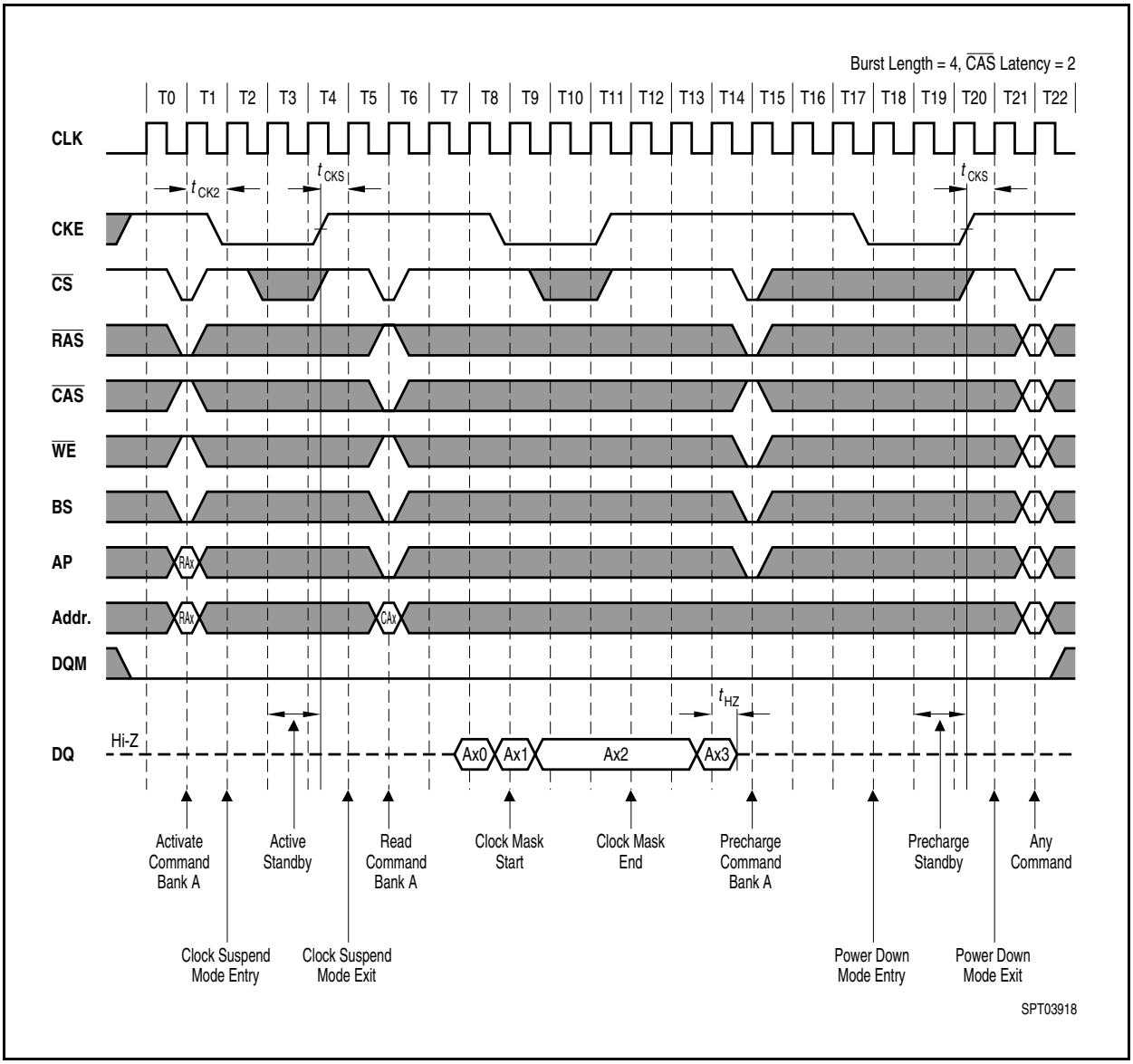


Figure 24 Power Down Mode and Clock Suspend

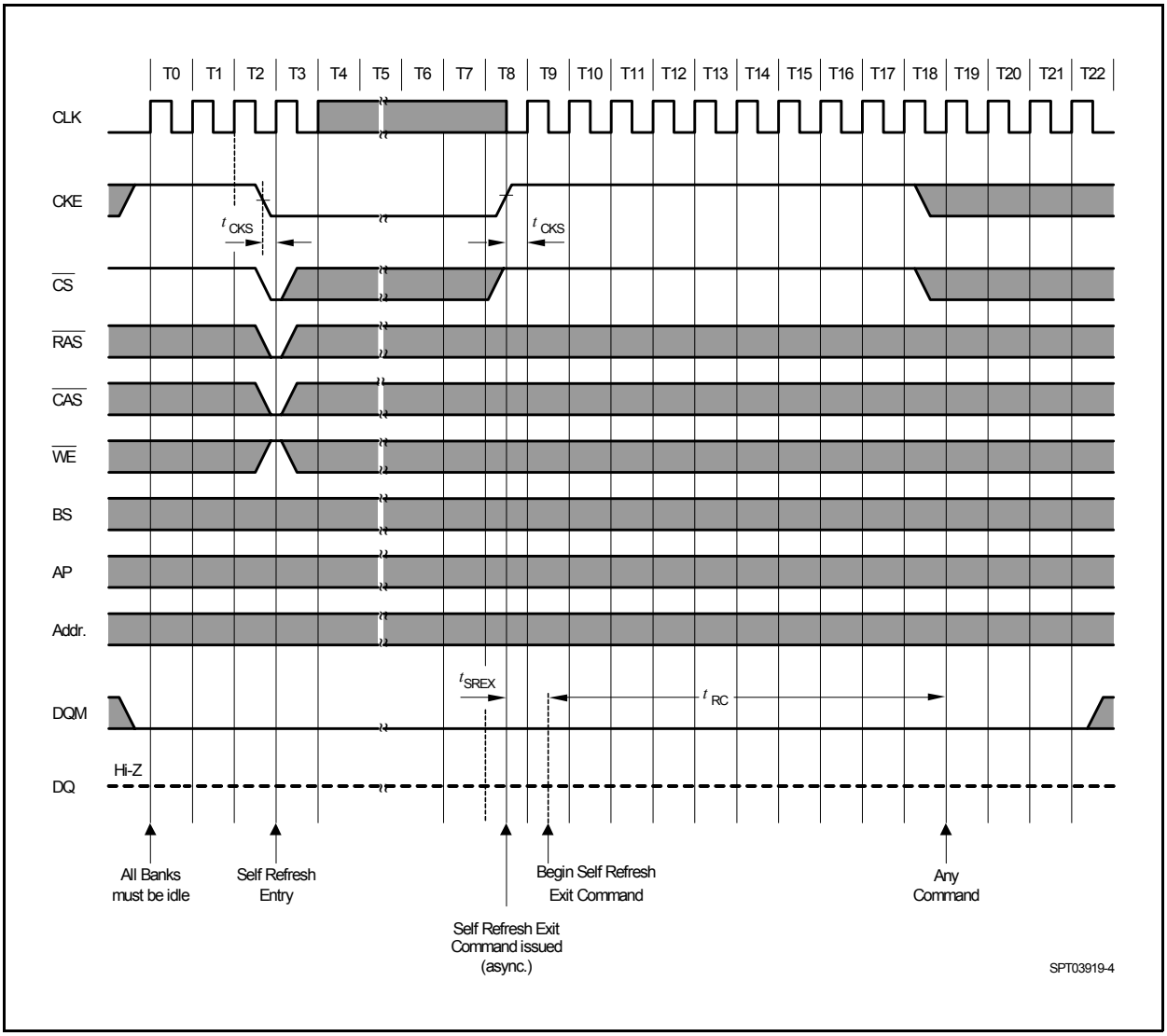


Figure 25 Self Refresh (Entry and Exit)

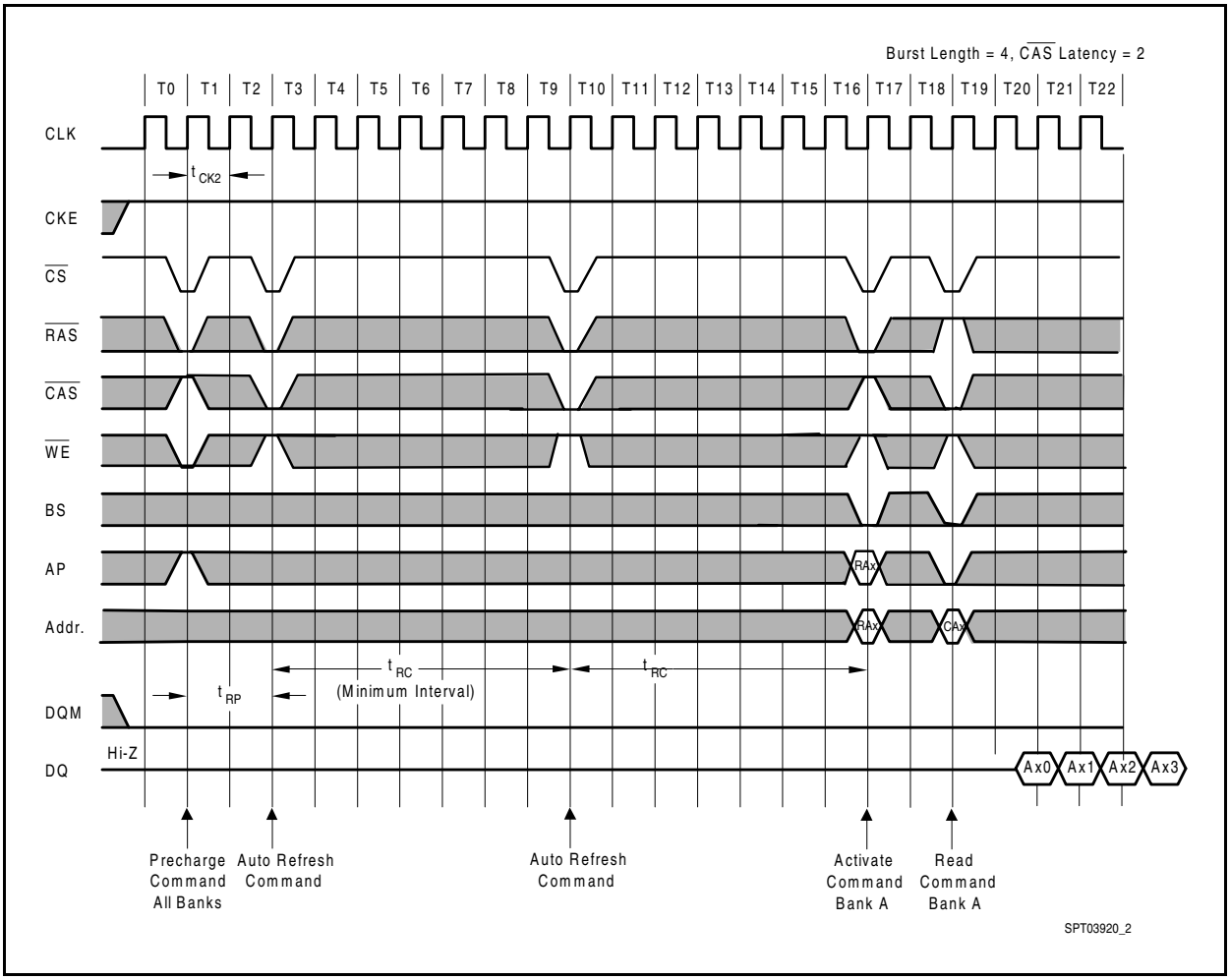


Figure 26 Auto Refresh (CBR)

Random Column Read (Page within same Bank)

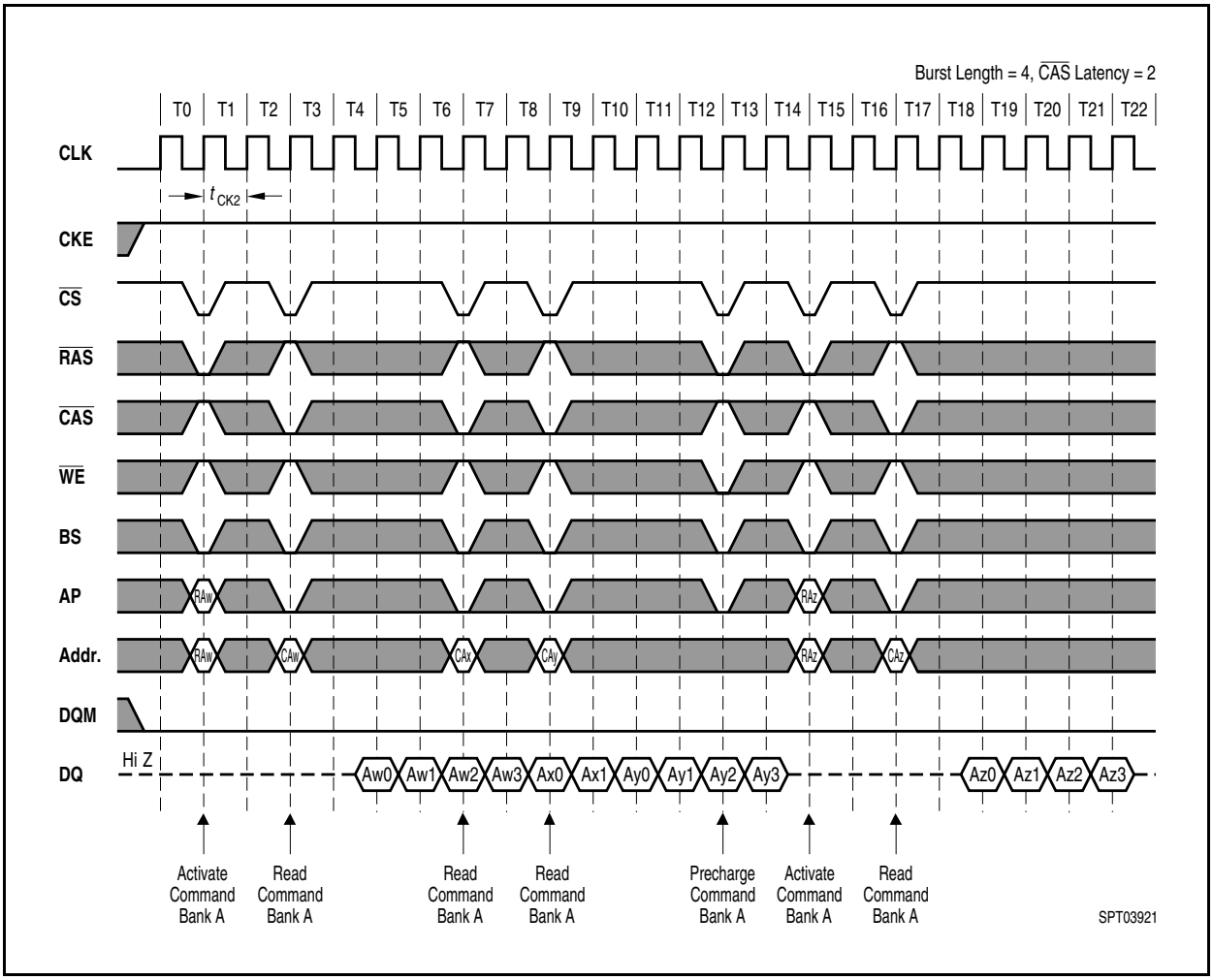


Figure 27 CAS Latency = 2

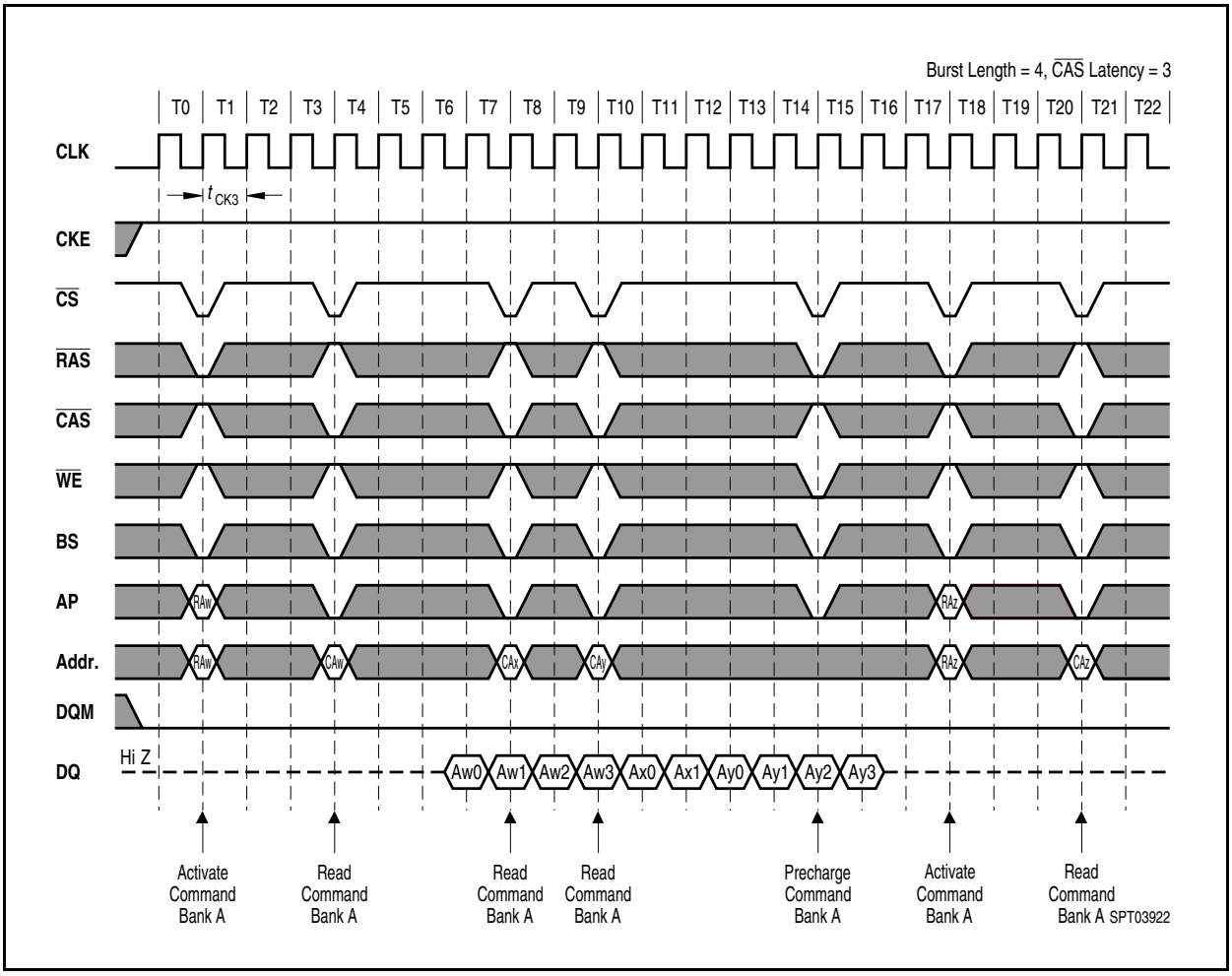


Figure 28 CAS Latency = 3

Random Column write (Page within same Bank)

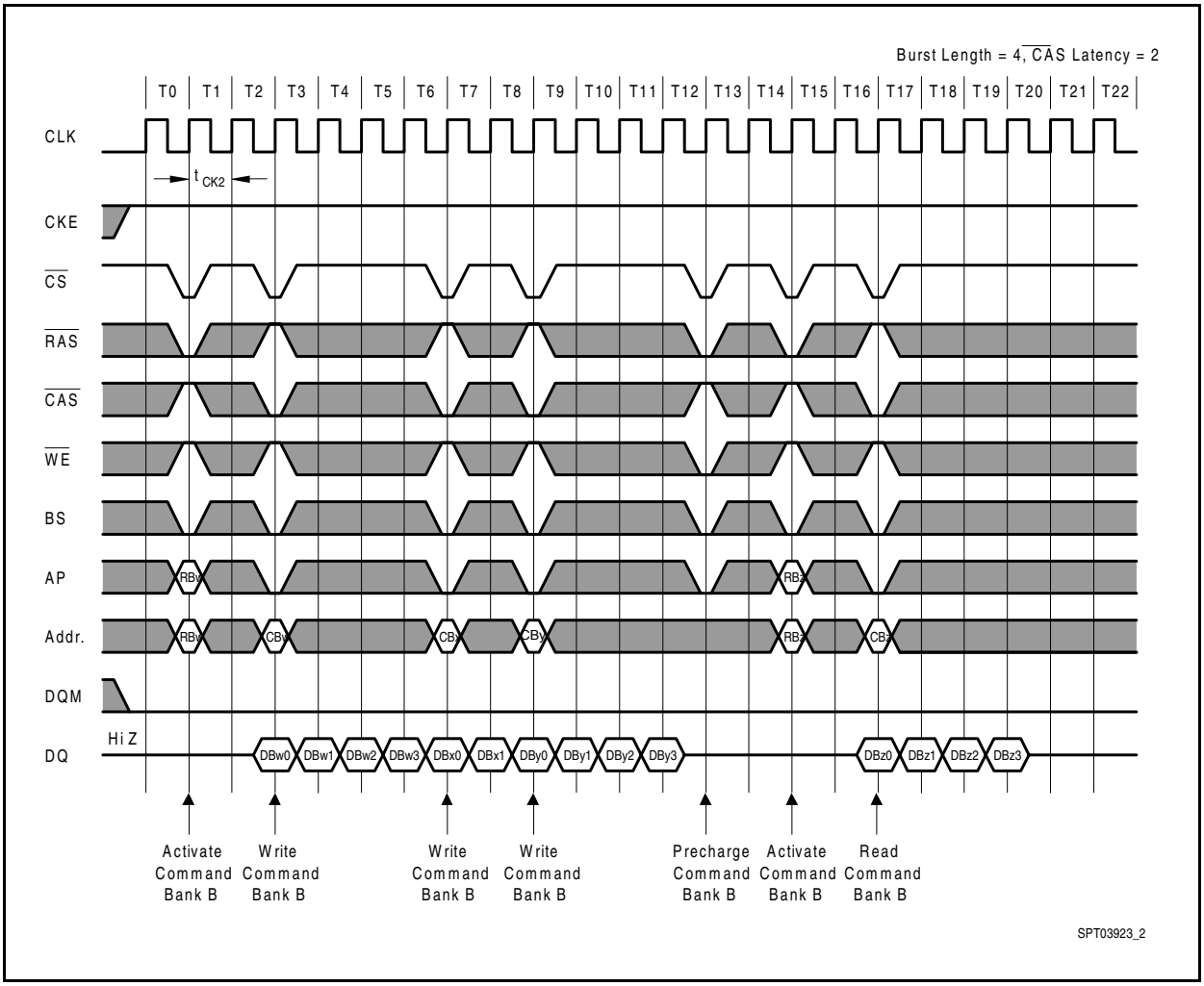


Figure 29 CAS Latency = 2

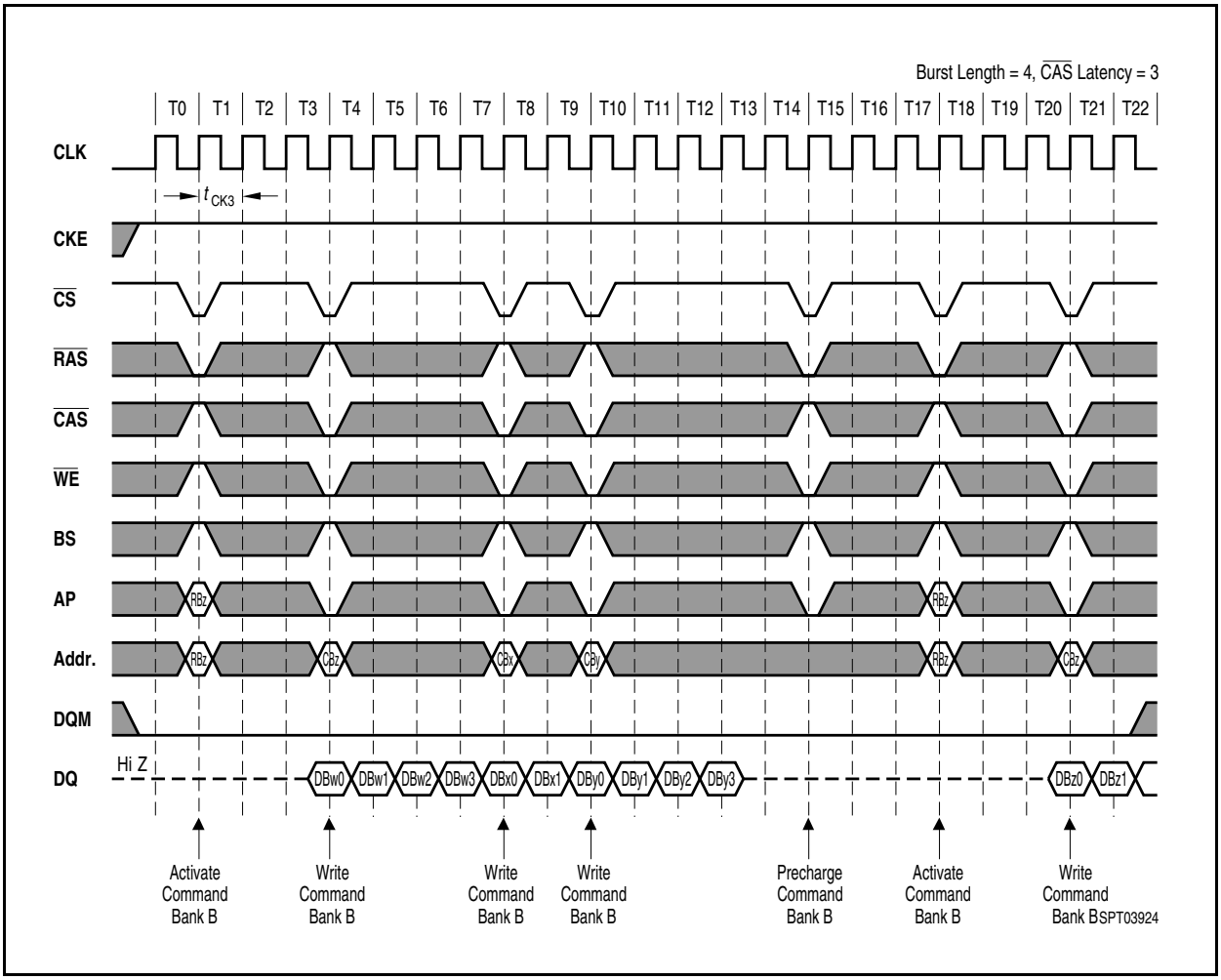


Figure 30 CAS Latency = 3

Random Row Read (Interleaving Banks) with Precharge

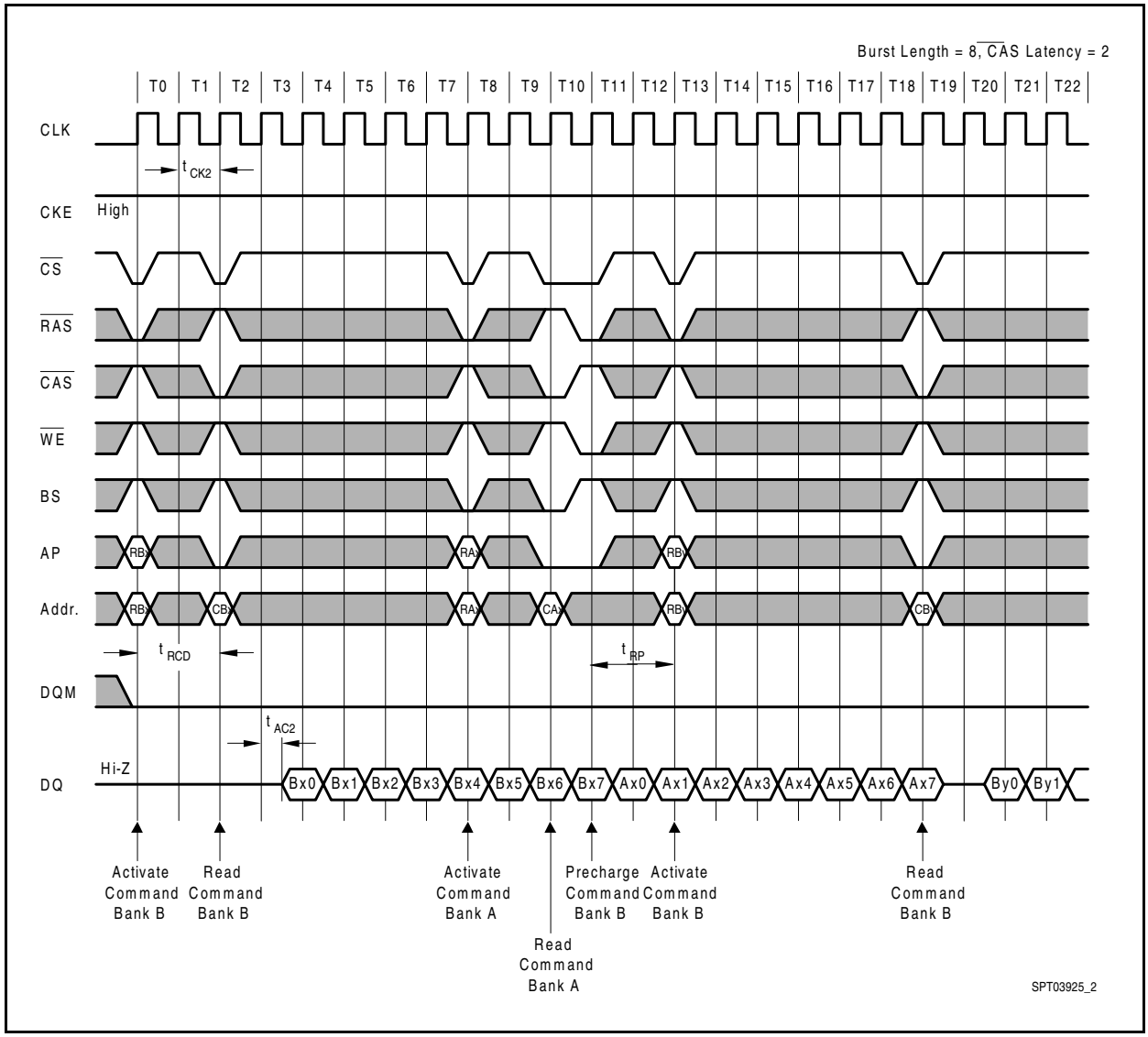


Figure 31 CAS Latency = 2

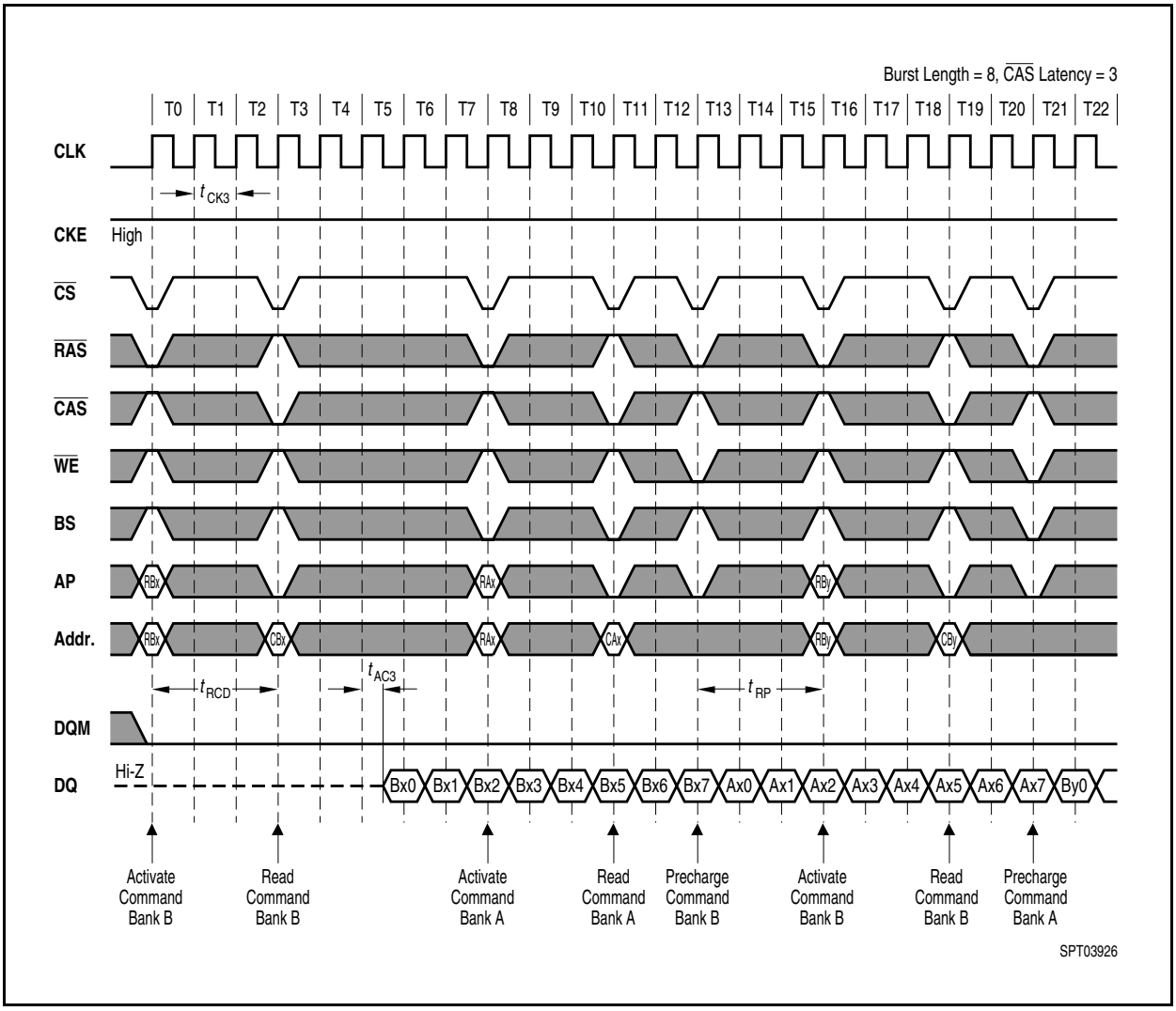


Figure 32 CAS Latency = 3

Random Row Write (Interleaving Banks) with Precharge

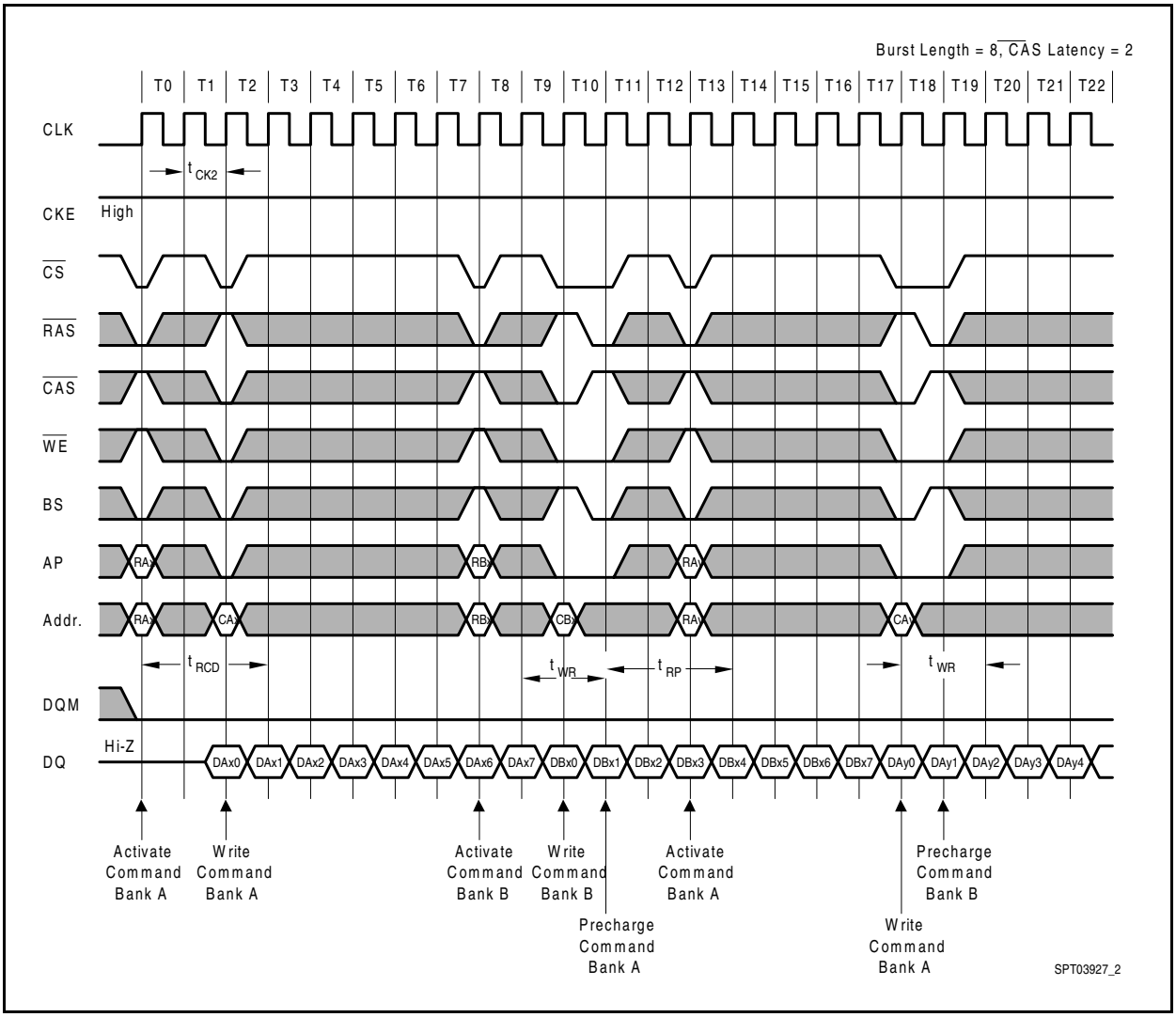


Figure 33 CAS Latency = 2

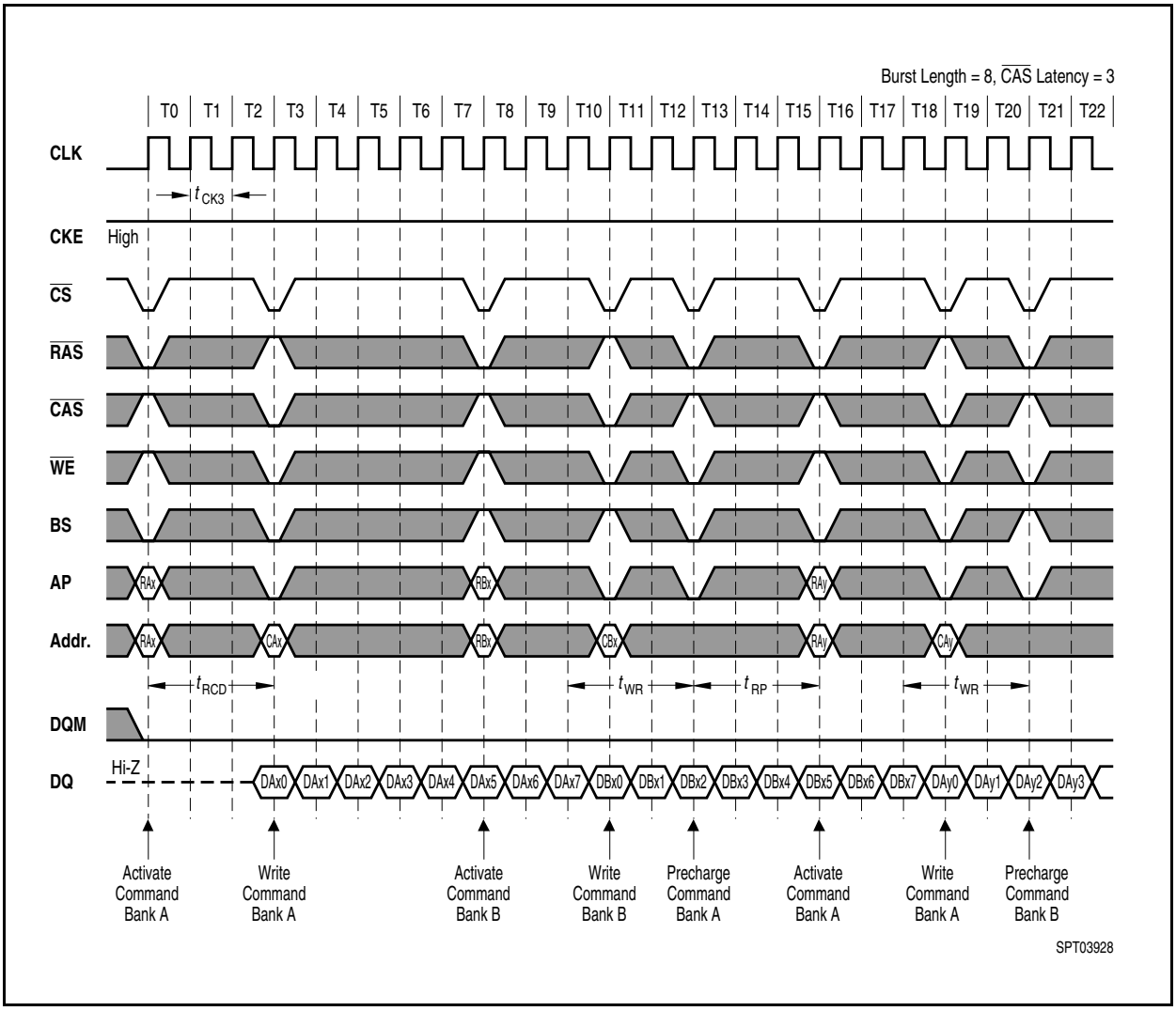


Figure 34 CAS Latency = 3

Precharge termination of a Burst

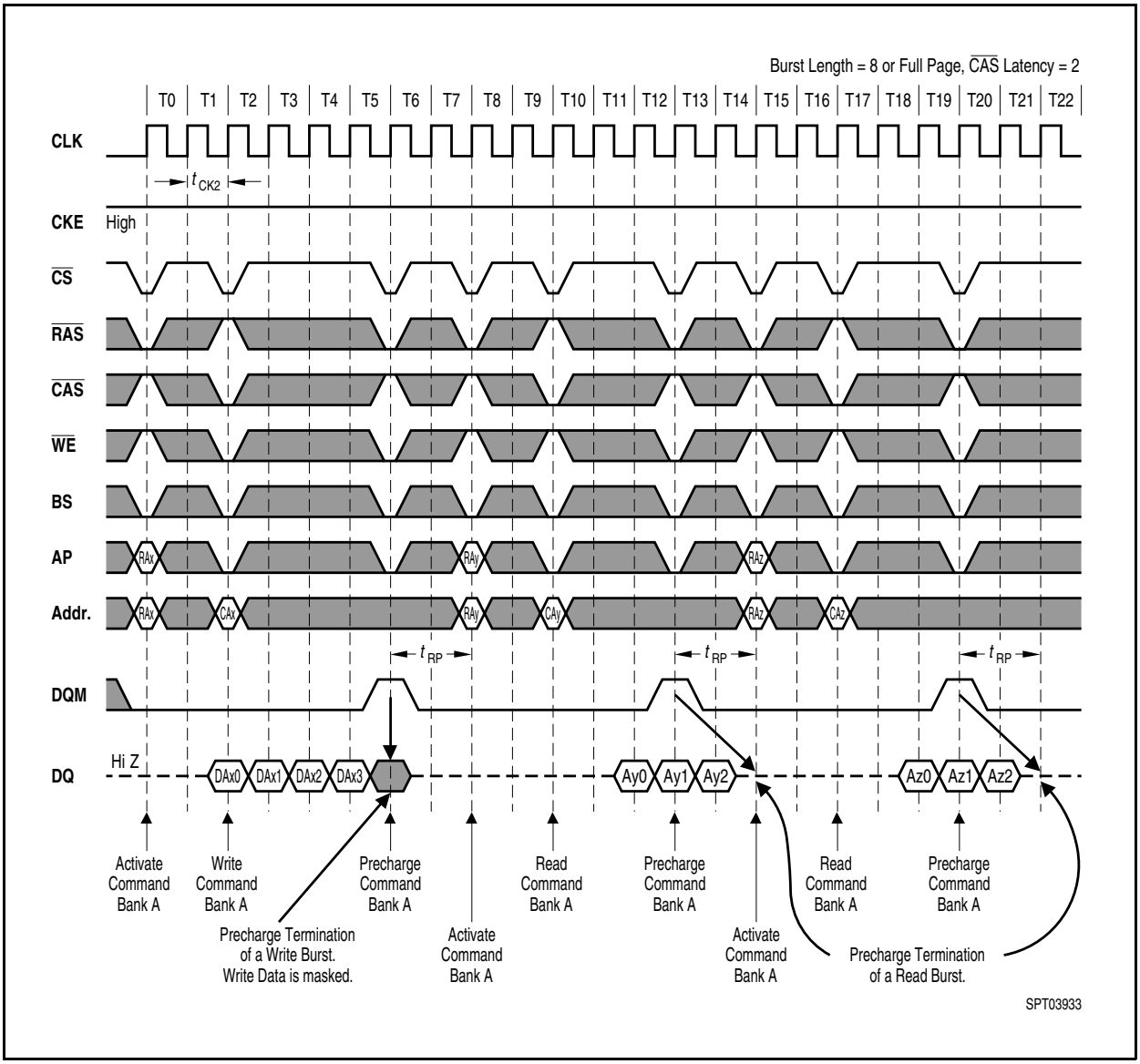


Figure 35 CAS Latency = 2

Deep Power Down Mode

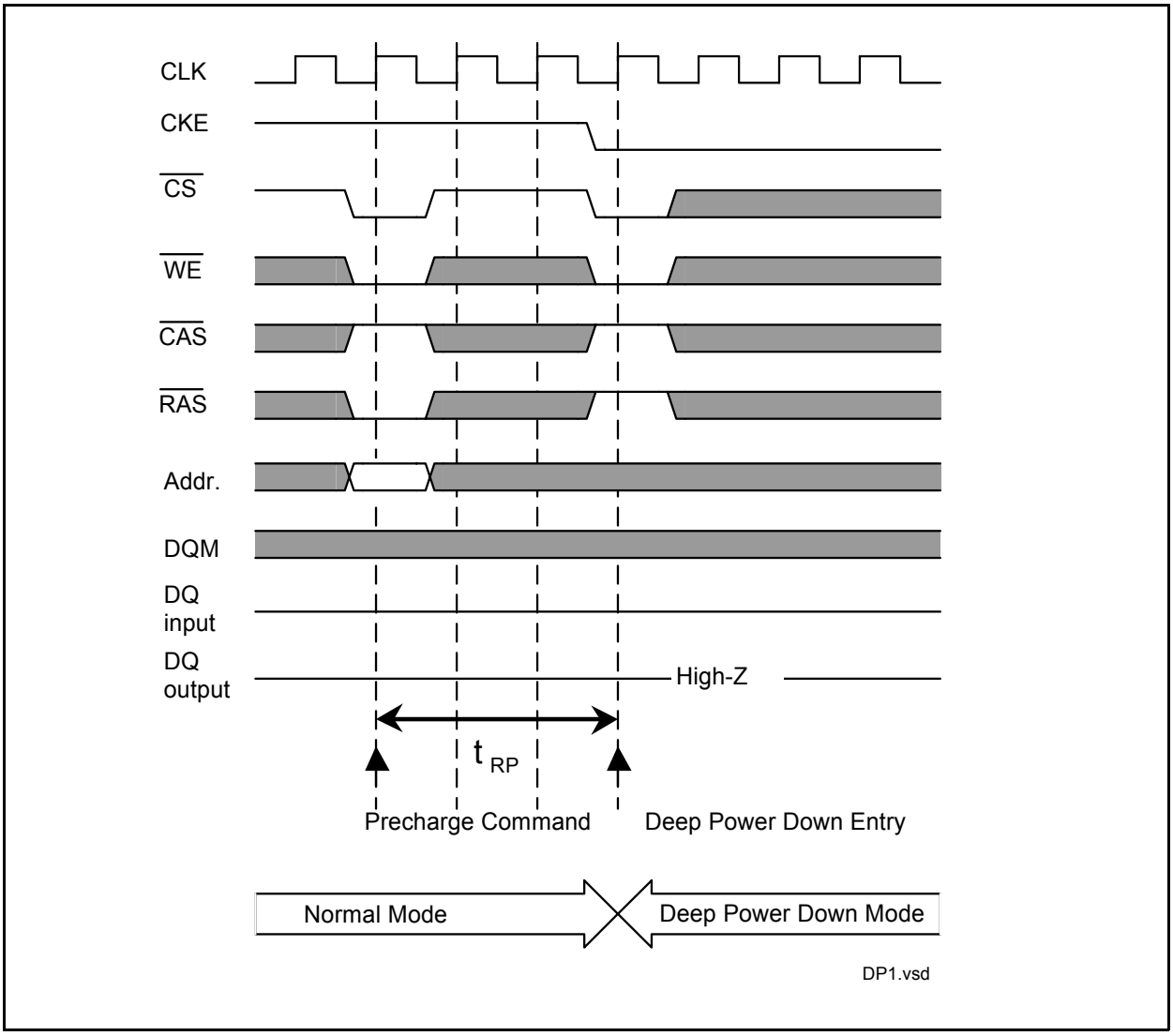


Figure 36 Deep Power Down Mode Entry

Note: The deep power down mode has to be maintained for a minimum of 100µs.

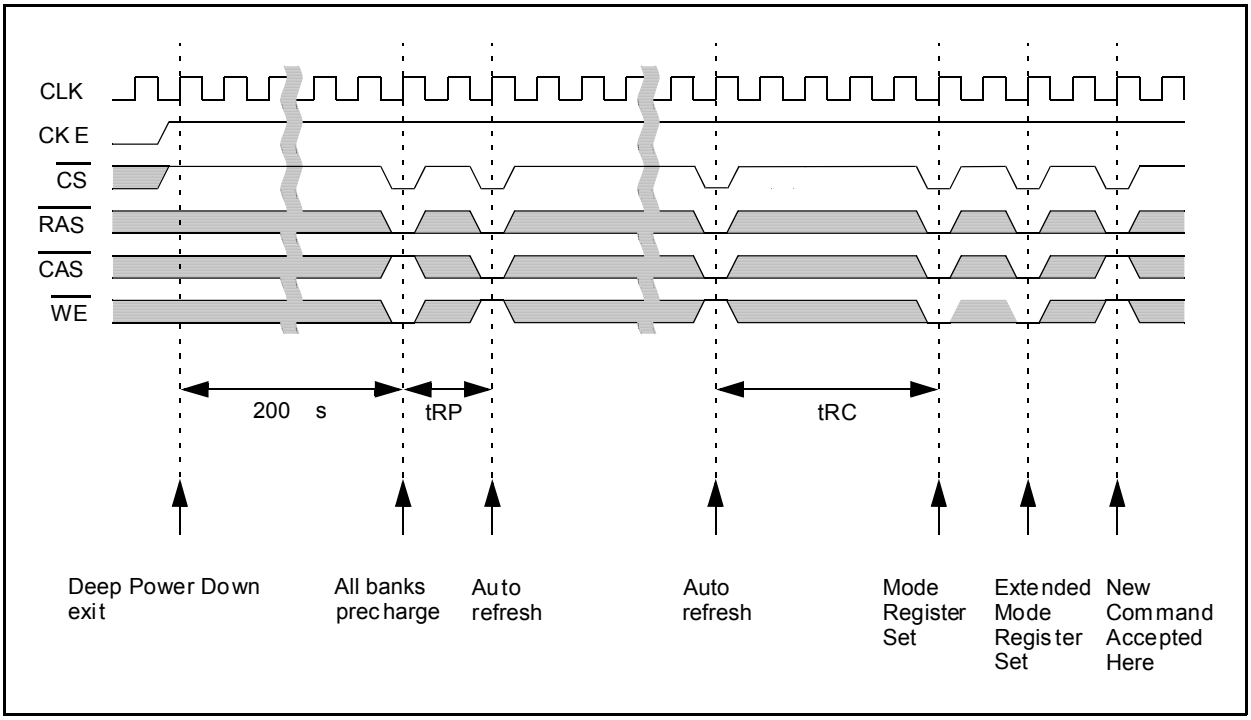


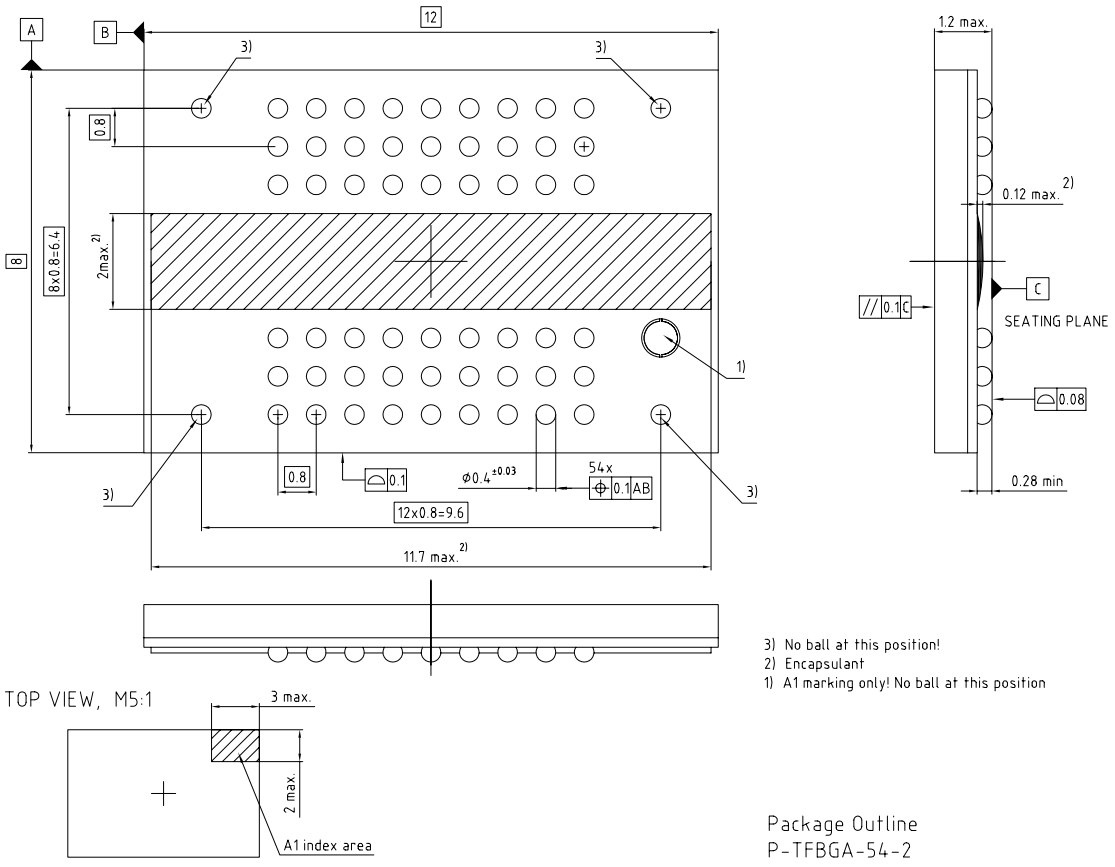
Figure 37 Deep Power Down Exit

Note: The deep power down mode is exited by asserting CKE high. After the exit, the following sequence is needed to enter a new command:

1. *Maintain NOP input conditions for a minimum of 200 µs*
2. *Issue precharge commands for all banks of the device*
3. *Issue eight or more autorefresh commands*
4. *Issue a mode register set command to initialize the mode register*
5. *Issue an extended mode register set command to initialize the extende mode register*

6 Package Outline

P-TFBGA-54
(Plastic Thin Small Outline Package Type II)



tolerance ±0.1mm for length and width

Figure 38 Package Outline

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

http://www.infineon.com

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