Document Title

2Bank x 512K x 16bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	Jan. 2004	Preliminary
0.2	Change : PC100 CL2 tAC --> 5.5ns tDPL --> 1CLK	Apr. 2004	Preliminary

DESCRIPTION

The Hynix HY5V16EF6(P) series is a 16,777,216bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY5V16EF6(P) is organized as 2banks of 524,288x16.

HY5V16EF6(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 1,2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

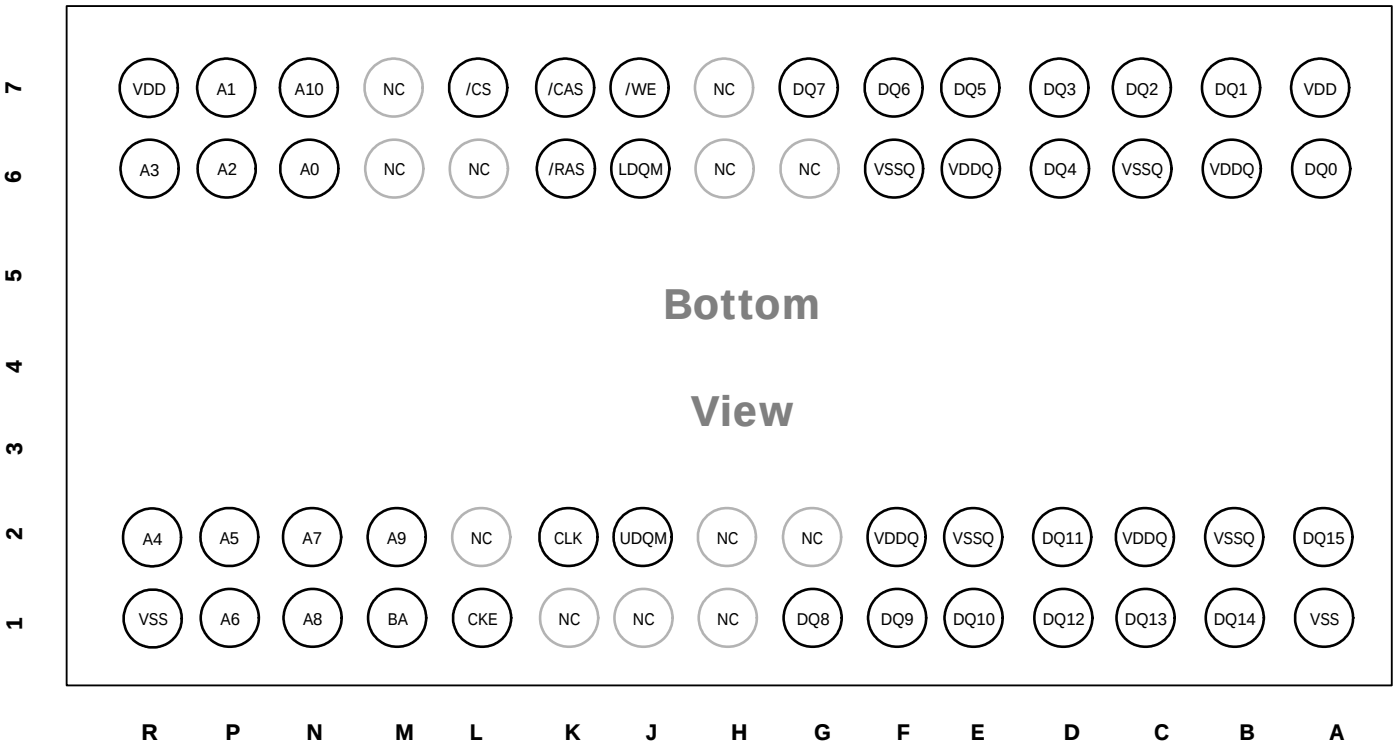
FEATURES

- Voltage : Single 3.0V to 3.6V power supply
- All device pins are compatible with LVTTL interface
- 60Ball FBGA_(Lead, Lead Free)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM and LDQM
- Internal two banks operation
- Auto refresh and self refresh
- 2048 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

Part No.	Clock Frequency	CAS Latency	Organization	Interface	Package
HY5V16EF6-H	133MHz	3	2Banks x 512K x16bit	LVTTL	60Ball FBGA, Lead
HY5V16EF6-P	100MHz	2			
HY5V16EF6-S	100MHz	3			
HY5V16EF6P-H	133MHz	3			60Ball FBGA, Lead Free
HY5V16EF6P-P	100MHz	2			
HY5V16EF6P-S	100MHz	3			

Ball CONFIGURATION

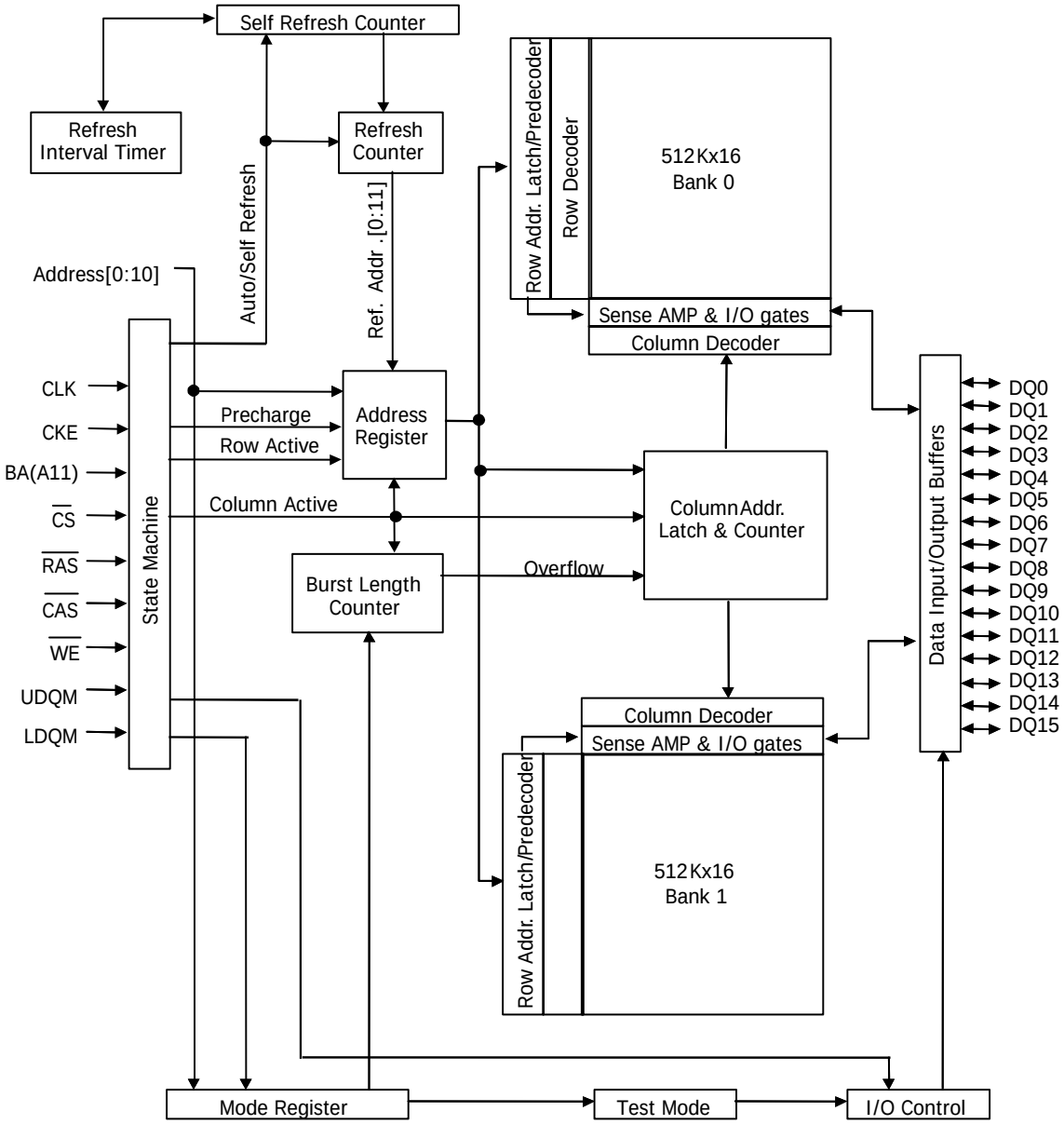


Ball FUNCTION DESCRIPTIONS

SYMBOL	Ball NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/ Ground	Power supply for internal circuits and input buffers
VDDQ/ VSSQ	Data output Power-Power/Ground	Power supply for DQ
NC	No connection	No connection

FUNCTIONAL BLOCK DIAGRAM

512K x 2banks x 16 I/O Low Power Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 4.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	1
Input High Voltage	V_{IH}	2.0	3.3	V_{DDQ}+0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	1, 3

Note : 1. All voltages are referenced to V_{SS} = 0V
2. V_{IH}(max) is acceptable 4.6V AC pulse width with <=3ns of duration.
3. V_{IL}(min) is acceptable -1.5V AC pulse width with <=3ns of duration

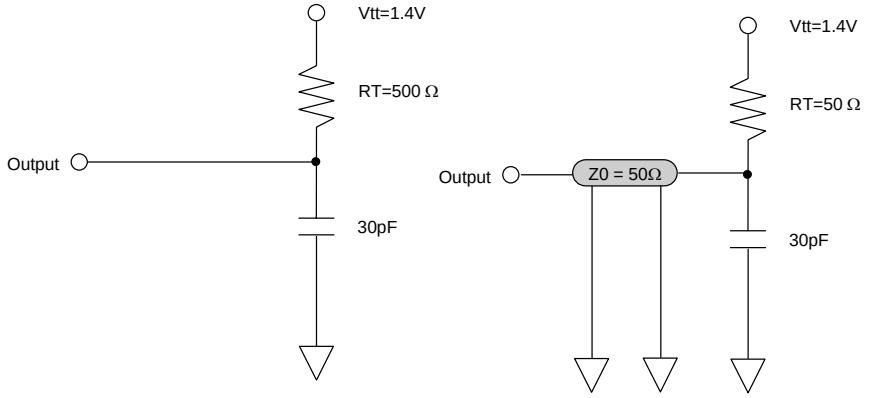
AC OPERATING TEST CONDITION (T_A= 0 to 70 °C, V_{DD}=3.3±0.3V, V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	t_R / t_F	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	30	pF	

CAPACITANCE (TA= 0 to 70 °C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.5	4	pF
	A0 ~ A10, BA, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM	CI2	2.5	5	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	4	6.5	pF

Note 1.



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS I (TA= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Power supply voltage	VDD	3.0	3.6	uA	1, 2
Input Leakage Current	ILI	-1	1	uA	3
Output Leakage Current	ILO	-1	1	uA	4
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note :

1.VDD(min) is 3.15V when HY5V16EF(P)-7 operates at CAS latency=2 and tCK2=8.9ns.

2. VIN = 0 to 3.6V, All other balls are not tested under VIN =0V

3. DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II (TA= 0 to 70°C)

Parameter	Symbol	Test Condition		Speed			Unit	Note
				H	P	S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		110			mA	2
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		2			mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		1			mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		25			mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		15				
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		3.0			mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		3.0				
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		50			mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		30				
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	110	90		mA	3
			CL=2	110				
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active		110			mA	
Self Refresh Current	IDD6	CKE ≤ 0.2V		2.0			mA	

Note : 1.VDD(min) is 3.15V when HY5V16EF(P)-7 operates at CAS latency=2 and tCK2=8.9ns.
2.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
3.Min. of tRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	H		P		S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency=3	tCK3	7.5	1000	10	1000	10	1000	ns	
	CAS Latency=2	tCK2	10		10		12		ns	
Clock High Pulse Width		tCHW	2.5	-	3.0	-	3.0	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	3.0	-	3.0	-	ns	1
Access Time From Clock	CAS Latency=3	tAC3	-	5.5	-	5.5	-	5.5	ns	2
	CAS Latency=2	tAC2	-	5.5	-	5.5	-	8	ns	
Data-out Hold Time		tOH	2.0	-	2.0	-	2.0	-	ns	
Data-Input Setup Time		tDS	1.5	-	2.0	-	2.0	-	ns	1
Data-Input Hold Time		tDH	0.8	-	1.0	-	1.0	-	ns	1
Address Setup Time		tAS	1.5	-	2.0	-	2.0	-	ns	1
Address Hold Time		tAH	0.8	-	1.0	-	1.0	-	ns	1
CKE Setup Time		tCKS	1.5	-	2.0	-	2.0	-	ns	1
CKE Hold Time		tCKH	0.8	-	1.0	-	1.0	-	ns	1
Command Setup Time		tCS	1.5	-	2.0	-	2.0	-	ns	1
Command Hold Time		tCH	0.8	-	1.0	-	1.0	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.5	-	1.0	-	2.0	-	ns	
CLK to Data Output in High-Z Time	CAS Latency=3	tOHZ3	-	5.4	-	6.0	-	6.0	ns	
	CAS Latency=2	tOHZ2	-	5.4	-	6.0	-	6.0	ns	

Note :

1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & t_F > 1ns, then [(t_R+t_F)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If t_R > 1ns, then (t_R/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	H		P		S		Unit	Note
			Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	65	-	70	-	70	-	ns	
$\overline{RAS}$ Cycle Time	Auto Refresh	tRRC	65	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	20	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	45	100K	50	100K	50	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	15	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP							
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output High-Z	$\overline{CAS}$ Latency=3	tPROZ3	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency=2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note : 1. A new command can be given tRC after self refresh exit.

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	L	X	A9 ball High (Other balls OP code)			MRS Mode
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

PACKAGE INFORMATION

60 Ball 10mm x 6.4mm FBGA