Data Sheet March 2001 File Number 3651.6

Digital Quadrature Tuner

The Digital Quadrature Tuner (DQT) provides many of the functions required for digital demodulation. These functions include carrier LO generation and mixing, baseband sampling, programmable bandwidth filtering, baseband AGC, and IF AGC error detection. Serial control inputs are provided which can be used to interface with external symbol and carrier tracking loops. These elements make the DQT ideal for demodulator applications with multiple operational modes or data rates. The DQT may be used with HSP50210 Digital Costas Loop to function as a demodulator for BPSK, QPSK, 8-PSK OQPSK, FSK, FM, and AM signals.

The DQT processes a real or complex input digitized at rates up to 52 MSPS. The channel of interest is shifted to DC by a complex multiplication with the internal LO. The quadrature LO is generated by a numerically controlled oscillator (NCO) with a tuning resolution of 0.012Hz at a 52MHz sample rate. The output of the complex multiplier is gain corrected and fed into identical low pass FIR filters. Each filter is comprised of a decimating low pass filter followed by an optional compensation filter. The decimating low pass filter is a 3 stage Cascaded-Integrator-Comb (CIC) filter. The CIC filter can be configured as an integrate and dump filter or a third order CIC filter with a $(\sin(X)/X)^3$ response. Compensation filters are provided to flatten the $(\sin(X)/X)^N$ response of the CIC. If none of the filtering options are desired, they may be bypassed. The filter bandwidth is set by the decimation rate of the CIC filter. The decimation rate may be fixed or adjusted dynamically by a symbol tracking loop to synchronize the output samples to symbol boundaries. The decimation rate may range from 1-4096. An internal AGC loop is provided to maintain the output magnitude at a desired level. Also, an input level detector can be used to supply error signal for an external IF AGC loop closed around the A/D.

The DQT output is provided in either serial or parallel formats to support interfacing with a variety DSP processors or digital filter components. This device is configurable over a general purpose 8-bit parallel bidirectional microprocessor control bus.

Features

- Input Sample Rates to 52MSPS
- Internal AGC Loop for Output Level Stability
- Parallel or Serial Output Data Formats
- 10-Bit Real or Complex Inputs
- Bidirectional 8-Bit Microprocessor Interface
- Frequency Selectivity <0.013Hz
- Low Pass Filter Configurable as Three Stage Cascaded-Integrator-Comb (CIC), Integrate and Dump, or Bypass
- Fixed Decimation from 1-4096, or Adjusted by NCO Synchronization with Baseband Waveforms
- Input Level Detection for External IF AGC Loop
- Designed to Operate with HSP50210 Digital Costas Loop
- 84 Lead PLCC

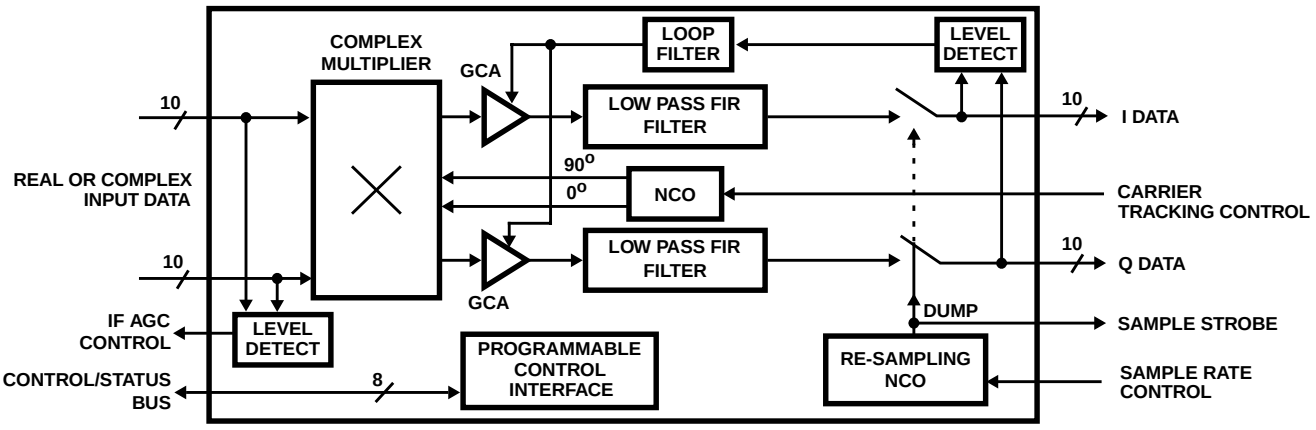
Applications

- Satellite Receivers and Modems
- Complex Upconversion/Modulation
- Tuner for Digital Demodulators
- Digital PLLs
- Related Products: HSP50210 Digital Costas Loop; A/D Products HI5703, HI5746, HI5766
- HSP50110/210EVAL Digital Demod Evaluation Board

Ordering Information

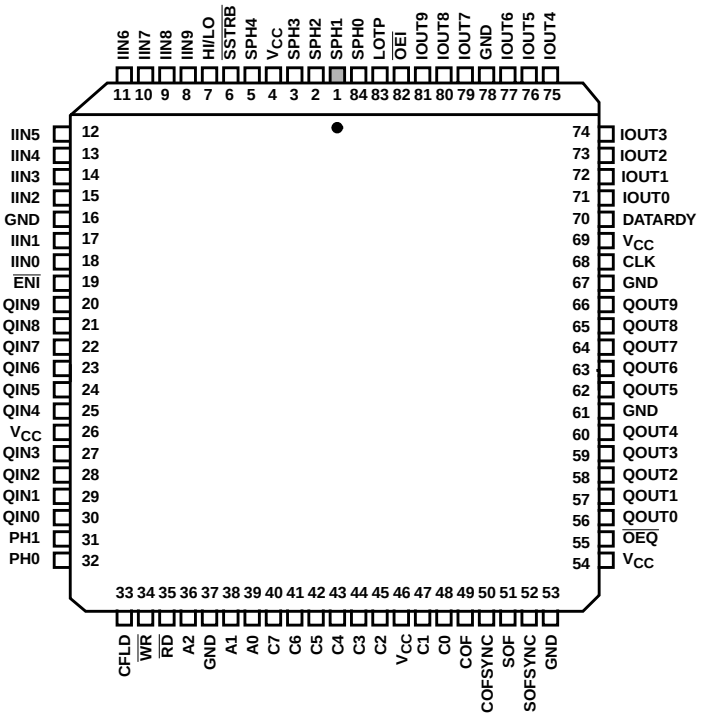
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HSP50110JC-52	0 to 70	84 Ld PLCC	N84.1.15
HSP50110JI-52	-40 to 85	84 Ld PLCC	N84.1.15

Block Diagram



Pinout

HSP50110 (PLCC)
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power Supply.
GND	-	Ground.
IIN9-0	I	In-Phase Input. Data input for in-phase (real) samples. Format may be either two's complement or offset binary format (see I/O Formatting/Control Register in Table 9). IIN9 is the MSB.
QIN9-0	I	Quadrature Input. Data input for quadrature (imaginary) samples. Format may be either two's complement or offset binary format (see I/O Formatting/Control Register in Table 9). QIN9 is the MSB.
$\overline{ENI}$	I	Input Enable. When $\overline{ENI}$ is active 'low', data on IIN9-0 and QIN9-0 is clocked into the processing pipeline by the rising edge of CLK. This input also controls the internal data processing as described in the Input Controller Section of the data sheet. $\overline{ENI}$ is active 'low'.
PH1-0	I	Carrier Phase Offset. The phase of the internally generated carrier frequency may be shifted by 0, 90, 180, or 270 degrees by controlling these pins (see Synthesizer/Mixer Section). The phase mapping for these inputs is given in Table 1.
CFLD	I	Carrier Frequency Load. This input loads the Carrier Frequency Register in the Synthesizer NCO (see Synthesizer/Mixer Section). When this input is sampled 'high' by clock, the contents of the Microprocessor Interface Holding Registers are transferred to the carrier frequency register in the Synthesizer NCO (see Microprocessor Interface Section). ***NOTE: This pin must be 'low' when loading other configuration data via the Microprocessor Interface. Active high Input.***
COF	I	Carrier Offset Frequency Input. This serial input is used to load the Carrier Offset Frequency into the Synthesizer NCO (see Serial Interface Section). The new offset frequency is shifted in MSB first by CLK starting with the clock cycle after the assertion of COFSYNC.
COFSYNC	I	Carrier Offset Frequency Sync. This signal is asserted one CLK cycle before the MSB of the offset frequency data word (see Serial Interface Section).

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
SOF	I	Sampler Offset Frequency. This serial input is used to load the Sampler Offset Frequency into the Re-Sampler NCO (see Serial Interface Section). The new offset frequency is shifted in MSB first by CLK starting with the clock cycle after assertion of SOFSYNC.
SOFSYNC	I	Sampler Offset Frequency Sync. This signal is asserted one CLK cycle before the MSB of Sampler Offset Frequency data word (see Serial Interface Section).
A2-0	I	Address Bus. These inputs specify a target register within the Microprocessor Interface (see Table 5). A2 is the MSB. This input is setup and held to the rising edge of $\overline{WR}$.
C7-0	I/0	Control Bus. This is the bidirectional data bus for reads and writes to the Microprocessor Interface (see Microprocessor Interface Section). C7 is the MSB.
$\overline{WR}$	I	Write. This is the write strobe for the Microprocessor Interface (see Microprocessor Interface Section).
$\overline{RD}$	I	Read. This is the read enable for the Microprocessor Interface (see Microprocessor Interface Section).
IOUT9-0	O	In-Phase Output. The data on these pins is output synchronous to CLK. New data on IOUT9-0 is indicated by the assertion of the DATARDY pin. Data may be output parallel or serial mode (see Output Formatter Section). In the parallel mode, IOUT9 is the MSB. When the serial mode is used, IOUT0 is data, and IOUT9 is the serial clock. Other pins not used in serial mode may be set high or low via the control interface.
QOUT9-0	O	Quadrature Output. The data on these pins is output synchronous to CLK. New data on the QOUT(9-0) pins is indicated by the DATARDY pin. Data may be output parallel or serial mode. In the parallel mode, IOUT9 is the MSB. When the serial mode is used, QOUT0 is data.
DATARDY	O	Data Ready. This output is asserted on the first clock cycle that new data is available on the IOUT and QOUT data busses (see Output Formatter Section). This pin may be active ‘high’ or ‘low’ depending on the configuration of the I/O Formatting/Control Register (see Table 9). In serial mode, DATARDY is asserted one IQ clock before for first bit of serial data.
$\overline{OEI}$	I	In-Phase Output Enable. This pin is the three-state control for IOUT9-0. When $\overline{OEI}$ is ‘high’, the IOUT bus is held in the high impedance state.
$\overline{OEQ}$	I	Quadrature Output Enable. This pin is the three-state control for QOUT9-0. When $\overline{OEQ}$ is ‘high’, the QOUT bus is held in the high impedance state.
LOTP	0	Local Oscillator Test Point. This output is the MSB of the Synthesizer NCO phase accumulator (see Synthesizer/Mixer Section). This is provided as a test point for monitoring the frequency of the Synthesizer NCO.
$\overline{SSTRB}$	0	Sample Strobe. This is the bit rate strobe for the bit rate NCO. $\overline{SSTRB}$ has two modes of operation: continuous update and sampled. In continuous update mode, this is the carry output of the Re-Sampler NCO. In sampled mode, $\overline{SSTRB}$ is active synchronous to the DATARDY signal for parallel output mode. The sampled mode is provided to signal the nearest output sample aligned with or following the symbol boundary. This signal can be used with SPH(4-0) below to control a resampling filter to time shift its impulse response to align with the symbol boundaries.
SPH4-0	0	Sample Phase. These are five of the most significant 8 bits of the Re-Sampler NCO phase accumulator. Which five bits of the eight is selected via the Chip Configuration Register (see Table 11). These pins update continuously when the $\overline{SSTRB}$ output is in the continuous update mode. When the $\overline{SSTRB}$ pin is in the sampled mode, SPH4-0 update only when the $\overline{SSTRB}$ pin is asserted. In the sampled mode, these pins indicate how far the bit phase has advanced past the symbol boundary when the output sample updates. SPH4 is the MSB.
HI/LO	0	HI/LO. The output of the Input Level Detector is provided on this pin (see Input Level Detector Section). The sense of the HI/LO pin is set via the Chip Configuration Register (see Table 11). This signal can be externally averaged and used to control the gain of an amplifier to close an AGC loop around the A/D converter. This type of AGC sets the level based on the median value on the input.
CLK	I	Clock. All I/O’s with the exception of the output enables and the microprocessor interface are synchronous to clock.

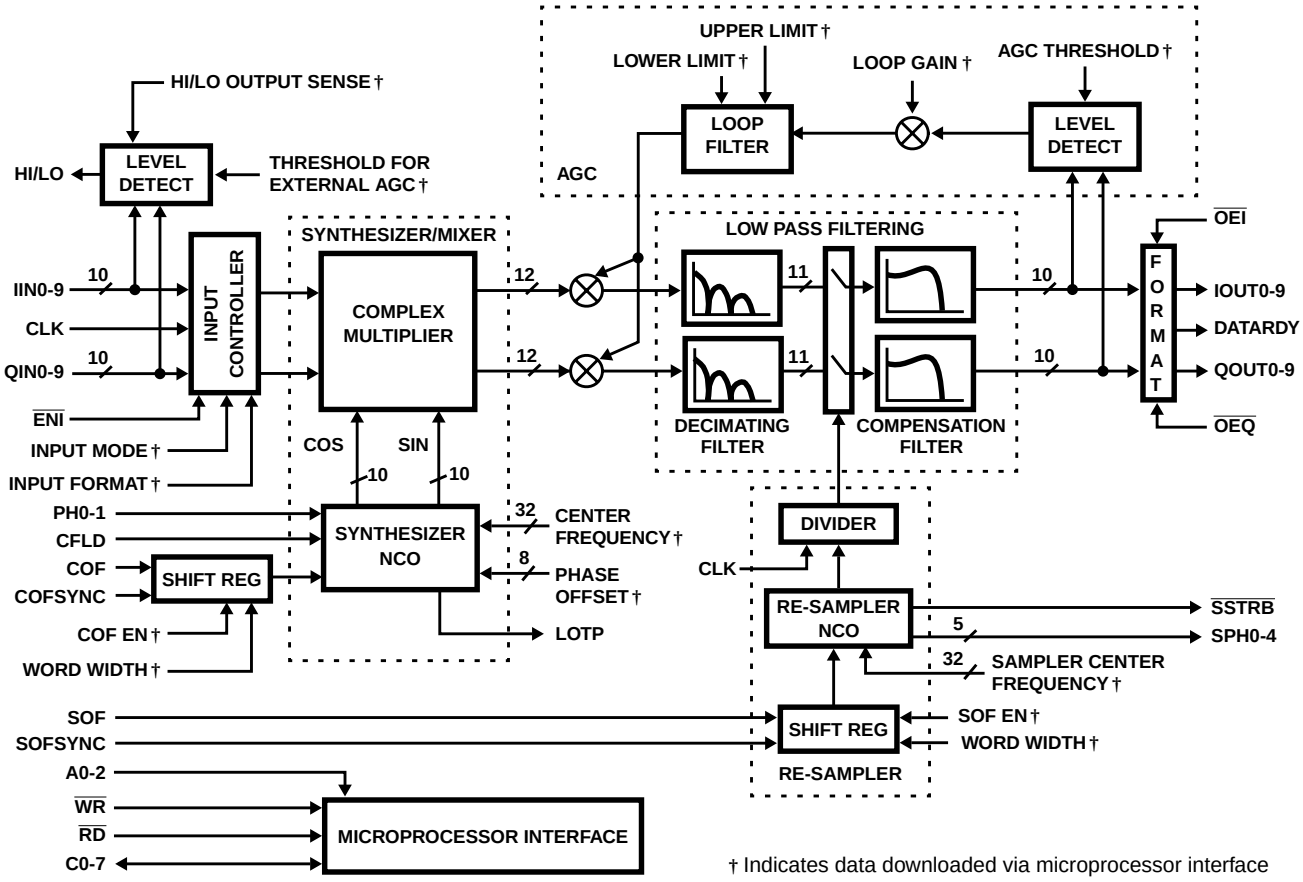


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF HSP50110

Functional Description

The Digital Quadrature Tuner (DQT) provides many of the functions needed for digital demodulation including: carrier LO generation, mixing, low-pass filtering, baseband sampling, baseband AGC, and IF AGC error detection. A block diagram of the DQT is provided in Figure 1. The DQT processes a real or complex input at rates up to 52 MSPS. The digitized IF is input to the Synthesizer/Mixer where it is multiplied by a quadrature LO of user programmable frequency. This operation tunes the channel of interest to DC where it is extracted by the Low Pass FIR Filtering section. The filter bandwidth is set through a user programmable decimation factor. The decimation factor is set by the Re-Sampler which controls the baseband sampling rate. The baseband sample rate can be adjusted by an external symbol tracking loop via a serial interface. Similarly, a serial interface is provided which allows the frequency of the Synthesizer/Mixer's NCO to be controlled by an external carrier tracking loop. The serial interfaces were designed to mate with the output of loop filters on the HSP50210 Digital Costas Loop.

The DQT provides an input level detector and an internal AGC to help maintain the input and output signal magnitudes at user specified levels. The input level detector compares the input signal magnitude to a programmable level and generates an error signal. The error signal can be externally averaged to set the gain of an amplifier in front of the A/D which closes the AGC loop. The output signal level is maintained by an internal AGC loop closed around the Low Pass Filtering. The AGC loop gain and gain limits are programmable.

Input Controller

The input controller sets the input sample rate of the processing elements. The controller has two operational modes which include a Gated Input Mode for processing sample rates slower than CLK, and an Interpolated Input Mode for increasing the effective time resolution of the samples. The mode is selected by setting bit 1 of the I/O Formatting Control Register in Table 9.

In Gated Input Mode, the Input Enable ($\overline{ENI}$) controls the data flow into the input pipeline and the processing of the internal elements. When this input is sampled "low" by CLK, the data on IIN0-9 and QIN0-9 is clocked into the processing pipeline; when $\overline{ENI}$ is sampled "high", the data inputs are disabled. The Input Enable is pipelined to the internal processing elements so that they are enabled once for each time $\overline{ENI}$ is sampled low. This mode minimizes the

processing pipeline latency, and the latency of the part's serial interfaces while conserving power. ***Note: the effective input sample rate to the internal processing elements is equal to the frequency with which $\overline{ENI}$ is asserted "low".***

In Interpolated Input Mode, the $\overline{ENI}$ input is used to insert zeroes between the input data samples. This process increases the input sample rate to the processing elements which improves the time resolution of the processing chain. When $\overline{ENI}$ is sampled "high" by CLK, a zero is input into the processing pipeline. When $\overline{ENI}$ is sampled "low" the input data is fed into the pipeline. ***Note: Due to the nature of the rate change operation, consideration must be given to the scaling and interpolation filtering required for a particular rate change factor.***

In either the Gated or Interpolated Input Mode, the Synthesizer NCO is gated by the $\overline{ENI}$ input. This only allows clocking of the NCO when external samples are input to the processing pipeline. As a result, the NCO frequency must be set relative to the input sample rate, not the CLK rate (see Synthesizer/Mixer Section). ***NOTE: Only fixed interpolation rates should be used when operating the part in Interpolated Mode at the Input Controller.***

Input Level Detector

The Input Level Detector generates a one-bit error signal for an external IF AGC filter and amp. The error signal is generated by comparing the magnitude of the input samples to a user programmable threshold. The HI/LO pin is then driven "high" or "low" depending the relationship of its magnitude to the threshold. The sense of the HI/LO pin is programmable so that a magnitude exceeding the threshold can either be represented as a "high" or "low" logic state. The threshold and the sense of the HI/LO pin are configured by loading the appropriate control registers via the Microprocessor Interface (see Tables 7 and 11).

The high/low outputs can be integrated by an external loop filter to close an AGC loop. Using this method the gain of the loop forces the median magnitude of the input samples to the threshold. When the magnitude of half the samples are above the threshold and half are below, the error signal is integrated to zero by the loop filter.

The algorithm for determining the magnitude of the complex input is given by:

$$Mag(I,Q) = |I| + .375 \times |Q| \quad \text{if } |I| > |Q| \qquad \text{(EQ. 1)}$$

or:

$$Mag(I,Q) = |Q| + .375 \times |I| \quad \text{if } |Q| > |I|, \qquad \text{(EQ. 2)}$$

Using this algorithm, the magnitude of complex inputs can be estimated with an error of <0.55dB or approximately 6.5%. For real inputs, the magnitude detector reduces to a an absolute value detector with negligible error.

Note: an external AGC loop using the Input Level Detector may go unstable for a real sine wave input whose frequency is exactly one quarter of the sample rate ($F_S/4$). The Level Detector responds to such an input by producing a square wave output with a 50% duty cycle for a wide range of thresholds. This square wave integrates to zero, indicating no error for a range of input signal amplitudes.

Synthesizer/Mixer

The Synthesizer/Mixer spectrally shifts the input signal of interest to DC for subsequent baseband filtering. This function is performed by using a complex multiplier to multiply the input with the output of a quadrature numerically controlled oscillator (NCO). The multiplier operation is:

$$I_{OUT} = I_{IN} \times \cos(\omega_C) - Q_{IN} \times \sin(\omega_C) \qquad \text{(EQ. 3)}$$

$$Q_{OUT} = I_{IN} \times \sin(\omega_C) + Q_{IN} \times \cos(\omega_C) \qquad \text{(EQ. 4)}$$

The complex multiplier output is rounded to 12 bits. For real inputs this operation is similar to that performed by a quadrature downconverter. For complex inputs, the Synthesizer/Mixer functions as a single-sideband or image reject mixer which shifts the frequency of the complex samples without generating images.

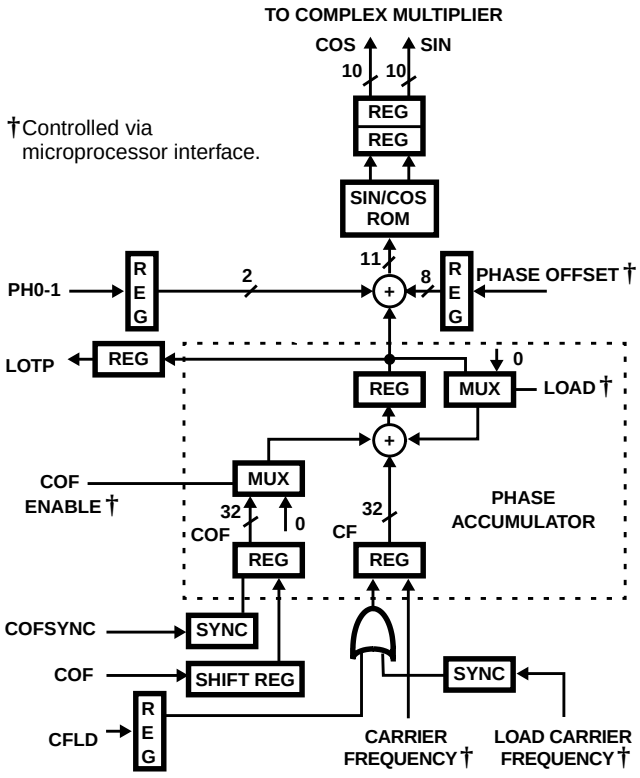


FIGURE 2. SYNTHESIZER NCO

The quadrature outputs of the NCO are generated by driving a sine/cosine lookup table with the output of a phase accumulator as shown in Figure 2. Each time the phase accumulator is clocked, its sum is incremented by the sum of

the contents of the Carrier Frequency (CF) Register and the Carrier Offset Frequency (COF) Register. As the accumulator sum transitions from 0 to 2^{32}, the SIN/COS ROM produces quadrature outputs whose phase advances from 0^o to 360^o. The sum of the CF and COF Registers represent a phase increment which determines the frequency of the quadrature outputs. Large phase increments take fewer clocks to transition through the sine wave cycle which results in a higher frequency NCO output.

The NCO frequency is set by loading the CF and COF Registers. The contents of these registers set the NCO frequency as given by the following,

$$F_C = F_S \times (CF + COF)/2^{32}, \quad \text{(EQ. 5)}$$

where f_S is the sample rate set by the Input Controller, CF is the 32-bit two's complement value loaded into the Carrier Frequency Register, and COF is the 32-bit two's complement value loaded into the Carrier Offset Frequency Register. This can be rewritten to have the programmed CF and COF value on the left:

$$(CF + COF) = INT[(F_C/F_S)2^{32}]_{HEX} \quad \text{(EQ. 5A)}$$

As an example, if the CF Register is loaded with a value of 3000 0000 (Hex), the COF Register is loaded with a value of 1000 0000 (Hex), and the input sample rate is 40 MSPS, an the NCO would produce quadrature terms with a frequency of 10MHz. When the sum of CF and COF is a negative value, the cos/sin vector generated by the NCO rotates clockwise which downconverts the upper sideband; when the sum is positive, the cos/sin vector rotates counterclockwise which upconverts the lower sideband. ***Note: the input sample rate F_S is determined by the rate at which $\overline{ENI}$ is asserted low (see Input Controller Section). If $\overline{ENI}$ is tied low, the input sample rate is equal to the CLK rate.***

The Carrier Frequency Register is loaded via the Microprocessor Interface and the Carrier Offset Frequency is loaded serially using the COF and COFSYNC inputs. The procedure for loading these registers is discussed in the Microprocessor Interface Section and the Serial Input Section.

The phase of the NCO's quadrature outputs can be adjusted by adding an offset value to the output of the phase accumulator as shown in Figure 2. The offset value can be loaded into the Phase Offset (PO) Register or input via the PH0-1 inputs. If the PO Register is used, the phase can be adjusted from $-\pi$ to π with a resolution of ~1.4^o. The phase offset is given by the following equation,

$$\phi = \pi \times (PO/128), \quad \text{(EQ. 6)}$$

where PO is the 8-bit two's complement value loaded into the Phase Offset Register (see Phase Offset Register in Table 12).

As an example, a value of 32, (20_{HEX}), loaded into the Phase Offset Register would produce a phase offset of 45^o.

An alternative method for controlling the NCO Phase uses the PH0-1 inputs to shift the phase of NCO's output by 0^o, 90^o, 180^o, or 270^o. The PH0-1 inputs are mapped to phase shifts as shown in Table 1. The phase may be updated every clock supporting the $\pi/2$ phase shifts required for modulation or despreading of CDMA signals.

The output of the complex multiplier is scaled by 2^{-36}. See "Setting DQT Gains" below.

TABLE 1. PH0-1 INPUT PHASE MAPPING

PH1-0	PHASE SHIFT
00	0^o
01	90^o
10	270^o
11	180^o

AGC

The level of the Mixer output is gain adjusted by an AGC closed around the Low Pass Filtering. The AGC provides the coarse gain correction necessary to help maintain the output of the HSP50110 at a signal level which maintains an acceptable dynamic range. The AGC consists of a Level Detector which generates an error signal, a Loop Gain multiplier which amplifies the error, and a Loop Filter which integrates the error to produce gain correction (see Figure 4).

The Level Detector generates an error signal by comparing the magnitude of the DQT output against a user programmable threshold (see AGC Control Register in Table 8). In the normal mode of operation, the Level Detector outputs a -1 for magnitudes above the threshold and +1 for those below the threshold. The ± 1 outputs are then multiplied by a programmable loop gain to generate the error signal integrated by the Loop Filter. The Level Detector uses the magnitude estimation algorithm described in the Input Level Detector Section. The sense of the Level Detector Output may be changed via the Chip Configuration Register, bit 0 (see Table 11).

The Loop Filter consists of a multiplier, an accumulator and a programmable limiter. The multiplier computes the product of the output of the Level Detector and the Programmable Loop Gain. The accumulator integrates this product to produce the AGC gain, and the limiter keeps the gain between preset limits (see AGC Control Register, Table 8). The output of the AGC Loop Filter Accumulator can be read via the Microprocessor Interface to estimate signal strength (see Microprocessor Interface Section).

The Loop Filter Accumulator uses a pseudo floating point format to provide up to ~48dB of gain correction. The format

of the accumulator output is shown in Figure 3. The AGC gain is given by:

$$Gain_{AGC} = (1.0 + M) \times 2^{E} \quad \text{(EQ. 7)}$$

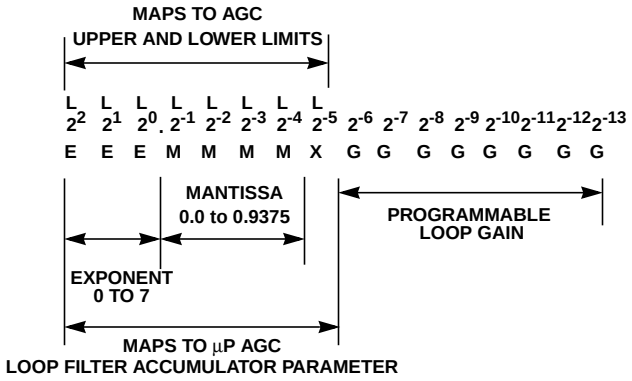
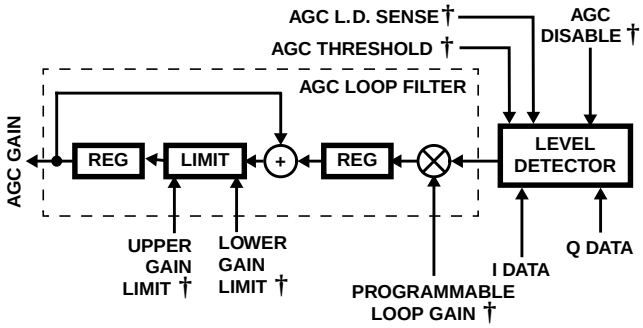


FIGURE 3. BINARY FORMAT FOR LOOP FILTER ACCUMULATOR

where M is the 4-bit mantissa value ranging from 0.0 to 0.9375, and E is the three bit exponent ranging from 0 to 7. The result is a piece wise linear transfer function whose overall response is logarithmic, as shown in Figure 5. The exponent bits provide a coarse gain setting of $2^{(EEE)}$. This corresponds to a gain range from 0dB to 42dB (2^0 to 2^7) with the MSB representing a 24dB gain, the next bit a 12dB gain, and the final bit a 6dB gain. The four mantissa bits map to an additional gain of 1.0 to 1.9375 (0 to ~6dB). Together, the exponent and the mantissa portion of the limit set a gain range from 0 to ~48dB.



† Indicates data downloaded via microprocessor interface.

FIGURE 4. AGC BLOCK DIAGRAM

The limiter restricts the AGC gain range by keeping the accumulator output between the programmed limits. If the accumulator exceeds the upper or lower limit, then the accumulator is held to that limit. The limits are programmed via eight bit words which express the values of the upper and lower limits as eight bit pseudo floating point numbers as shown in Figure 3 (see AGC Control Register, Table 8). The format for the limits is the same as the format of the eight most significant bits of the Loop Filter Accumulator. Examples of how to set the limits for a specific output signal level are provided in the “Setting DQT Gains” Section below. ***NOTE: A fixed AGC gain may be set by programming the upper and lower limits to the same value.***

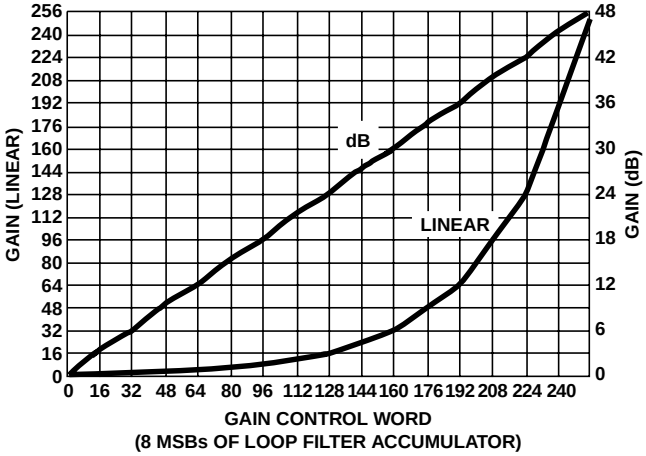


FIGURE 5. GAIN CONTROL TRANSFER FUNCTION

The response time of the AGC is determined by the Programmable Loop Gain. The Loop Gain is an unsigned 8-bit value whose significance relative to the AGC gain is shown in Figure 3. The loop gain is added or subtracted from the accumulator depending on the output of the Level Detector. The accumulator is updated at the output sample rate. If the accumulator exceeds the upper or lower limit, the accumulator is loaded with that limit. The slew rate of the AGC ranges between ~0.001dB and 0.266dB per output sample for Loop Gains between 01(HEX) and FF (HEX) respectively.

The user should exercise care when using maximum loop gain when the (x/sin(x)) or the $(x/sin(x))^3$ compensation filter is enabled. At high decimation rates, the delay through the compensation filter may be large enough to induce oscillations in the AGC loop. The Basic Architectural Configurations Section contains the necessary detailed block diagrams to determine the loop delay for different matched filter configurations.

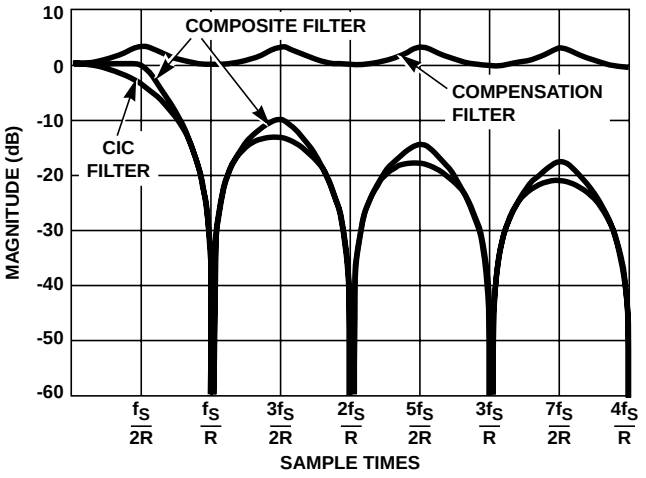
Low Pass Filtering

The gain corrected signal feeds a Low Pass Filtering Section comprised of a Cascaded Integrator Comb (CIC) and compensation filter. The filtering section extracts the channel of interest while providing decimation to match the output sample rate to the channel bandwidth. A variety of filtering configurations are possible which include integrate and dump, integrate and dump with x/sin(x) compensation, third order CIC, and third order CIC with ((x)/sin(x))3 compensation. If none of these filtering options are desired, the entire filtering section may be bypassed.

The Integrate and Dump filter exhibits a frequency response given by

$$H(f) = \frac{1}{R}\sin(\pi fR)/\sin(\pi f) \quad \text{(EQ. 8)}$$

where f is normalized frequency relative to the input sample rate, F_S, and R is the decimation rate [1]. The decimation rate is equivalent to the number of samples in the integration period. As an example, the frequency response for an integrate and dump filter with decimation of 64 is shown in Figure 6. The decimation rate is controlled by the Re-Sampler and may range in value from 2 to 4096 (see Re-Sampler Section).



NOTE: Example plotted is for R = 64 with 64 samples/symbol.

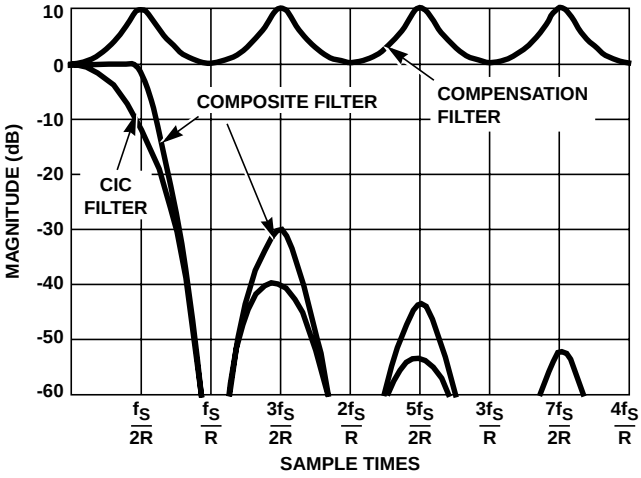
FIGURE 6. INTEGRATE AND DUMP FILTER (FIRST ORDER CIC) FREQUENCY RESPONSE

For applications requiring better out of band attenuation, the Third Order CIC filter may be selected. This filter has a frequency response given by

$$H(f) = [\sin(\pi fR)/\sin(\pi f)]^3\,[1/R]^3 \quad \text{(EQ. 9)}$$

where f is normalized frequency relative to the input sample rate, and R is the decimation rate [1]. As with the integrate and dump filter, the decimation rate is controlled by the Re-Sampler. The decimation rate may range in value from 2-4096 when using CLK, or 3-4096 when using the Re-Sampler NCO as a CLK source to the filter. The frequency response for the third order CIC with a decimation rate of 64 is shown in Figure 7.

Compensation filters may be activated to flatten the frequency responses of the integrate and dump and third order CIC filters. The compensation filters operate at the decimated data rate, and flatten the roll off the decimating filters from DC to approximately one half of the output sample rate. Together, the Integrate and Dump filter and x/sin(x) compensation filter typically yield a lowpass frequency response that is flat to $0.45F_S$ with 0.03dB of ripple, and the third order CIC with $((x)/\sin(x))^3$ compensation typically yields a flat passband to $0.45F_S$ with 0.08dB of ripple. The overall passband ripple degrades slightly for decimation rates of less than 10. Some examples of compensation filter performance for the Integrate and dump and third order CIC filter are shown overlaid on the frequency responses of the uncompensated filters in Figure 6 and Figure 7. The coefficients for the compensation filters are given in Table 2.



NOTE: Example plotted is for R = 64 with 64 samples/symbol.

FIGURE 7. THIRD ORDER CIC FREQUENCY RESPONSE

TABLE 2. COMPENSATION FILTER COEFFICIENTS

COEFFICIENT INDEX	x/sin(x) [2]	$[x/\sin(x)]^3$
0	-1	-1
1	2	4
2	-4	-16
3	10	32
4	-34	-64
5	384	136
6	-34	-352
7	10	1312
8	-4	-352
9	2	136
10	-1	-64
11		32
12		-16
13		4
14		-1

The out of band channels and noise attenuated by the decimating filters are aliased into the output spectrum as a result of the decimating process. A summation of the alias terms at each frequency of the output spectrum produce alias profiles which can be used to determine the usable output bandwidth. A set of profiles representative of what would be observed for decimation factors of ~10 or more are shown in Figures 8 through 11. The Integrate and Dump filter is typically used as a matched filter for square pulses

and less as a high order decimating filter. This is evident by the narrow alias free part of the output bandwidth as shown in Figures 8 and 9. The more rapid roll off of the third order CIC produces an output spectrum containing a much higher usable bandwidth versus output sample rate as shown in Figures 10 and 11. For example, the aliasing noise at $F_S/4$ for the uncompensated third order CIC filter is approximately ~29dB below the full scale input.

Understanding the Alias Profile

For digital filters that utilize decimation techniques to reduce the rate of the digital processing, care must be taken to understand the ramifications, in the frequency domain, of decimation (rate reduction). Of primary concern is the “noise” level increase due to signals that may be aliased inside the band of interest. The potential magnitude of these signals may render significant portions of the previously thought usable bandwidth, unusable for applications that require significant (>60dB) attenuation of undesired signals.

Consider a digital filter with sampling frequency fs, whose frequency response shown in Figure 12A, the top spectrum. At first glance the usable bandwidth would appear to be the 3dB bandwidth of the main lobe. This filter is to be decimated to a rate of 1/8 f_S. We concern ourselves with those elements less than $f_S/2$, as shown in Figure 12B. The decimation process will fold the various lobes of the frequency response around the new sampling folding frequency of $f_S/2R$. The first lobe is folded over the dotted line and a significant portion of the first lobe appears in the passband of the filter. Any unwanted signals in this part of the spectrum will appear in the band of interest with the greatest amplitude. The second lobe is translated down to be centered on the dashed line. The third lobe is spectrally inverted and translated to be centered on the dotted line. The fourth lobe is simply translated to be centered on the dotted line. If there were more lobes to the filter, the process would continue to spectrally invert the odd numbered lobes prior to translation to $f_S/2R$. This process is shown in the “C” portion of Figure 12.

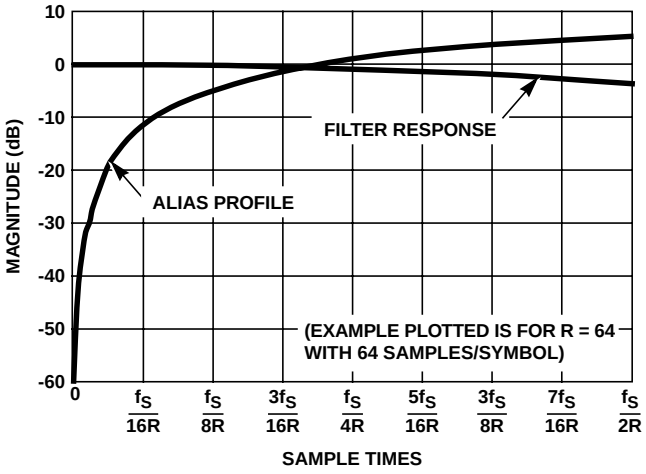


FIGURE 8. ALIAS PROFILE: INTEGRATE/DUMP FILTER, NO COMPENSATION

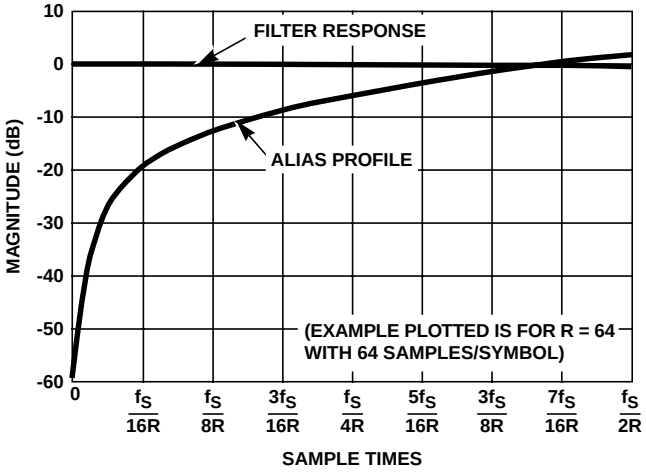


FIGURE 9. ALIAS PROFILE: INTEGRATE/DUMP FILTER WITH COMPENSATION

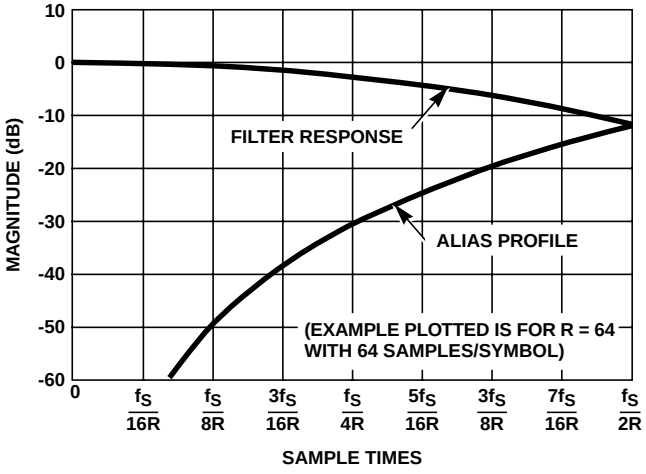


FIGURE 10. ALIAS PROFILE: 3RD ORDER CIC, NO COMPENSATION

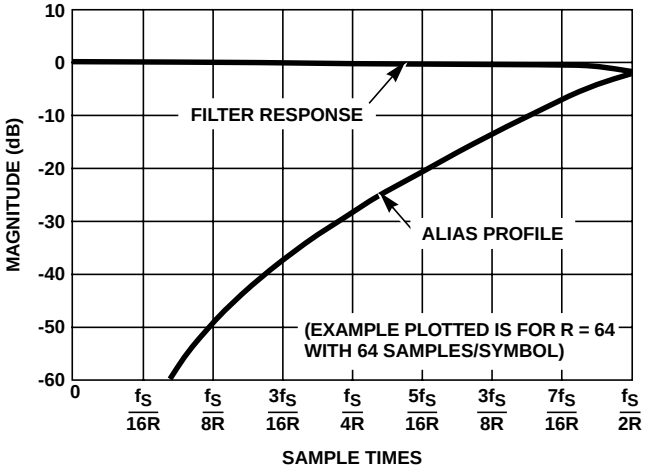


FIGURE 11. ALIAS PROFILE: 3RD ORDER CIC WITH COMPENSATION

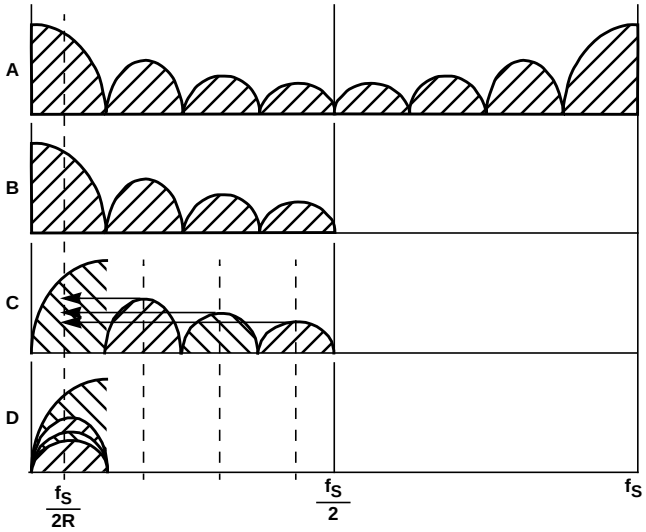


FIGURE 12.

To create the alias profile, a composite response, the components of which are shown in the ”D” portion of Figure 12, is made from the sum of all the alias elements. The primary use of an alias profile is used to determine what bandwidth yields the desired suppression of unwanted signals for a particular application.

Reviewing Figures 9 through 11, note the following observations:

1. The uncompensated I&D (1st order CIC) filter yields about 12dB of alias suppression at $f_S/16R$. This usable bandwidth is considerably narrower than the 3dB filter bandwidth. The I&D filter is the matched filter for square wave data that has not been bandlimited.
2. The compensated I&D filter offers a flatter, wider bandwidth than just the I&D alone. This filter compensates for the frequency roll off due to the A/D converter.
3. The uncompensated 3rd order CIC filter yields over 60dB of alias suppression at $f_S/16R$. Typical application is found in tuners, where the DQT is followed by a very narrow band filter.
4. The 3rd order CIC with compensation yields alias suppression comparable to the 3rd order CIC, but with the flatter, wider passband. This filter is selected for most SATCOM applications.

Which filter is selected, is dependent on the application. It is important to utilize these alias responses in calculating the filter to be used, so that the signal suppression prediction will accurately reflect the digital filter performance.

Noise Equivalent Bandwidth

The noise equivalent bandwidth (B_N) performance of the channel filter is dependent on the combination of Decimation Filter and Compensation Filter chosen. For configurations using the Integrate and Dump filter, B_N is constant regardless of decimation rate. However, for configurations which use the third order CIC filter, B_N converges to a constant for decimation factors of over ~50. A summary of equivalent IF B_N’s for different filter configurations and decimation rates is given in Table 3. These noise bandwidths are provided so that output SNR can be calculated from input SNR. In detection applications this bandwidth indicates the detection bandwidth.

TABLE 3. DOUBLE SIDED NOISE EQUIVALENT BANDWIDTH FOR DIFFERENT FILTER CONFIGURATIONS AND OUTPUT SAMPLE RATES

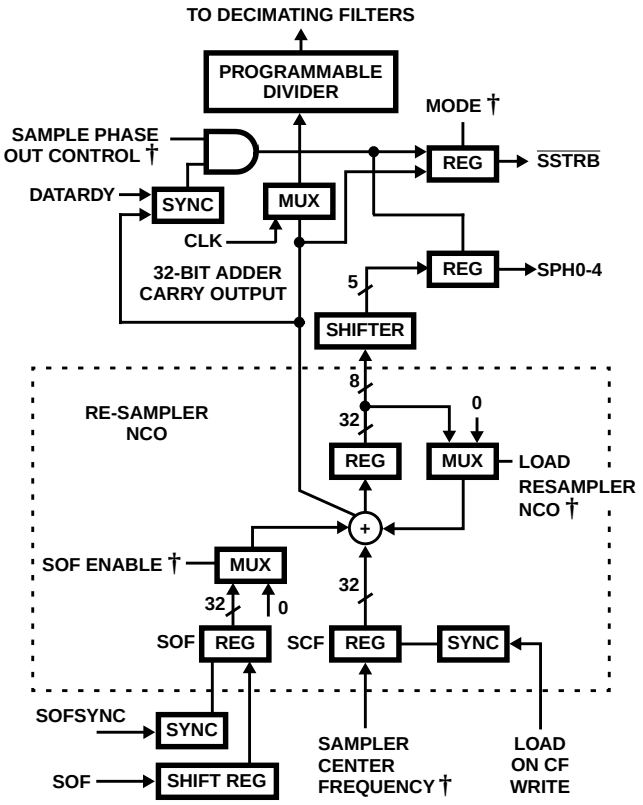
DEC	INTEGRATE/ DUMP	INTEGRATE/ DUMP W/ x/sin(x)	3RD ORDER CIC	3RD ORDER CIC W/ $[x/sin(x)]^3$
2	1.0000	1.3775	0.6250	1.3937
10	1.0000	1.3775	0.5525	1.0785
18	1.0000	1.3775	0.5508	1.0714
26	1.0000	1.3775	0.5504	1.0698
34	1.0000	1.3775	0.5502	1.0691
42	1.0000	1.3775	0.5501	1.0688
50	1.0000	1.3775	0.5501	1.0687
58	1.0000	1.3775	0.5501	1.0686
66	1.0000	1.3775	0.5501	1.0685
74	1.0000	1.3775	0.5500	1.0684
82	1.0000	1.3775	0.5500	1.0684
90	1.0000	1.3775	0.5500	1.0684
98	1.0000	1.3775	0.5500	1.0684
106	1.0000	1.3775	0.5500	1.0684
114	1.0000	1.3775	0.5500	1.0683
122-4096	1.0000	1.3775	0.5500	1.0683

Re-Sampler

The Re-Sampler sets the output sample rate by controlling the sample rate of the decimation filters (see Low Pass Filter Section). The output sample rate may be fixed or adjusted dynamically to synchronize with baseband waveforms. The reduction in sample rate between the Low Pass Filter input and output represents the decimation factor.

The Decimating filter output is sampled by the programmable divider shown in Figure 13. The divider is a counter which is decremented each time it is clocked. When the divider reaches its terminal count, the output of the decimating filter is sampled. The divider may be programmed with a divisor of from 1 to 4096 (see Table 10 Decimating Filter Configuration Register).

One of two internal clock sources are chosen for the divider based on whether a fixed or adjustable sample rate is desired. For fixed output sample rates, a clock equal to the input sample rate is selected (see Decimating Filter Configuration Table 10). For adjustable output sample rates, a clock generated by the carry out from the Re-Sampler NCO is chosen.



† Controlled via microprocessor interface.

FIGURE 13. RE-SAMPLER

The calculation of the decimation factor depends on whether the output sample rate is fixed or adjusted dynamically. For a fixed sample rate, the decimation factor is equal to the divisor loaded into the programmable divider. For example, if the divider is configured with a divisor of 8, the decimation factor is 8 (i.e., the output data rate is $F_S/8$). If the decimation factor is adjusted dynamically, it is a function of both the programmable divisor and the frequency of carry outs from the Re-Sampler NCO (F_{CO}) as given by:

Decimation Factor =
(Programmable Divisor) x F_S/F_{CO} (EQ. 10)

For example, if the programmable divisor is 8 and F_S/F_{CO} = 40, the decimation factor would be 320.

NOTE: The CIC filter architecture only supports decimation factors up to 4096.

The phase accumulator in the Re-Sampler NCO generates the carry outs used to clock the programmable divider. The frequency at which carry outs are generated (F_{CO}) is determined by the values loaded into the Sampler Center Frequency (SCF) and Sampler Offset Frequency (SOF) Registers. The relationship between the values loaded into these registers and the frequency of the carry outs is given by:

$$F_{CO} = F_S \times (SCF + SOF)/2^{32} \quad \text{(EQ. 11)}$$

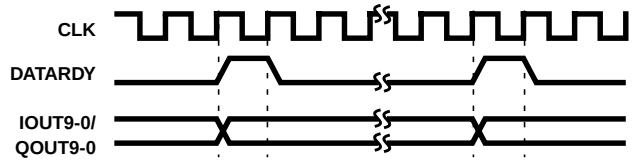
where F_S is the input sample rate of the Low Pass Filter Section, SCF is the 32-bit value loaded into the Sampler Center Frequency Register, and SOF is the 32-bit value loaded into the Sample Offset Frequency Register. The SCF Register is loaded through the Microprocessor Interface (see Microprocessor Interface Section), and the SOF Register is loaded serially via the SOF and SOFSYNC inputs (see Serial Input Section). The sample rate F_S is a function of the Input Controller Mode. If the Controller is in Gated Input Mode, F_S is the frequency with which $\overline{ENI}$ is asserted. In Interpolated Input Mode, F_S is the CLK frequency (see Input Controller Section).

The carry out and 5 of the most significant 8 bits of the NCO's phase accumulator are output to control a resampling filter such as the HSP43168. The resampling filter can be used to provide finer time (symbol phase) resolution than can be achieved by the sampling clock alone. This may be needed to improve transmit/receive timing or better, align a matched filter's impulse response with the symbol boundaries of a baseband waveform at high symbol rates. The carry out of the NCO's phase accumulator is output on $\overline{SSTRB}$, and a window of 5 of the 8 most significant 8 bits of the Phase Accumulator are output on SPH0-4.

Output Formatter

The Output Formatter supports either Word Parallel or Bit Serial output modes. The output can be chosen to have a two's complement or offset binary format. The configuration is selected by loading the I/O Formatting/Control Register (see Table 9).

In parallel output mode, the in-phase and quadrature samples are output simultaneously at rates up to the maximum CLK. The DATARDY output is asserted on the first CLK cycle that new data is available on IOUT0-9 and QOUT0-9 as shown in Figure 14. Output enables ($\overline{OEI}$, $\overline{OEQ}$) are provided to individually three-state IOUT0-9 and QOUT0-9 for output multiplexing.

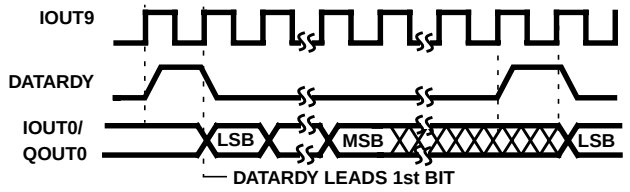


NOTE: DATARDY may be programmed active high or low.

FIGURE 14. PARALLEL OUTPUT TIMING

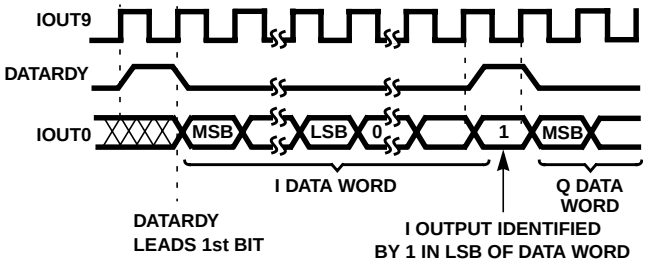
When bit serial output is chosen, two serial output modes are provided, Simultaneous I/Q Mode and I Followed by Q Mode. In Simultaneous I/Q Mode, the 10-bit I and Q samples are output simultaneously on IOUT0 and QOUT0 as shown in Figure 15. In I Followed by Q Mode, both samples are output on IOUT0 with I samples followed by Q samples as shown in Figure 16. In this mode, the I and Q samples are packed into separate 16-bit serial words (10 data bits + 6 zero bits). The 10 data bits are the 10 MSBs of the serial word, and the I sample is differentiated from the Q sample by a 1 in the LSB position of the 16-bit data word. A continuous serial output clock is provided on IOUT9 which is derived by dividing the

CLK by a programmable factor of 2, 4, or 8. When the programmable clock factor is 1, IOUT9 is pulled high, and the CLK signal should be used as the clock. The beginning of a serial data word is signaled by the assertion of DATARDY one serial clock before the first bit of the output word. In I followed by Q Mode, DATARDY is asserted prior to each 16-bit data word. For added flexibility, the Formatter may be configured to output the data words in either MSB or LSB first format.



NOTE: Assumes data is being output LSB first.

FIGURE 15. SERIAL TIMING (SIMULTANEOUS I/Q MODE)



NOTE: Assumes data is being output MSB first.
DATARDY may be programmed active high or low.

FIGURE 16. SERIAL TIMING (I FOLLOWED BY Q MODE)

Gain Distribution

The gain distribution in the DQT is shown in Figure 17. These gains consist of a combination of fixed, programmable, and adaptive gains. The fixed gains are introduced by processing elements like the Synthesizer/Mixer and CIC Filter. The programmable and adaptive gains are set to compensate for the fixed gains as well as variations in input signal strength.

The bit range of the data path between processing elements is shown in Figure 17. The quadrature inputs to the data path are 10-bit fractional two's complement numbers. They are multiplied by a 10-bit quadrature sinusoid and rounded to 12-bits in the Synthesizer/Mixer. The I and Q legs are then scaled by a fixed gain of 2^{-36} to compensate for the worst case gain of the CIC filter. Next, a gain block with an adaptive and programmable component is used to set the output signal level within the desired range of the 10-bit output (see Setting DQT Gains Section). The adaptive component is produced by the AGC and has a gain range from 1.0 to $1.9375*2^7$. The programmable component sets the gain range of the CIC shifter which may range from 2^0 to 2^{63}. Care must be taken when setting the AGC gain limits and the CIC Shifter gain since the sum of these gains could shift the CIC Scaler output beyond the bit range (-2^8 to 2^{-46}) of the CIC Filter input. The CIC Filter introduces a gain factor given by R^N where R is the decimation rate of the filter and N is the CIC order. The CIC order is either 1 (integrate and dump filter) or 3. Depending on configuration, the CIC Filter introduces a gain factor from 2^0 to 2^{36}. The output of the CIC Filter is then rounded and limited to an 11-bit window between bit positions 2^1 to 2^{-9}. Values outside this range saturate to these 11 bits. The Compensation Filter introduces a final gain factor of 1.0, 0.65,

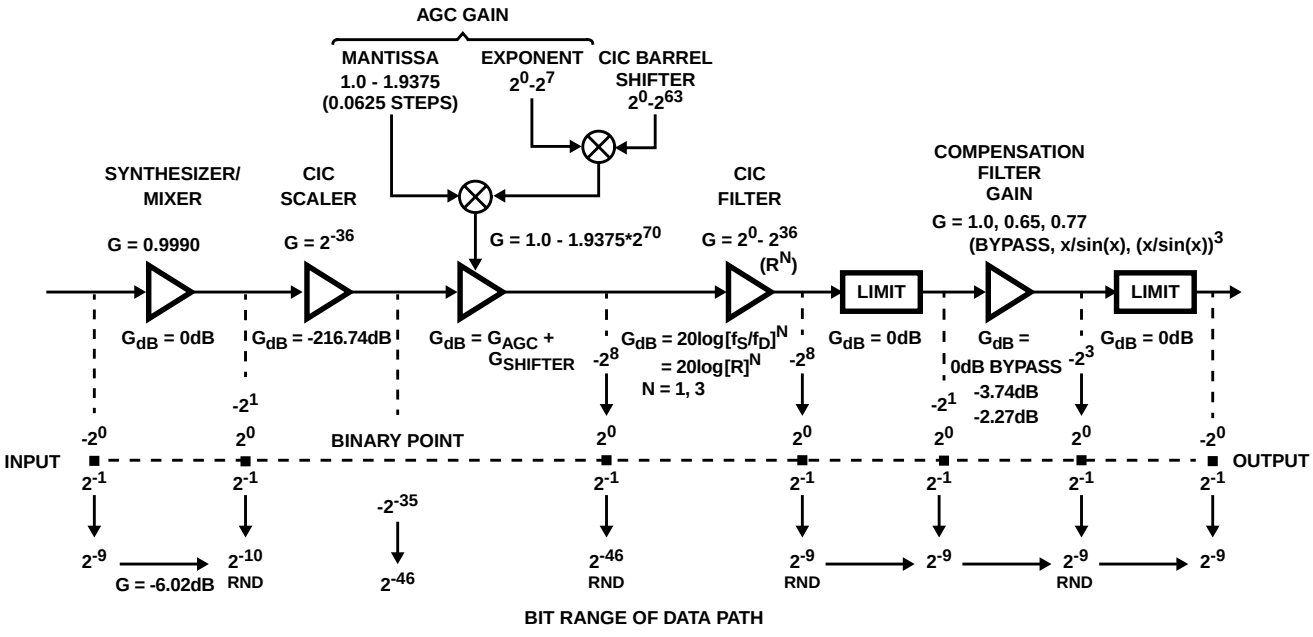


FIGURE 17. GAIN DISTRIBUTION AND INTERMEDIATE BIT WEIGHTINGS

or 0.77 depending on whether the bypass, x/sin(x) or $(x/\sin(x))^3$ configuration is chosen. The Compensation Filter output is then rounded and limited to a 10-bit output range corresponding to bit positions 2^0 to 2^{-9}.

Setting DQT Gains

The AGC and CIC Shifter gains are programmed to maintain the output signal at a desired level. The gain range required depends on the signal levels expected at the input and the A/D backoff required to prevent signal + noise from saturating the A/D. The signal level at the input is based on the input SNR which itself is derived from the either output SNR or output E_S/N_0. Below are two examples which describe setting the gains using either an output SNR or E_S/N_0 specification.

In applications based on the transmission of digital data, it is useful to specify the DQT's output in terms of E_S/N_0. The following example uses this parameter and the others given in Table 4 to show how the DQT's gain settings can be derived.

TABLE 4. EXAMPLE SYSTEM PARAMETERS

PARAMETER	MAIN MENU ITEM	SETTING
Input Sample Rate	(2)	40 MSPS
Output Sample Rate (F_{SOUT}) (Notes 1, 2)	(8), (9)	32 KSPS
Input Filter Noise Bandwidth (NBW)	(10)	10MHz
Minimum Output E_S/N_0	(15)	-3dB
Signal + Noise Backoff at A/D Input	(18), (19)	12dB
Output Signal Magnitude (0 to 1)	(21)	0.5
Number of CIC stages	(11)	3
Compensation Filter	(11)	$(x/\sin(x))^3$
Noise Eq. Bandwidth of Comp. Filter (B_N*F_{SOUT})	N/A	34.18kHz
Input Type (Real/Complex)	(4)	Real

NOTES:
1. Two samples per symbol assumed.
2. Decimation = 40 MSPS/32 KSPS = 1250.

First, the maximum and minimum input signal levels must be determined. The maximum input signal level is achieved in a noise free environment where the input signal is attenuated by 12dB as a result of the A/D backoff. The minimum input signal is determined by converting the minimum output E_S/N_0 specification into an Input SNR. Using the example parameters in Table 4 the minimum input SNR is given by:

$$SNR_{IN} = 10\log_{10}(E_S/N_0) + 10\log_{10}(\text{Symbol Rate}) - 10\log_{10}(\text{NBW})$$
$$= -3\text{dB} + 10\log_{10}(0.5\text{x}32 \times 10^3) - 10\log_{10}(10 \times 10^6)$$
$$= -30.96\text{dB} \quad \text{(EQ. 12)}$$

NOTE: $10\log_{10}(x)$ is used because these items are power related.

Thus, the minimum input signal will then be -42.96dB below full scale (-30.96dB -12dB for A/D backoff). Note: in this example the symbol rate is assumed to be one half of the output sample rate (i.e., there are 2 samples per symbol).

The output signal is related to the input signal by:

$$S_{OUT} = S_{IN} \times G_{MIXER} \times G_{SCALER} \times G_{AGC} \times \quad \text{(EQ. 13)}$$
$$G_{SHIFTER} \times G_{CIC} \times G_{COMP} \quad \text{(EQ. 14)}$$

Using this equation, limits for G_{AGC} and $G_{SHIFTER}$ can be determined from the minimum and maximum input signal conditions as given below (all gains specified in dB):

Min Input Level (Maximum Gain Required):

$$-6.02\text{dB} \geq -42.96 - 6.02 - 216.74 + G_{AGC} + G_{SHIFTER} + 20 \times \log((40 \times 10^6/32 \times 10^3)^3) - 2.27 \quad \text{(EQ. 15)}$$

Max Input Level (Minimum Input Gain Required)

$$-6.02\text{dB} \leq -12 - 6.02 - 216.74 + G_{AGC} + G_{SHIFTER} + 20 \times \log((40 \times 10^6/32 \times 10^3)^3) - 2.27 \quad \text{(EQ. 16)}$$

NOTE: $20\log_{10}(x)$ is used because these items are amplitude related.

Solving the above inequalities for G_{AGC} and $G_{SHIFTER}$, the gain range can be expressed as,

$$45.20\text{dB} < (G_{AGC} + G_{SHIFTER}) < 76.16\text{dB}. \quad \text{(EQ. 17)}$$

The shifter gain provides a programmable gain which is a factor of 2. Since $G_{AGC} \geq 1.0$, $G_{SHIFTER}$ is set as close to the minimum gain requirement as possible:

$$G_{SHIFTER} = 2^N, \quad \text{(EQ. 18)}$$

where

$$N = \text{floor}(\log_2(10^{(G_{MIN}/20)}))$$
$$= \text{floor}(\log_2(10^{(45.20/20)})) = 7$$

The limits on the AGC gain can then be determined by substituting the shifter gain into Equation 18 above. The resulting limits are given by:

$$3.05\text{dB} < G_{AGC} < 34.02\text{dB}. \quad \text{(EQ. 19)}$$

In some applications it is more desirable to specify the DQT output in terms of SNR. This example, covers derivation of the gain settings based on an output SNR of 15dB. The other system parameters are given in Table 4.

As in the previous examples the minimum and maximum input signal levels must be determined. The minimum input signal strength is determined by from the minimum output SNR as given by:

$$SNR_{IN} = SNR_{OUT} - 10\log(\text{NBW}) + 10\log(B_N \times F_{SOUT})$$
$$= 15 - 10\log(10 \times 10^6) + 10\log(34.18 \times 10^3)$$
$$= -9.66\text{dB} \quad \text{(EQ. 20)}$$

Thus, the minimum input signal will be -21.66dB below full scale (-9.66 -12 for A/D Backoff). As before the maximum input signal in the absence of noise is -12dB down due to A/D backoff.

From Equation 14, the gain relationships for maximum and minimum input can be written as follows:

Min Input Level

$$-6.02dB \geq -21.66 -6.02 - 216.74 + G_{AGC} + G_{SHIFTER} + 20*\log((40 \times 10^6/32 \times 10^3)^3)-2.27 \quad \text{(EQ. 21)}$$

Max Input Level

$$-6.02dB \leq -12 - 6.02 - 216.74 + G_{AGC} + G_{SHIFTER} + 20 \times \log((40 \times 10^6/32 \times 10^3)^3) -2.27 \quad \text{(EQ. 22)}$$

Using the upper and lower limits found above, the gain range can be expressed as,

$$45.20dB < G_{AGC} + G_{SHIFTER} < 54.86dB. \quad \text{(EQ. 23)}$$

Using Equation 2 in the previous example, the shifter gain is determined to be 2^7, resulting in an AGC gain range of 3.05dB $< G_{AGC} <$12.72dB. (EQ. 24)

Basic Architectural Configurations

Detailed architectural diagrams are presented in Figures 18 through 20 for the basic configurations, Integrate/Dump filtering with optional compensation, 3rd Order CIC filtering with optional compensation, and Decimating Filter bypass. Only one of the data paths is shown since the processing on either the inphase or quadrature legs is identical. These diagrams are useful for determining the throughput pipeline delay or the loop delay of the AGC as all the internal registers are shown.

All registers with the exception of those denoted by daggers (†) are enabled every CLK rate to minimize pipeline latency. The registers marked by daggers are enabled at the output sample rate as required by the filtering operation performed. The Loop Filter accumulator in the AGC is enabled once per output sample, and represents a delay of one output sample. The accumulators in the CIC filter each represent a delay of one CLK, but they are enabled for processing once per input sample. In Interpolated Input Mode the accumulators are enabled every CLK since the sample rate is determined by the CLK rate (see Input Controller Section). In Gated Input Mode, the processing delay of the accumulators is one CLK but they are only enabled once for each sample gated into the processing pipeline. As a result, the latency through the accumulators is 3 CLKs rather than 3 input sample periods when configured as a 3rd order CIC filter.

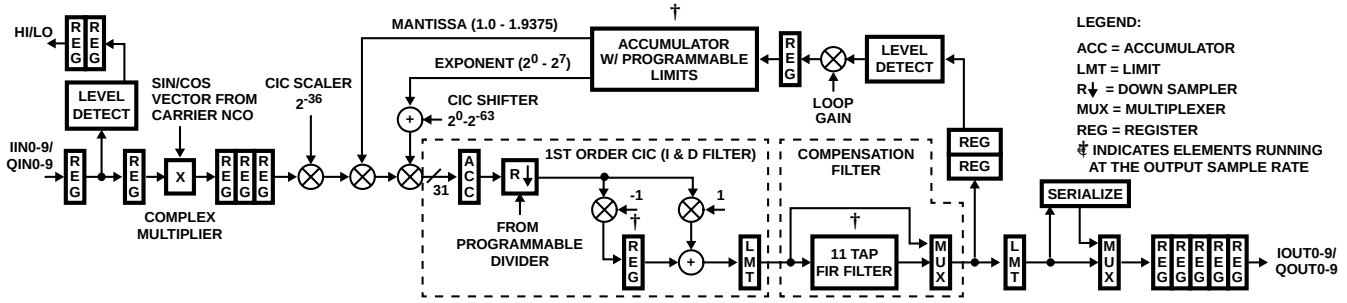


FIGURE 18. DATA FLOW FOR INTEGRATE/DUMP CONFIGURATION

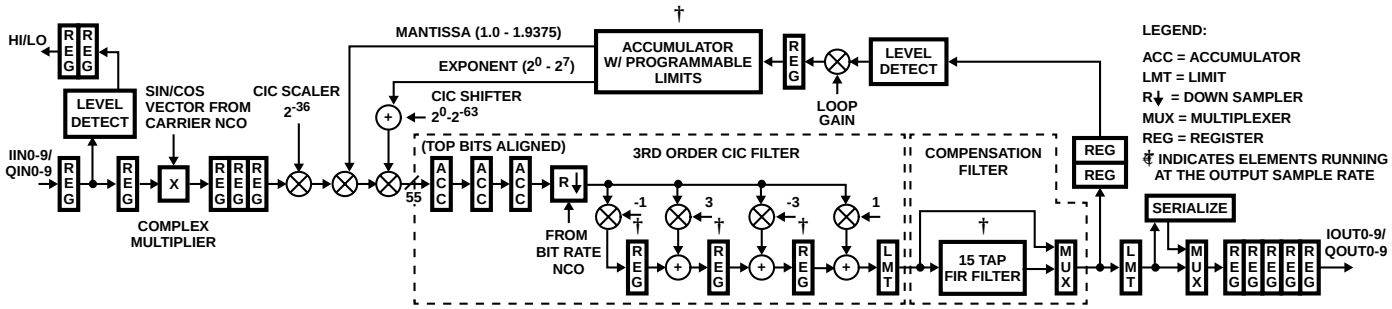


FIGURE 19. DATA FLOW FOR 3RD ORDER CIC CONFIGURATION

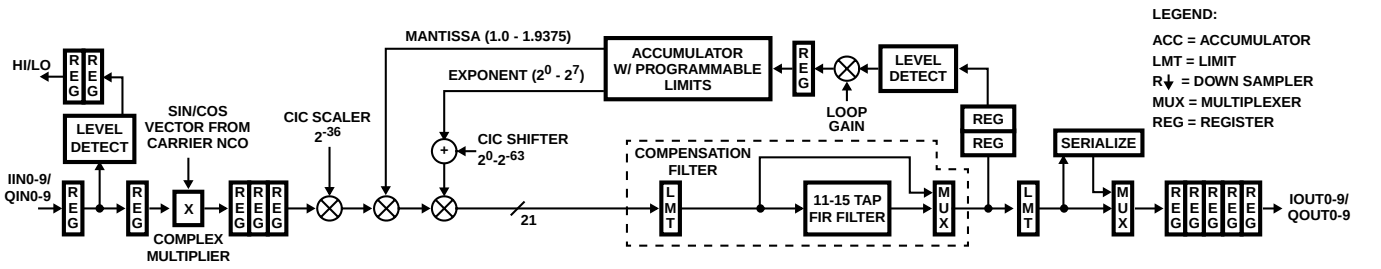
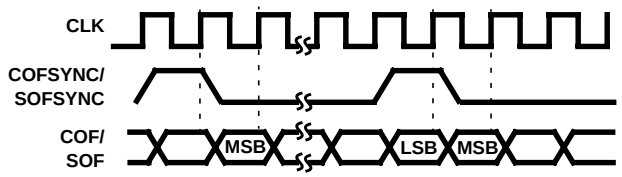


FIGURE 20. DATA FLOW WITH CIC STAGE BYPASSED

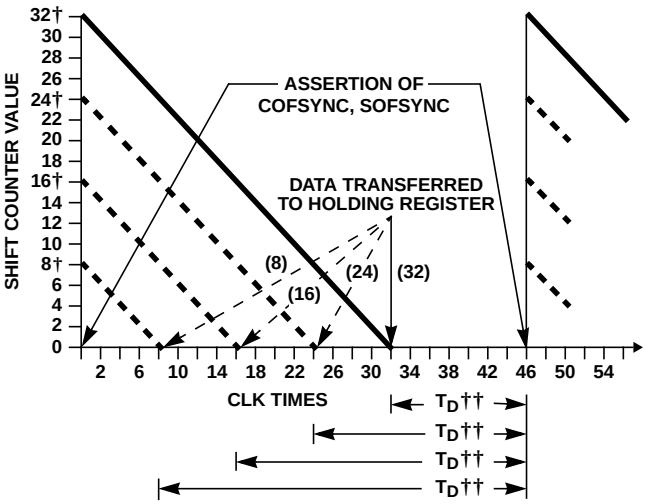
Serial Input Interfaces

Frequency control data for the NCOs contained in the Synthesizer/Mixer and the Re-Sampler are loaded through two separate serial interfaces. The Carrier Offset Frequency Register controlling the Synthesizer NCO is loaded via the COF and COFSYNC pins. The Sample Offset Frequency Register controlling the Re-Sampler NCO is loaded via the SOF and SOFSYNC pins.



OTE: Data must be loaded MSB first.

IGURE 21. SERIAL INPUT TIMING FOR COF AND SOF INPUTS



Serial word width can be: 8, 16, 24, 32 bits wide.

† T_D is determined by the COFSYNC, COFSYNC rate. Note that T_D can be 0, and the fastest rate is with 8-bit word width.

FIGURE 22. SERIAL DATA LOAD TO HOLDING REGISTERS SEQUENCE

The procedure for loading data through these two pin interfaces is identical. Each serial word has a programmable word width of either 8, 16, 24, or 32 bits (see Chip Configuration Register in Table 11). On the rising edge CLK, data on COF or SOF is clocked into an Input Shift Register. The beginning of a serial word is designated by asserting either COFSYNC or SOFSYNC “high” one CLK prior to the first data bit as shown in Figure 21. The assertion of the SOFSYNC starts a count down from the programmed word width. On following CLKs, data is shifted into the register until the specified number of bits have been input. At this point data shifting is disabled and the contents of the register are transferred from the Shift Register to the respective 32-bit Holding Register. The Shift Register is enabled to accept new data on the following CLK. If the serial input word is defined to be less than 32 bits, it will be transferred to the MSBs of the 32-bit holding register and the LSBs of the holding register will be zeroed. See Figure 22 for details. ***Note: serial data must be loaded MSB first, and COFSYNC or SOFSYNC should not be asserted for more than one CLK cycle.***

Test Mode

The Test Mode is used to program each of the output pins to “high” or “low” state via the Microprocessor Interface. If this mode is enabled, the output pins are individually set or cleared through the control bits of the Test Register in Table 13. When serial output mode is selected, the Test Register may be used to set the state of the unused output bits.

Microprocessor Interface

The Microprocessor Interface is used for writing data to the DQT’s Control Registers and reading the contents of the AGC Loop accumulator (see AGC Section). The Microprocessor Interface consists of a set of four 8-bit holding registers and one 8-bit Address Register. These registers are accessed via a 3-bit address bus (A0-2) and an 8-bit data bus (C0-7). The address map for these registers is given in Table 5. The registers are loaded by setting up the address (A0-2) and data (C0-7) to the rising edge of $\overline{WR}$.

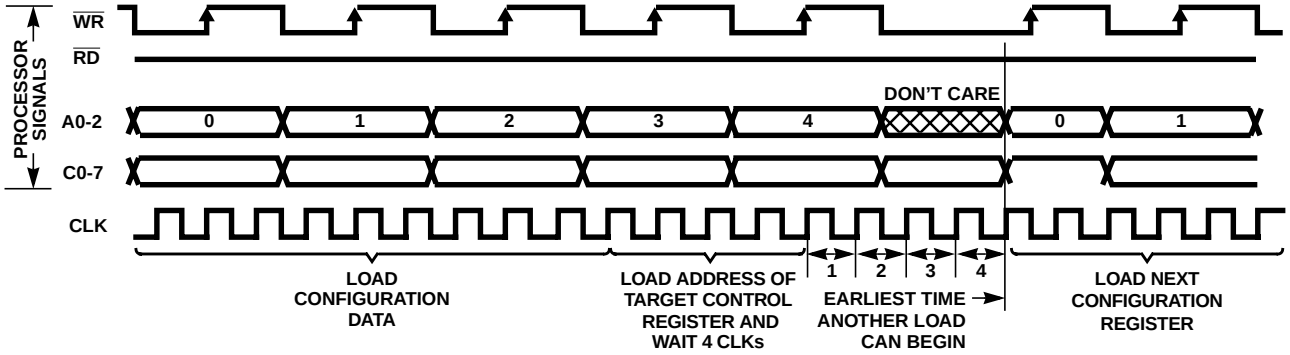
TABLE 5. ADDRESS MAP FOR MICROPROCESSOR INTERFACE

A2-0	REGISTER DESCRIPTION
0	Holding Register 0. Transfers to bits 7-0 of the 32-bit Destination Register. Bit 0 is the LSB of the 32-bit register.
1	Holding Register 1. Transfers to bits 15-8 of a 32-bit Destination Register.
2	Holding Register 2. Transfers to bits 23-16 of a 32-bit Destination Register.
3	Holding Register 3. Transfers to bits 31-24 of a 32-bit Destination Register. Bit 31 is the MSB of the 32-bit register.
4	This is the Destination Address Register. On the fourth CLK following a write to this register, the contents of the Holding Registers are transferred to the Destination Register. The lower 4 bits written to this register are decoded into the Destination Register address. The destination address map is given in Tables 6-15.

The HSP50110 is configured by loading a series of nine 32-bit Control Registers via the Microprocessor Interface. A Control Register is loaded by first writing the four 8-bit Holding Registers and then writing the destination address to the Address Register as shown in Figure 23. The Control Register Address Map and bit definitions are given in Tables 6-15. Data is transferred from the Holding Registers to a Control Register on the fourth clock following a write to the Address Register. As a result, the Holding Registers should not be updated any sooner than 4 CLK’s after an Address Register write (see Figure 23). ***NOTE: the unused bits in a Control Register need not be loaded into the Holding Register.***

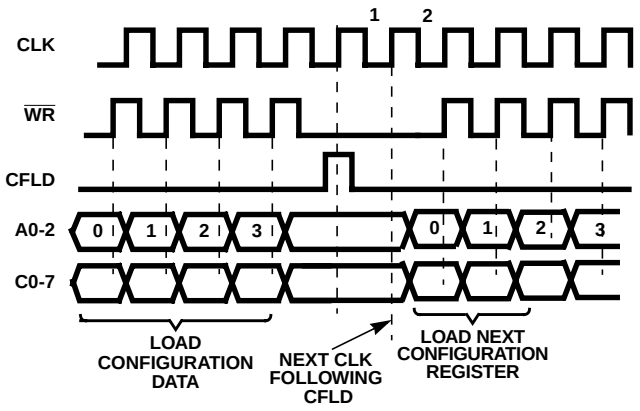
For added flexibility, the CFLD input provides an alternative mechanism for transferring data from the Microprocessor Interfaces's Holding Registers to the Center Frequency Register. When CFLD is sampled "high" by the rising edge of clock, the contents of the Holding Registers are transferred to the Center Frequency Register as shown in Figure 23. Using this loading mechanism, an update of the Center Frequency Register can be synchronized with an external event. Caution should be taken when using the CFLD since the Holding Register contents will be transferred to the Center Frequency Register whenever CFLD is asserted. ***NOTE: CFLD should not be asserted any sooner than 2 CLK's following the last Holding Register load.*** As Shown in Figure 24, the next Configuration Register can be loaded one CLK after CFLD has been loaded on the rising edge of CLK.

The Microprocessor Interface can be used to read the upper 8 bits of the AGC Loop Filter Accumulator. The procedure for reading the Loop Accumulator consists of first sampling the loop accumulator by writing 9 to the Destination Address Register and then reading the loop accumulator value on C0-7 by asserting RD. The sampled value is enabled for output on C0-7 by forcing RD "low" no sooner than 6 CLK's after the writing the Destination Register as shown in Figure 25. The 8-bit output corresponds to the 3 exponent bits and 5 fractional bits to the right of the binary point (see Figure 3). The 3 exponent bits map to C7-5 with C7 being the most significant. The fractional bits map to C4-0 in decreasing significance from C4 to C0.



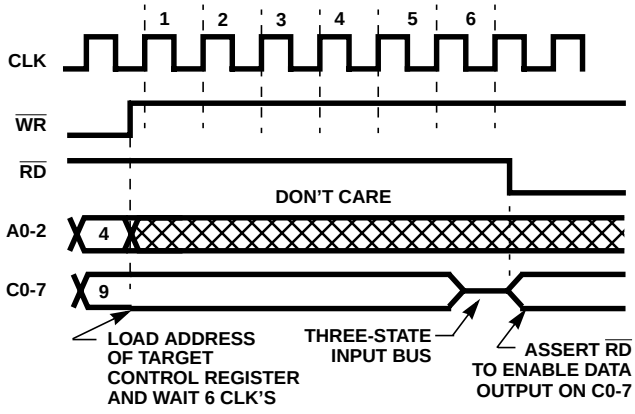
NOTE: These processor signals are representative. The actual shape of the waveforms will be set by the microprocessor used. Verify that the microprocessor waveforms meet the parameters in the Waveforms Section of this data sheet to ensure proper operation. While the microprocessor waveforms are not required to be synchronous to CLK, they are shown as synchronous waveforms for clarity in the illustration.

FIGURE 23. CONTROL REGISTER LOADING SEQUENCE



NOTE: These processor signals are meant to be representative. The actual shape of the waveforms will be set by the microprocessor used. Verify that the processor waveforms meet the parameters in the Waveforms Section of this data sheet to ensure proper operation. The Processor waveforms are not required to be synchronous to CLK. They are shown that way to clarify the illustration.

FIGURE 24. CENTER FREQUENCY CONTROL REGISTER LOADING SEQUENCE USING CF LOAD



NOTE: These processor signals are meant to be representative. The actual shape of the waveforms will be set by the microprocessor used. Verify that the processor waveforms meet the parameters in the Waveforms Section of this data sheet to ensure proper operation. The Processor waveforms are not required to be synchronous to CLK. They are shown that way to clarify the illustration.

FIGURE 25. AGC READ SEQUENCE

TABLE 6. CENTER FREQUENCY REGISTER

DESTINATION ADDRESS = 0		
BIT POSITIONS	**FUNCTION**	**DESCRIPTION**
31-0	Center Frequency	This register controls the center frequency of the Synthesizer/Mixer NCO. This 32-bit two's complement value sets the center frequency as described in the Synthesizer/Mixer Section. Center Center Frequency $= CF_H = \left[\frac{F_C}{F_S} 2^{32}\right]_H - \dot{COF}_H$ Format: [XXXXXXXX]H Range: (0000000 - FFFFFFF)H.

TABLE 7. SAMPLER CENTER FREQUENCY REGISTER

DESTINATION ADDRESS = 1		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
31-0	Sampler Center Frequency	This register controls the center frequency of the Re-Sampler NCO. This 32-bit value together with the setting of a programmable divider set the decimation factor of the CIC Filter (see Re-Sampler and Low Pass Filter Sections). SamplerCenter Frequency $= SCF_H = \left[\frac{F_{NCO}}{F_S} 2^{32}\right]_H - SCOF_{H.}$ Format: [XXXXXXXX]H Range: (0000000 - FFFFFFF)H.

TABLE 7. INPUT THRESHOLD REGISTER

DESTINATION ADDRESS = 2		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
7-0	Input Level Detector Threshold	This register sets the magnitude threshold for the Input Level Detector (see Input Level Detector Section). This 8-bit value is a fractional unsigned number whose format is given by: $2^0. 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6} 2^{-7}$. The possible threshold values range from 0 to 1.9961 $(00 - FF)_H$. The magnitude range for complex inputs is 0.0 - 1.4142 while that for real inputs is 0.0 - 1.0. Threshold values of greater than 1.4142 will never be exceeded.
31-8		Reserved.

TABLE 8. AGC CONTROL REGISTER

DESTINATION ADDRESS = 3		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
7-0	AGC Level Detector Threshold	Magnitude threshold for the AGC Level Detector (see AGC Section). The magnitude threshold is represented as an 8-bit fractional unsigned value with the following format: $2^0. 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6} 2^{-7}$. The possible threshold values range from 0 to 1.9961. However, the usable range of threshold values span from 0 to 1.4142, since full scale outputs on both I and Q correspond to a magnitude of $\sqrt{I^2 + Q^2} = \sqrt{2} = 1.4142$. Threshold values of greater than 1.4142 will force the AGC gain to the upper limit.
15-8	Loop Filter Upper Limit (Maximum Gain)	Upper limit for Loop Filter's accumulator (see AGC Section). The three most significant bits are the exponent and the five least significant bits represent the mantissa (see Figure 3). The three exponent bits map to bit positions 15-13 (15 is the MSB) and the five mantissa bits map to bit positions 12-8 (12 is the MSB). $(EEE.MMMMM)_{2.}$
23-16	Loop Filter Lower Limit (Minimum Gain)	Lower limit for Loop Filter's accumulator (see AGC Section). The format is the same as that for the upper limit described above. The 3 exponent bits map to bit positions 23-21 (23 is the MSB) and the mantissa bits map to bit positions 20-16 (20 is the MSB). $(EEE.MMMMM)_{2.}$
31-24	Programmable Loop Gain	Programmable part of Loop Gain word (see AGC Section). The Loop Gain value increments or decrements the Loop Filter's Accumulator at bit positions 2^{-6} through 2^{-13} as shown in Figure 3. The 8-bit loop gain is loaded into bit positions 31-24 (31 is the MSB and maps to the 2^{-6} position in the Accumulator). $(GGGGGGGG)_{2.}$

TABLE 9. I/O FORMATTING/CONTROL

DESTINATION ADDRESS = 4		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
0	Input Format	0 = Two's complement input format, 1 = Offset binary input format. Note: if a real input with offset binary weighting is used, the unused quadrature input pins should be tied to 1000000000.
1	Input Mode	0 = Input Controller operates in Interpolated Input Mode. 1 = Input Controller operates in Gated Input Mode. (See Input Controller Section).
2	Serial/Parallel Output Select	1 = Serial Output, 0 = Parallel Output. (See Output Formatter Section).
3	Test Enable	0 = Test Mode Disabled, 1 = Test Mode Enabled. (See Test Mode Section).
5-4	Serial Output Clock Select	Bits 5-4 Serial Output Clock Rate 0 0 CLK (Serial Output Clock Pin = High) 0 1 Clk/2 1 0 CLK/4 1 1 CLK/8 (See Output Formatter Section).
6	Serial Output Mode	1 = I Followed by Q Mode, 0 = Simultaneous I and Q Mode. (See Output Formatter Section)
7	Serial Output Word Orientation	1 = MSB First, 0 = LSB First.
8	Output Data Format	1 = Offset Binary, 0 = Two's Complement.
9	DATARDY Polarity	1 = Active Low, 0 = Active High. This applies to both serial and parallel output modes. (See Output Formatter Section).
10	Output Clock Polarity	1 = High to Low clock transition at midsample. 0 = Low to High clock transition at midsample.
31-11		Reserved.

TABLE 10. DECIMATING FILTER CONFIGURATION REGISTER

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
5-0	CIC Shifter Gain	These 6 bits set the fixed gain of the CIC shifter. The gain factor is of the form, 2^N, where N is the valued stored in this location. A gain range from 2^0 to 2^{63} is provided. Since the CIC shifter sets the signal level at the input to the CIC FIlter, care must be taken so that the signal is not shifted outside of the input bit range of the filter. (See Gain Distribution Section).
17-6	Programmable Divider	These 12 bits specify the divisor for the programmable divider in the Re-Sampler. The actual divisor is equal to the 12-bit value +1 for a total range of 1 to 4096. For example, a value of 7 would produce a sampling rate of 1/8 the CLK or 1/8 the carry-out frequency of the Re-Sampler NCO depending on configuration. (See Re-Sampler).
18	Programmable Divider Clock Source	1 = Divider clocked at sample rate of data input to the Low Pass Filter. 0 = Divider clocked by Re-Sampler NCO. (See Re-Sampler).
20-19	CIC Filter Configuration	0 0 3 stage CIC filter. 0 1 1 stage CIC (Integrate and dump) filter. 1 X bypass CIC. When a 3 stage CIC filter is chosen, a decimation factor >3 must be used if the Re-Sampler NCO is used to set the output sampling rate. (See Re-Sampler Section and Low Pass Filtering Section).
22-21	Compensation Filtering	0 0 x/sinx filtering. 0 1 $(x/sinx)^3$ filtering. 1 X bypass compensation filter. (See Low Pass Filtering Section).

SOURCE	PROGRAMMABLE DIVIDER RANGE
CLK	1-4096
ReSampler	2-4096

TABLE 10. DECIMATING FILTER CONFIGURATION REGISTER (Continued)

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
31-23		Reserved.

TABLE 11. CHIP CONFIGURATION REGISTER

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
0	HI/LO Output Sense	1 = HI/LO output of 1 means input > threshold. 0 = HI/LO output of 1 means input ≤ threshold. (See Input Level Detector Section).
1	AGC Disable	1 = AGC disabled, gain forced to 1.0 (0dB), 0 = Normal operation. (See AGC Section).
2	AGC Level Detector Sense	1 = Error signal is 1 when output > threshold, -1 otherwise. 0 = Error signal is -1 when output > threshold, 1 otherwise. Set to 0 for normal operation. (See AGC Section).
4-3	Carrier Offset Frequency Word Width	0 0 = 8 bits 0 1 = 16 bits 1 0 = 24 bits 1 1 = 32 bits (See Synthesizer/Mixer Section).
6-5	Sample Rate Offset Frequency Word Width	0 0 = 8 bits 0 1 = 16 bits 1 0 = 24 bits 1 1 = 32 bits (See Re-Sampler Section).
7	Carrier Offset Frequency Enable	1 = Enable Offset Frequency, 0 = Zero Offset Frequency. (See Synthesizer/Mixer Section).
8	Sample Rate Offset Frequency Enable	1 = Enable Offset Frequency, 0 = Zero Offset Frequency. (See Re-Sampler Section).
9	Load Synthesizer NCO	1 = Accumulation enabled. 0 = Feedback in accumulator is zeroed. (See Synthesizer/Mixer Section) Set to 1 for normal operation.
10	Load Re-Sampler NCO	1 = Accumulation enabled. 0 = Feedback in accumulator is zeroed. (See Re-Sampler Section) Set to 1 for normal operation.
12-11	Sample Phase Output Select	Selects 5 of the 8 MSBs of the Re-Sampler NCO's phase accumulator for output on SPH0-4. (See Re-Sampler Section). 0 0 Bits 28:24. 0 1 Bits 29:25. 1 0 Bits 30:26. 1 1 Bits 31:27.
13	Sample Phase Output Control	Selects whether the sample phase output pins and $\overline{\text{SSTRB}}$ update continuously or only when the DATARDY is active. (See Re-Sampler Section). 1 = Continuous Update. 0 = Updated by DATARDY.
14	Clear Accumulators	Writing a 1 to the Clear Accumulator bit forces the contents of all accumulators to 0. Accumulators will remain at 0 until a 0 is written to this bit. The following accumulators are affected by this bit. • Carrier NCO Accumulator • Cascode CIC Filter Accumulator • AGC Loop Filter Accumulator • Serial Output Shifter Counter • Serial Output Clock Logic • ReSampler NCO Carry Output Programmable Divider
31-15		Reserved.

TABLE 12. PHASE OFFSET REGISTER

DESTINATION ADDRESS = 7		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
7-0	Phase Offset	This 8 bit two's complement value specifies a carrier phase offset of π(n/128) where n is the two's complement value. This provides a range of phase offsets from -π to π*(127/128). (See Synthesizer/Mixer Section).
31-8		Reserved.

TABLE 13. TEST REGISTER

DESTINATION ADDRESS = 8		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
4-0	Force SPH4-0	When Test Mode enabled*, SPH4-0 is forced to the values programmed in these bit locations. Bit position 4 maps to SPH4. (See Test Mode Section).
5	Force $\overline{\text{SSTRB}}$	When Test Mode enabled*, $\overline{\text{SSTRB}}$ is forced to state of this bit.
6	Force HI/LO	When Test Mode enabled*, HI/LO is forced to state of this bit.
16-7	Force IOUT9-0	When Test Mode enabled*, IOUT9-0 if forced to the values programmed in these bit locations. Bit position 16 maps to IOUT9.
17	Force DATARDY	When Test Mode enabled*, DATARDY is forced to state of this bit.
18	Force LOTP	When Test Mode enabled*, LOTP is forced to state of this bit.
28-19	Force QOUT9-0	When Test Mode enabled*, QOUT9-0 is forced to the values programmed in these bit locations. Bit position 16 maps to QOUT9.
31-29		Reserved.

* Test Mode Enable is Destination Address = 4, bit-3.

TABLE 14. AGC SAMPLE STROBE REGISTER

DESTINATION ADDRESS = 9		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
7-0	AGC Read	Writing this address samples the accumulator in the AGC's Loop Filter. The procedure for reading the sampled value out of the part on C0-7 is discussed in the Microprocessor Interface Section. (See Microprocessor Interface Section).

References

[1] Hogenauer, Eugene, "An Economical Class of Digital Filters for Decimation and Interpolation", IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29 No. 2, April 1981.

[2] Samueli, Henry "The Design of Multiplierless FIR filters for Compensating D/A Converter Frequency Response Distortion", IEEE Transaction Circuits and Systems, Vol. 35, No. 8, August 1988.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD . . . . . Class 3

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range
Commercial . . . . . 0^oC to 70^oC
Industrial. . . . . -40^oC to 85^oC

Thermal Information (Typical)

	θ_{JA} ($^oC/W$)
Thermal Resistance (Typical, Note 3)	
PLCC Package	23

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

Die Characteristics

Gate Count . . . . . 38,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC Commercial, T_A = -40^o to 85^oC Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, CLK = 52.6MHz Notes 4, 5	-	350	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	V
Clock Input High	V_{IHC}	V_{CC} = Max, CLK	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = Min, CLK	-	0.8	V
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.4	V
Input Capacitance	C_{IN}	CLK = 1MHz All measurements referenced to GND. T_A = 25^oC, Note 6	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

NOTES:

4. Power supply current is proportional to frequency. Typical rating is 7mA/MHz.
5. Output load per test circuit and C_L = 40pF.
6. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

Note 8, V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC Commercial, T_A = -40^o to 85^oC Industrial

PARAMETER	SYMBOL	NOTES	-52 (52.6MHz)		UNITS
			MIN	MAX	
CLK Period	T_{CP}		19	-	ns
CLK High	T_{CH}		7	-	ns
CLK Low	T_{CL}		7	-	ns
Setup Time IIN9-0, QIN9-0, $\overline{ENI}$, PH1-0, CFLD, COF, SOF, COFSYNC, and SOFSYNC to CLK	T_{DS}		7	-	ns
Hold Time IIN9-0, QIN9-0, $\overline{ENI}$, PH1-0, CFLD, COF, SOF, COFSYNC, and SOFSYNC from CLK	T_{DH}		1	-	ns
Setup Time A0-2, C0-7 to Rising Edge of $\overline{WR}$	T_{WS}		15	-	ns
Hold Time A0-2, C0-7 from Rising Edge of $\overline{WR}$	T_{WH}		0	-	ns

AC Electrical Specifications

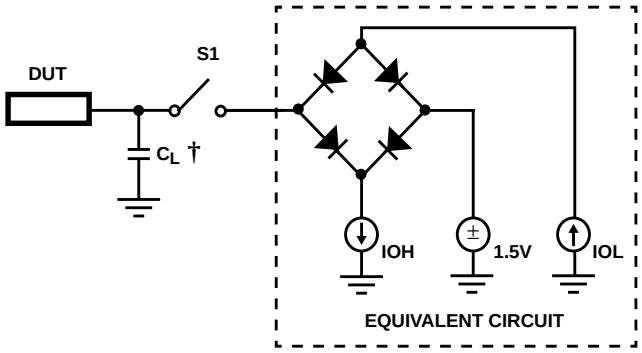
Note 8, V_{CC} = 5.0V ±5%, T_A = 0° to 70°C Commercial, T_A = -40° to 85°C Industrial **(Continued)**

PARAMETER	SYMBOL	NOTES	-52 (52.6MHz)		UNITS
			MIN	MAX	
CLK to IOUT9-0, QOUT9-0, DATARDY, LOTP, $\overline{SSTRB}$, SPH4-0, HI/LO	T_{DO}		-	8	ns
$\overline{WR}$ High	T_{WRH}		16	-	ns
$\overline{WR}$ Low	T_{WRL}		16	-	ns
$\overline{RD}$ Low	T_{RDL}		16	-	ns
$\overline{RD}$ LOW to Data Valid	T_{RDO}		-	15	ns
$\overline{RD}$ HIGH to Output Disable	T_{ROD}	Note 8	-	8	ns
Output Enable	T_{OE}		-	8	ns
$\overline{WR}$ to CLK	T_{WC}	Note 9	8	-	ns
Output Disable Time	T_{OD}	Note 8	-	8	ns
Output Rise, Fall Time	T_{RF}	Note 8	-	3	ns

NOTES:

7. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level for CLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
8. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
9. Set time to ensure action initiated by $\overline{WR}$ or SERCLK will be seen by a particular clock.

AC Test Load Circuit



SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

† Test head capacitance.

Waveforms

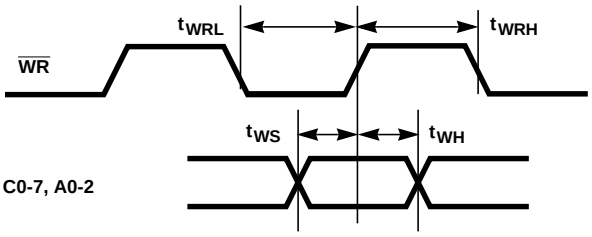


FIGURE 26. TIMING RELATIVE TO $\overline{WR}$

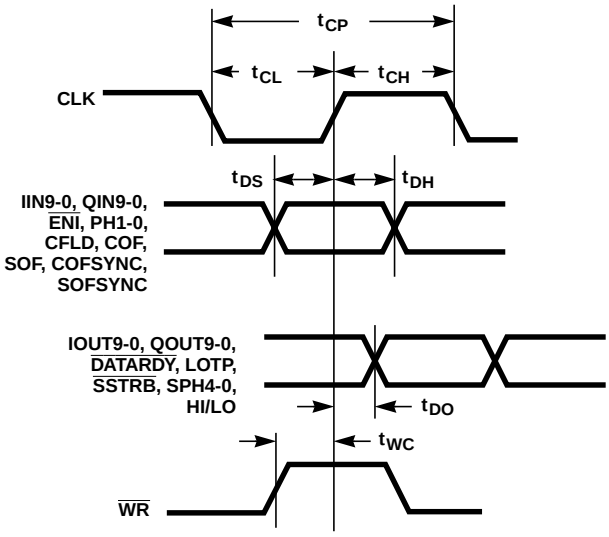


FIGURE 27. TIMING RELATIVE TO CLK

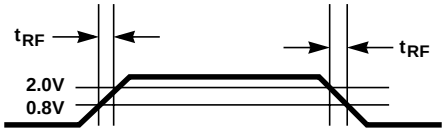


FIGURE 28. OUTPUT RISE AND FALL TIMES

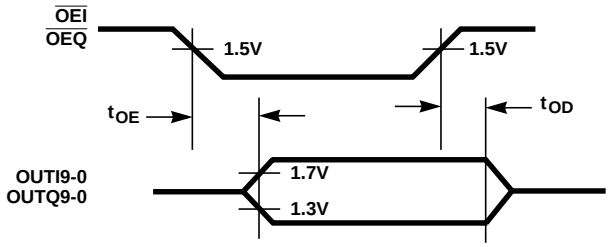


FIGURE 29. OUTPUT ENABLE/DISABLE

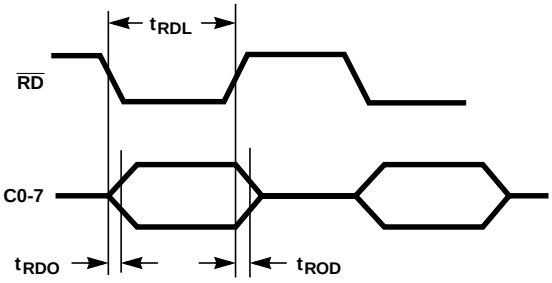
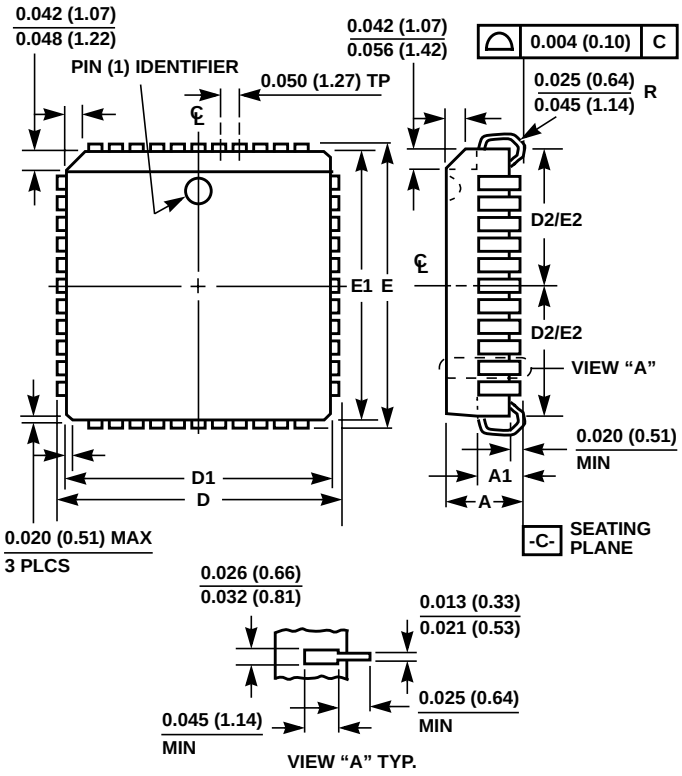


FIGURE 30. TIMING RELATIVE TO READ

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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