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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM628512C Series

4 M SRAM (512-kword × 8-bit)



ADE-203-1212C (Z)
Rev. 3.0
Aug. 5, 2002

Description

The Hitachi HM628512C is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512C is suitable for battery backup system.

Features

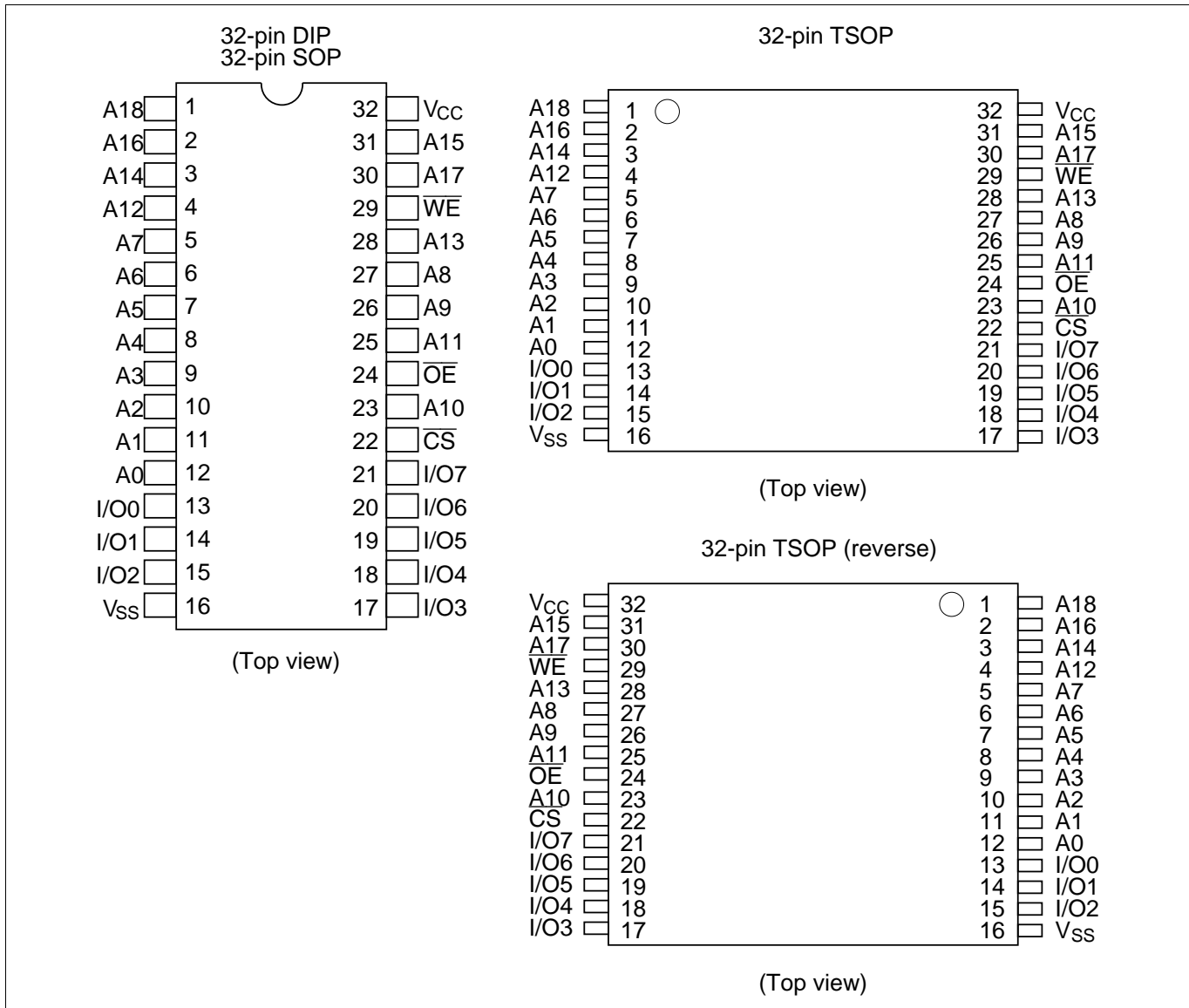
- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 10 mW/MHz (typ)
 - Standby: 4 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

HM628512C Series

Ordering Information

| Type No. | Access time | Package |
|------------------|-------------|---|
| HM628512CLP-7 | 70 ns | 600-mil 32-pin plastic DIP (DP-32) |
| HM628512CLP-5SL | 55 ns | |
| HM628512CLFP-7 | 70 ns | 525-mil 32-pin plastic SOP (FP-32D) |
| HM628512CLFP-5SL | 55 ns | |
| HM628512CLTT-7 | 70 ns | 400-mil 32-pin plastic TSOP II (TTP-32D) |
| HM628512CLTT-5SL | 55 ns | |
| HM628512CLRR-7 | 70 ns | 400-mil 32-pin plastic TSOP II reverse (TTP-32DR) |
| HM628512CLRR-5SL | 55 ns | |

Pin Arrangement

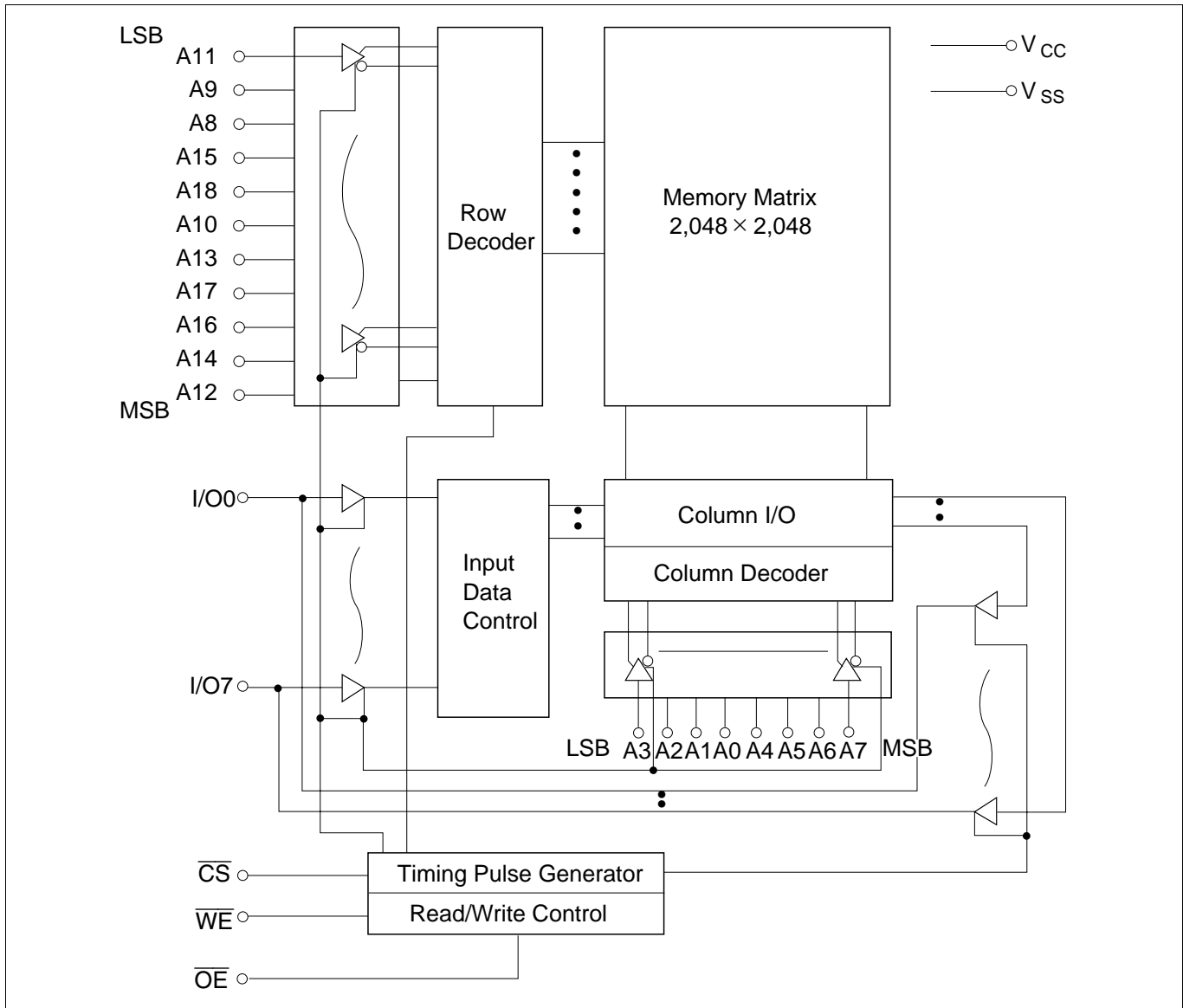


Pin Description

| Pin name | Function |
|-----------------|-------------------|
| A0 to A18 | Address input |
| I/O0 to I/O7 | Data input/output |
| \overline{CS} | Chip select |
| \overline{OE} | Output enable |
| \overline{WE} | Write enable |
| V _{CC} | Power supply |
| V _{SS} | Ground |

HM628512C Series

Block Diagram



Function Table

| \overline{WE} | \overline{CS} | \overline{OE} | Mode | V_{CC} current | Dout pin | Ref. cycle |
|-----------------|-----------------|-----------------|----------------|-------------------|----------|-----------------|
| × | H | × | Not selected | I_{SB}, I_{SB1} | High-Z | — |
| H | L | H | Output disable | I_{CC} | High-Z | — |
| H | L | L | Read | I_{CC} | Dout | Read cycle |
| L | L | H | Write | I_{CC} | Din | Write cycle (1) |
| L | L | L | Write | I_{CC} | Din | Write cycle (2) |

Note: ×: H or L

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------|---|------|
| Power supply voltage | V_{CC} | -0.5 to +7.0 | V |
| Voltage on any pin relative to V_{SS} | V_T | -0.5* ¹ to $V_{CC} + 0.3$ * ² | V |
| Power dissipation | P_T | 1.0 | W |
| Operating temperature | T_{opr} | -20 to +70 | °C |
| Storage temperature | T_{stg} | -55 to +125 | °C |
| Storage temperature under bias | T_{bias} | -20 to +85 | °C |

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.
 2. Maximum voltage is 7.0 V.

Recommended DC Operating Conditions ($T_a = -20$ to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------|----------|--------------------|-----|----------------|------|
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input high voltage | V_{IH} | 2.2 | — | $V_{CC} + 0.3$ | V |
| Input low voltage | V_{IL} | -0.3* ¹ | — | 0.8 | V |

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns.

HM628512C Series

DC Characteristics

| Parameter | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions |
|--------------------------------------|-----------------------|-----|-------------------|------------------|---------------|---|
| Input leakage current | $ I_{LI} $ | — | — | 1 | μA | $V_{in} = V_{SS} \text{ to } V_{CC}$ |
| Output leakage current | $ I_{LO} $ | — | — | 1 | μA | $\overline{CS} = V_{IH} \text{ or } \overline{OE} = V_{IH} \text{ or } \overline{WE} = V_{IL}, V_{IO} = V_{SS} \text{ to } V_{CC}$ |
| Operating power supply current: DC | I_{CC} | — | 1.5 | 3 | mA | $\overline{CS} = V_{IL},$ others = $V_{IH}/V_{IL}, I_{IO} = 0 \text{ mA}$ |
| Operating power supply current | HM628512C-5 I_{CC1} | — | 8 | 25 | mA | Min cycle, duty = 100% $\overline{CS} = V_{IL},$ others = V_{IH}/V_{IL} $I_{IO} = 0 \text{ mA}$ |
| | HM628512C-7 I_{CC1} | — | 7 | 25 | mA | |
| Operating power supply current | I_{CC2} | — | 2 | 5 | mA | Cycle time = 1 μs , duty = 100% $I_{IO} = 0 \text{ mA}, \overline{CS} \leq 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}, V_{IL} \leq 0.2 \text{ V}$ |
| Standby power supply current: DC | I_{SB} | — | 0.1 | 0.5 | mA | $\overline{CS} = V_{IH}$ |
| Standby power supply current (1): DC | I_{SB1} | — | 0.8* ² | 20* ² | μA | $V_{in} \geq 0 \text{ V}, \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ |
| | | — | 0.8* ³ | 10* ³ | μA | |
| Output low voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 2.1 \text{ mA}$ |
| Output high voltage | V_{OH} | 2.4 | — | — | V | $I_{OH} = -1.0 \text{ mA}$ |

- Notes: 1. Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.
 2. This characteristics is guaranteed only for L version.
 3. This characteristics is guaranteed only for L-SL version.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1 \text{ MHz}$)

| Parameter | Symbol | Typ | Max | Unit | Test conditions |
|--|----------|-----|------------------|-------------|------------------------|
| Input capacitance* ¹ | C_{in} | — | 8 | pF | $V_{in} = 0 \text{ V}$ |
| Input/output capacitance* ¹ | C_{IO} | — | 10* ² | pF | $V_{IO} = 0 \text{ V}$ |

- Notes: 1. This parameter is sampled and not 100% tested.
 2. C_{IO} max = 12 pF only for HM628512CLP Series.

AC Characteristics ($T_a = -20$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512C-7)
 1 TTL Gate + C_L (50 pF) (HM628512C-5)
 (Including scope & jig)

Read Cycle

| Parameter | Symbol | HM628512C | | | | Unit | Notes |
|--------------------------------------|-----------|-----------|-----|-----|-----|------|-------|
| | | -5 | | -7 | | | |
| | | Min | Max | Min | Max | | |
| Read cycle time | t_{RC} | 55 | — | 70 | — | ns | |
| Address access time | t_{AA} | — | 55 | — | 70 | ns | |
| Chip select access time | t_{CO} | — | 55 | — | 70 | ns | |
| Output enable to output valid | t_{OE} | — | 25 | — | 35 | ns | |
| Chip selection to output in low-Z | t_{LZ} | 10 | — | 10 | — | ns | 2 |
| Output enable to output in low-Z | t_{OLZ} | 5 | — | 5 | — | ns | 2 |
| Chip deselection to output in high-Z | t_{HZ} | 0 | 20 | 0 | 25 | ns | 1, 2 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 20 | 0 | 25 | ns | 1, 2 |
| Output hold from address change | t_{OH} | 10 | — | 10 | — | ns | |

HM628512C Series

Write Cycle

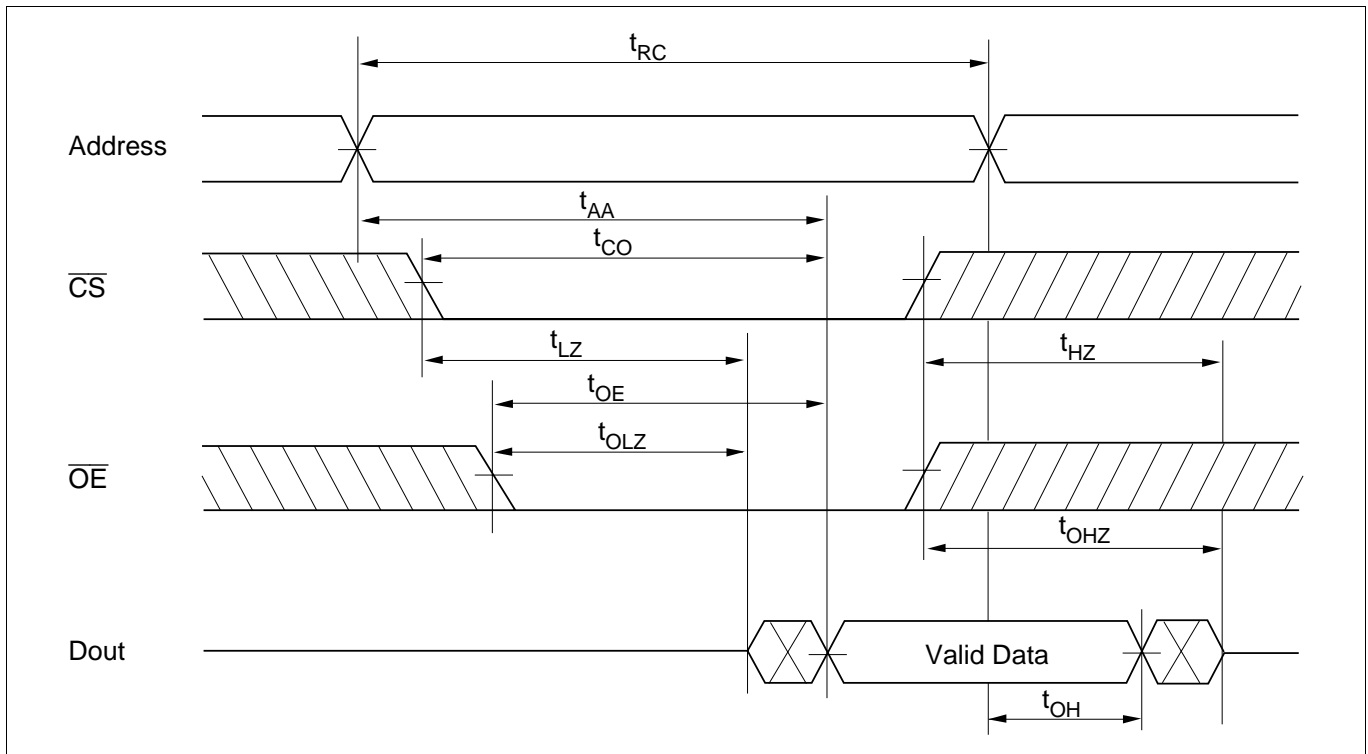
| Parameter | Symbol | HM628512C | | | | Unit | Notes |
|-------------------------------------|-----------|-----------|-----|-----|-----|------|---------|
| | | -5 | | -7 | | | |
| | | Min | Max | Min | Max | | |
| Write cycle time | t_{WC} | 55 | — | 70 | — | ns | |
| Chip selection to end of write | t_{CW} | 50 | — | 60 | — | ns | 4 |
| Address setup time | t_{AS} | 0 | — | 0 | — | ns | 5 |
| Address valid to end of write | t_{AW} | 50 | — | 60 | — | ns | |
| Write pulse width | t_{WP} | 40 | — | 50 | — | ns | 3, 12 |
| Write recovery time | t_{WR} | 0 | — | 0 | — | ns | 6 |
| \overline{WE} to output in high-Z | t_{WHZ} | 0 | 20 | 0 | 25 | ns | 1, 2, 7 |
| Data to write time overlap | t_{DW} | 25 | — | 30 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | ns | |
| Output active from output in high-Z | t_{OW} | 5 | — | 5 | — | ns | 2 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 20 | 0 | 25 | ns | 1, 2, 7 |

Notes: 1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from \overline{CS} going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If \overline{CS} is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

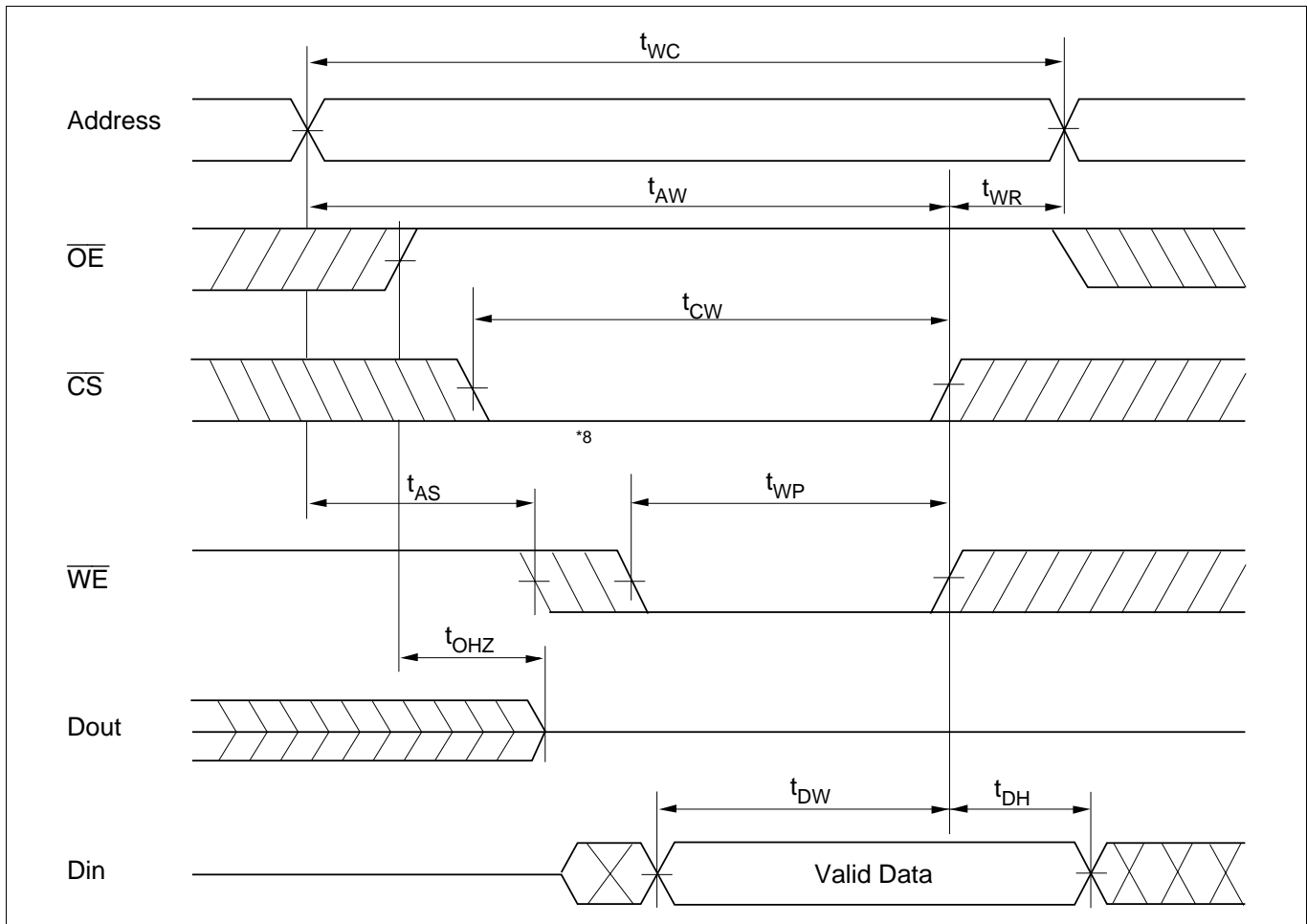
Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)

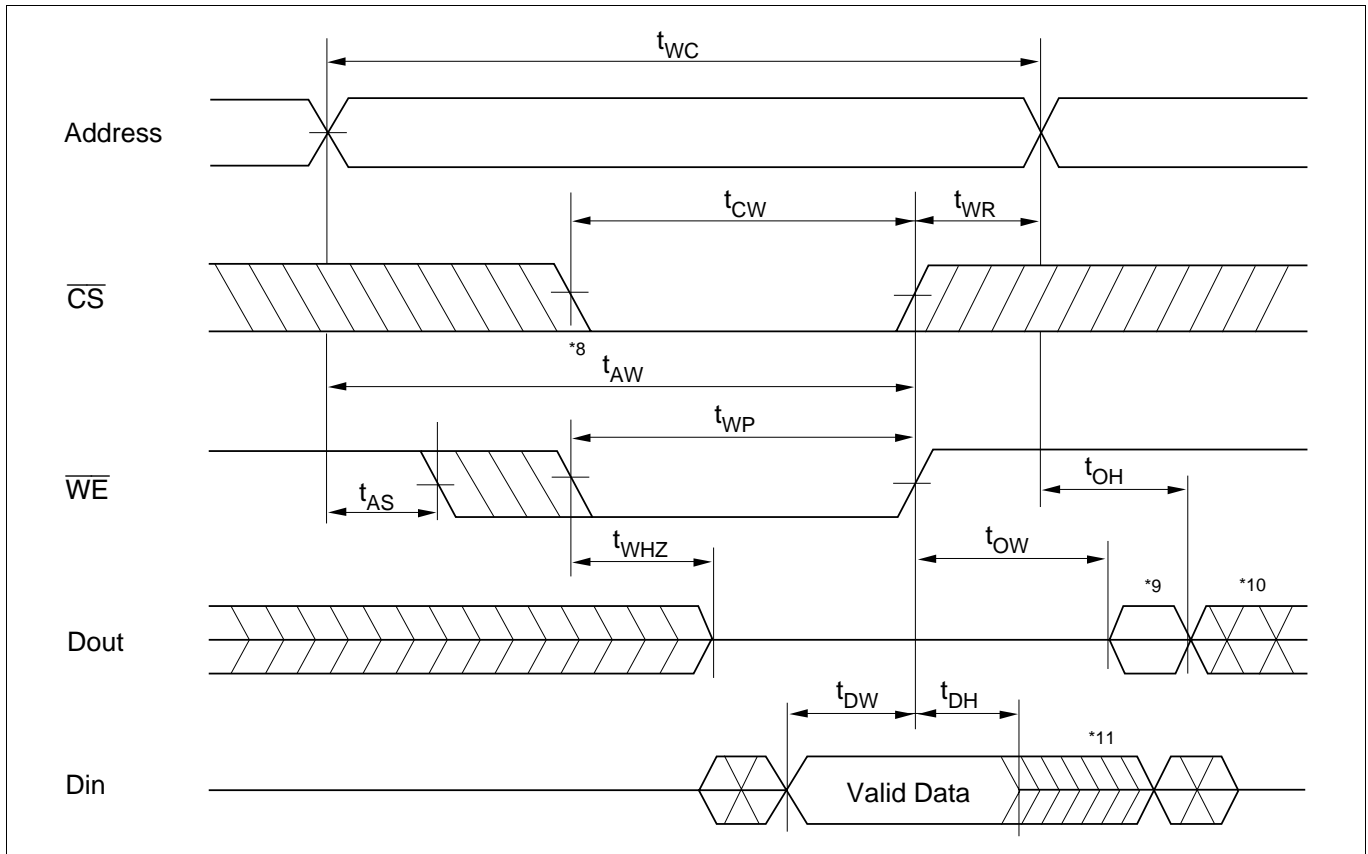


HM628512C Series

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) (\overline{OE} Low Fixed)



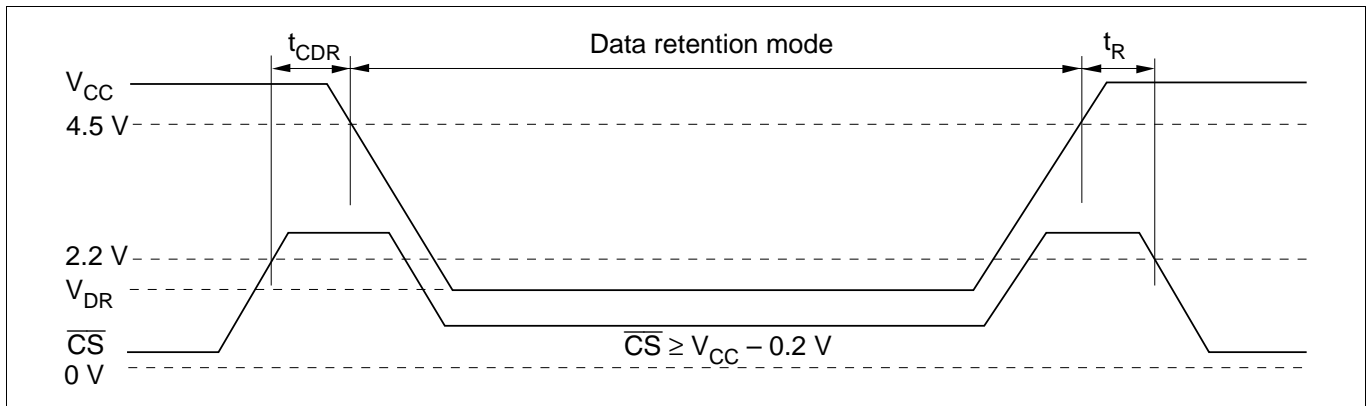
HM628512C Series

Low V_{CC} Data Retention Characteristics ($T_a = -20$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions* ³ |
|--------------------------------------|------------|---------------|------------|-----------|---------------|---|
| V_{CC} for data retention | V_{DR} | 2 | — | — | V | $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$ |
| Data retention current | I_{CCDR} | — | 0.8^{*4} | 20^{*1} | μA | $V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ |
| | | — | 0.8^{*4} | 10^{*2} | μA | |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | t_{RC}^{*5} | — | — | ns | |

- Notes: 1. For L-version and $10 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.
 2. For L-SL-version and $3 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.
 3. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and Din buffer. In data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.
 5. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)

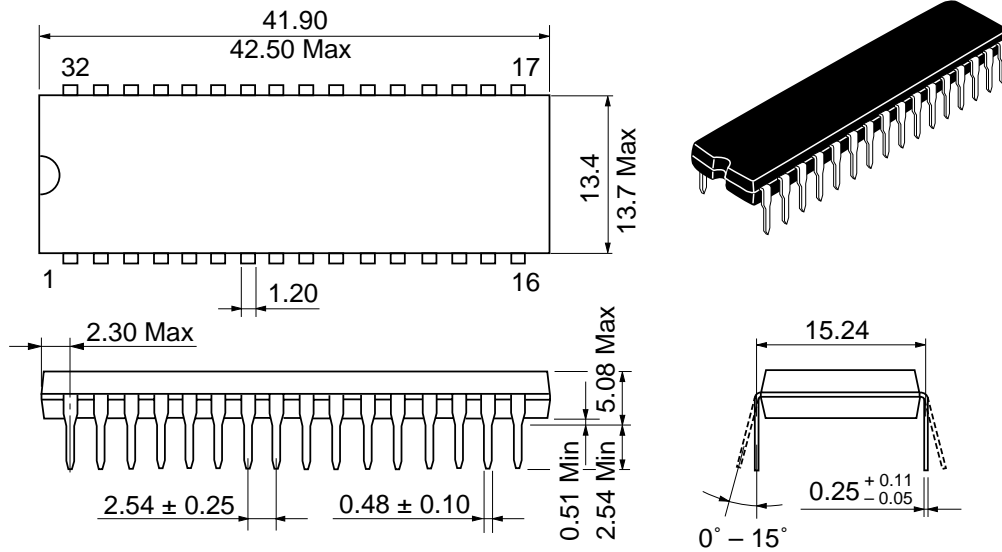


Package Dimensions

HM628512CLP Series (DP-32)

As of January, 2002

Unit: mm



| | |
|------------------------|----------|
| Hitachi Code | DP-32 |
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 5.1 g |

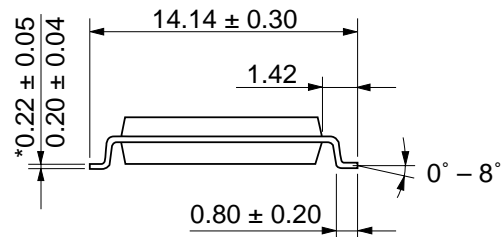
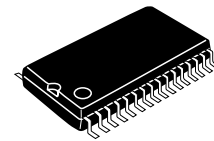
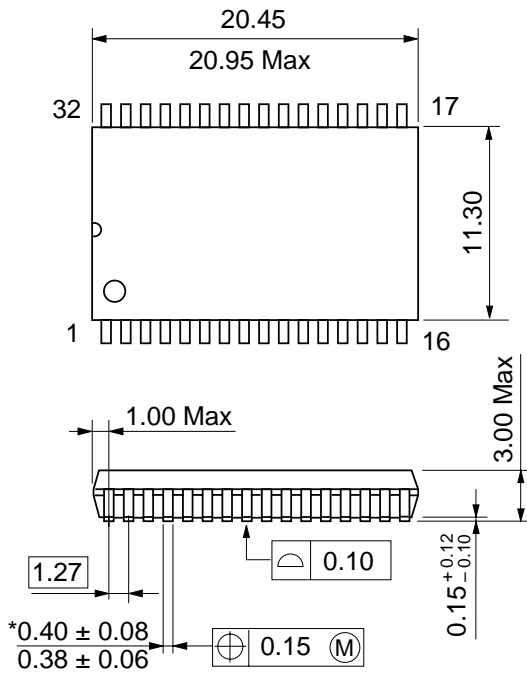
HM628512C Series

Package Dimensions (cont.)

HM628512CLFP Series (FP-32D)

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

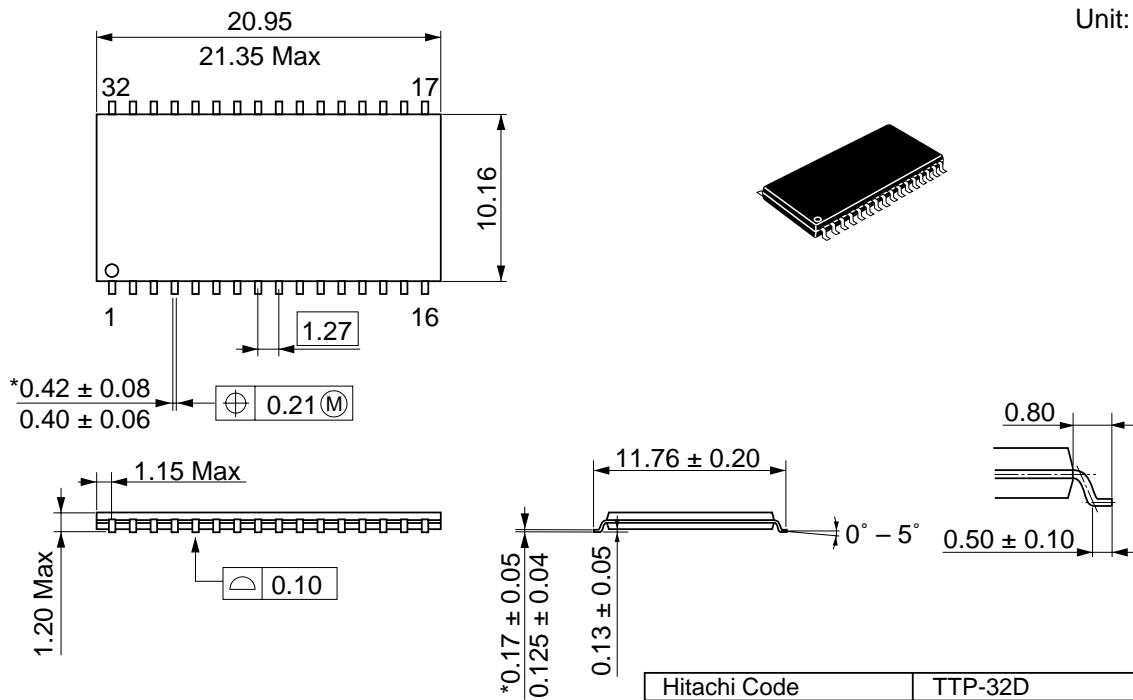
| | |
|------------------------|----------|
| Hitachi Code | FP-32D |
| JEDEC | Conforms |
| JEITA | — |
| Mass (reference value) | 1.3 g |

Package Dimensions (cont.)

HM628512CLTT Series (TTP-32D)

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | TTP-32D |
| JEDEC | Conforms |
| JEITA | — |
| Mass (reference value) | 0.51 g |

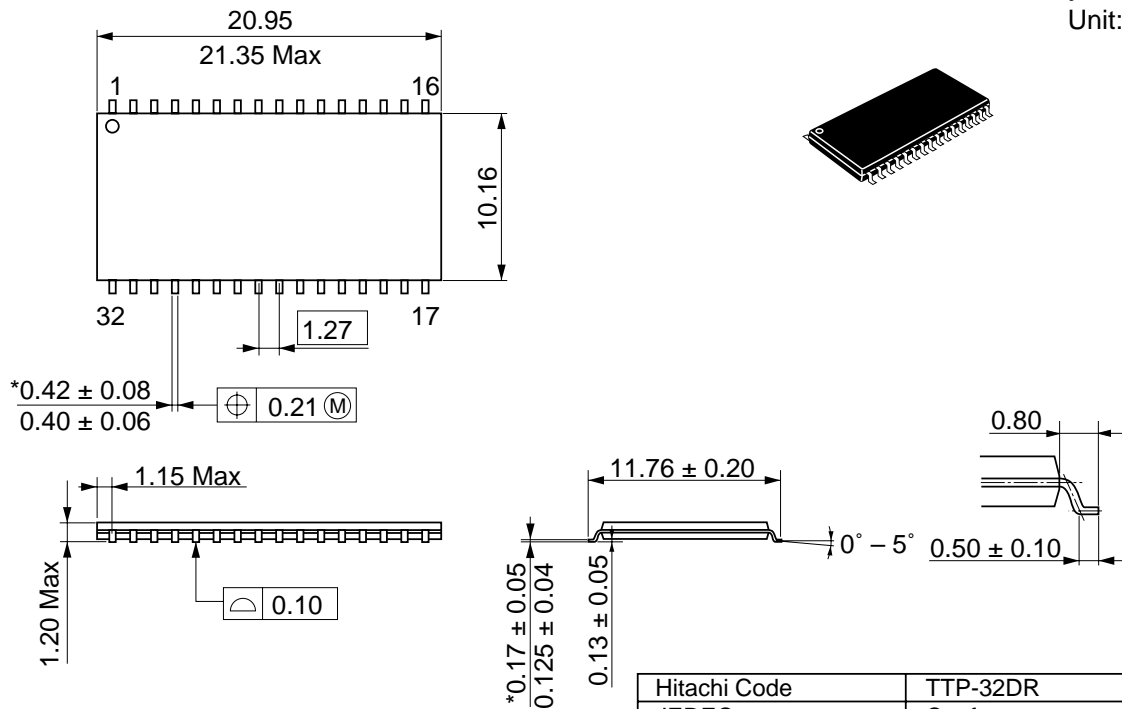
HM628512C Series

Package Dimensions (cont.)

HM628512CLRR Series (TTP-32DR)

As of January, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | TTP-32DR |
| JEDEC | Conforms |
| JEITA | — |
| Mass (reference value) | 0.51 g |

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