

---

# HM51W4265C Series

262,144-word × 16-bit Dynamic Random Access Memory

# HITACHI

ADE-203-477A (Z)  
Rev. 1.0  
Jul. 31, 1996

---

## Description

The Hitachi HM51W4265C Series is a CMOS dynamic RAM organized as 262,144-word × 16-bit. HM51W4265C Series has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM51W4265C Series offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM51W4265C Series to be packaged in standard 400-mil 44-pin plastic TSOPII.

## Features

- Single 3.3 V (±0.15 V) (HM51W4265C-6R)  
Single 3.3 V (±0.3 V) (HM51W4265C-6/7/8)
- High speed
  - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 576 mW/552 mW/468 mW/396 mW (max)
  - Standby mode: 6.9 mW (max) (HM51W4265C-6R)  
7.2 mW (max) (HM51W4265C-6/7/8)  
0.69 mW (max)(L-version) (HM51W4265CL-6R)  
0.72 mW (max) (L-version) (HM51W4265CL-6/7/8)
- EDO page mode capability
- 512 refresh cycles: 8 ms  
128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Self refresh
- $2\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)

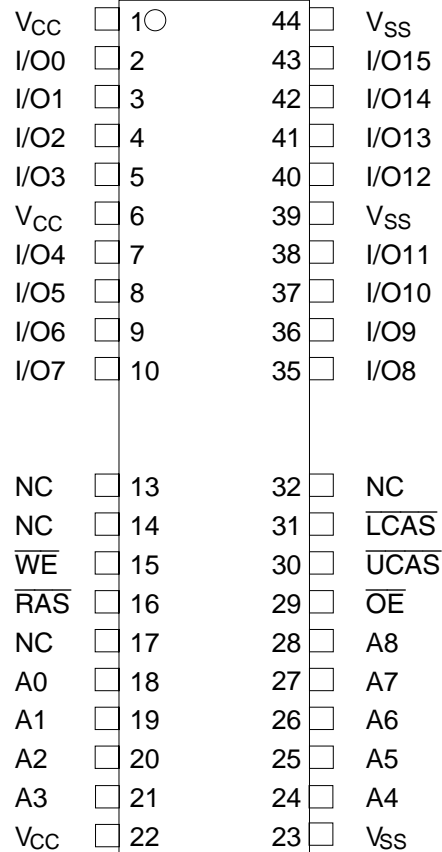
# HM51W4265C Series

## Ordering Information

Type No.	Access time	Package
HM51W4265CTT-6	60 ns	400-mil 44-pin plastic TSOPII (TTP-44/40DB)
HM51W4265CTT-6R	60 ns	
HM51W4265CTT-7	70 ns	
HM51W4265CTT-8	80 ns	
HM51W4265CLTT-6	60 ns	
HM51W4265CLTT-6R	60 ns	
HM51W4265CLTT-7	70 ns	
HM51W4265CLTT-8	80 ns	

## Pin Arrangement

HM51W4265CTT/CLTT Series

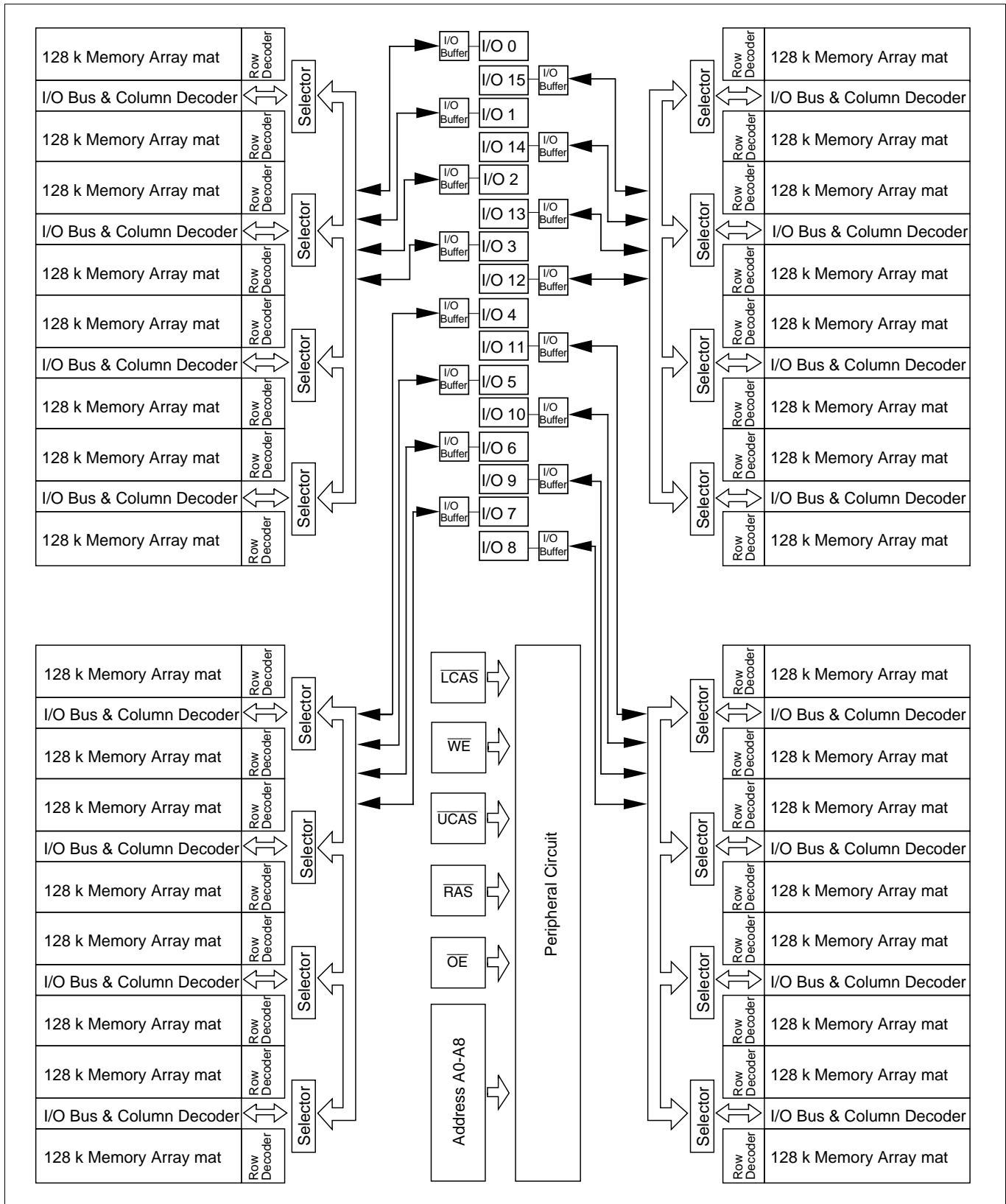


(Top view)

## Pin Description

<b>Pin name</b>	<b>Function</b>
A0 to A8	Address input — Row address A0 to A8 — Column address A0 to A8 — Refresh address A0 to A8
I/O0 to I/O15	Data-in/data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/write enable
$\overline{\text{OE}}$	Output enable
$V_{\text{CC}}$	Power
$V_{\text{SS}}$	Ground
NC	No connection

## Block Diagram



## Operation Mode

The HM51W4265C series has the following 11 operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5.  $\overline{\text{RAS}}$ -only refresh cycle
6.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle
7. Self refresh cycle
8. EDO page mode read cycle
9. EDO page mode early write cycle
10. EDO page mode delayed write cycle
11. EDO page mode read-modify-write cycle

### Inputs

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output	Operation
H	H	H	D	D	Open	Standby
H	L	L	H	L	Valid	Standby
L	L	L	H	L	Valid	Read cycle
L	L	L	L* <sup>2</sup>	D	Open	Early write cycle
L	L	L	L* <sup>2</sup>	H	Undefined	Delayed write cycle
L	L	L	H to L	L to H	Valid	Read-modify-write cycle
L	H	H	D	D	Open	$\overline{\text{RAS}}$ -only refresh cycle
H to L	H	L	D	D	Open	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle
	L	H				Self refresh cycle
	L	L				
L	H to L	H to L	H	L	Valid	EDO page mode read cycle
L	H to L	H to L	L* <sup>2</sup>	D	Open	EDO page mode early write cycle
L	H to L	H to L	L* <sup>2</sup>	H	Undefined	EDO page mode delayed write cycle
L	H to L	H to L	H to L	L to H	Valid	EDO page mode read-modify-write cycle
L	L	L	H	H	Open	Read cycle (Output disabled)

# HM51W4265C Series

- Notes: 1. H: High(inactive) L: Low(active) D: H or L  
2.  $t_{wCS} \geq 0$  ns Early write cycle  
 $t_{wCS} < 0$  ns Delayed write cycle  
3. Mode is determined by the OR function of the  $\overline{UCAS}$  and  $\overline{LCAS}$ . (Mode is set by the earliest of  $\overline{UCAS}$  and  $\overline{LCAS}$  active edge and reset by the latest of  $\overline{UCAS}$  and  $\overline{LCAS}$  inactive edge.) However write OPERATION and output HIZ control are done independently by each  $\overline{UCAS}$ ,  $\overline{LCAS}$ .  
ex. if  $\overline{RAS} = H$  to  $L$ ,  $\overline{UCAS} = H$ ,  $\overline{LCAS} = L$ , then  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle is selected.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to +4.6	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

## Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{SS}$	0	0	0	V	2
	$V_{CC}$ (HM51W4265C-6R)	3.15	3.3	3.45	V	1, 2
	$V_{CC}$ (HM51W4265C-6/7/8)	3.0	3.3	3.6	V	1, 2
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	-0.3	—	0.8	V	1

- Notes: 1. All voltage referred to  $V_{SS}$ .  
2. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
The supply voltage with all  $V_{SS}$  pins must be on the same level.

**DC Characteristics**

 (Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ±0.15 V, V<sub>SS</sub> = 0 V) (HM51W4265C-6R)

 (Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ±0.3 V, V<sub>SS</sub> = 0 V) (HM51W4265C-6/7/8)

Parameter	Symbol	HM51W4265C						Unit	Test conditions
		-6/6R		-7		-8			
		Min	Max	Min	Max	Min	Max		
Operating current* <sup>1, *2</sup>	I <sub>CC1</sub>	—	120	—	110	—	95	mA	RAS cycling UCAS or LCAS cycling t <sub>RC</sub> = min
Standby current	I <sub>CC2</sub>	—	2	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V <sub>IH</sub> Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS, WE, OE ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
Standby current (L-version)	I <sub>CC2</sub>	—	200	—	200	—	200	μA	CMOS interface RAS, UCAS, LCAS, WE, OE ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
RAS-only refresh current* <sup>2</sup>	I <sub>CC3</sub>	—	120	—	105	—	92	mA	t <sub>RC</sub> = min
Standby current* <sup>1</sup>	I <sub>CC5</sub>	—	5	—	5	—	5	mA	RAS = V <sub>IH</sub> , UCAS or LCAS = V <sub>IL</sub> Dout = enable
CAS-before-RAS refresh current* <sup>2</sup>	I <sub>CC6</sub>	—	120	—	105	—	92	mA	t <sub>RC</sub> = min
EDO page mode current* <sup>1, *3</sup>	I <sub>CC4</sub>	—	160	—	130	—	110	mA	t <sub>HPC</sub> = min
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	200	—	200	—	200	μA	Standby: CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 250 μs t <sub>RAS</sub> ≤ 1 μs, UCAS, LCAS = V <sub>IL</sub> WE, OE = V <sub>IH</sub>
Self-refresh mode current	I <sub>CC11</sub>	—	1	—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Self-refresh mode current (L-version)	I <sub>CC11</sub>	—	200	—	200	—	200	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

---

## HM51W4265C Series

---

- Notes:
1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.
  2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .
  3. Address can be changed once or less within one EDO page cycle.
  4.  $V_{IH} \geq V_{CC} - 0.2$  V,  $0 \leq V_{IL} \leq 0.2$  V, Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

### Capacitance

( $T_a = +25^\circ\text{C}$ ,  $V_{CC} = 3.3$  V  $\pm 0.15$  V) (HM51W4265C-6R)

( $T_a = +25^\circ\text{C}$ ,  $V_{CC} = 3.3$  V  $\pm 0.3$  V) (HM51W4265C-6/7/8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	—	5	pF	1
Input capacitance (Clocks)	$C_{i2}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{i/O}$	—	10	pF	1, 2

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
  2.  $\overline{UCAS}$  and  $\overline{LCAS} = V_{IH}$  to disable Dout.



**AC Characteristics**

(Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.15 V, V<sub>SS</sub> = 0 V) (HM51W4265C-6R)\*<sup>1, \*14, \*15, \*17, \*18</sup>

(Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V) (HM51W4265C-6/7/8)\*<sup>1, \*14, \*15, \*17, \*18</sup>

**Test Conditions**

- Input rise and fall time: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C<sub>L</sub> (50 pF) (Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)**

Parameter	Symbol	HM51W4265C						Unit	Notes
		-6/6R		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	104	—	124	—	144	—	ns	
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	60	10000	70	10000	80	10000	ns	27
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	10	10000	13	10000	15	10000	ns	28
Row address setup time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row address hold time	t <sub>RAH</sub>	10	—	10	—	10	—	ns	
Column address setup time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	19
Column address hold time	t <sub>CAH</sub>	10	—	13	—	15	—	ns	19
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	20	45	20	50	20	60	ns	8
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	15	30	15	35	15	40	ns	9
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	48	—	58	—	68	—	ns	29
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	10	—	10	—	10	—	ns	20
$\overline{\text{OE}}$ to Din delay time	t <sub>ODD</sub>	15	—	18	—	20	—	ns	
$\overline{\text{OE}}$ delay time from Din	t <sub>DZO</sub>	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ setup time from Din	t <sub>DZC</sub>	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t <sub>T</sub>	2	50	2	50	2	50	ns	7
Refresh period	t <sub>REF</sub>	—	8	—	8	—	8	ms	
Refresh period (L-version)	t <sub>REF</sub>	—	128	—	128	—	128	ms	

# HM51W4265C Series

## Read Cycle

Parameter	Symbol	HM51W4265C						Unit	Notes
		-6/6R		-7		-8			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	20	—	20	ns	3, 4, 13
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	$t_{\text{OAC}}$	—	15	—	20	—	20	ns	3, 23
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	19
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	16, 20
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	18	—	23	—	28	—	ns	
Output buffer turn-off time	$t_{\text{OFF1}}$	—	15	—	15	—	15	ns	6, 25
Output buffer turn-off time to $\overline{\text{OE}}$	$t_{\text{OFF2}}$	—	15	—	15	—	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	15	—	18	—	20	—	ns	
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WDD}}$	15	—	18	—	20	—	ns	
$\overline{\text{OE}}$ pulse width	$t_{\text{OEP}}$	15	—	20	—	20	—	ns	23
Turn-off to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	15	—	15	—	15	ns	6, 25
Turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	15	—	15	—	15	ns	6
Output data hold time	$t_{\text{OH}}$	5	—	5	—	5	—	ns	
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	5	—	5	—	5	—	ns	
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	60	—	70	—	80	—	ns	
Read command hold time from $\overline{\text{CAS}}$	$t_{\text{RCHC}}$	15	—	18	—	20	—	ns	
Read command hold time from column address	$t_{\text{RCHA}}$	30	—	35	—	40	—	ns	

Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{WCS}$	0	—	0	—	0	—	ns	10, 19
Write command hold time	$t_{WCH}$	10	—	13	—	15	—	ns	19
Write command pulse width	$t_{Wp}$	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	10	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	10	—	13	—	15	—	ns	21
Data-in setup time	$t_{DS}$	0	—	0	—	0	—	ns	11
Data-in hold time	$t_{DH}$	10	—	13	—	15	—	ns	11

Read-Modify-Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	133	—	159	—	183	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	77	—	90	—	102	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	32	—	38	—	42	—	ns	10
Column address to $\overline{WE}$ delay time	$t_{AWD}$	47	—	55	—	62	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	15	—	18	—	20	—	ns	

Refresh Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	10	—	10	—	10	—	ns	19
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	10	—	ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	10	—	10	—	10	—	ns	19
$\overline{CAS}$ precharge time in normal mode	$t_{CPN}$	10	—	13	—	15	—	ns	22

# HM51W4265C Series

## EDO Page Mode Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	$t_{HPC}$	25	—	30	—	35	—	ns	24
EDO page mode $\overline{CAS}$ precharge time	$t_{CP}$	10	—	13	—	15	—	ns	
EDO page mode $\overline{RAS}$ pulse width	$t_{RASC}$	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	$t_{ACP}$	—	35	—	40	—	45	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{RHCP}$	35	—	40	—	45	—	ns	
Output data hold time from CAS low	$t_{DOH}$	3	—	3	—	3	—	ns	26
$\overline{CAS}$ hold time referred $\overline{OE}$	$t_{COL}$	10	—	13	—	20	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	$t_{COP}$	5	—	5	—	5	—	ns	
Read command hold time from CAS precharge	$t_{RCHP}$	35	—	40	—	45	—	ns	

## EDO Page Mode Read-Modify-Write Cycle

		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	$t_{HPCM}$	66	—	77	—	86	—	ns	
EDO page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	$t_{CPW}$	52	—	60	—	67	—	ns	10

## Self Refresh Mode

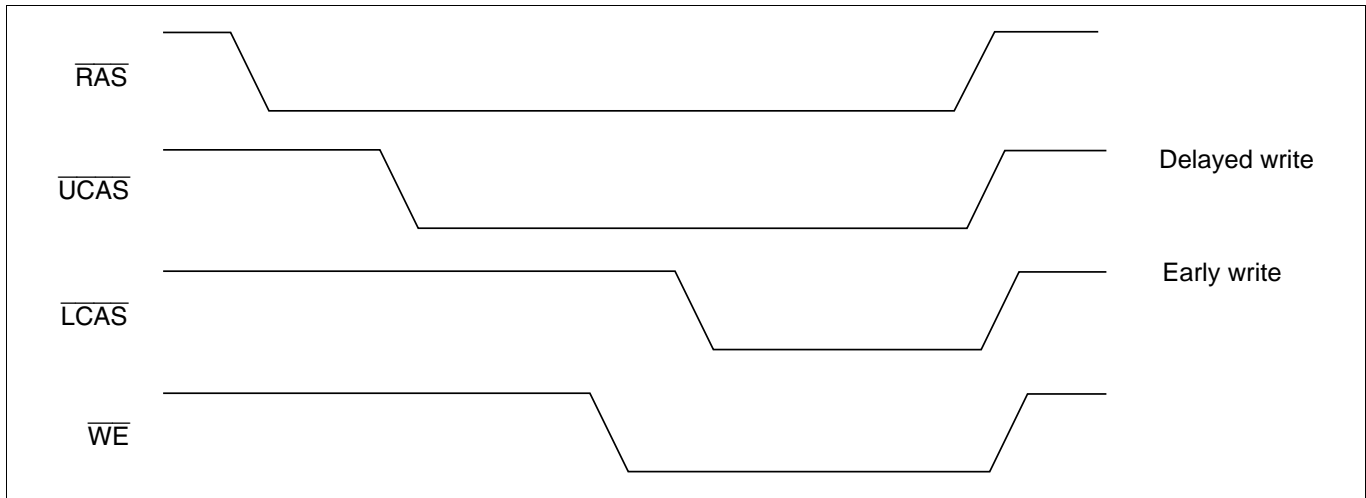
		HM51W4265C							
		-6/6R		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	$t_{RASS}$	100	—	100	—	100	—	$\mu s$	30, 31, 32
$\overline{RAS}$ precharge time (self refresh)	$t_{RPS}$	130	—	130	—	130	—	ns	
$\overline{CAS}$ hold time (self refresh)	$t_{CHS}$	-50	—	-50	—	-50	—	ns	21

- Notes:
1. AC measurements assume  $t_T = 2$  ns.
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 1 TTL loads and 50 pF. ( $V_{OH} = 2.0$  V,  $V_{OL} = 0.8$  V)
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \geq t_{RAD}(\text{max})$ .
  6.  $t_{OFF1}(\text{max})$ ,  $t_{OFF2}(\text{max})$ ,  $t_{OFR}(\text{max})$  and  $t_{WEZ}(\text{max})$  define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
  7.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in an early write cycle and to  $\overline{\text{WE}}$  leading edge in a delayed write or a read-modify-write cycle.
  12.  $t_{RASC}$  defines  $\overline{\text{RAS}}$  pulse width in EDO mode cycles.
  13. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$ .
  14. An initial pause of 100  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh cycle or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles is required.
  15. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
  16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  17. When both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  go low at the same time, all 16-bit data are written into the device.  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  cannot be staggered within the same write/read cycles.
  18. All the  $V_{CC}$  and  $V_{SS}$  pins shall be supplied with the same voltages.
  19.  $t_{ASC}$ ,  $t_{CAH}$ ,  $t_{RCS}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{CSR}$  and  $t_{RPC}$  are determined by the earlier falling edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  20.  $t_{CRP}$ ,  $t_{CHR}$ ,  $t_{ACP}$ ,  $t_{CPW}$  and  $t_{RCH}$  are determined by the later rising edge of  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ .
  21.  $t_{CWL}$ ,  $t_{DH}$ ,  $t_{DS}$  and  $t_{CHS}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  22.  $t_{CPN}$  and  $t_{CP}$  are determined by the time that both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.
  23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH}(\text{min})/V_{IL}(\text{max})$  level.
  24.  $t_{HPC}(\text{min})$  can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of  $\overline{\text{CAS}}$  cycle  $t_{HPC}$  ( $t_{CAS} + t_{CP} + 2t_T$ ) becomes greater than the specified  $t_{HPC}(\text{min})$  value.
  25. Data output turns off and becomes high impedance from later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . Hold time and turn off time are specified by the timing specifications of later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  between  $t_{OHR}$  and  $t_{OH}$ , and between  $t_{OFR}$  and  $t_{OFF}$ .

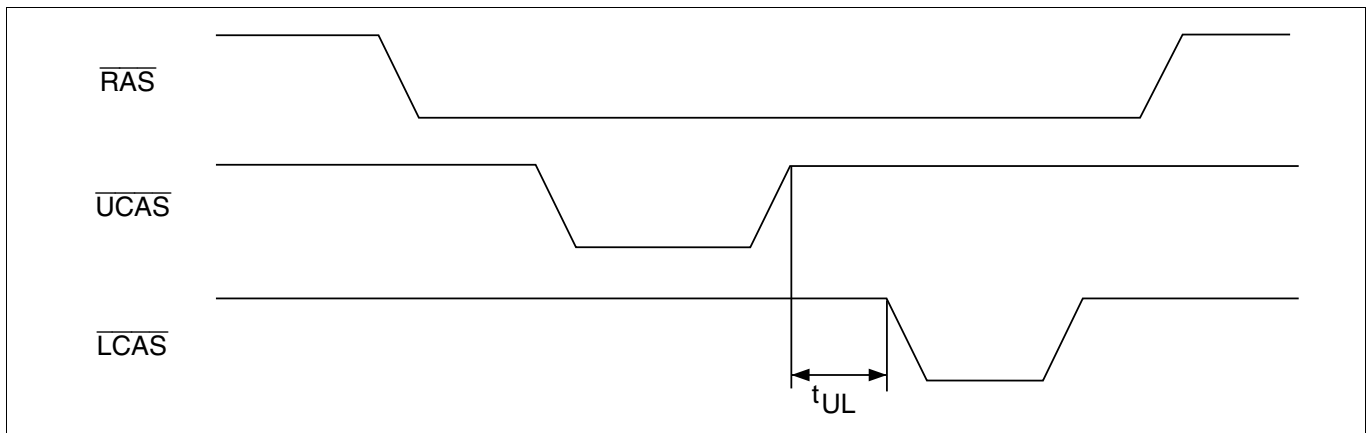
26.  $t_{DOH}$  defines the time at which the output level satisfied the output timing reference levels.  
Measured with the test conditions.
27.  $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$  in read-modify-write cycle.
28.  $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$  in read-modify-write cycle.
29.  $t_{CSH}(\text{min})$  can be achieved when  $t_{RCD} \leq t_{CSH}(\text{min}) - t_{CAS}(\text{min})$ .
30. Please do not use  $t_{RASS}$  timing,  $10 \mu\text{s} \leq t_{RASS} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100 \mu\text{s}$ , then  $\overline{RAS}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
31. If you use distributed CBR refresh mode with  $15.6 \mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6 \mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
32. If you use  $\overline{RAS}$  only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with  $15.6 \mu\text{s}$  interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
33. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
34. XXX: H or L (H:  $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$ , L:  $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$ )  
/////: Invalid Dout
- When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{IH}$  or  $V_{IL}$ .

Notes concerning  $\overline{2CAS}$  control

1. Each of the  $\overline{UCAS}/\overline{LCAS}$  should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



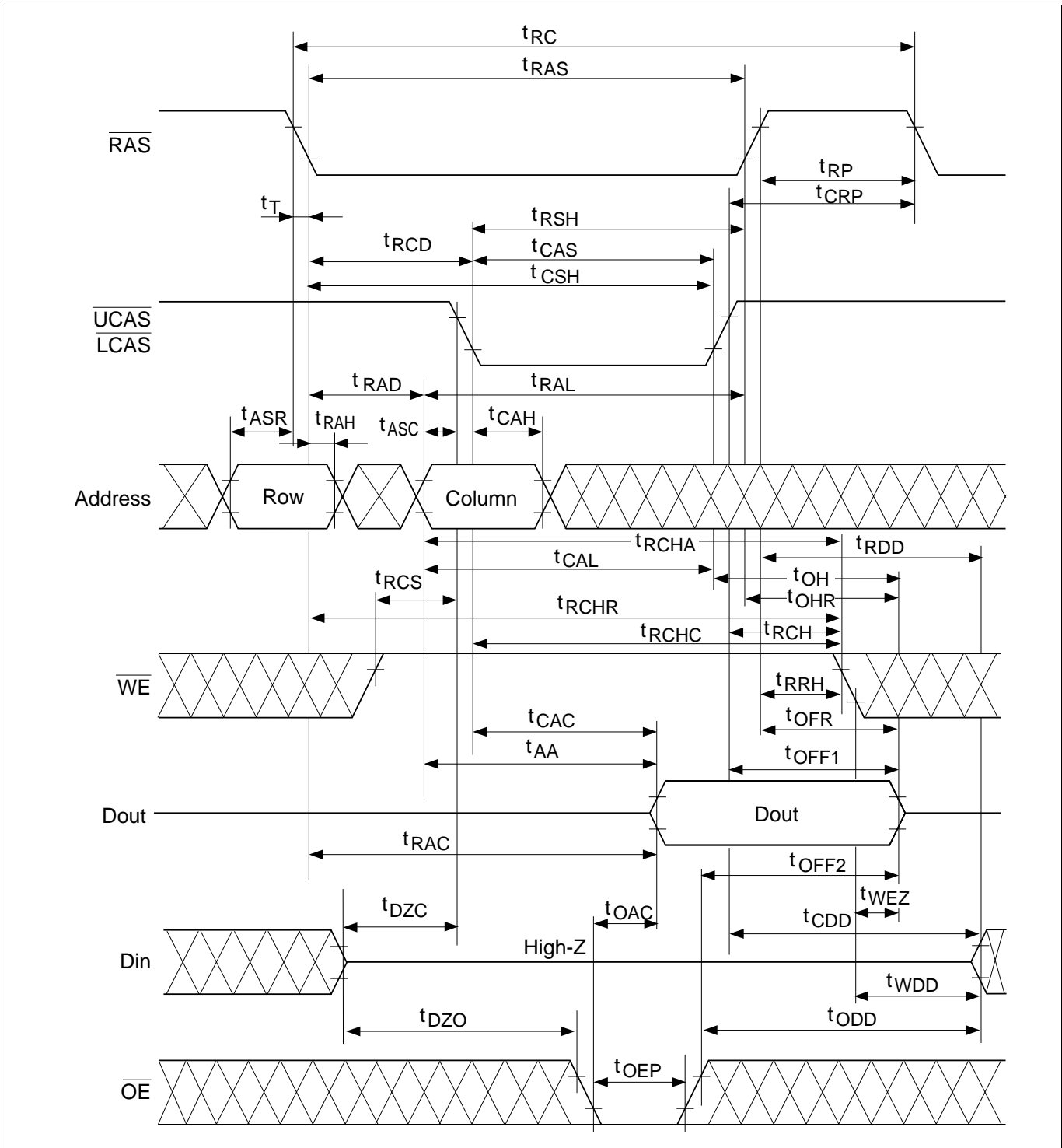
3. Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied, EDO page mode can be performed.



4. Byte control operation by remaining  $\overline{UCAS}$  or  $\overline{LCAS}$  high is guaranteed.

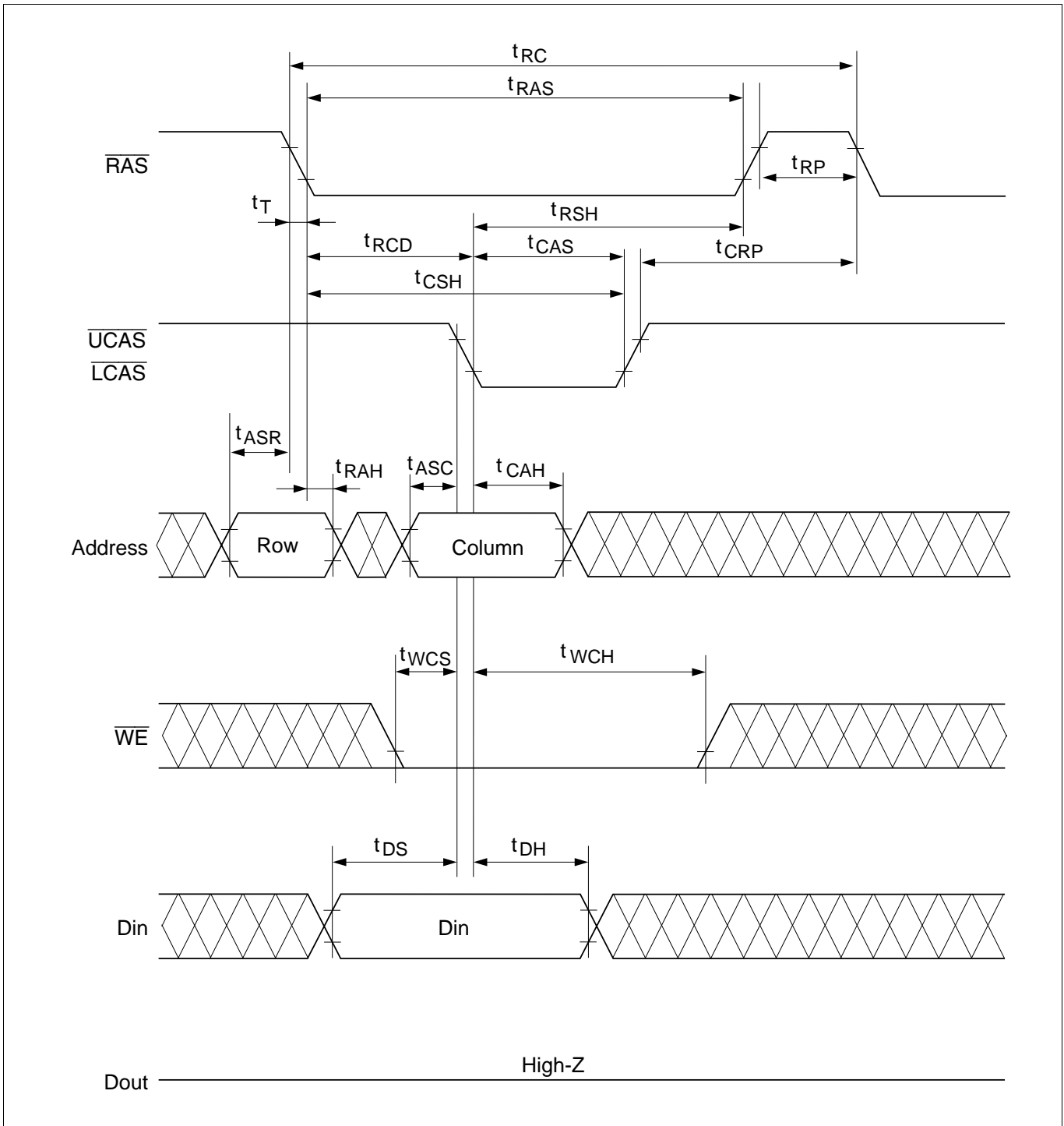
## Timing Waveforms\*34

### Read Cycle

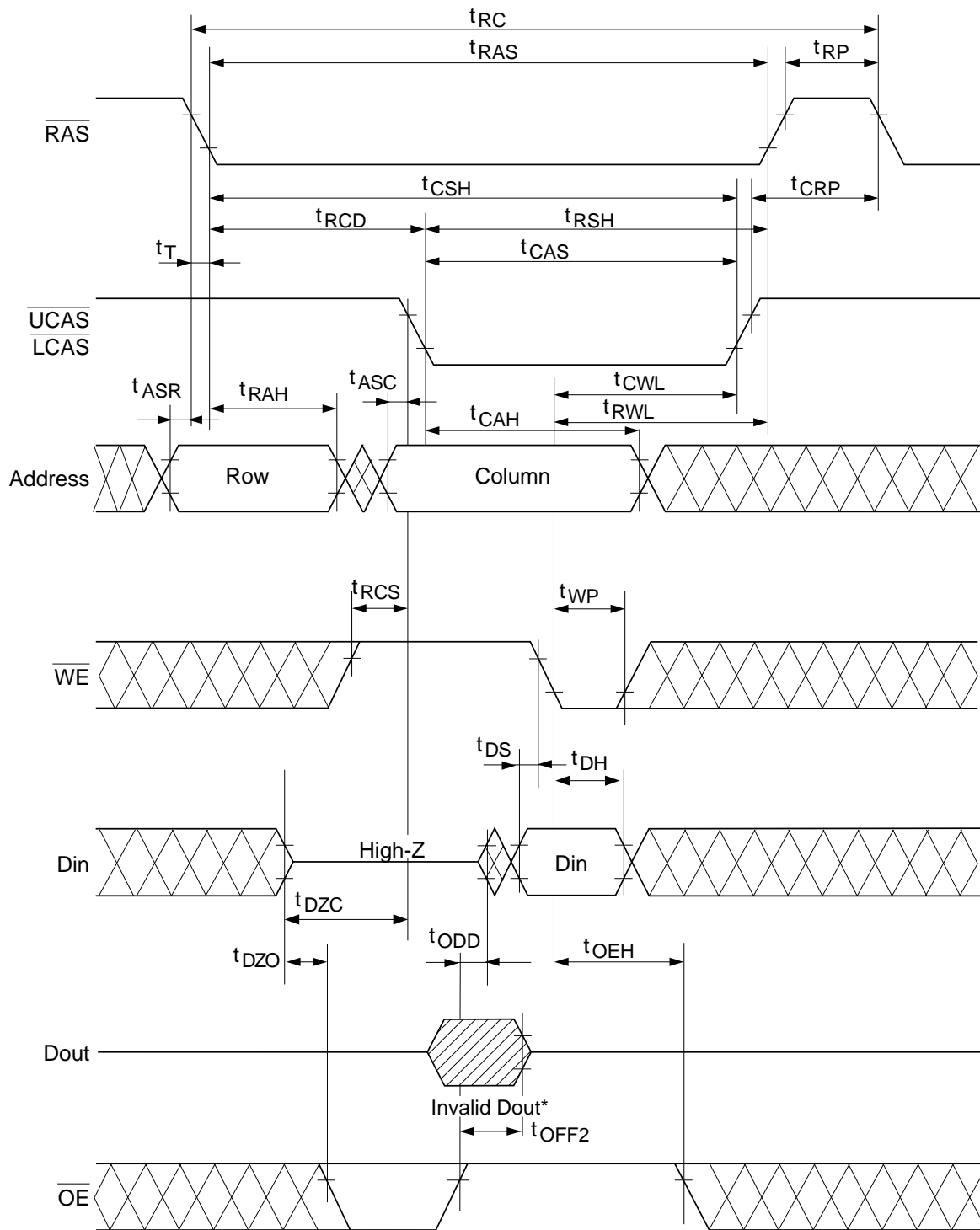




Early Write Cycle

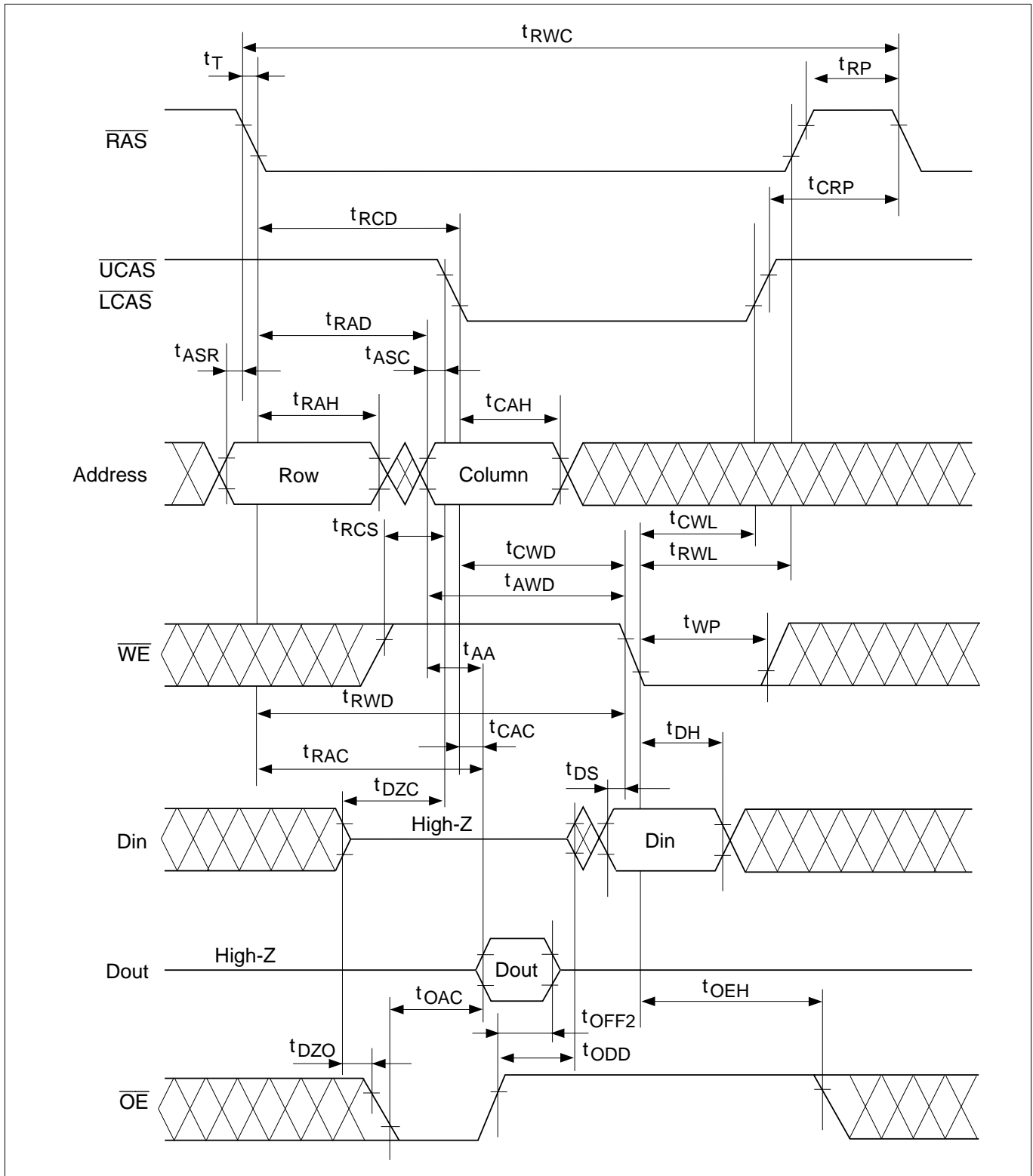


## Delayed Write Cycle

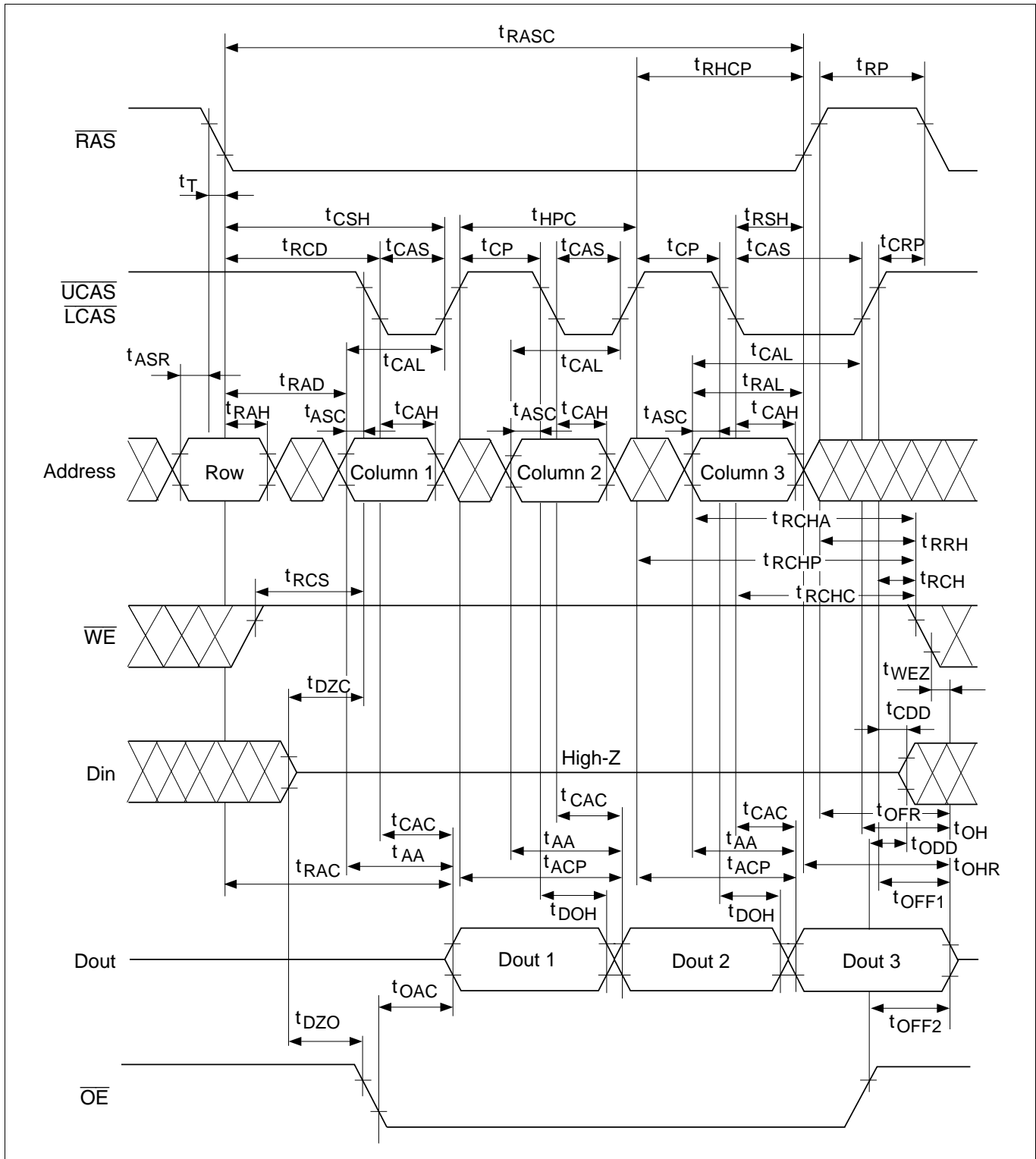


\* Do not enable Dout during delayed write cycle.

Read-Modify-Write Cycle

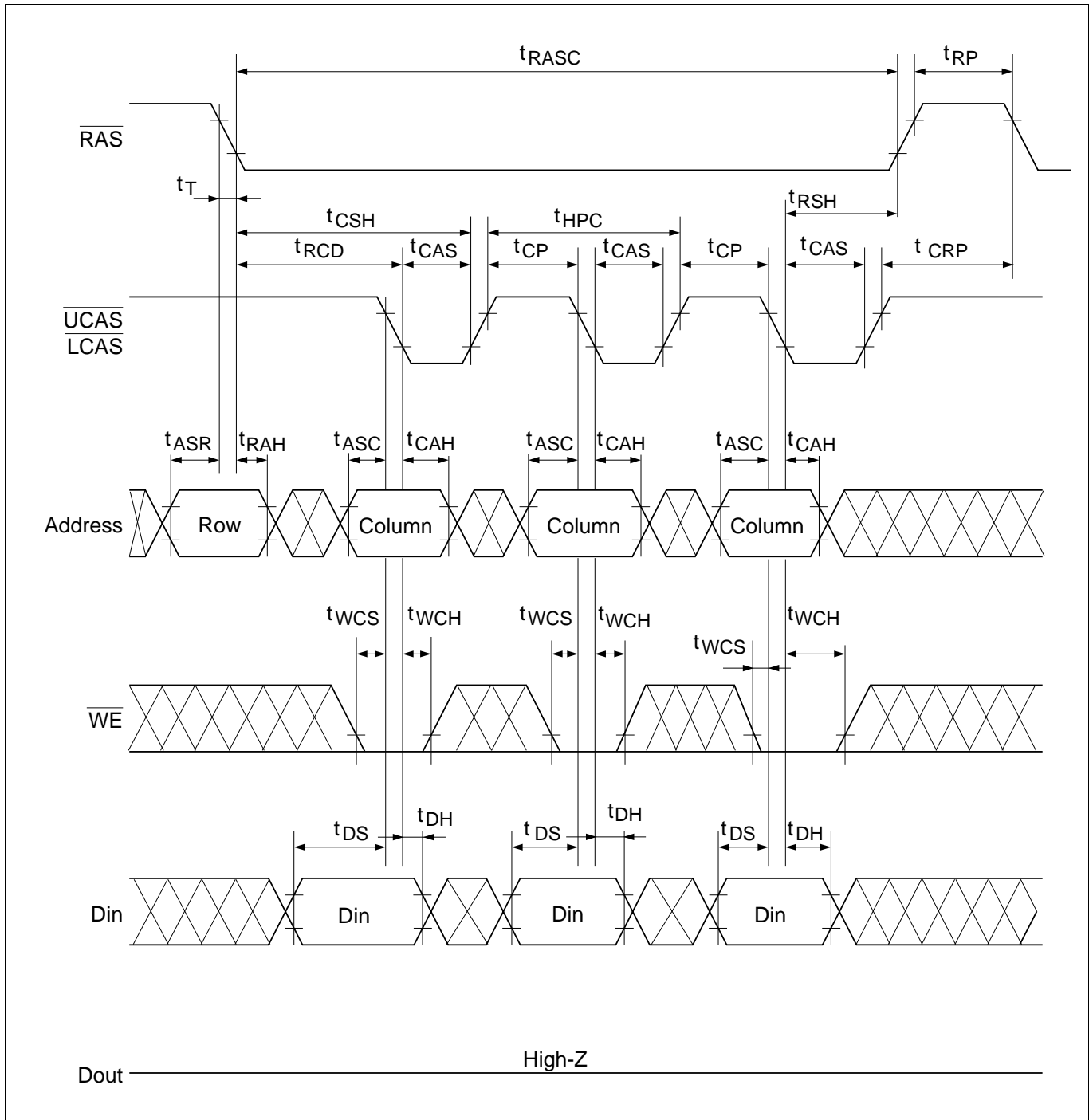


## EDO Page Mode Read Cycle ( $t_{HPC}$ minimum cycle operation)

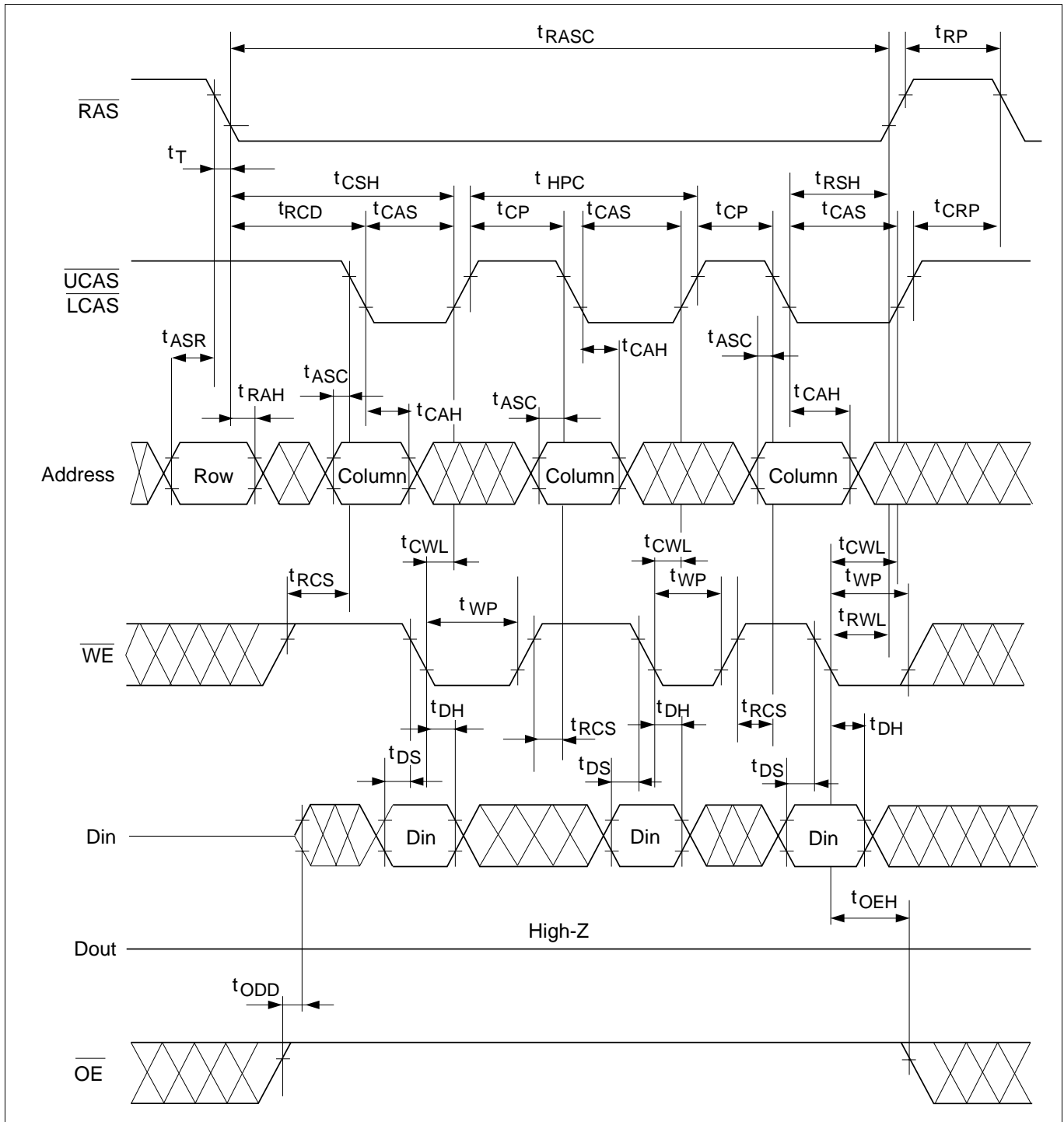




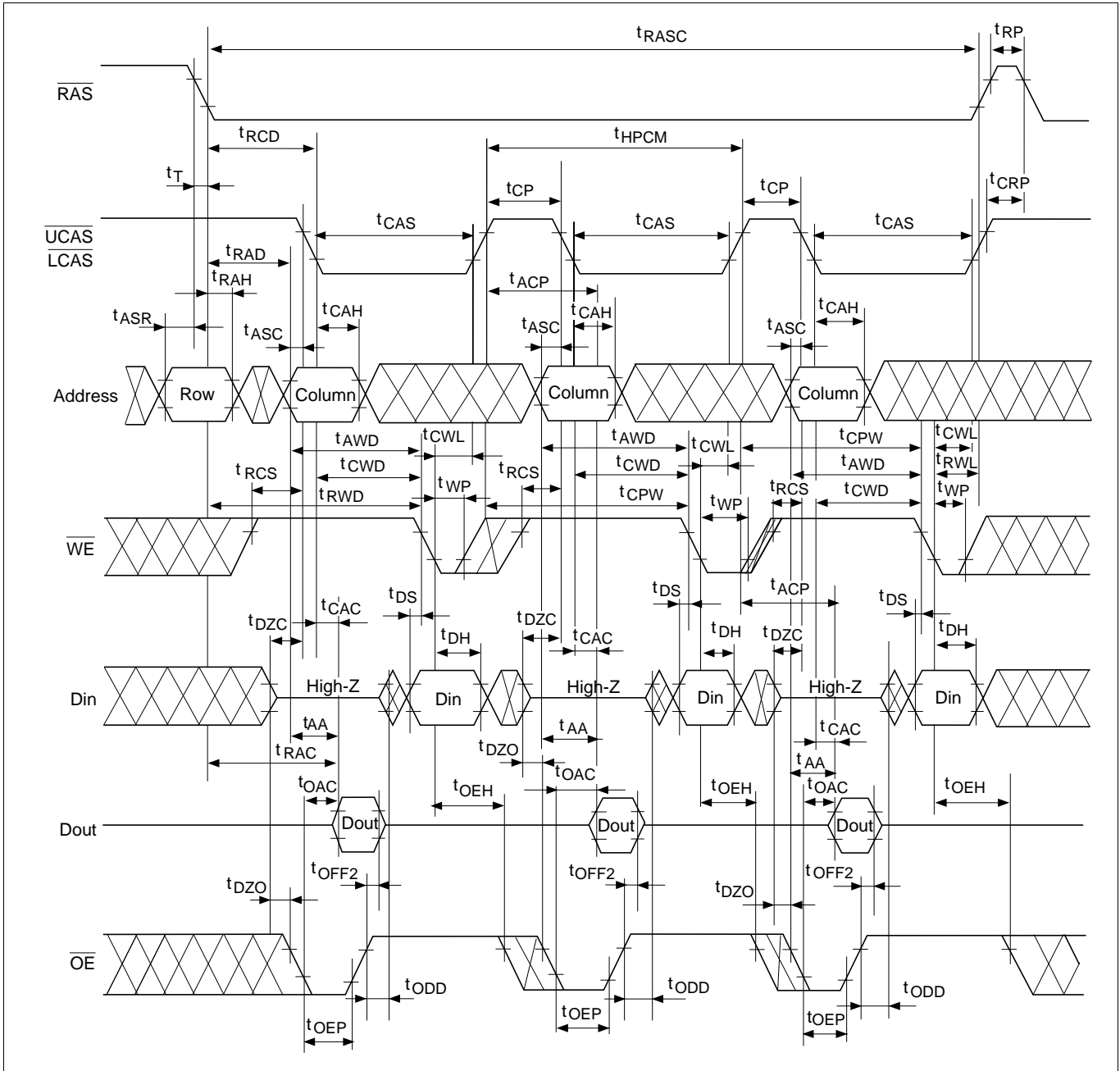
## EDO Page Mode Early Write Cycle ( $t_{HPC}$ minimum cycle operation)



EDO Page Mode Delayed Write Cycle

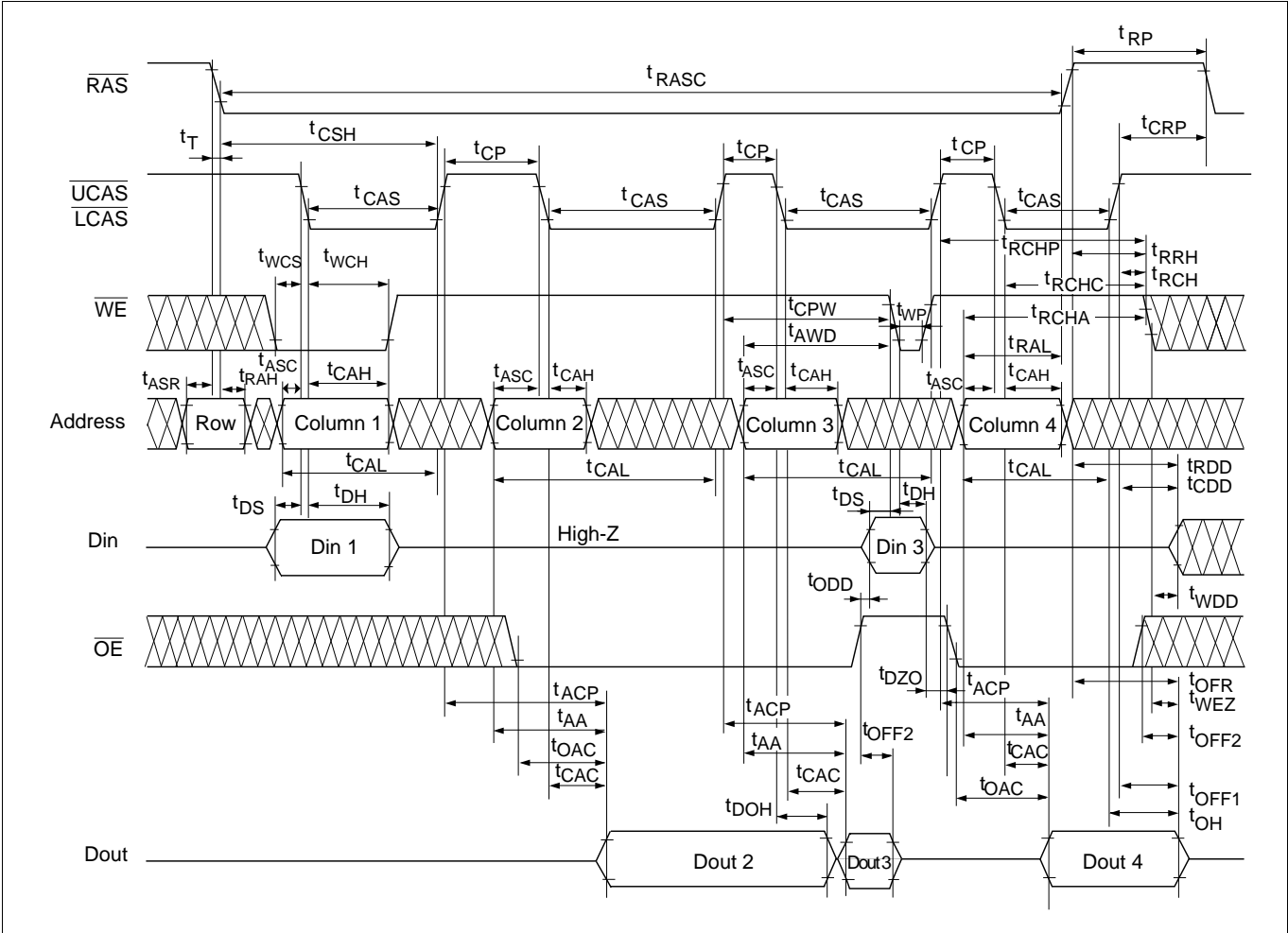


## EDO Page Mode Read-Modify-Write Cycle



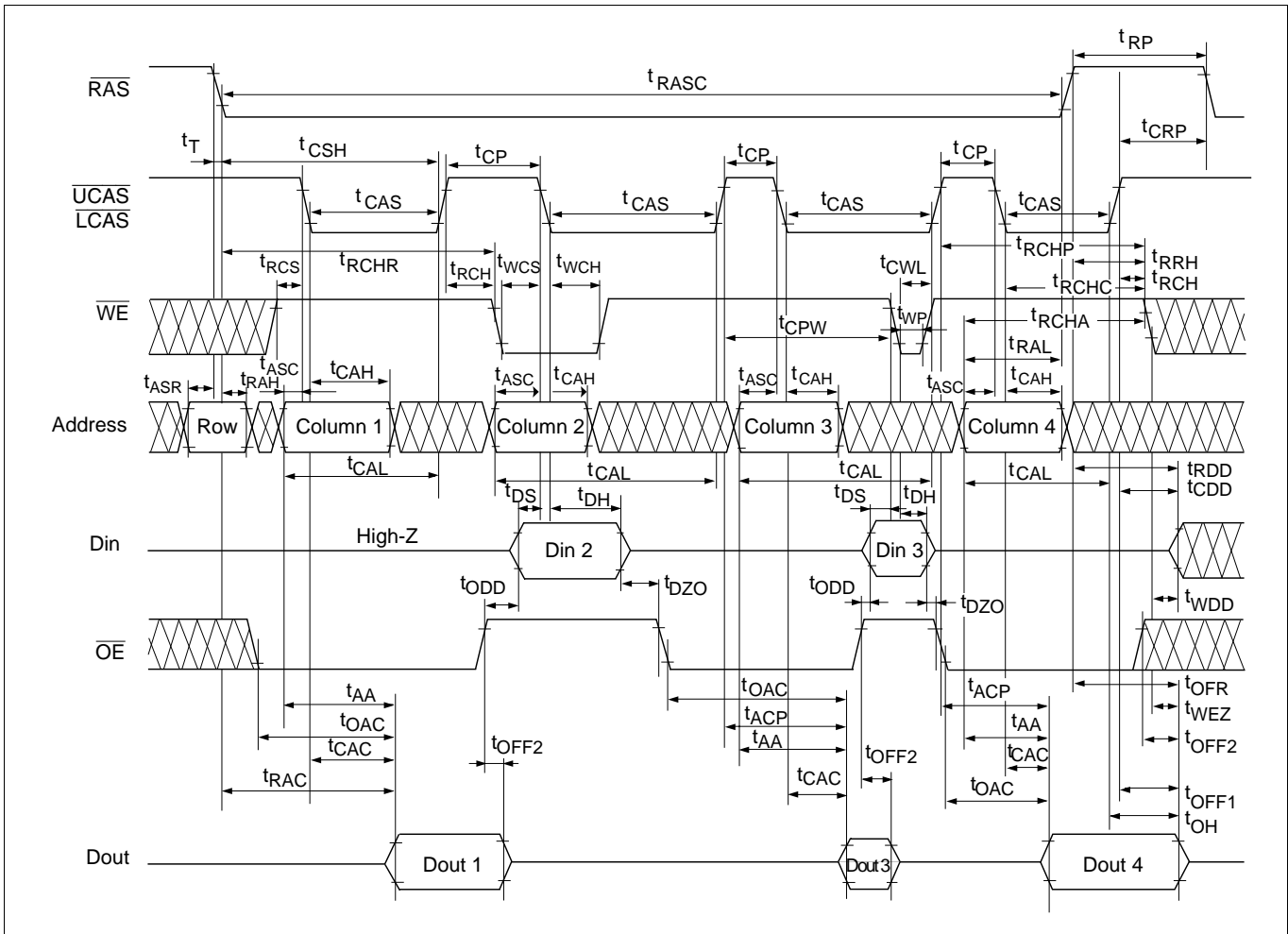


EDO Page Mode Mix Cycle (1)\*24

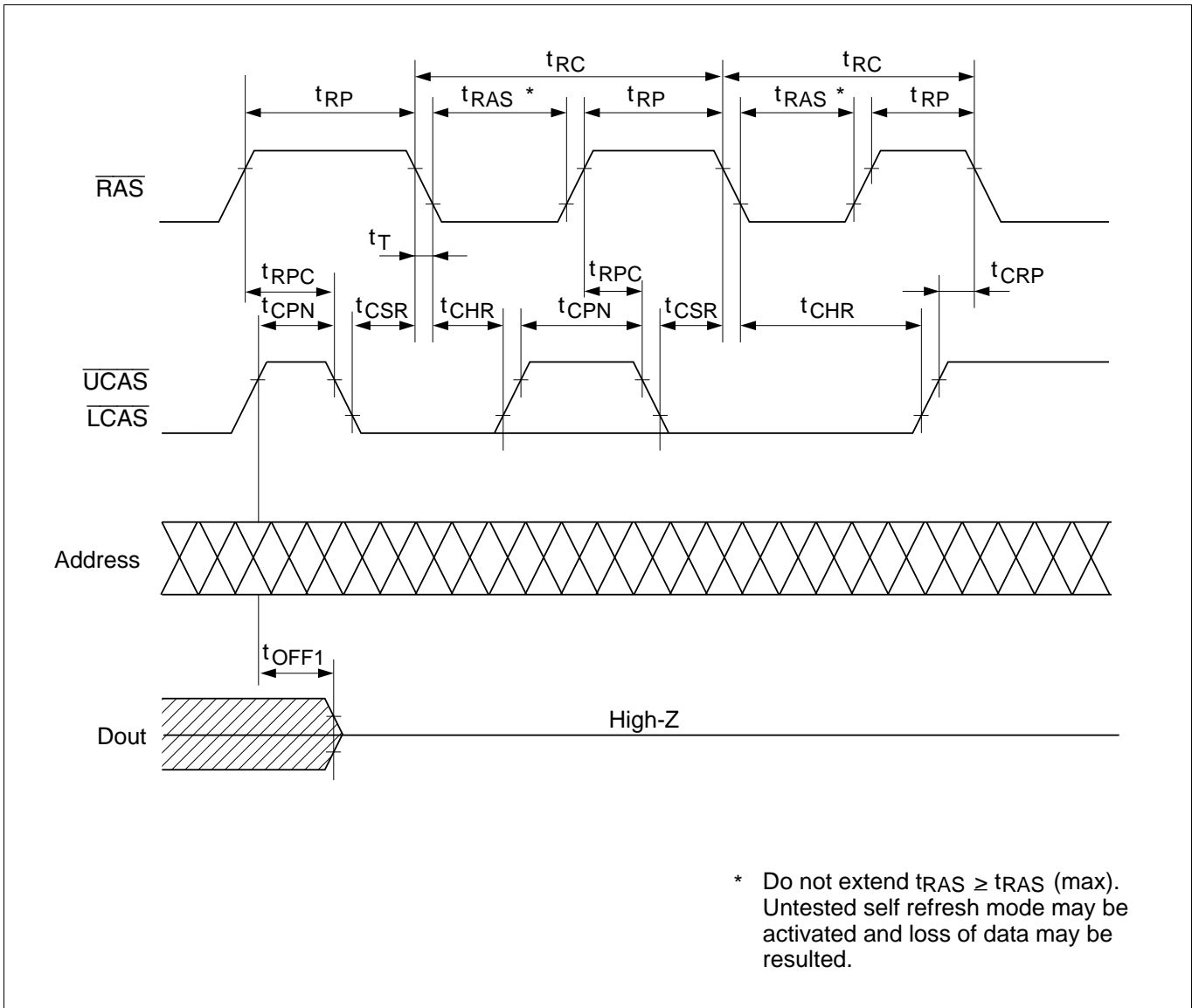


# HM51W4265C Series

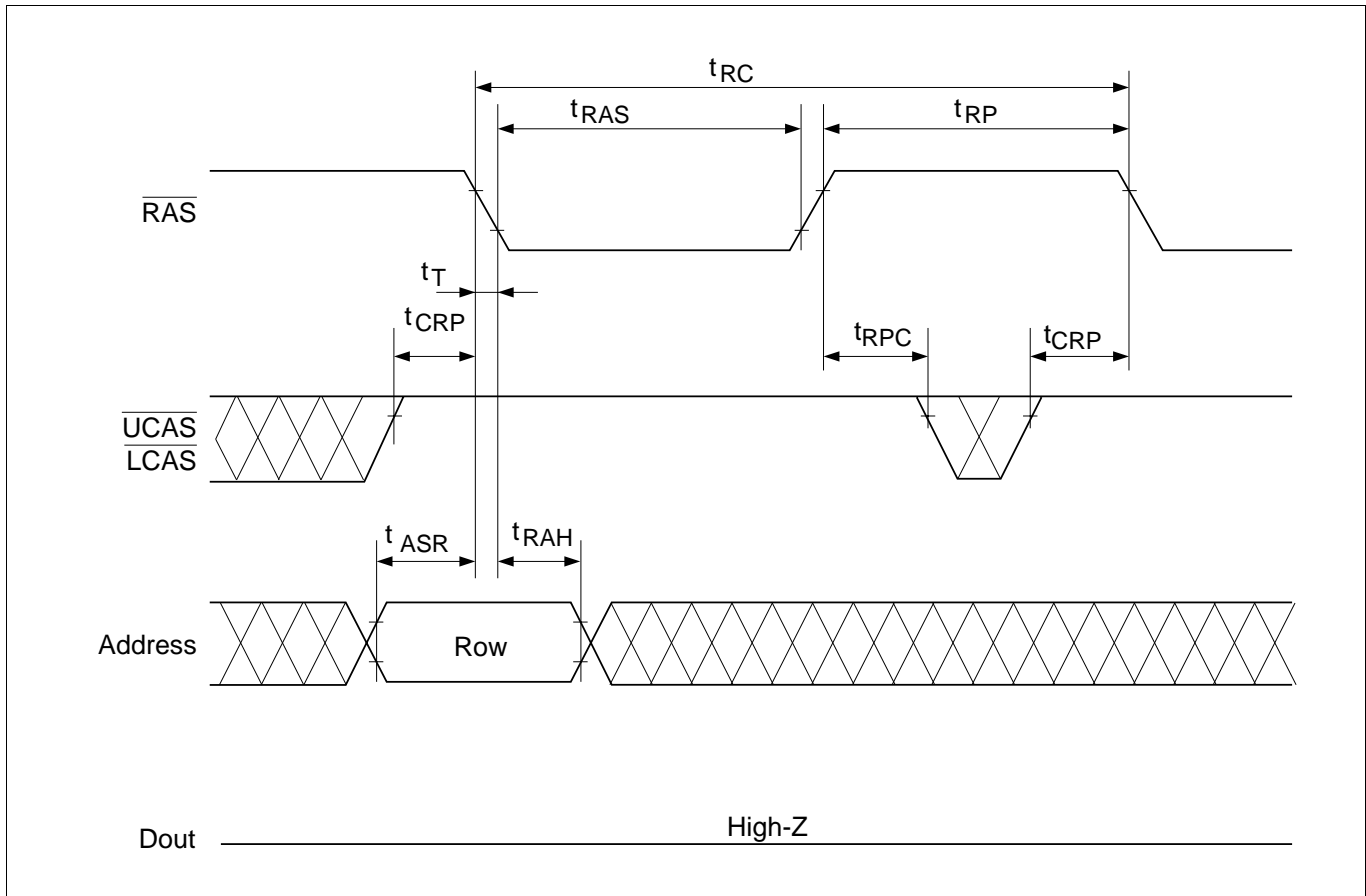
## EDO Page Mode Mix Cycle (2)\*24



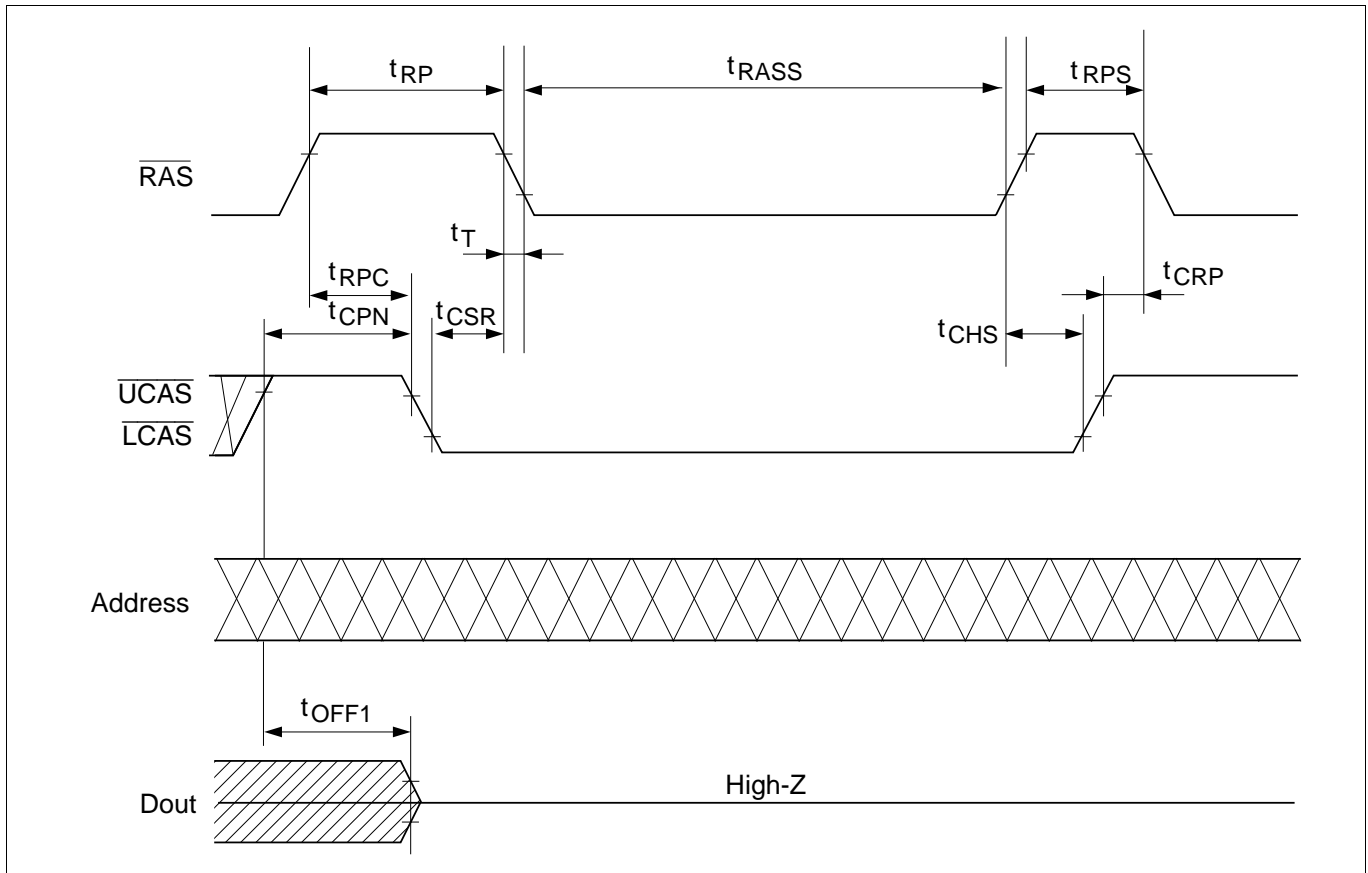
CAS-Before-RAS Refresh Cycle



## RAS-Only Refresh Cycle



Self Refresh Cycle\*30, 31, 32, 33

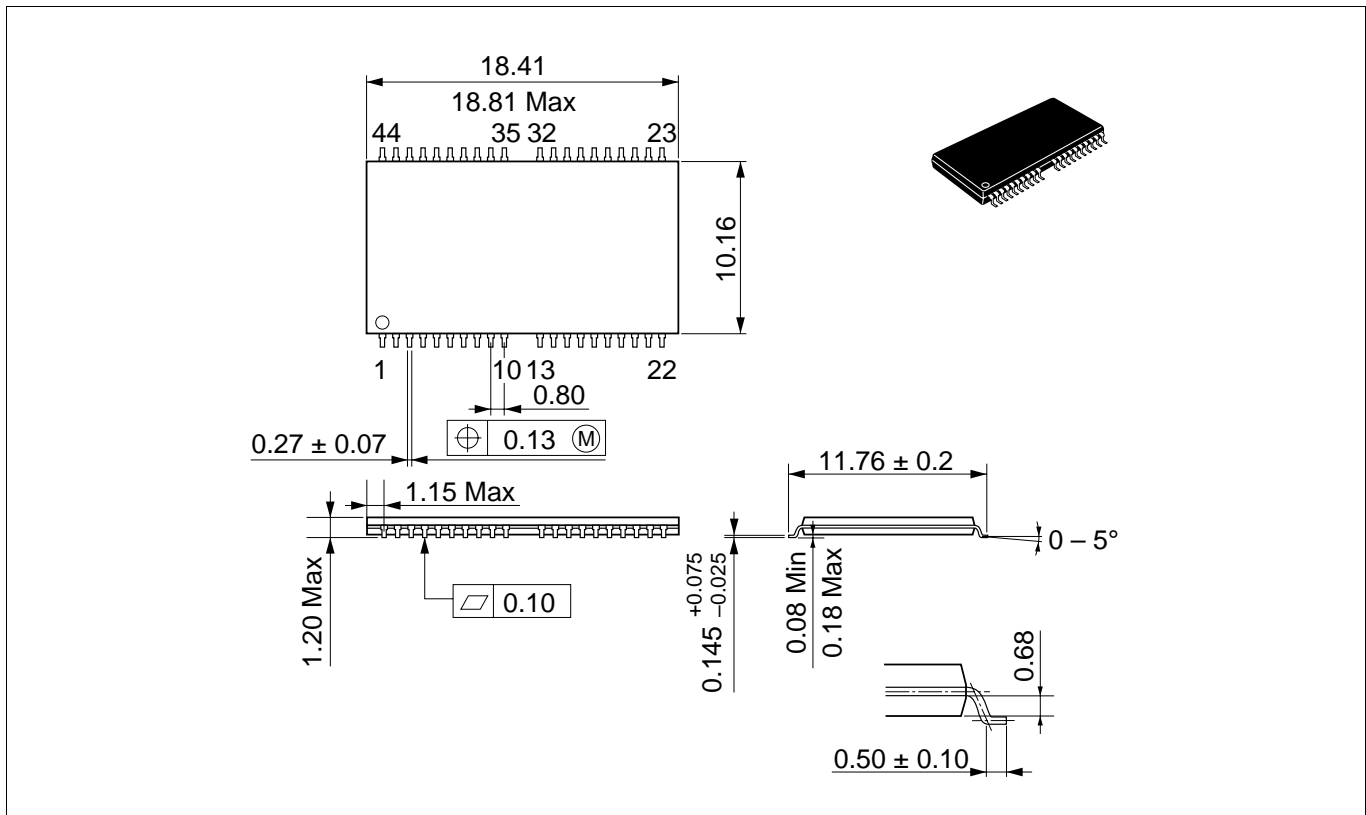


# HM51W4265C Series

## Package Dimensions

HM51W4265CTT/CLTT Series (TTP-44/40DB)

Unit: mm



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

---

---

# HITACHI

## **Hitachi, Ltd.**

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

### **For further information write to:**

Hitachi America, Ltd.  
Semiconductor & IC Div.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1835  
U S A  
Tel: 415-589-8300  
Fax: 415-583-4207

Hitachi Europe GmbH  
Electronic Components Group  
Continental Europe  
Dornacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 0628-585000  
Fax: 0628-778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 0104  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071

---

# HM51W4265C Series

---

## Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dec. 1, 1995	Initial issue	T. Oono	S. Suzuki
1.0	Jul. 31, 1996	Addition of HM51W4265C-6 Series AC Characteristics Change of note 25, 34 Addition of note 30 Notes concerning $\overline{2CAS}$ control Addition of note 4 Timing waveforms Deletion of notes about undefined pins. Early write cycle. EDO pagemode early write cycle. $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle. $\overline{RAS}$ - only refresh cycle. Self refresh cycle.		

---