EL4421, EL4422, EL4441, EL4442, EL4443, EL4444

January 1996, Rev. C FN7166

Multiplexed-Input Video Amplifiers

The EL44XX family of video multiplexed-amplifiers offers a very quick 8ns switching time and low glitch along with very low video distortion. The amplifiers have good gain accuracy even when driving low-impedance loads. To save power, the amplifiers do not require heavy loading to remain stable.

The EL4421 and EL4422 are two-input multiplexed amplifiers. The -inputs of the input stages are wired together and the device can be used as a pin-compatible upgrade from the MAX453.

The EL4441 and EL4442 have four inputs, also with common feedback. These may be used as upgrades of the MAX454.

The EL4443 and EL4444 are also 4-input multiplexed amplifiers, but both positive and negative inputs are wired separately. A wide variety of gain- and phase-switching circuits can be built using independent feedback paths for each channel.

The EL4421, EL4441, and EL4443 are internally compensated for unity-gain operation. The EL4422, EL4442, and EL4444 are compensated for gains of +2 or more, especially useful for driving back-matched cables.

The amplifiers have an operational temperature of -40°C to +85°C and are packaged in plastic 8- and 14-pin DIP and 8- and 14-pin SO.

The EL44XX multiplexed-amplifier family is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

Features

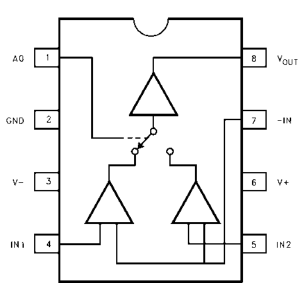
- Unity or + 2-gain bandwidth of 80MHz
- 70dB off-channel isolation at 4MHz
- Directly drives high-impedance or 75Ω loads
- 0.02% and 0.02° differential gain and phase errors
- 8ns switching time
- < 100mV switching glitch
- 0.2% loaded gain error
- Compatible with ±3V to ±15V supplies
- 160mW maximum dissipation at ±5V supplies

Ordering Information

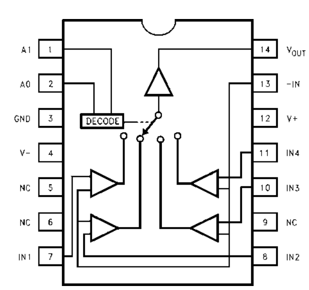
PART NIMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4421CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL4421CS	-40°C to +85°C	8-Pin SO	MDP0027
EL4422CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL4422CS	-40°C to +85°C	8-Pin SO	MDP0027
EL4441CN	-40°C to +85°C	14-Pin PDIP	MDP0031
EL4441CS	-40°C to +85°C	14-Pin SO	MDP0027
EL4442CN	-40°C to +85°C	14-Pin PDIP	MDP0031
EL4442CS	-40°C to +85°C	14-Pin SO	MDP0027
EL4443CN	-40°C to +85°C	14-Pin PDIP	MDP0031
EL4443CS	-40°C to +85°C	14-Pin SO	MDP0027
EL4444CN	-40°C to +85°C	14-Pin PDIP	MDP0031
EL4444CS	-40°C to +85°C	14-Pin SO	MDP0027

Pinouts

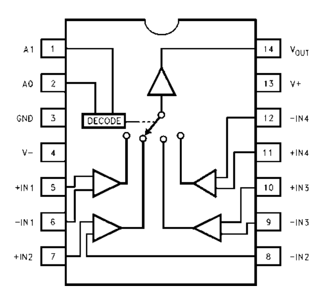
EL4421/EL4422
(8-PIN PDIP, SO)
TOP VIEW



EL4441/EL4442
(14-PIN PDIP, SO)
TOP VIEW



EL4443/EL4444
(14-PIN PDIP, SO)
TOP VIEW



Manufactured under U.S. Patent No. 5,352,987

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V
V_S	V+ to V- Supply Voltage	33V
V_{IN}	Voltage at any Input or Feedback	V+ to V-
V_{IN}	Difference between Pairs of Inputs or Feedback	6V
V_{LOGIC}	Voltage at A0 or A1	-4V to 6V
I_{IN}	Current into any Input, Feedback, or Logic Pin	4mA
I_{OUT}	Output Current	30mA
P_D	Maximum Power Dissipation	See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

Power supplies at ±5V, T_A = 25°C, R_L = 500Ω, unless otherwise specified

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	'21, '41, and '43	-9	±3	9	mV
		'22, '42, and '44	-7	±2	7	
I_B	Input Bias Current, Positive Inputs Only of the '21, '22, '41, '42, and All Inputs of the '43 and '44		-12	-5	0	µA
I_{FB}	Input Bias Currents of Common Feedback	'21 and '22	-24	-10	0	µA
		'41 and '42	-48	-20	0	µA
I_{OS}	Input Offset Currents of the '43 and '44			60	350	nA
E_G	Gain Error (Note 1)	'21 and '41 and '43		0.2	0.6	%
		'22, '42 and '44		0.1	0.6	V/V
A_{VOL}	Open-Loop Gain (Note 1)	EL4443	350	500		V/V
		EL4444	500	750		V/V
V_{IN}	Input Signal Range, EL4421 and EL4441 (Note 2)		±2.5	±3		V
CMRR	Common-Mode Rejection Ratio, EL4443 and EL4444		70	90		dB
PSRR	Power Supply Rejection Ratio V_S from ±5V to ±15V		60	70		dB
CMIR	Common-Mode Input Range EL4443 and EL4444 (Note 3)		±2.5	±3		V
V_{OUT}	Output Swing		±2.5	±3.5		V
I_{SC}	Output Short-Circuit Current		±40	±80		mA
F_T	Unselected Channel Feedthrough Attenuation (Note 1)	'21, '41, '43	70	80		dB
		'22, '42, '44	55	64		dB
I_{LOGIC}	Input Current at A0 and A1 with Input = 0V and 5V		-16	-8	0	µA
V_{LOGIC}	Logic Valid High and Low Input Levels		0.8		2.0	V
I_S	Supply Current	EL4421 and EL4422		11	14	mA
		EL4441, EL4442, EL4443, and EL4444	13	16		

NOTES:

1. The '21, '41, and '43 devices are connected for unity-gain operation with 75Ω load and an input span of ±1V. The '22, '42, and '44 devices are connected for a gain of +2 with a 150Ω load and a ±1V input span with $R_F = R_G$ = 270Ω.
2. The '21 and '41 devices are connected for unity gain with a ±3V input span while the output swing is measured.
3. CMIR is assured by passing the CMRR test at input voltage extremes.

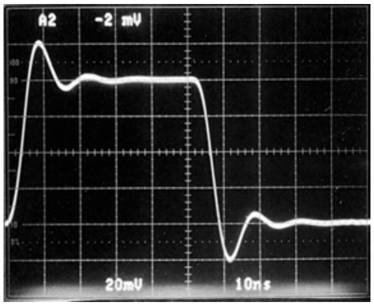
Closed-Loop AC Electrical Specifications

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3pF; for all C_L = 15pF

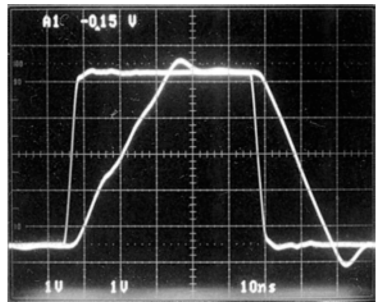
PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
BW - 3dB	-3dB Small-Signal Bandwidth	EL4421, '41, '43		80		MHz
		EL4422, '42, '44		65		MHz
BW ± 0.1dB	0.1dB Flatness Bandwidth			10		MHz
Peaking	Frequency Response Peaking			0.5		dB
SR	Slewrate, V_{OUT} between -2.5V and +2.5V, V_S = ±12V	EL4421, EL4441, EL4443	150	200		V/µsec
		EL4422, EL4442, EL4444	180	240		V/µsec
V_N	Input-Referred Noise Voltage Density	EL4421, EL4441, EL4443		18		nV/√Hz
		EL4422, EL4442, EL4444		14		nV/√Hz
d_G	Differential Gain Error, V_{OFFSET} between -0.7V and +0.7V	EL4421, '41, '43 (V_S = ±12V)		0.01		%
		EL4421, '41, '43 (V_S = ±5V)		0.10		%
		EL4422, '42, '44 (V_S = ±12V)		0.02		%
		EL4422, '42, '44 (V_S = ±5V)		0.11		%
$d_Ø$	Differential Phase Error, V_{OFFSET} between -0.7V and +0.7V	EL4421, '41, '43 (V_S = ±12V)		0.01		°
		EL4421, '41, '43 (V_S = ±5V)		0.1		°
		EL4422, '42, '44 (V_S = ±12V)		0.02		°
		EL4422, '42, '44 (V_S = ±5V)		0.15		°
T_{MUX}	Multiplex Delay Time, Logic Threshold to 50% Signal Change	EL4421, '22		8		nsec
		EL4441, '42, '43, '44		12		nsec
V_{GLITCH}	Peak Multiplex Glitch	EL4421, '22		70		mV
		EL4441, '42, '43, '44		100		mV
ISO	Channel Off Isolation at 3.58MHz (See Text)	EL4421, EL4441, EL4443		76		dB
		EL4422, EL4442, EL4444		63		dB

Typical Performance Curves

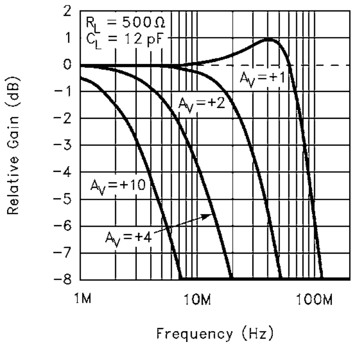
EL4421, EL4441, and EL4443
Small-Signal Transient Response
V_S = ±5V, R_L = 500Ω



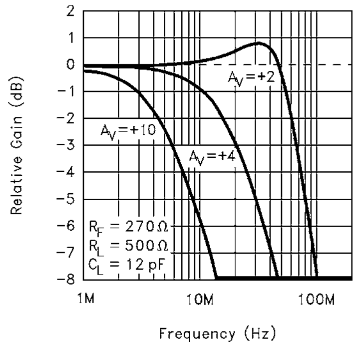
EL4421, EL4441, and EL4443
Large-Signal Response
V_S = ±12V, R_L = 500Ω



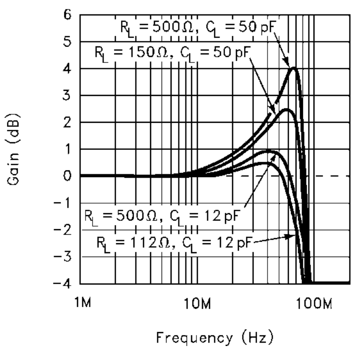
EL4421, EL4441, and EL4443
Frequency Response for
Various Gains



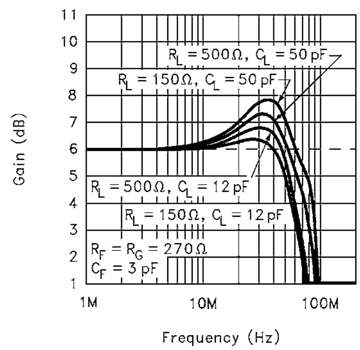
EL4422, EL4442, and EL4444
Frequency Response for
Various Gains



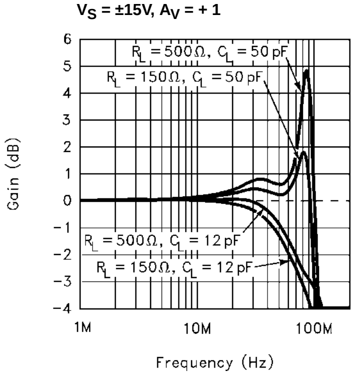
EL4421, EL4441, and EL4443
Frequency Response for Various Loads
V_S = ±5V, A_V = +1



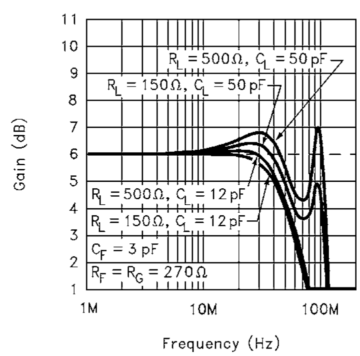
EL4422, EL4442, and EL4444
Frequency Response for Various Loads
V_S = ±5V, A_V = +2



Frequency Response
for Various Loads
V_S = ±15V, A_V = + 1

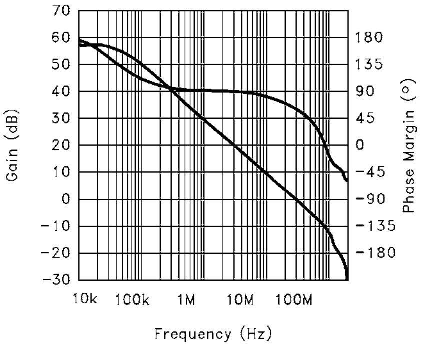


EL4422, EL4442, and EL4444
Frequency Response for Various Loads
V_S = ±15V, A_V = +2

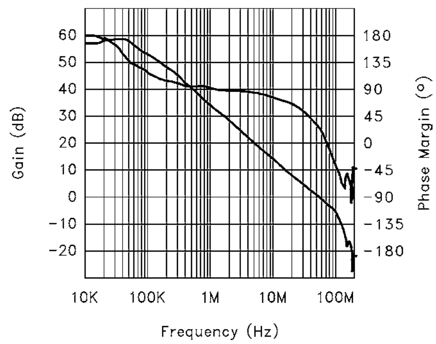


Typical Performance Curves (Continued)

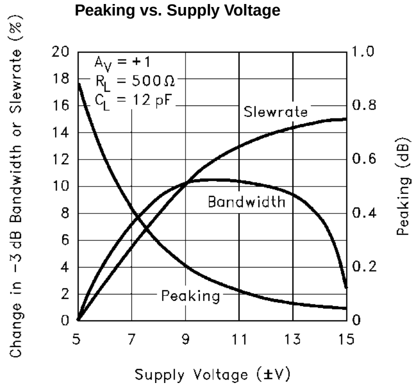
EL4443 Open-Loop Gain and Phase vs. Frequency



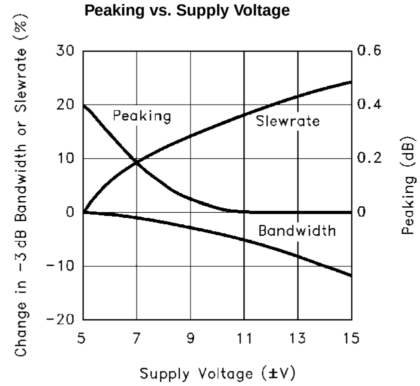
EL4444 Open-Loop Gain and Phase vs. Frequency



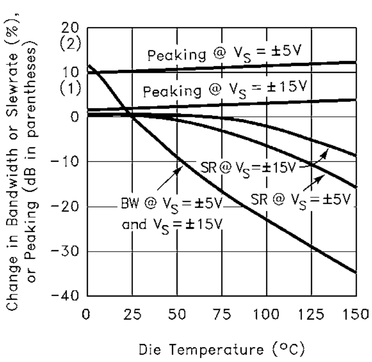
EL4421, EL4441, and EL4443 -3dB Bandwidth, Slewrate, and Peaking vs. Supply Voltage



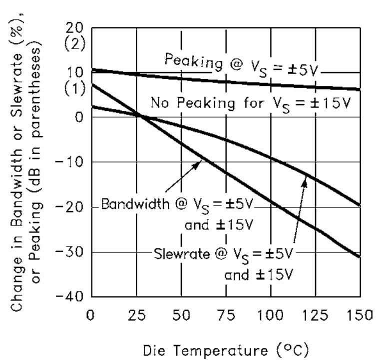
EL4422, EL4442, and EL4444 -3dB Bandwidth, Slewrate, and Peaking vs. Supply Voltage



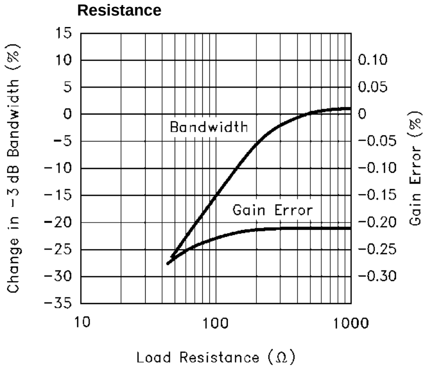
EL4421, EL4441, and EL4443 Bandwidth, Slewrate, and Peaking vs. Temperature, $A_V = +1$, $R_L = 500\Omega$



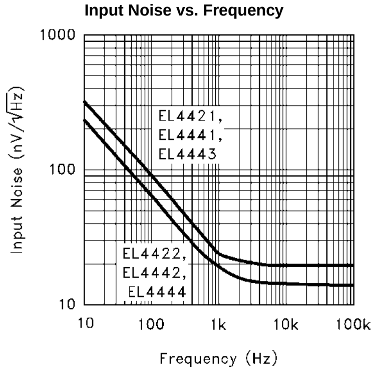
EL4422, EL4442, and EL4444 Bandwidth, Slewrate, and Peaking vs. Temperature, $A_V = +2$, $R_L = 150\Omega$, $R_I = R_G = 270\Omega$, $C_F = 3pF$



EL4421, EL4441, and EL4443 -3dB Bandwidth and Gain Error vs. Load Resistance

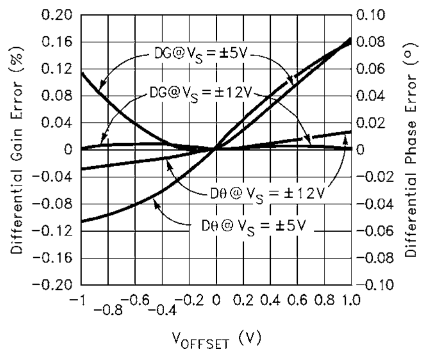


Input Noise vs. Frequency

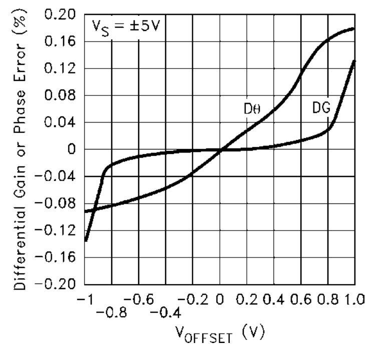


Typical Performance Curves (Continued)

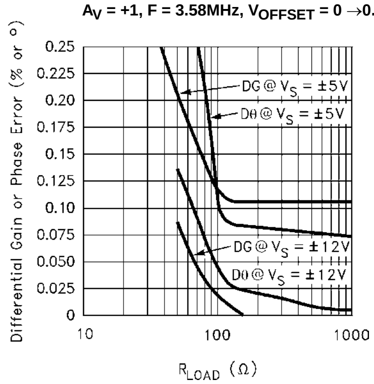
EL4421, EL4441, and EL4443 Differential Gain and Phase Errors, vs. Input Offset, A_V = +1, R_L = 500Ω, F = 3.58MHz



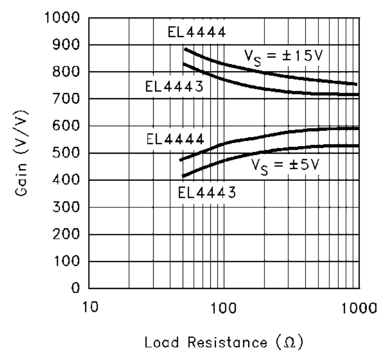
EL4422, EL4442, and EL4444 Differential Gain and Phase Error vs. Input Offset; A_V = +2, R_L = 150Ω, F = 3.58MHz



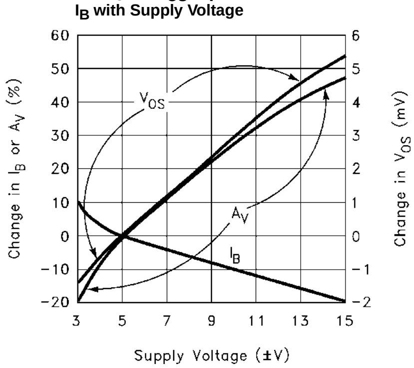
EL4421, EL4441, and EL4443 Differential Gain and Phase Error vs. Load Resistance; A_V = +1, F = 3.58MHz, V_{OFFSET} = 0 →0.714V



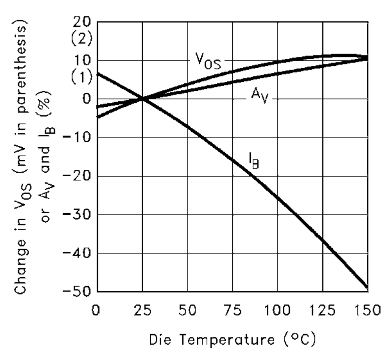
EL4443 and EL4444 Open-Loop Gain vs. Load Resistance



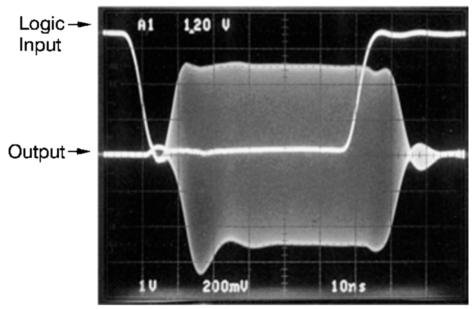
Change in V_{OS}, A_V, and I_B with Supply Voltage



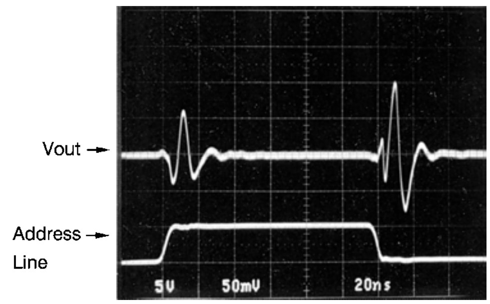
Change in V_{OS}, I_B, and A_V vs. Temperature



Switching Waveforms Switching from Grounded Input to Uncorrelated Sinewave and Back

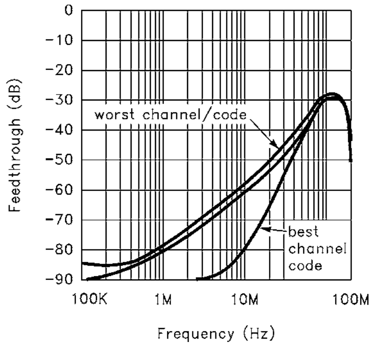


Channel-to-Channel Switching Glitch

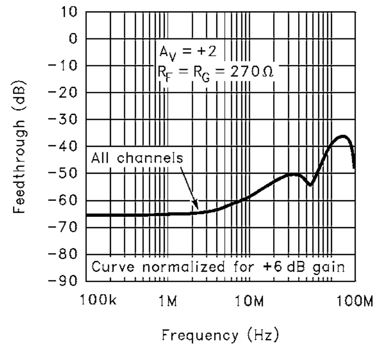


Typical Performance Curves (Continued)

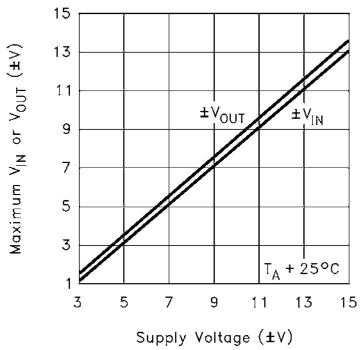
EL4421, EL4441, and EL4443
Unselected Channel
Feedthrough vs. Frequency



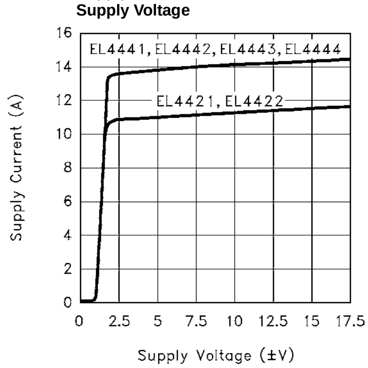
EL4422, EL4442, and EL4444
Unselected Channel
Feedthrough vs. Frequency



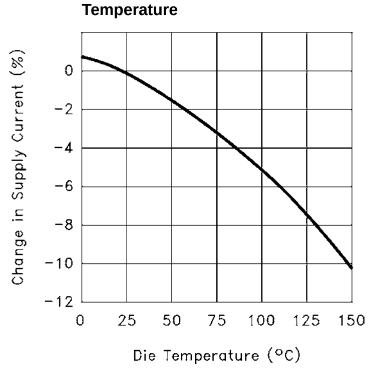
EL4443 and EL4444
Input and Output Range vs.
Supply Voltage (Output Unloaded)



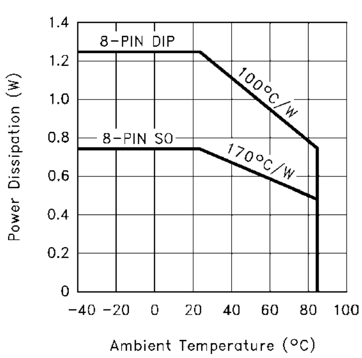
Supply Current vs.
Supply Voltage



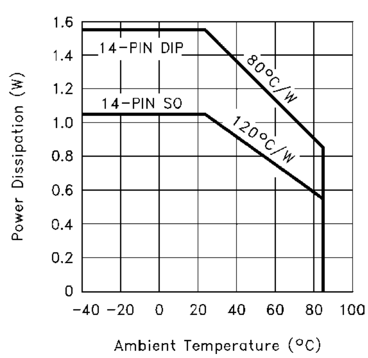
Supply Current vs.
Temperature



8-Pin Package
Power Dissipation vs.
Ambient Temperature



14-Pin Package
Power Dissipation vs.
Ambient Temperature



Applications Information

General Description

The EL44XX family of video mux-amps are composed of two or four input stages whose inputs are selected and control an output stage. One of the inputs is active at a time and the circuit behaves as a traditional voltage-feedback op-amp for that input, rejecting signals present at the unselected inputs. Selection is controlled by one or two logic inputs.

The EL4421, EL4422, EL4441, and EL4442 have all -inputs wired in parallel, allowing a single feedback network to set the gain of all inputs. These devices are wired for positive gains. The EL4443 and EL4444, on the other hand, have all +inputs and -inputs brought out separately so that the input stage can be wired for independent gains and gain polarities with separate feedback networks.

The EL4421, EL4441, and EL4443 are compensated for unity-gain stability, while the EL4422, EL4442, and EL4444 are compensated for a fed-back gain of +2, ideal for driving back-terminated cables or maintaining bandwidth at higher fed-back gains.

Switching Characteristics

The logic inputs work with standard TTL levels of 0.8V or less for a logic 0 and 2.0V or more for a logic 1, making them compatible for TTL and CMOS drivers. The ground pin is the logic threshold biasing reference. The simplified input circuitry is shown in Figure 1 below.

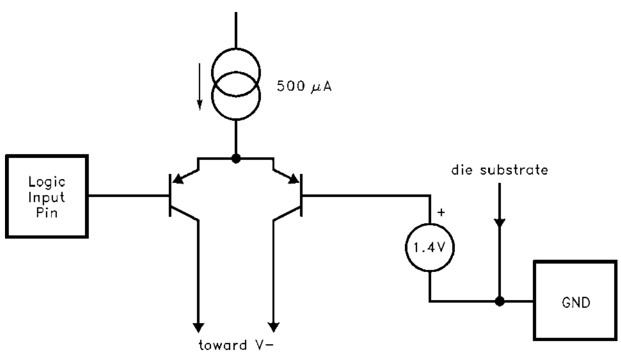


FIGURE 1. SIMPLIFIED LOGIC INPUT CIRCUITRY

The ground pin draws a maximum DC current of 6µA, and may be biased anywhere between (V-) +2.5V and (V+) -3.5V. The logic inputs may range from (V-)+2.5V to V+, and are additionally required to be no more negative than V(Gnd pin)-4V and no more positive than V(Gnd pin)+6V.

For example, within these constraints, we can power the EL44XX's from +5V and +12V without a negative supply by using these connections.

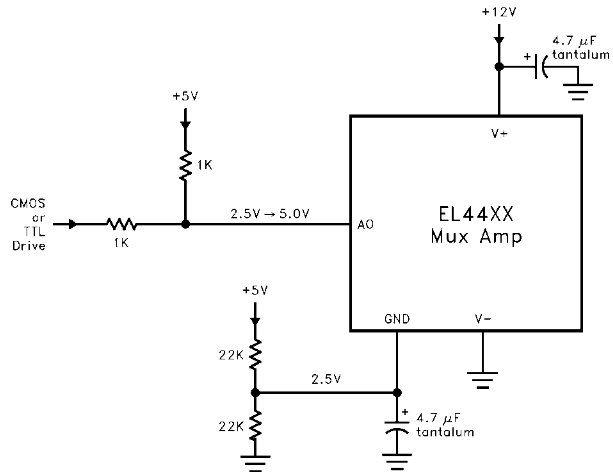


FIGURE 2. USING THE EL44XX MUX AMPS WITH +5V AND +12V SUPPLIES

The logic input(s) and ground pin are shifted 2.5V above system ground to correctly bias the mux-amp. Of course, all the signal inputs and output will have to be shifted 2.5V above system ground to ensure proper signal path biasing.

A final caution: the ground pin is also connected to the IC's substrate and frequency compensation components. The ground pin must be returned to system ground by a short wire or nearby bypass capacitor. In Figure 2, the 22kΩ resistors also serve to isolate the bypassed ground pin from the +5V supply noise.

Signal Amplitudes

Signal input and output voltages must be between (V-)+2.5V and (V+)-2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. In unity-gain connections, any input could have ±3V applied and the output would be at ±3V, putting us at our 6V differential limit. Higher-gain circuit applications divide the output voltage and allow for larger outputs. For instance, at a gain of +2 the maximum input is again ±3V and the output swing is ±6V. The EL4443 or EL4444 can be wired for inverting gain with even more amplitude possible.

The output and positive inputs respond to overloading amplitudes correctly; that is, they simply clamp and remain monotonic with increasing +input overdrive. A condition exists, however, where the -input of an active stage is overdriven by large outputs. This occurs mainly in unity-gain connections, and only happens for negative inputs. The overloaded input cannot control the feedback loop correctly and the output can become non-monotonic. A typical scenario has the circuit running on ±5V supplies, connected for unity gain, and the input is the maximum ±3V. Negative input extremes can cause the output to jump from -3V to around -2.3V. This will never happen if the input is restricted to ±2.5V, which is the guaranteed maximum input compliance with ±5V supplies, and is not a problem with greater supply voltages. Connecting the feedback network with a divider will prevent the overloaded output voltage from being large enough to overload the -input and monotonic behavior is assured. In any event, keeping signals within guaranteed compliance limits will assure freedom from overload problems.

The input and output ranges are substantially constant with temperature.

Power Supplies

The mux-amps work well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Switching Characteristics section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7µF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01µF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used as described in the Switching Characteristics section. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the mux-amps increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2V_S \times I_S,max + (V_S - V_O) \times V_O / R_{PAR}$$

Where

I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4422 draws a maximum of 14mA and we might require a 2V peak output into 150Ω and a 270Ω +270Ω feedback divider. The R_{PAR} is 117Ω. The dissipation with ±5V supplies is 191mW. The maximum Supply voltage that the device can run on for a given P_D and the other parameter is

$$V_S, max = (P_D + V_O^2/R_{PAR})/2I_S + V_O/R_{PAR})$$

The maximum dissipation a package support is

$$P_D, max = (T_D, max - T_A, max)/R_{TH}$$

Where

T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70° for commercial and 85°C for industrial range

R_{TH} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The most difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°, the 65° temperature rise and package thermal resistance of 170°/W gives a maximum dissipation of 382mW. This allows a maximum supply voltage of ±9.2V for the EL4422 operated in our example. If the EL4421 were driving a light load ($R_{PAR} \rightarrow \infty$), it could operate on ±15V supplies at a 70° maximum ambient.

The EL4441 through EL4444 can operate on ±12V supplies in the SO package, and all parts can be powered by ±15V supplies in DIP packages.

Output Loading

The output stage of the mux-amp is very powerful, and can source 80mA and sink 120mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion only a bit, becoming noticeably worse for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5dB with even a 220pF load.

Input Connections

The input transistors can be driven from resistive and capacitive sources but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6 of unterminated input transmission line. The oscillation has a characteristic frequency of 500MHz.

Often simply placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the mux-amp input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Feedback Connections

A feedback divider is used to increase circuit gain, and some precautions should be observed. The first is that parasitic capacitance at the -input will add phase lag to the feedback path and increase frequency response peaking or even cause oscillation. One solution is to choose feedback resistors whose parallel value is low. The pole frequency of the feedback network should be maintained above at least 200MHz. For a 3pF parasitic, this requires that the feedback divider have less than 265Ω impedance, equivalent to two 510Ω resistors when a gain of +2 is desired. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should match the parasitic capacitance at the -input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10pF capacitors across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

The other major concern about the divider concerns unselected-channel crosstalk. The differential input impedance of each input stage is around 200kΩ. The unselected input's signal sources thus drive current through that input impedance into the feedback divider, inducing an unwanted output. The gain from unselected input to output, the crosstalk attenuation, if R_F/R_{IN}. In unity-gain connection the feedback resistor is 0Ω and very little crosstalk is induced. For a gain of +2, the crosstalk is about -60dB.

Feedthrough Attenuation

The channels have different crosstalk levels with different inputs. Here is the typical attenuation for all combinations of inputs for the mux-amps at 3.58MHz:

FEEDTHROUGH OF EL4441 AND EL4443 AT 3.58MHz

SELECT INPUTS, A1 A0	IN1	IN2	IN3	IN4
00	Selected	-77dB	-90dB	-92dB
01	-80dB	Selected	-77dB	-90dB
10	-101dB	-76dB	Selected	-66dB
11	-96dB	-84dB	-66dB	Selected

FEEDTHROUGH OF EL4421 AT 3.58MHz

CHANNEL SELECT INPUT, A0	IN1	IN2
0	Selected	-88dB
1	-93dB	Selected

Switching Glitches

The output of the mux-amps produces a small “glitch' voltage in response to a logic input change. A peak amplitude of only about 90mV occurs, and the transient settles out in 20ns. The glitch does not change amplitude with different gain settings.

With the four-input multiplexers, when two logic inputs are simultaneously changed, the glitch amplitude doubles. The increase can be a avoided by keeping transitions at least 6ns apart. This can be accomplished by inserting one gate delay in one of the two logic inputs when they are truly synchronous.