Data Sheet | January 1996, Rev E | FN7044

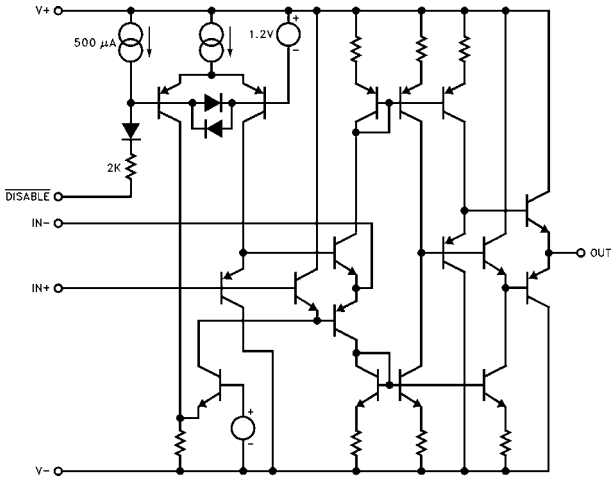
100MHz Current Feedback Amplifier

The EL2120 is a wideband current feedback amplifier optimized for video performance. Its 0.01% differential gain and 0.03 degree differential phase performance when at ±5V supplies exceeds the performance of other amplifiers running on ±15V supplies. Operating on ±8 to ±15V supplies reduces distortions to 0.01% and 0.01 degrees and below. The EL2120 can operate with supplies as low as ±2.5V or a single +5V supply.

Being a current feedback design, bandwidth is a relatively constant 100MHz over the ±1 to ±10 gain range. The EL2120 has been optimized for flat gain over frequency and all characteristics are maintained at positive unity gain. Because the input slew rate is similar to the 700V/µs output slew rate the part makes an excellent high-speed buffer.

The EL2120 has a superior output disable function. Time to enable or disable is 50ns and does not change markedly with temperature. Furthermore, in disable mode the output does not draw excessive currents when driven with 1000V/µs slew rates. The output appears as a 3pF load when disabled.

Simplified Schematic



Features

- Excellent differential gain and phase on ±5V to ±15V supplies
- 100MHz -3dB bandwidth from gains of ±1 to ±10
- 700V/µs slew rate
- 0.1dB flatness to 20MHz
- Output disable in 50ns - remains high impedance even when driven with large slew rates
- Single +5V supply operation
- AC characteristics are lot and temperature stable
- Available in small SO-8 package

Applications

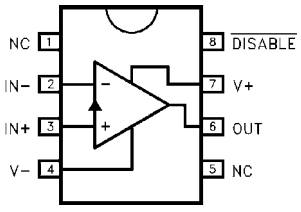
- Video gain block
- Residue amplifier
- Multiplexer
- Current to voltage converter
- Coax cable driver with gain of 2
- ADC driver

Ordering Information

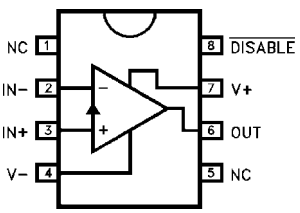
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2120CN	0°C to +75° C	8-Pin PDIP	MDP0031
EL2120CS	0°C to +75° C	8-Pin SO	MDP0027

Pinouts

EL2120 (8-PIN PDIP)
TOP VIEW



EL2120 (8-PIN SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V- 33V
Voltage at +IN, -IN, V_{OUT} . . . . . (V-) - 0.5V to (V+) + 0.5V
Voltage between +IN and -IN . . . . . .±5V
Voltage at /Disable . . . . . (V+) - 10V to (V+) + 0.5V
Current into +IN, -IN, and /Disable . . . . . ±5mA
Output Current . . . . . ±50mA
Internal Power Dissipation . . . . . See Curves
Operating Ambient Temperature Range . . . . . .0° to 7 5°C
Operating Junction Temperature PDIP or SO . . . . . 150°C
Storage Temperature Range . . . . . .-65°C to +15 0°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

V_S = ±5V; R_L = 150Ω, T_A = 25° C unless otherwise specified

PARAMETER	DESCRIPTION	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage V_S = ±15V	Full Full		4 2	20 25	mV mV
V_{OS}/T	Input Offset Drift	Full		20		µV/°C
I_{B+}	$+V_{IN}$ Input Bias Current	Full		5	15	µA
I_{B-}	$-V_{IN}$ Input Bias Current	Full		10	50	µA
CMRR	Common-Mode Rejection (Note 1)	Full	50	55		dB
-ICMR	-Input Current Common-Mode Rejection (Note 1)	Full		8	20	µA/V
PSRR	Power Supply Rejection (Note 2)	Full	65	80		dB
+IPSR	+Input Current Power Supply Rejection (Note 2)	25° C		0.03		µA/V
-IPSR	-Input Current Power Supply Rejection (Note 2)	Full		0.6	5	µA/V
R_{OL}	Transimpedance	Full	70	140		kΩ
A_{VOL}	Voltage Gain	Full	58	66		dB
$+R_{IN}$	$+V_{IN}$ Input Impedance	25° C		2		MΩ
V_{IN}	$+V_{IN}$ Range	Full	±3.0	±3.5		V
V_O	Output Voltage Swing	Full	±3.0	±3.5		V
I_{SC}	Output Short-Circuit Current	25° C		100		mA
$I_{O,DIS}$	Output Current, Disabled	Full		5	50	µA
$V_{DIS,ON}$	Disable Pin Voltage for Output Enabled	Full	(V+) - 1			V
$V_{DIS,OFF}$	Disable Pin Voltage for Output Disabled	Full			(V+) - 4	V
$I_{DIS,ON}$	Disable Pin Current for Output Enabled	Full			5	µA
$I_{DIS,OFF}$	Disable Pin Current for Output Disabled	Full	1.0			mA
I_S	Supply Current (V_S = ±15V)	Full		17	20	mA

NOTES:

1. The input is moved from -3V to +3V
2. The supplies are moved from ±5V to ±15V

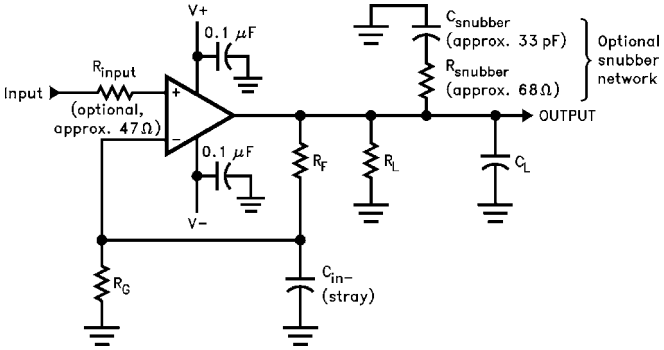
Closed-Loop AC Electrical Specifications

V_S = ±15V; A_V = +2 (R_F = R_G = 270Ω); R_L = 150Ω; C_L = 7pF; C_{IN-} = 2pF; T_A = 25°C

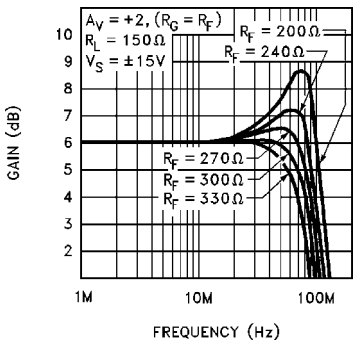
PARAMETER	DESCRIPTION	MIN	TYP	MAX LEVEL	UNITS
SR	Slew Rate; V_{OUT} from -3V to +3V Measured at -2V and +2V				
	V_S = ±15V		750		V/µs
	V_S = ±5V		550		V/µs
t_S	Settling Time to 0.25% of a 0 to +10V Swing; A_V = +1 with R_F = 270Ω, R_G = ×, and R_L = 400Ω		50		ns
BW	Bandwidth -3dB		95		MHz
	±1dB		50		MHz
	±0.1dB		16		MHz
BW@2.5V	Bandwidth at -3dB		75		MHz
	V_S = ±2.5V ±1dB		35		MHz
	±0.1dB		11		MHz
Peaking			0.5		dB
dG	Differential Gain; DC Offset from -0.7V through +0.7V, AC Amplitude 286 mVp–p				
	V_S = ±15V, f = 3.58MHz		<0.01		%
	V_S = ±15V, f = 30MHz		0.1		%
	V_S = ±5V, f = 3.58MHz		0.01		%
dθ	Differential Phase; DC Offset from -0.7V through +0.7V, AC Amplitude 286 mVp–p				
	V_S = ±15V, f = 3.58MHz		0.01		°
	V_S = ±15V, f = 30MHz		0.1		°
	V_S = ±5V, f = 3.58MHz		0.06		°

Typical Performance Curves

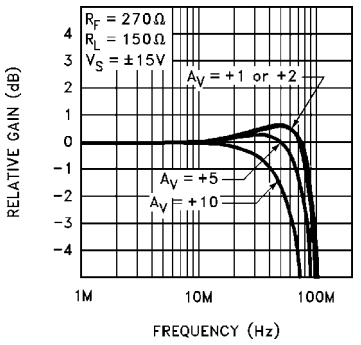
AC Test Circuit



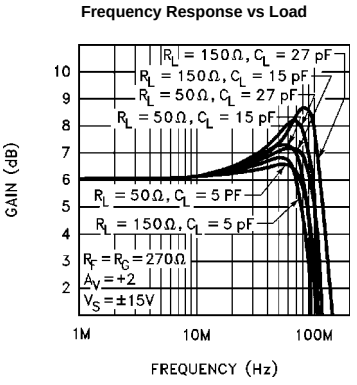
Frequency Response vs R_F



Frequency Response vs Gain

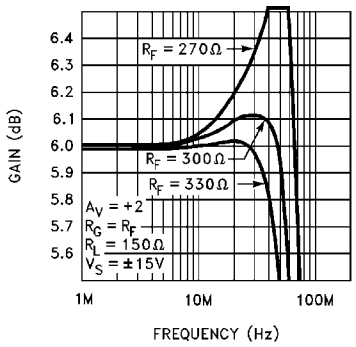


Frequency Response vs Load

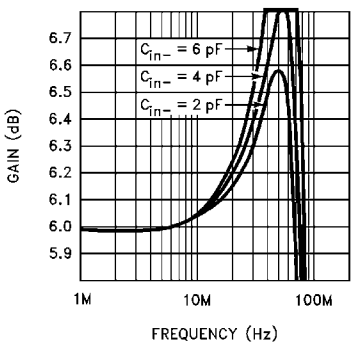


Typical Performance Curves (Continued)

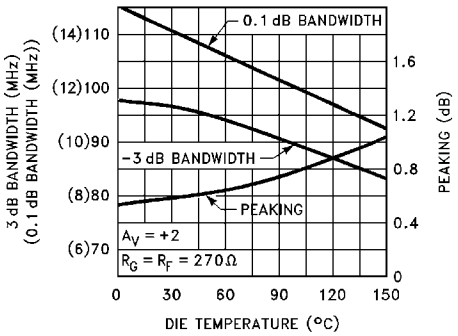
Gain Flatness vs R_F



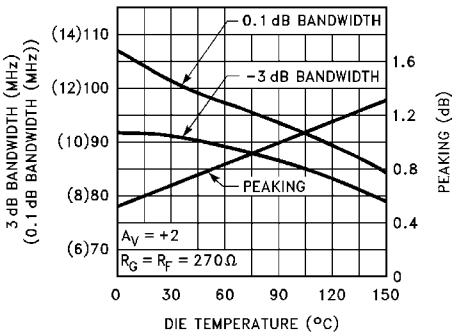
Gain Flatness vs C_{IN-}



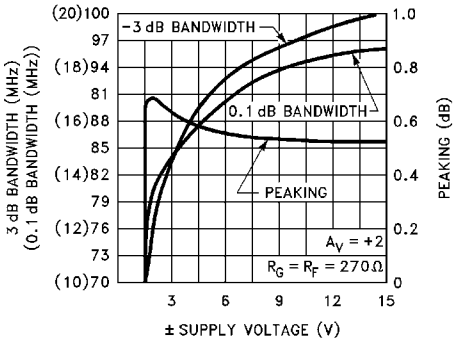
-3dB Bandwidth, 0.1dB Bandwidth, and Peaking vs Temperature at V_S ±15V



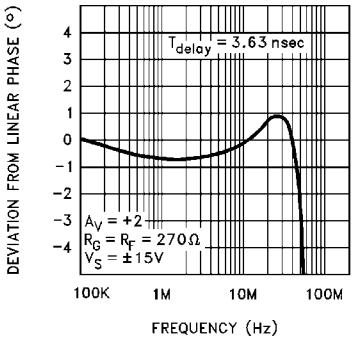
-3dB Bandwidth, 0.1dB Bandwidth, and Peaking vs Temperature at V_S ±5V



-3dB Bandwidth, 0.1dB Bandwidth, and Peaking vs Supply Voltage

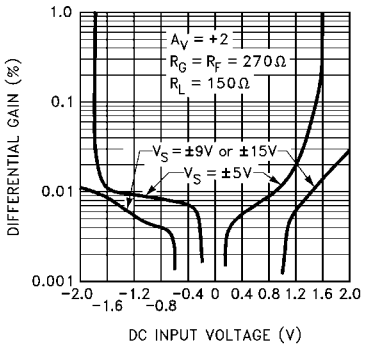


Deviation From Linear Phase vs Frequency

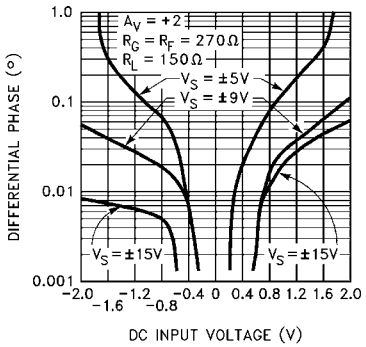


Typical Performance Curves (Continued)

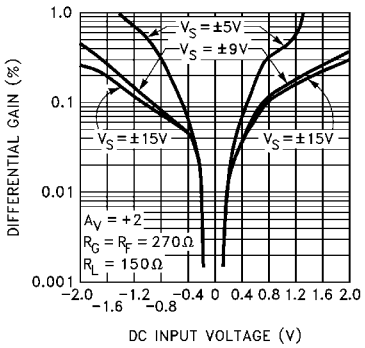
Differential Gain vs DC Input Offset at 3.58MHz



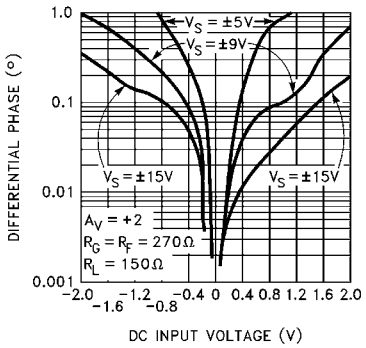
Differential Phase vs DC Input Offset at 3.58MHz



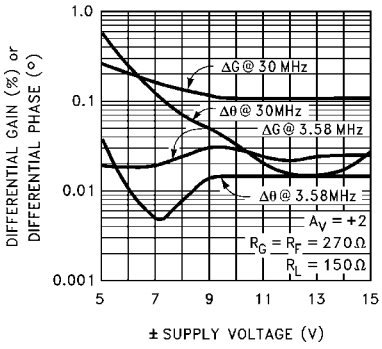
Differential Gain vs DC Input Offset at 30MHz



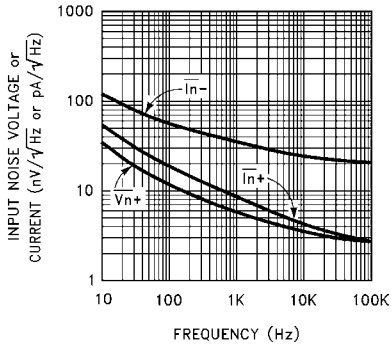
Differential Phase vs DC Input Offset at 30MHz



Differential Gain and Phase vs Supply Voltage (V_{IN}, DC from 0 to +0.7V)

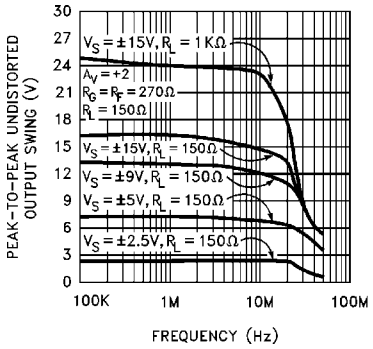


Input Noise Voltage and Current

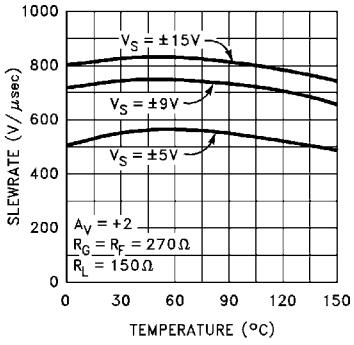


Typical Performance Curves (Continued)

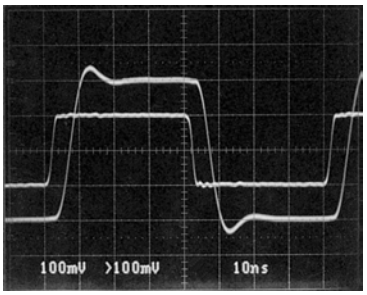
Undistorted Output Swing vs Frequency



Slew Rate vs Temperature

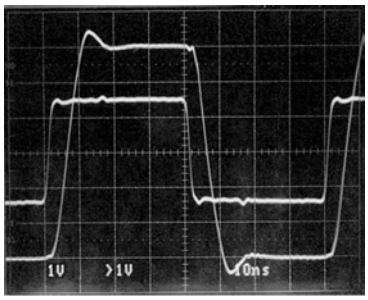


Small-Signal Transient Response



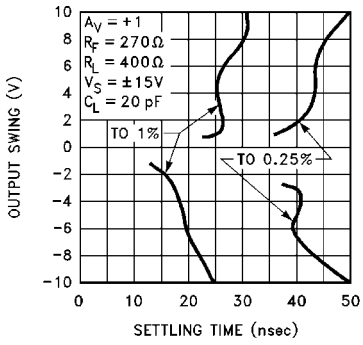
$A_V = +2$, $R_F = R_G = 270\Omega$, $R_L = 150\Omega$

Large-Signal Transient Response at 30MHz

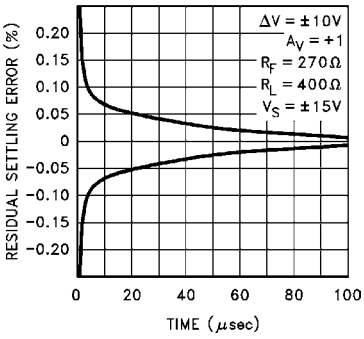


$A_V = +2$, $R_F = R_G = 270\Omega$, $R_L = 150\Omega$, $V_S = \pm 15V$

Settling Time vs Swing

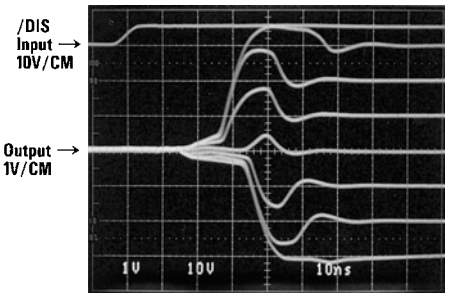


Long Term Settling Error



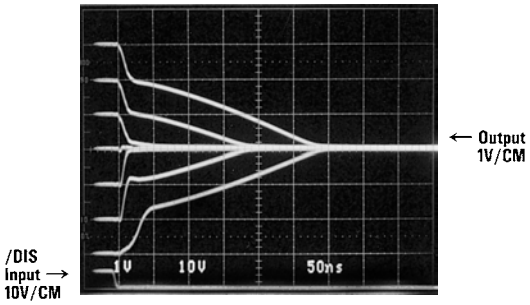
Typical Performance Curves (Continued)

Enable Response for a Family of Inputs



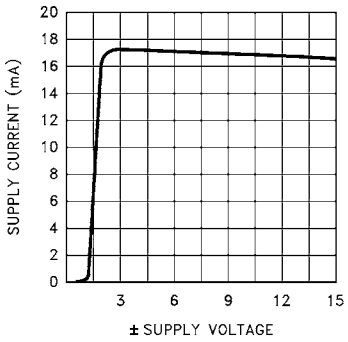
A_V = +2, R_L = 150Ω, V_S = ±5V

Disable Response for a Family of Inputs

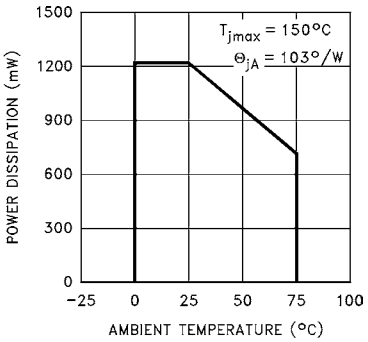


A_V = +2, R_L = 150Ω, V_S = ±5V

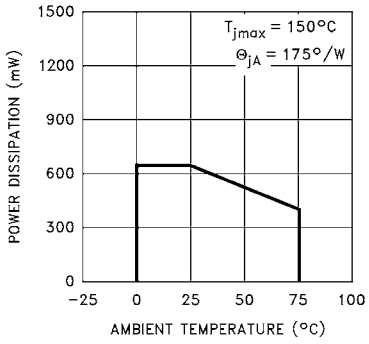
Supply Current vs Supply Voltage



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Pin SO Maximum Power Dissipation vs Ambient Temperature



Applications Information

The EL2120 represents the third generation of current-feedback amplifier design. It is designed to provide good high-frequency performance over wide supply voltage, load impedance, gain, temperature, and manufacturing lot variations. It is a well-behaved amplifier in spite of its 100MHz bandwidth, but a few precautions should be taken to obtain maximum performance.

The power supply pins must be well bypassed. 0.01µF ceramic capacitors are adequate, but lead length should be kept below 1/4” and a ground plane is recommended. Bypassing with 4.7µF tantalum capacitors can improve settling characteristics, and smaller capacitors in parallel will not be needed. The lead length of sockets generally deteriorates the amplifier's frequency response by exaggerating peaking and increasing ringing in response to transients. Short sockets cause little degradation.

Load capacitance also increases ringing and peaking. Capacitance greater than 35pF should be isolated with a series resistor. Capacitance at the V_{IN}- terminal has a similar effect, and should be kept below 5pF. Often, the inductance of the leads of a load capacitance will be self-resonant at frequencies from 40MHz to 200MHz and can cause oscillations. A resonant load can be de-Q'ed with a small series or parallel resistor. A “snubber” can sometimes

be used to reduce resonances. This is a resistor and capacitor in series connected from output to ground. Values of 68Ω and 33pF are typical. Increasing the feedback resistor can also improve frequency flatness.

The V_{IN}+ pin can oscillate in the 200MHz to 500MHz realm if presented with a resonant or inductive source impedance. A series 27Ω to 68Ω resistor right on the V_{IN}+ pin will suppress such oscillations without affecting frequency response.

-3dB bandwidth is inversely proportional to the value of feedback resistor R_F. The EL2120 will tolerate values as low as 180Ω for a maximum bandwidth of about 140MHz, but peaking will increase and tolerance to stray capacitance will reduce. At gains greater than 5, -3dB bandwidth begins to reduce, and a smaller R_F can be used to maximize frequency response.

The greatest frequency response flatness (to 0.1dB, for instance) occurs with R_F = 300Ω to 330Ω. Even the moderate peaking caused by lower values of R_F will cause the gain to peak out of the 0.1dB window, and higher values of R_F will cause an overcompensated response where the gain falls below the 0.1dB level. Parasitic capacitances will generally degrade the frequency flatness.

The EL2120 should not output a continuous current above 50mA, as stated in the ABSOLUTE MAXIMUM RATINGS table. The output current limit is set to 120mA at a die temperature of 25°C and reduces to 85mA at a die temperature of 150°C. This large current is needed to slew load capacitance and drive low impedance loads with low distortion but cannot be supported continuously. Furthermore, package dissipation capabilities cannot be met under short-circuit conditions. Current limit should not occur longer than a few seconds.

The output disable function of the EL2120 is optimized for video performance. While in disable mode, the feedthrough of the circuit can be modeled as a 0.2pF capacitor from V_{IN}+ to the output. No more than ±5V can be placed between V_{IN}+ and V_{IN}- in disable mode, but this is compatible with common video signal levels. In disabled state the output can withstand about 1000V/µs slew rate signals impressed on it without the output transistors turning on.

The /Disable pin logic level is referred to V+. With ±5V supplies, a CMOS or TTL driver with pull-up resistor will suffice. ±15V supplies require a +14/+11V drive span, or +15/+10V nominally. Open-collector TTL with a tapped pull-up resistor can provide these spans. The impedance of the divider should be 1k or less for optimum enable/disable speed.

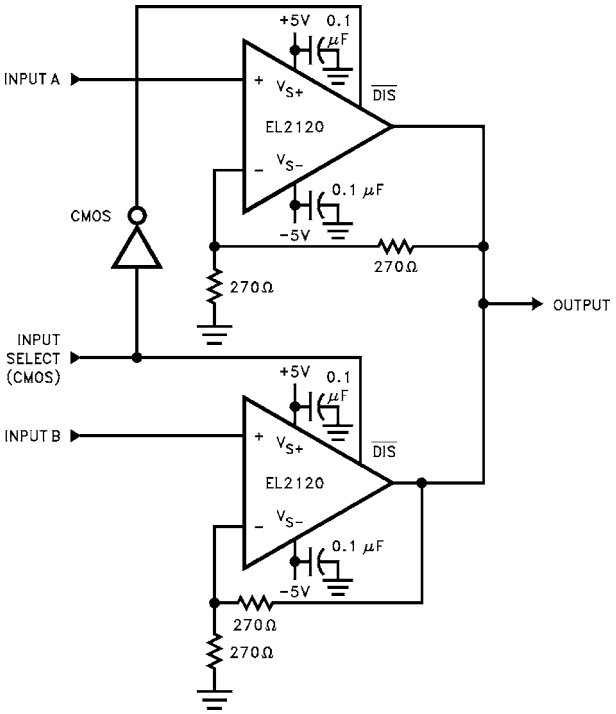
The EL2120 enables in 50ns or less. When V_{IN} = 0, only a small switching glitch occurs at the output. When V_{IN} is some other value, the output overshoots by about 0.7V when settling toward its new enabled value.

When the EL2120 disables, it turns off very rapidly for inputs of ±1V or less, and the output sags more slowly for inputs larger than this. For inputs as large as ±2.5V the output current can be absorbed by another EL2120 simultaneously enabled. Under these conditions, switching will be properly completed in 50ns or less.

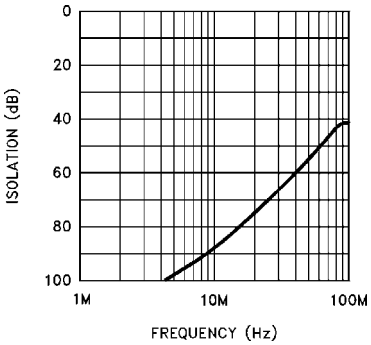
The greater thermal resistance of the SO-8 package requires that the EL2120 be operated from ±10V supplies or less to maintain the 150°C maximum die temperature over the commercial temperature range. The P-DIP package allows the full ±16.5V supply operation.

Typical Applications Circuit—A High Quality Two-Input Multiplexer

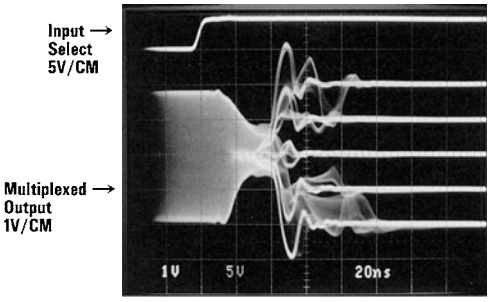
Dual EL2120 Multiplexer



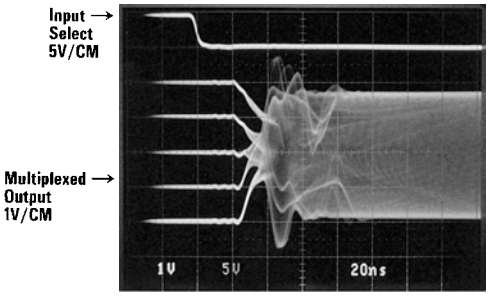
Channel-to-Channel Isolation of Dual EL2120 Multiplexer



Dual EL2120 Multiplexer Switching Channels: Uncorrelated Sinewave Switched to a Family of DC Levels



Dual EL2120 Multiplexer Switching Channels: a Family of DC Levels Switched to an Uncorrelated Sinewave



The EL2120 Macromodel

This macromodel has been developed to assist the user in simulating the EL2120 with surrounding circuitry. It was developed for the PSPICE simulator (copyrighted by the Microsim corporation), and may need to be rearranged for other simulators, particularly the H operator. It approximates frequency response and small-signal transients as well, although the effects of load capacitance does not show. This model is slightly more complicated than the models used for low-frequency op-amps, but is much more accurate for AC.

The model does not simulate these characteristics accurately:

- noise
- non-linearities
- slew rate limitations
- temperature effects
- settling time
- manufacturing variations
- input or output resonances
- CMRR and PSRR

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |      -Vsupply
*                   |     |     |      |     output
*                   |     |     |      |     |
.subckt M2120     3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 25
l1 11 12 20nH
iinp 3 0 10µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
s2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
15 30 17 1µH
c5 17 0 0.5pF
r5 17 0 600
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 140K
cdp 18 0 7.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
```

```
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 10mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 10K
r11 26 23 10K
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.1nS)
.model qp pnp (is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=4 n =4)
.ends
```

The EL2120 Macromodel (Continued)