

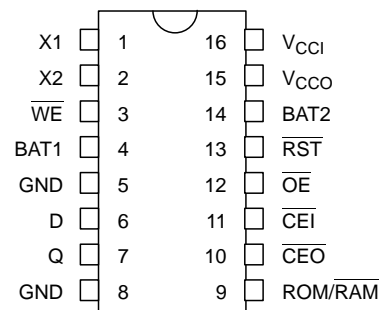
### FEATURES

- Keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adjusts for months with fewer than 31 days
- Leap year automatically corrected up to 2100
- No address space required
- Provides nonvolatile controller functions for battery backup of RAM
- Supports redundant batteries for high-reliability applications
- Uses a 32.768 KHz watch crystal
- Full  $\pm 10\%$  operating range
- Operating temperature range  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$
- Space-saving, 16-pin DIP package and SOIC
- Optional industrial temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (IND)

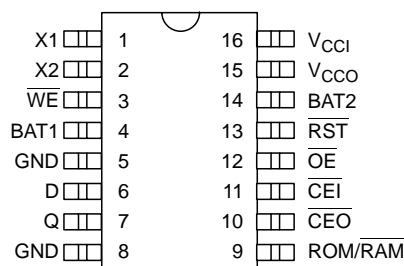
### DESCRIPTION

The DS1215 Phantom Time Chip is a combination of a CMOS timekeeper and a nonvolatile memory controller. In the absence of power, an external battery maintains the timekeeping operation and provides power for a CMOS static RAM. The watch keeps track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including correction for leap year every four years. The watch operates in one of two formats: a 12-hour mode with an AM/PM indicator or a 24-hour mode. The nonvolatile controller supplies all the necessary support circuitry to convert a CMOS RAM to a nonvolatile memory. The DS1215 can be interfaced with either RAM or ROM without leaving gaps in memory.

### PIN ASSIGNMENT



16-PIN DIP (300 MIL)



16-PIN SOIC (300 MIL)

### PIN DESCRIPTION

X1, X2	– 32.768 KHz Crystal Connections
$\overline{\text{WE}}$	– Write Enable
BAT1	– Battery 1 Input
GND	– Ground
D	– Data In
Q	– Data Out
$\text{ROM}/\overline{\text{RAM}}$	– ROM/RAM Select
$\overline{\text{CEO}}$	– Chip Enable Out
$\overline{\text{CEI}}$	– Chip Enable Input
$\overline{\text{OE}}$	– Output Enable
$\overline{\text{RST}}$	– Reset
BAT2	– Battery 2 Input
$\text{VCCO}$	– Switched Supply Output
$\text{VCCI}$	– +5 VDC Input

NOTE: Both pins 5 and 8 must be grounded.

### ORDERING INFORMATION

DS1215	16-pin DIP
DS1215S	16-pin SOIC
DS1215N	16-pin DIP (IND)
DS1215SN	16-pin SOIC (IND)

## OPERATION

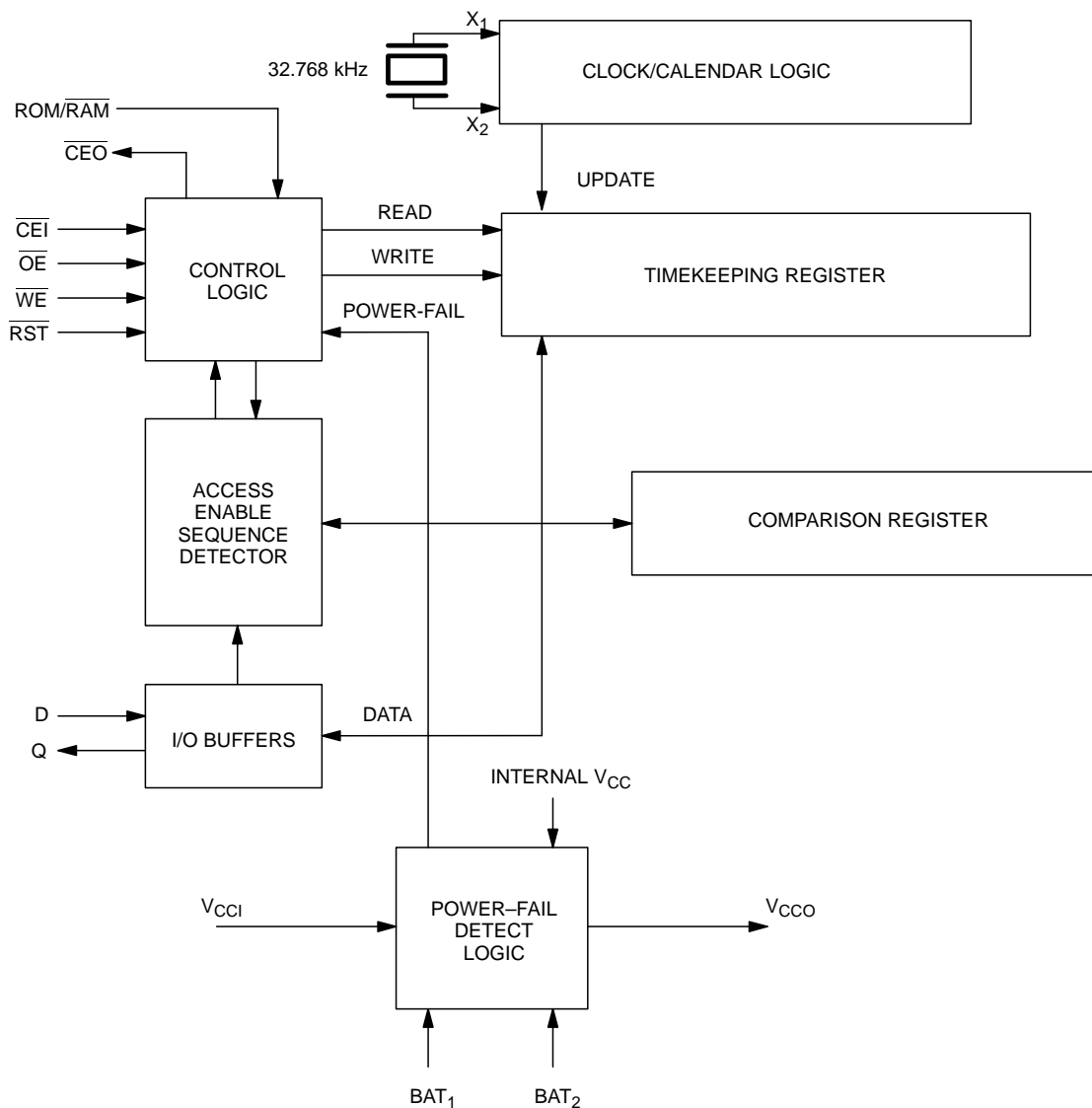
The block diagram of Figure 1 illustrates the main elements of the Time Chip. Communication with the Time Chip is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on data in (D). All accesses which occur prior to recognition of the 64-bit pattern are directed to memory via the chip enable output pin ( $\overline{\text{CEO}}$ ).

After recognition is established, the next 64 read or write cycles either extract or update data in the Time Chip and

$\overline{\text{CEO}}$  remains high during this time, disabling the connected memory.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable input ( $\overline{\text{CEI}}$ ), output enable ( $\overline{\text{OE}}$ ), and write enable ( $\overline{\text{WE}}$ ). Initially, a read cycle using the  $\overline{\text{CEI}}$  and  $\overline{\text{OE}}$  control of the Time Chip starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the  $\overline{\text{CEI}}$  and  $\overline{\text{WE}}$  control of the Time Chip. These 64 write cycles are used only to gain access to the Time Chip.

## TIMING BLOCK DIAGRAM Figure 1

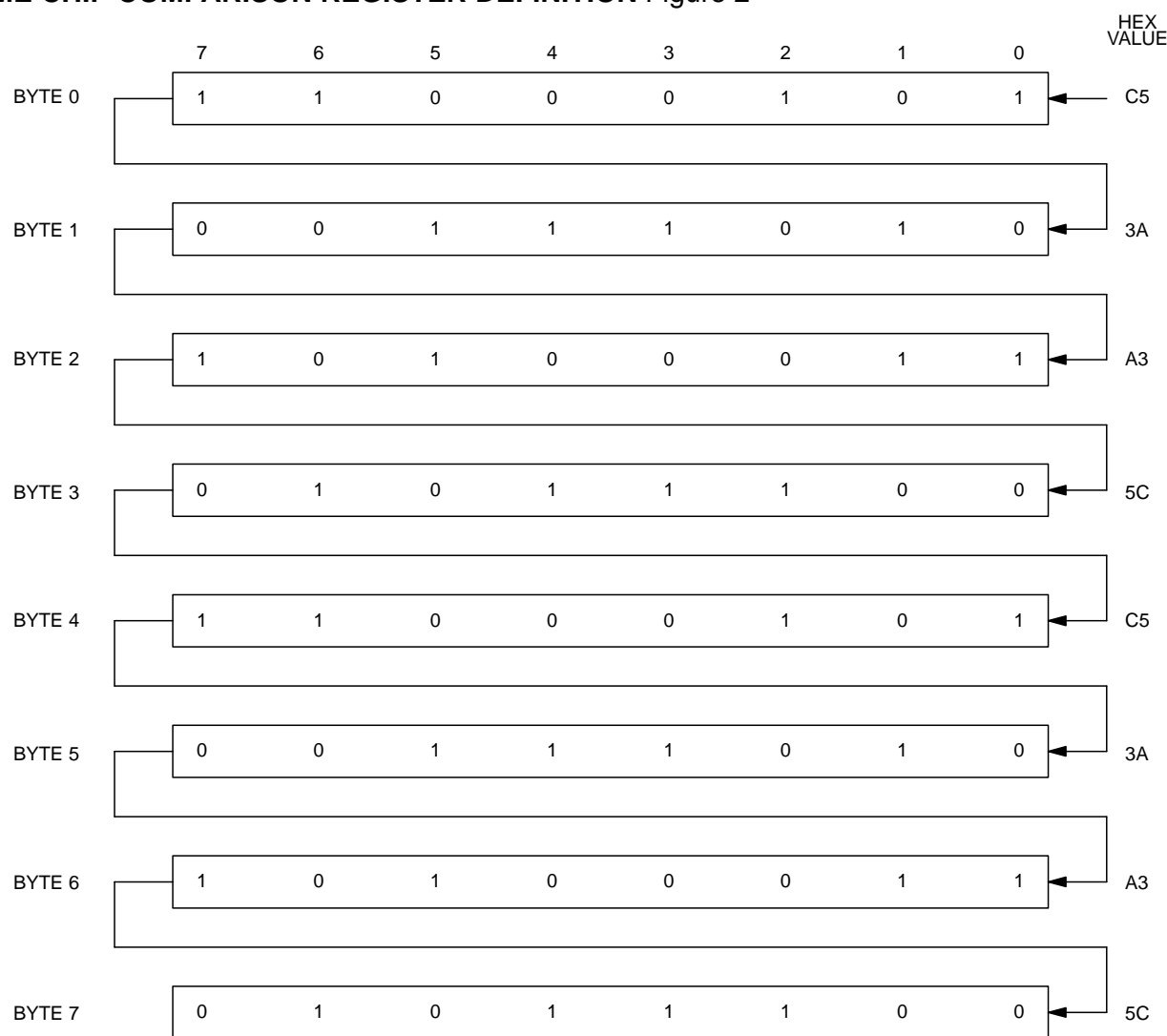


When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched. (This bit pattern is shown in Figure 2.) With a correct match for 64 bits, the Time Chip is enabled and data transfer to or from the timekeeping registers may proceed. The next

64 cycles will cause the Time Chip to either receive data on D, or transmit data on Q, depending on the level of  $\overline{OE}$  pin or the  $\overline{WE}$  pin. Cycles to other locations outside the memory block can be interleaved with  $\overline{CEI}$  cycles without interrupting the pattern recognition sequence or data transfer sequence to the Time Chip.

A 32,768 Hz quartz crystal can be directly connected to the DS1215 via pins 1 and 2 (X1, X2). The crystal selected for use should have a specified load capacitance ( $C_L$ ) of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks".

### TIME CHIP COMPARISON REGISTER DEFINITION Figure 2



#### NOTE:

The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the Time Chip are less than 1 in  $10^{19}$ .

## NONVOLATILE CONTROLLER OPERATION

The operation of the nonvolatile controller circuits within the Time Chip is determined by the level of the ROM/ $\overline{\text{RAM}}$  select pin. When ROM/ $\overline{\text{RAM}}$  is connected to ground, the controller is set in the RAM mode and performs the circuit functions required to make static CMOS RAM and the timekeeping function nonvolatile. A switch is provided to direct power from the battery inputs or  $V_{\text{CCI}}$  to  $V_{\text{CCO}}$  with a maximum voltage drop of 0.3 volts. The  $V_{\text{CCO}}$  output pin is used to supply uninterrupted power to CMOS SRAM. The DS1215 also performs redundant battery control for high reliability. On power-fail, the battery with the highest voltage is automatically switched to  $V_{\text{CCO}}$ . If only one battery is used in the system, the unused battery input should be connected to ground.

The DS1215 safeguards the Time Chip and RAM data by power-fail detection and write protection. Power-fail detection occurs when  $V_{\text{CCI}}$  falls below VTP, which is equal to  $1.26 \times V_{\text{BAT}}$ . The DS1215 constantly monitors the  $V_{\text{CCI}}$  supply pin. When  $V_{\text{CCI}}$  is less than VTP, a comparator outputs a power-fail signal to the control logic. The power-fail signal forces the chip enable output ( $\overline{\text{CEO}}$ ) to  $V_{\text{CCI}}$  or  $V_{\text{BAT}} - 0.2$  volts for external RAM write protection. During nominal supply conditions,  $\overline{\text{CEO}}$  will track  $\overline{\text{CEI}}$  with a maximum propagation delay of 20 ns. Internally, the DS1215 aborts any data transfer in progress without changing any of the Time Chip registers and prevents future access until  $V_{\text{CCI}}$  exceeds VTP. A typical RAM/Time Chip interface is illustrated in Figure 3.

When the ROM/ $\overline{\text{RAM}}$  pin is connected to  $V_{\text{CCO}}$ , the controller is set in the ROM mode. Since ROM is a read-only device that retains data in the absence of power, battery backup and write protection is not required. As a result, the chip enable logic will force  $\overline{\text{CEO}}$  low when power fails. However, the Time Chip does retain the same internal nonvolatility and write protection as described in the RAM mode. In addition, the chip enable output is set at a low level on power-fail as  $V_{\text{CCI}}$  falls below the level of  $V_{\text{BAT}}$ . A typical ROM/Time Chip interface is illustrated in Figure 4.

## TIME CHIP REGISTER INFORMATION

Time Chip information is contained in 8 registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the Time Chip registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 5.

Data contained in the Time Chip registers is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

## AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

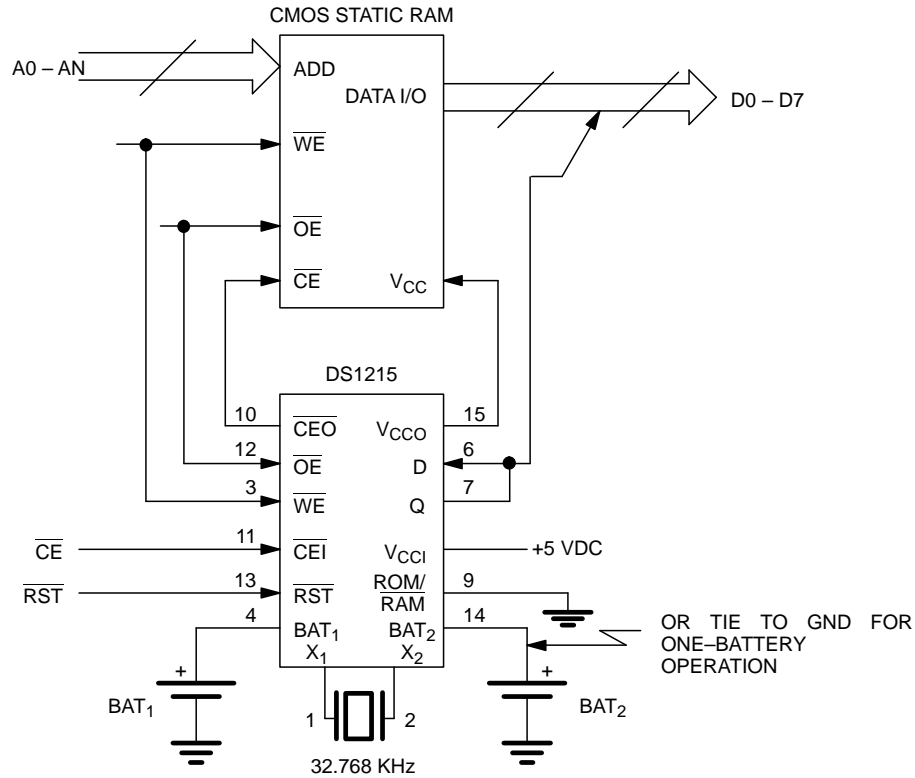
## OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the reset and oscillator functions. Bit 4 controls the reset pin (Pin 13). When the reset bit is set to logic 1, the reset input pin is ignored. When the reset bit is set to logic 0, a low input on the reset pin will cause the Time Chip to abort data transfer without changing data in the timekeeping registers. Reset operates independently of all other inputs. Bit 5 controls the oscillator. When set to logic 0, the oscillator turns on and the watch becomes operational.

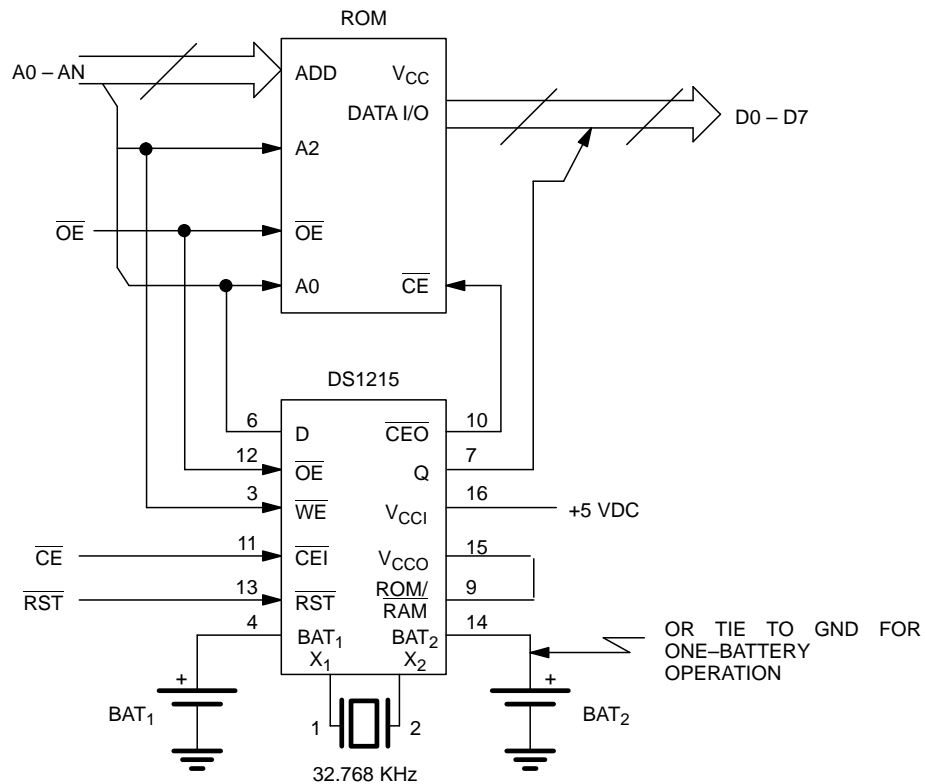
## ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

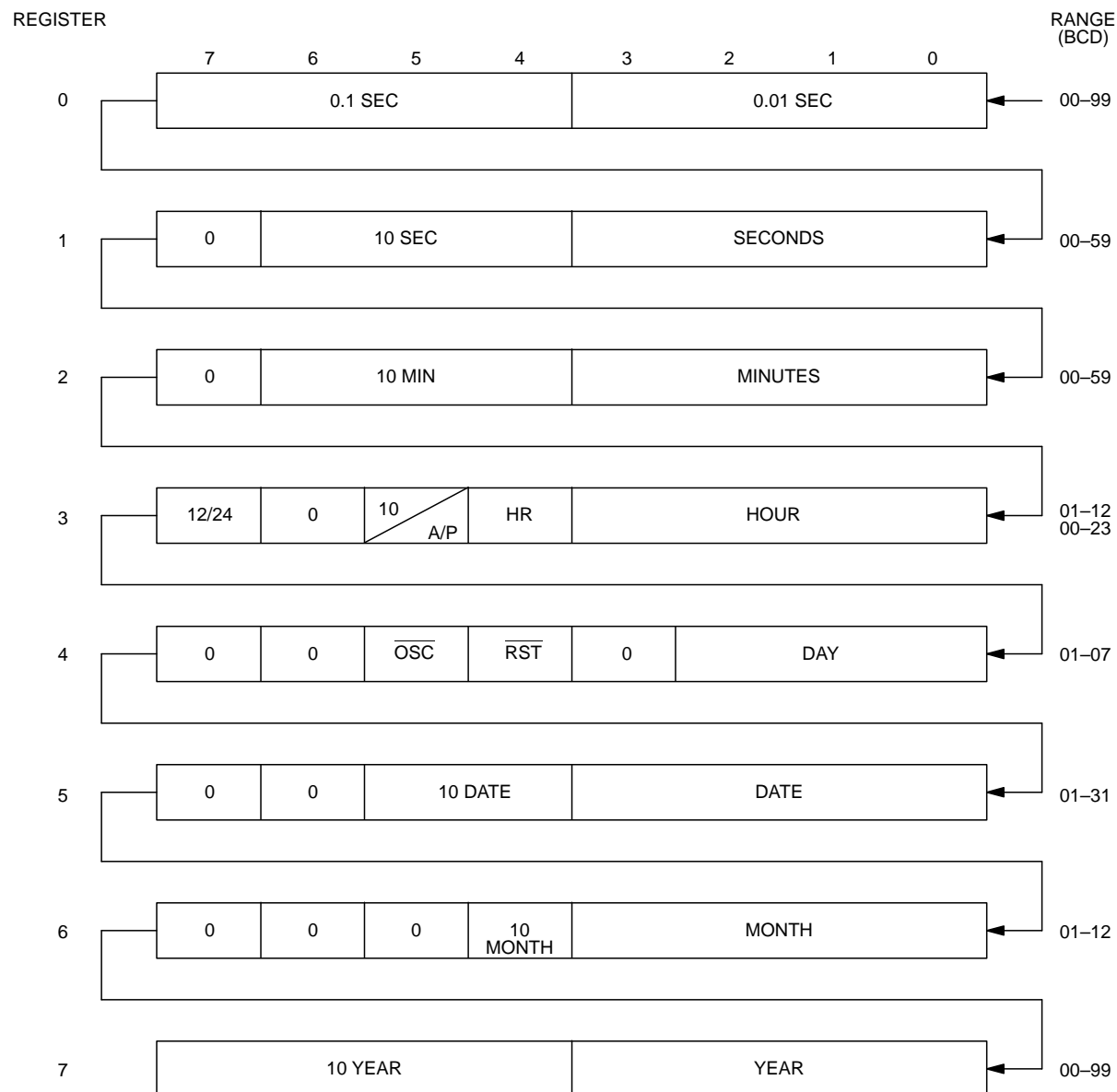
RAM/TIME CHIP INTERFACE Figure 3



ROM/TIME CHIP INTERFACE Figure 4



# TIME CHIP REGISTER DEFINITION Figure 5



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any Pin Relative to Ground

Operating Temperature

Storage Temperature

Soldering Temperature

−0.3V to +7.0V

0°C to 70°C

−55°C to +125°C

260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Logic 1	$V_{IH}$	2.2		$V_{CC}+0.3$		1
Logic 0	$V_{IL}$	−0.3		+0.8	V	1
$V_{BAT1}$ or $V_{BAT2}$ Battery Voltage	$V_{BAT}$	2.5		3.7	V	7

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 4.5$  to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	$I_{CCI}$			5	mA	6
Supply Current $V_{CCO} = V_{CCI}-0.3$	$I_{CCO1}$			80	mA	8
Input Leakage	$I_{IL}$	−1.0		+1.0	μA	11
Output Leakage	$I_{LO}$	−1.0		+1.0	μA	
Output @ 2.4V	$I_{OH}$	−1.0			mA	2
Output @ 0.4V	$I_{OL}$			4.0	mA	2

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C;  $V_{CC} < 4.5$ V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEO}$ Output	$V_{OH1}$	$V_{CCI}$ or $V_{BAT}-0.2$			V	9
$V_{BAT1}$ or $V_{BAT2}$ Battery Current	$I_{BAT}$			1	μA	6
Battery Backup Current @ $V_{CCO} = V_{BAT}-0.2$ V	$I_{CCO2}$			10	μA	10

**AC ELECTRICAL CHARACTERISTICS ROM/ $\overline{\text{RAM}}$  = GND**(0°C to 70°C;  $V_{CC}$  = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	120			ns	
$\overline{\text{CEI}}$ Access Time	$t_{CO}$			100	ns	
$\overline{\text{OE}}$ Access Time	$t_{OE}$			100	ns	
$\overline{\text{CEI}}$ to Output Low Z	$t_{COE}$	10			ns	
$\overline{\text{OE}}$ to Output Low Z	$t_{OEE}$	10			ns	
$\overline{\text{CEI}}$ to Output High Z	$t_{OD}$			40	ns	
$\overline{\text{OE}}$ to Output High Z	$t_{ODO}$			40	ns	
Read Recovery	$t_{RR}$	20			ns	
Write Cycle	$t_{WC}$	120			ns	
Write Pulse Width	$t_{WP}$	100			ns	
Write Recovery	$t_{WR}$	20			ns	4
Data Setup	$t_{DS}$	40			ns	5
Data Hold Time	$t_{DH}$	10			ns	5
$\overline{\text{CEI}}$ Pulse Width	$t_{CW}$	100			ns	
$\overline{\text{RST}}$ Pulse Width	$t_{RST}$	200			ns	
$\overline{\text{CEI}}$ Propagation Delay	$t_{PD}$	5	10	20	ns	2, 3
$\overline{\text{CEI}}$ High to Power-Fail	$t_{PF}$			0	ns	

**AC ELECTRICAL CHARACTERISTICS ROM/ $\overline{\text{RAM}}$  = GND**(0°C to 70°C;  $V_{CC}$  > 4.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	$t_{REC}$			2	ms	
$V_{CC}$ Slew Rate 4.5 – 3.0V	$t_F$	0			ms	

**CAPACITANCE**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$		5	10	pF	
Output Capacitance	$C_{OUT}$		5	10	pF	



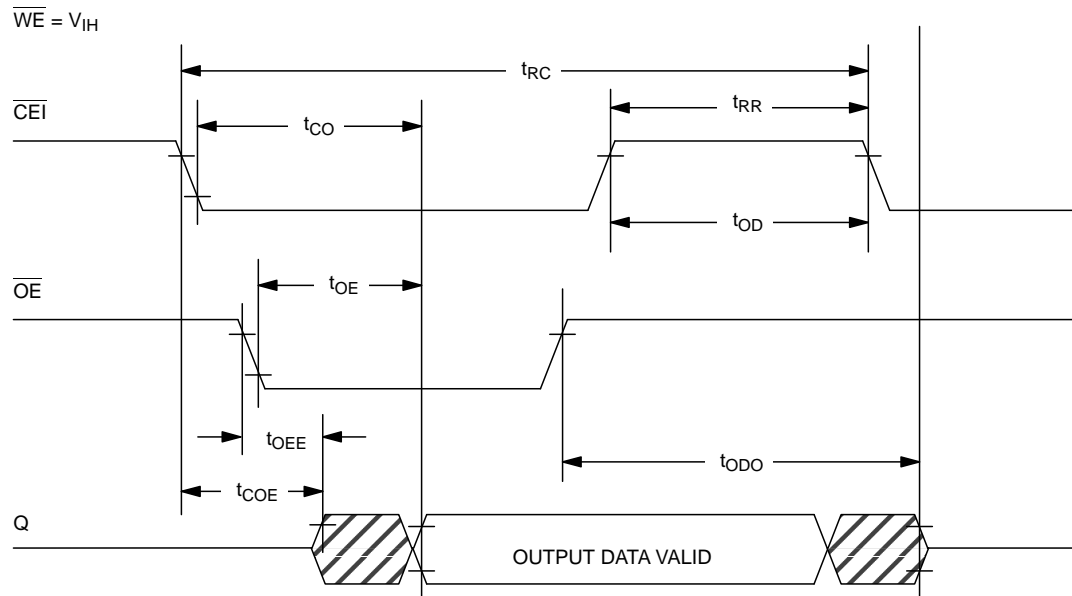
**AC ELECTRICAL CHARACTERISTICS ROM/RAM =  $V_{CC0}$**  (0°C to 70°C;  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	$t_{RC}$	120			ns	
$\overline{CEI}$ Access Time	$t_{CO}$			100	ns	
$\overline{OE}$ Access Time	$t_{OE}$			100	ns	
$\overline{CEI}$ to Output in Low Z	$t_{COE}$	10			ns	
$\overline{OE}$ to Output in Low Z	$t_{OEE}$	10			ns	
$\overline{CEI}$ to Output in High Z	$t_{OD}$			40	ns	
$\overline{OE}$ to Output in High Z	$t_{ODO}$			40	ns	
Address Setup Time	$t_{AS}$	20			ns	
Address Hold Time	$t_{AH}$			10	ns	
Read Recovery	$t_{RR}$	20			ns	
Write Cycle Time	$t_{WC}$	120			ns	
$\overline{CEI}$ Pulse Width	$t_{CW}$	100			ns	
$\overline{OE}$ Pulse Width	$t_{OW}$	100			ns	
Write Recovery	$t_{WR}$	20			ns	4
Data Setup Time	$t_{DS}$	40			ns	5
Data Hold Time	$t_{DH}$	10			ns	5
$\overline{RST}$ Pulse Width	$t_{RST}$	200			ns	
$\overline{CEI}$ Propagation Delay	$t_{PD}$	5	10	20	ns	2, 3
$\overline{CEI}$ High to Power Fail	$t_{PF}$			0	ns	

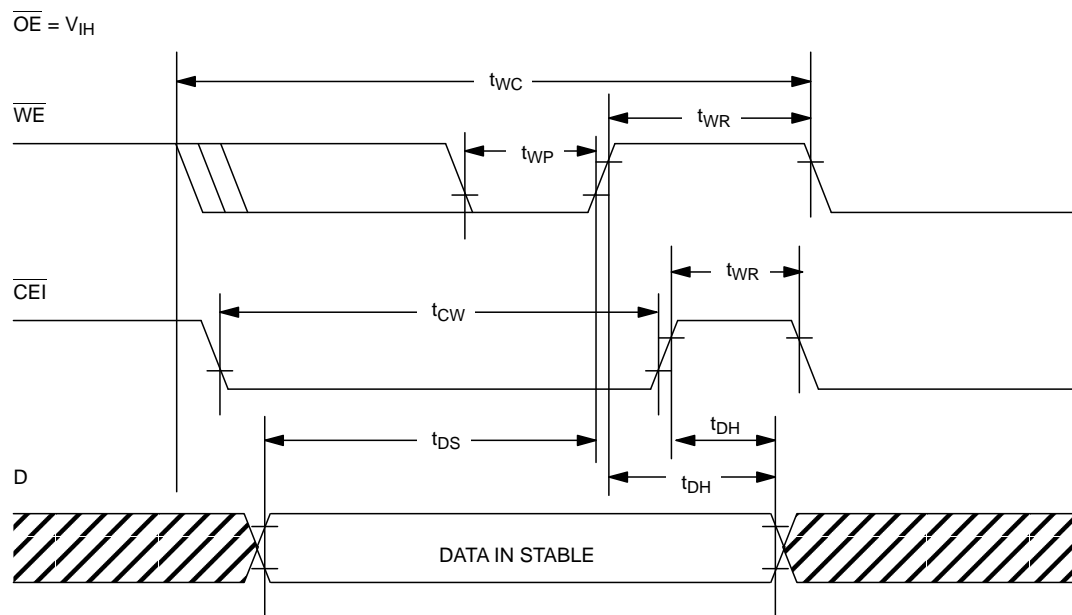
**AC ELECTRICAL CHARACTERISTICS ROM/RAM =  $V_{CC0}$**  (0°C to 70°C;  $V_{CC} < 4.5V$ )

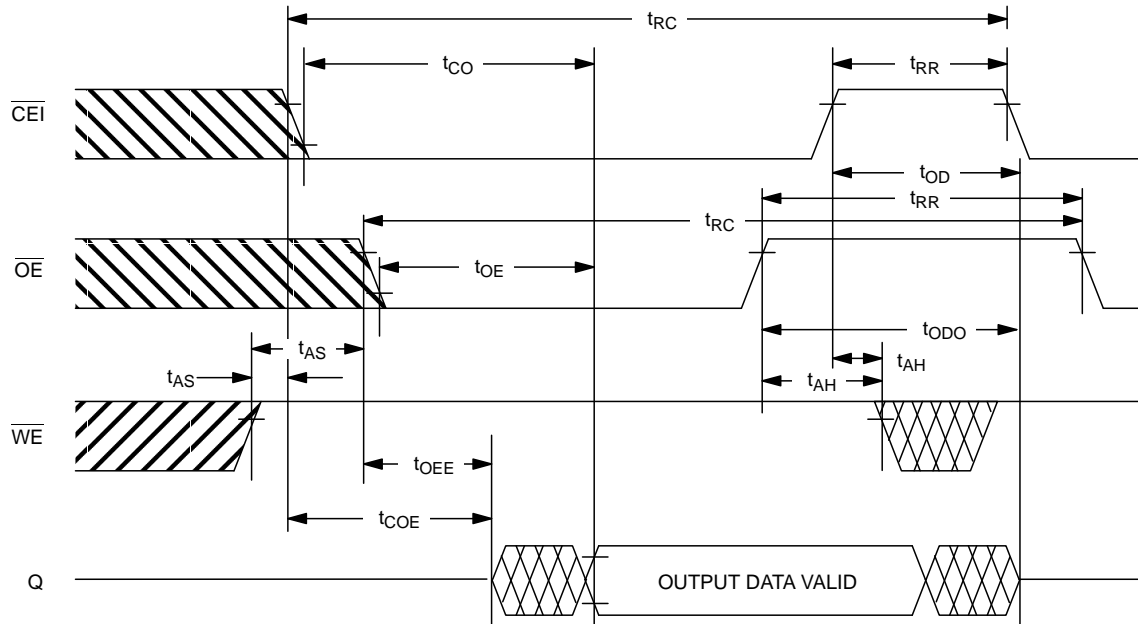
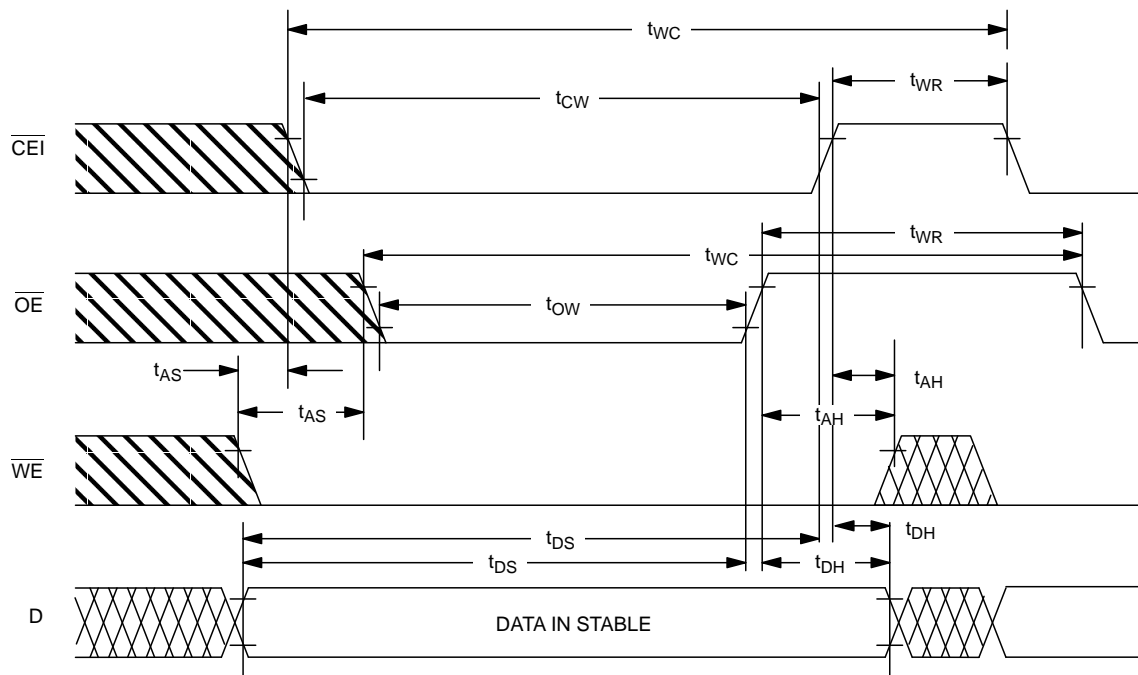
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power-Up	$t_{REC}$			2	ms	
$V_{CC}$ Slew Rate 4.5 – 3.0V	$t_F$	0			ms	

# TIMING DIAGRAM: READ CYCLE TO TIME CHIP ROM/ $\overline{\text{RAM}} = \text{GND}$

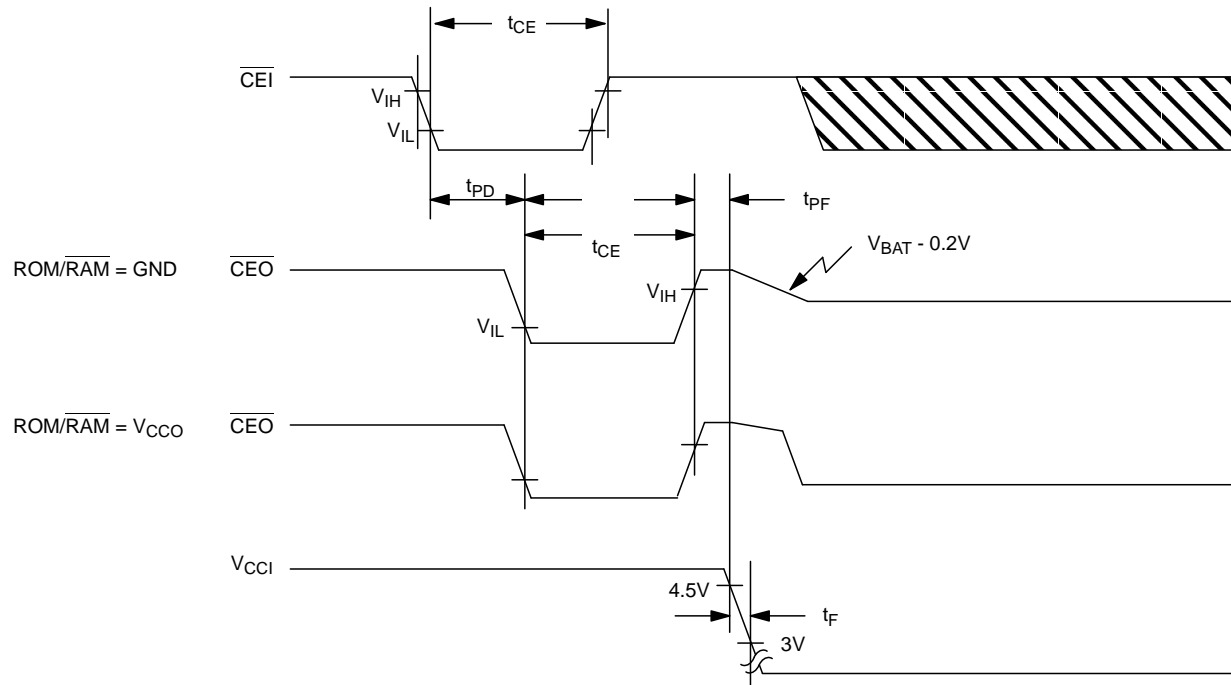


# TIMING DIAGRAM: WRITE CYCLE TO TIME CHIP ROM/ $\overline{\text{RAM}} = \text{GND}$

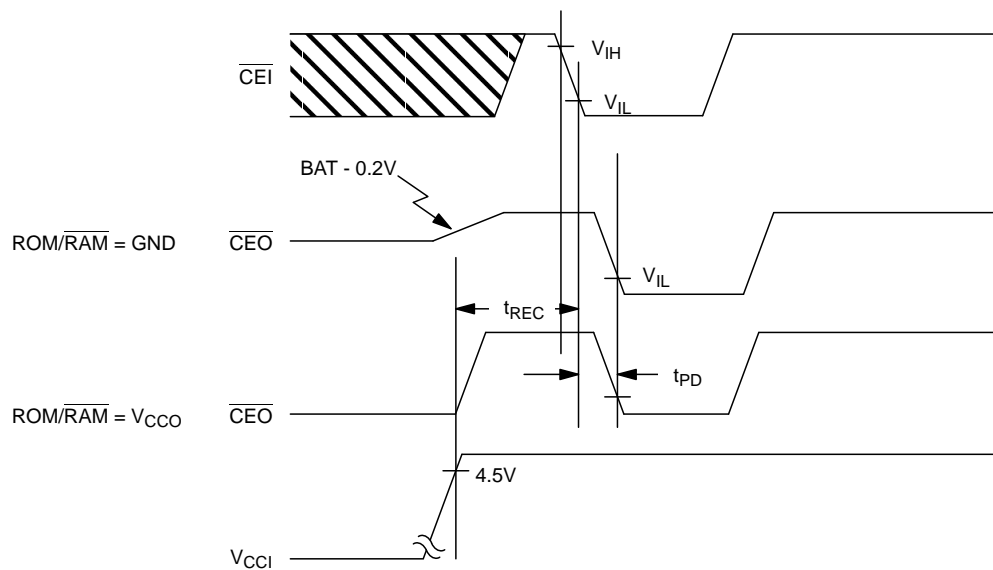


**TIMING DIAGRAM: READ CYCLE ROM/ $\overline{\text{RAM}} = V_{\text{CCO}}$** 

**TIMING DIAGRAM: WRITE CYCLE ROM/ $\overline{\text{RAM}} = V_{\text{CCO}}$** 


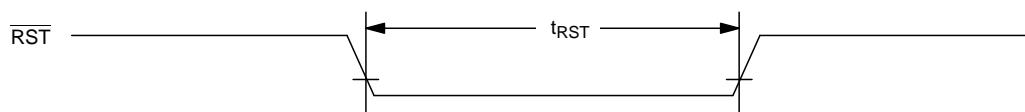
## TIMING DIAGRAM: POWER DOWN



## TIMING DIAGRAM: POWER UP

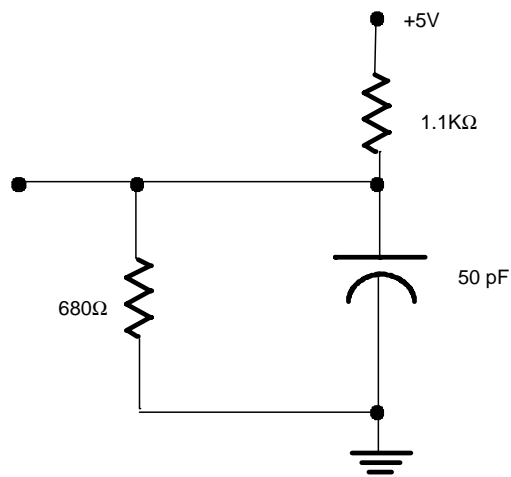


## TIMING DIAGRAM: RESET FOR TIME CHIP

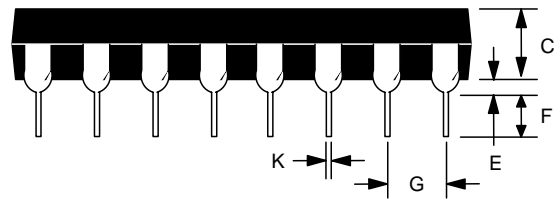
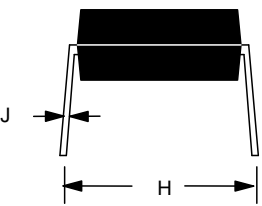
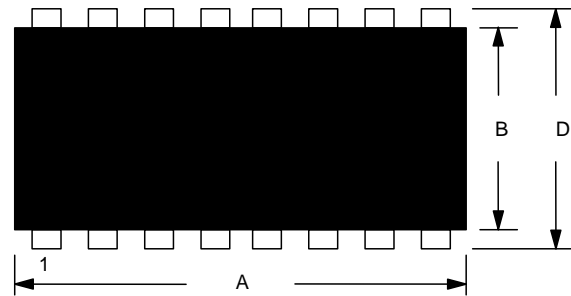


**NOTES:**

1. All voltages are referenced to ground.
2. Measured with load shown in Figure 6.
3. Input pulse rise and fall times equal 10 ns.
4.  $t_{WR}$  is a function of the latter occurring edge of  $\overline{WE}$  or  $\overline{CE}$  in RAM mode, or  $\overline{OE}$  or  $\overline{CE}$  in ROM mode.
5.  $t_{DH}$  and  $t_{DS}$  are functions of the first occurring edge of  $\overline{WE}$  or  $\overline{CE}$  in RAM mode, or  $\overline{OE}$  or  $\overline{CE}$  in ROM mode.
6. Measured without RAM connected.
7. Trip point voltage for power-fail detect.  $V_{TP} = 1.26 \times V_{BAT}$ . For 10%  $V_{CC} = 5V + 10\%$  operation  $V_{BAT} = 3.5V$  max.; for 5% operation  $V_{BAT} = 3.7V$  max.
8.  $I_{CC01}$  is the maximum average load current the DS1215 can supply to memory.
9. Applies to  $\overline{CEO}$  with the ROM/ $\overline{RAM}$  pin grounded. When the ROM/ $\overline{RAM}$  pin is connected to  $V_{CCO}$ ,  $\overline{CEO}$  will go to a low level as  $V_{CCI}$  falls below  $V_{BAT}$ .
10.  $I_{CC02}$  is the maximum average load current that the DS1215 can supply to memory in the battery backup mode.
11. Applies to all input pins except  $\overline{RST}$ .  $\overline{RST}$  is pulled internally to  $V_{CCI}$ .

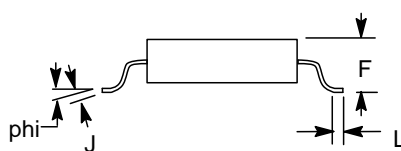
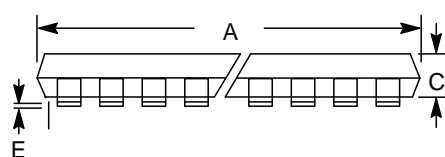
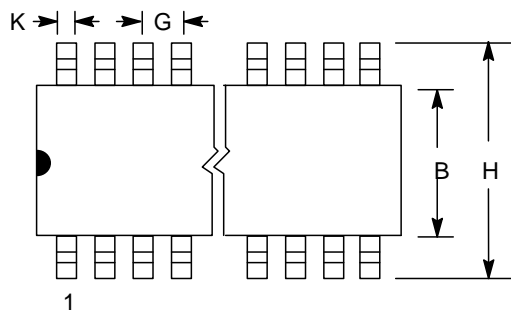
**OUTPUT LOAD Figure 6**

DS1215 TIME CHIP



PKG	16-PIN	
	MIN	MAX
A IN. MM	0.740	0.780
B IN. MM	0.240	0.260
C IN. MM	0.120	0.140
D IN. MM	0.300	0.325
E IN. MM	0.015	0.040
F IN. MM	0.110	0.140
G IN. MM	0.090	0.110
H IN. MM	0.300	0.370
J IN. MM	0.008	0.012
K IN. MM	0.015	0.021

# DS1215S SERIAL TIMEKEEPER 16-PIN SOIC



PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	0.050 BSC 1.27 BSC	
H IN. MM	0.398 10.11	0.416 10.57
J IN. MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN. MM	0.016 0.40	0.040 1.02
PHI	0°	8°