DS1004
5-Tap High Speed Silicon Delay Line

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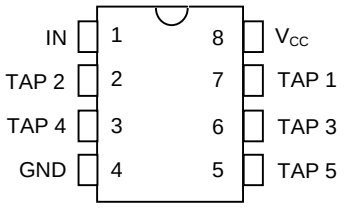
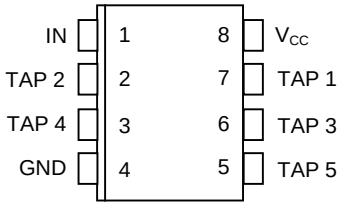
FEATURES

- All-silicon timing circuit
- Five delayed clock phases per input
- Precise tap-to-tap nominal delay tolerances of ±0.75 and ±1 ns
- Input-to-tap 1 delay of 5 ns
- Nominal Delay tolerances of ±1.5 ns
- Leading and trailing edge precision preserves the input symmetry
- CMOS design with TTL compatibility
- Standard 8-pin DIP and 150 mil 8-pin SOIC
- Vapor phase, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1004M 8-Pin DIP (300-mil)
See Mech. Drawings Section



DS1004Z 8-Pin SOIC (150-mil)
See Mech. Drawings Section

PIN DESCRIPTION

TAP 1-5	- TAP Output Number
V_{CC}	- +5V Supply
GND	- Ground
IN	- Input

DESCRIPTION

The DS1004 is a 5-tap all silicon delay line which can provide 2, 3, 4, or 5 ns tap-to-tap delays within a standard part family. The device is Dallas Semiconductor's fastest 5-tap delay line. It is available in a standard 8-pin DIP and 150 mil 8-pin mini-SOIC. The device features precise leading and trailing edge accuracies and has the inherent reliability of an all-silicon delay line solution.

The DS1004 is specified for tap-to-tap tolerances as shown in Table 1. Each device has a minimum input-to-tap 1 delay of 5 ns. Subsequent taps (taps 2 through 5) are precisely delayed by 2, 3, 4, or 5 ns. See Table 1 for details. Input to Tap Tolerance over temperature and voltage is ±1.5 ns in addition to the nominal delay tolerance. Nominal tap-to-tap tolerances range from ±0.75 ns to ±1.0 ns. Each output is capable of driving up to 10 LS loads.

For customers needing non-standard delay values, the Late Package Program (LPP) is available. Customers may contact Dallas Semiconductor at (972) 371–4348 for further details.

PART NUMBER TOLERANCE TABLE Table 1

PART NUMBER	INPUT-TO-TAP TOLERANCE		TAP-TO-TAP TOLERANCE	
	NOMINAL[1]	OVER TEMP & VOLTAGE[2]	NOMINAL[1]	OVER TEMP & VOLTAGE[2]
DS1004M-2	1.5 ns	±3.0 ns	±0.75 ns	±1.5 ns
DS1004M-3	1.5 ns	±3.0 ns	±0.75 ns	±1.5 ns
DS1004M-4	1.5 ns	±3.0 ns	±1.0 ns	±1.75 ns
DS1004M-5	1.5 ns	±3.0 ns	±1.0 ns	±1.75 ns
DS1004Z-2	1.5 ns	±3.0 ns	±0.75 ns	±1.5 ns
DS1004Z-3	1.5 ns	±3.0 ns	±0.75 ns	±1.5 ns
DS1004Z-4	1.5 ns	±3.0 ns	±1.0 ns	±1.75 ns
DS1004Z-5	1.5 ns	±3.0 ns	±1.0 ns	±1.75 ns

NOTES:

1. Nominal conditions are +25°C and V_{CC} = +5.0V

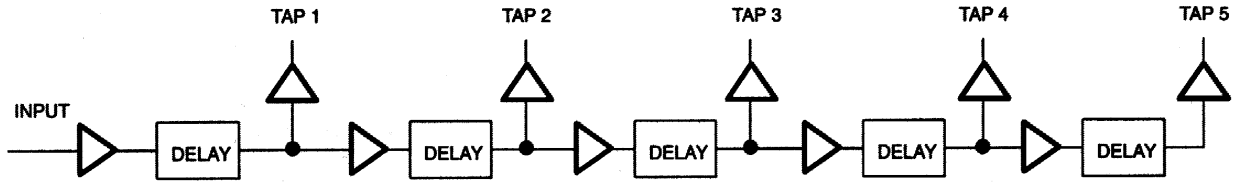
2. Temperature and voltage variations cover the range from V_{CC}=5.0V ± 5% and temperature range from 0°C to +70°C.

3. Delay accuracy for both leading and trailing edges.

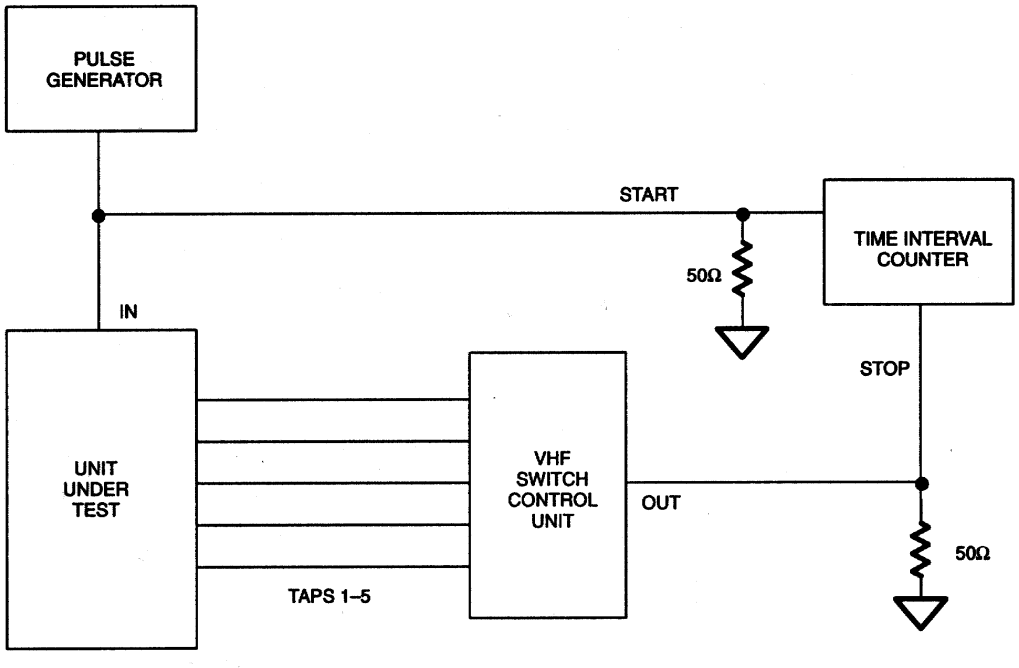
PART NUMBER DELAY TABLE Table 2

PART NUMBER	NOMINAL VALUES (FOR REFERENCE ONLY)				
	INPUT-TO-TAP1	INPUT-TO-TAP2	INPUT-TO-TAP3	INPUT-TO-TAP4	INPUT-TO-TAP5
DS1004M-2	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004M-3	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004M-4	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004M-5	5 ns	10 ns	15 ns	20 ns	25 ns
DS1004Z-2	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004Z-3	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004Z-4	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004Z-5	5 ns	10 ns	15 ns	20 ns	25 ns

LOGIC DIAGRAM



DS1004 TEST CIRCUIT Figure 1



TEST SETUP DESCRIPTION

Figure 1 illustrates the hardware configuration used for measuring the timing parameters of the DS1004. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1004 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
Active Current	I_{CC}	V_{CC}=5.25V Period=1 µs		35	75	mA	
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH}=4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL}=0.5V	12			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	3
Input to Tap 1 Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	2
Tap-to-Tap Delays	t_{PLH}		Table 1		ns	2
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power-up Time	t_{PU}			100	ms	

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

NOTES:

1. All voltages are referenced to ground.

2. V_{CC}=5V and 25°C. Delay accuracy on both the rising and falling edges within tolerances given in Table 1.

3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to decoupling, layout, etc.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns
Pulse Period:	1 µs
Output Load Capacitance:	15 pF

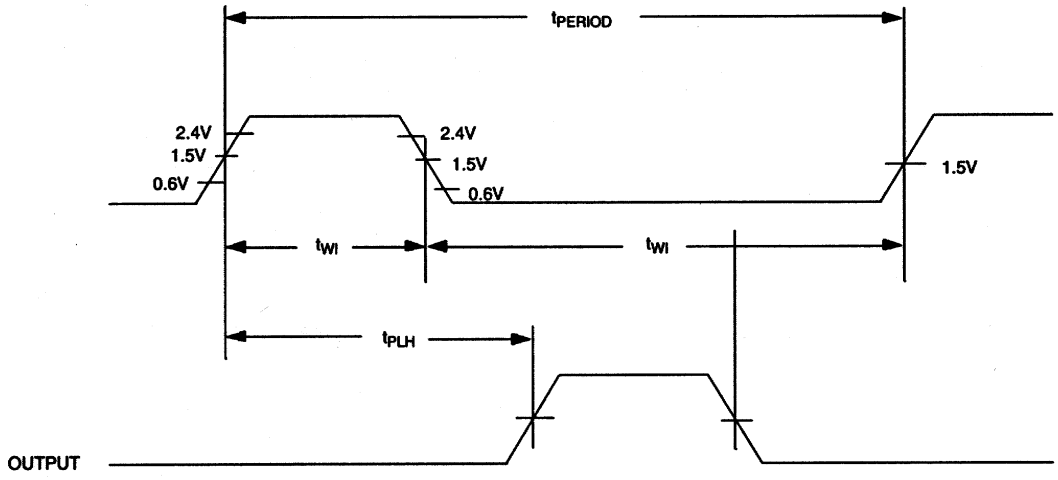
OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Data is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1004 INPUT TO OUTPUTS



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the falling edge of the input pulse and the 1.5V point on the falling edge of the output pulse.