SONY

CXA1391Q/R

Processing IC for Complementary Color Mosaic CCD Camera

Description

The CXA1391Q/R is a bipolar IC developed for signal processing in complementary color mosaic CCD cameras.

Features

- Low power consumption (170mW)
- Number of delay lines used for signal processing can be selected according to the system requirements
- The LPF peripheral to 1H delay line is built in

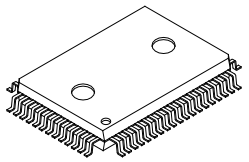
Structure

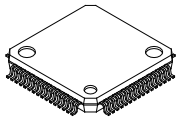
Bipolar silicon monolithic IC

Applications

Complementary color mosaic CCD cameras

CXA1391Q	CXA1391R
64 pin QFP (Plastic)	64 pin LQFP (Plastic)





Absolute Maximum Ratings

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	–55 to +150	℃
• Allowable power dissipation	P_D	690	mW

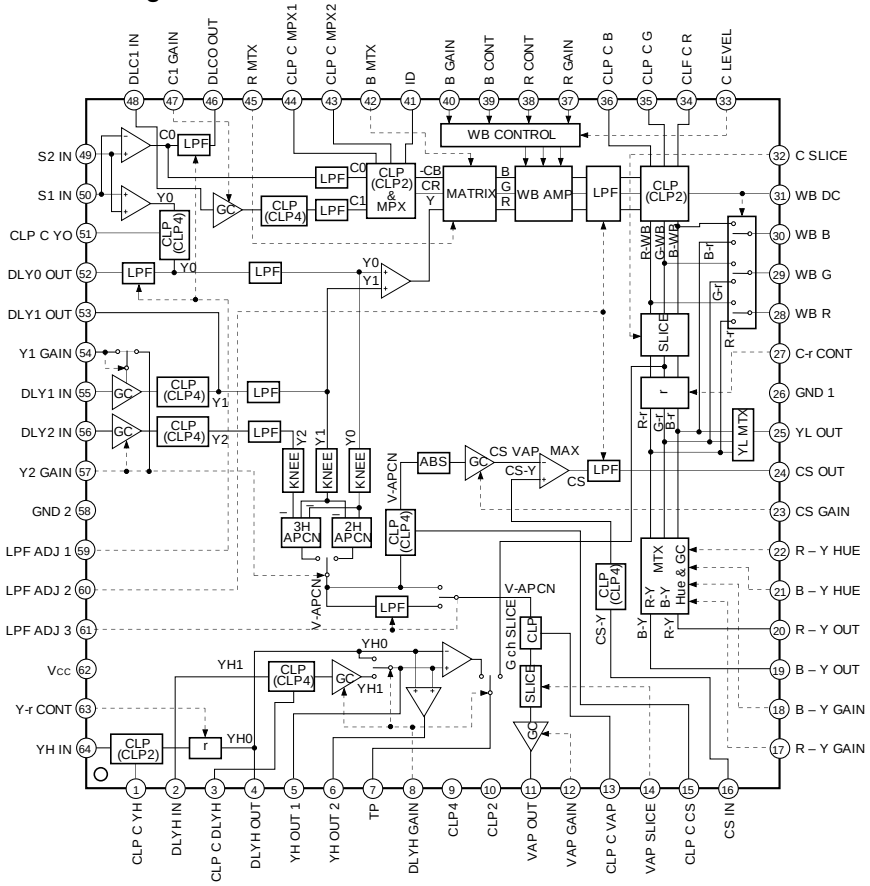
(LQFP: Ta = 25°C, without P.C.B)

Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V
• Ambient temperature	Topr	–20 to +75	℃

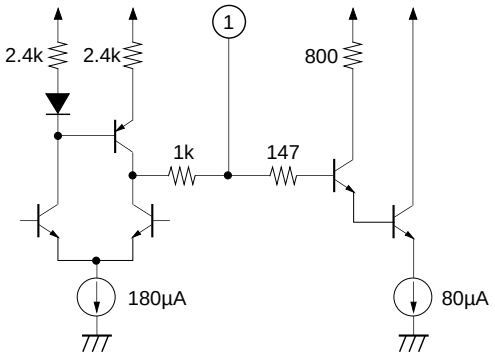
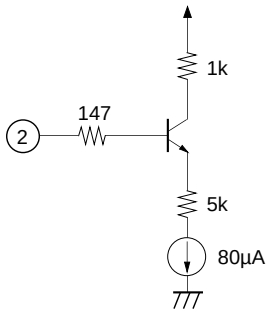
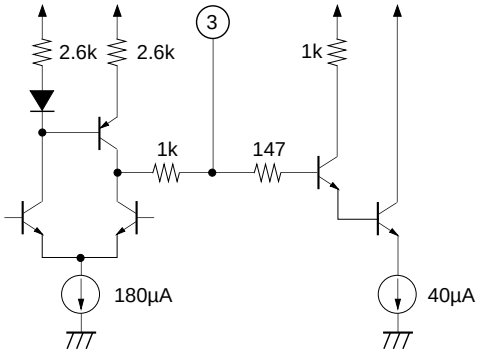
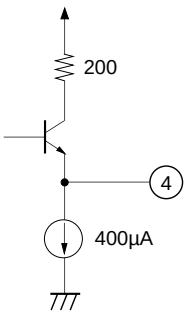
Block Diagram and Pin Configuration

(Top View)

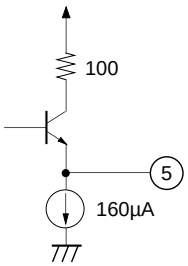
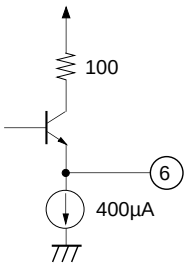
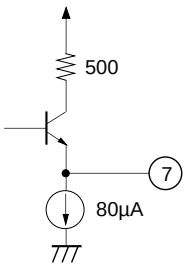
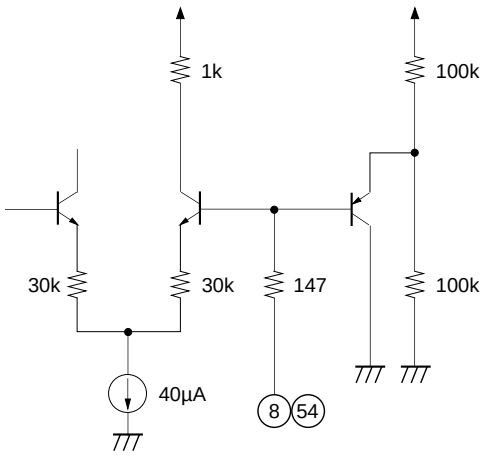


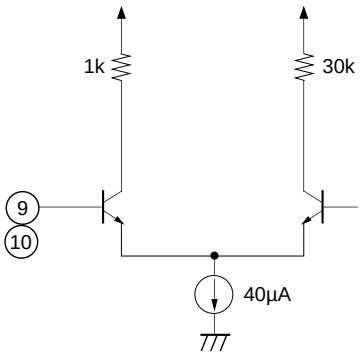
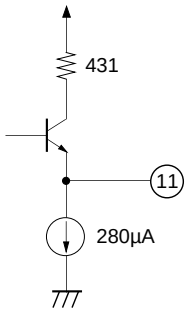
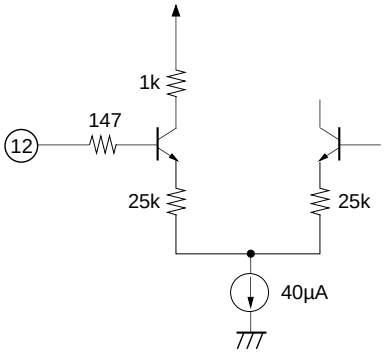
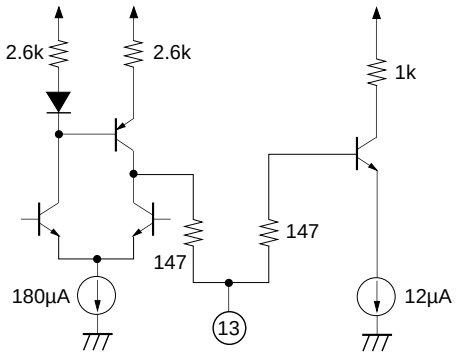
E89Z18-ST

Pin Description

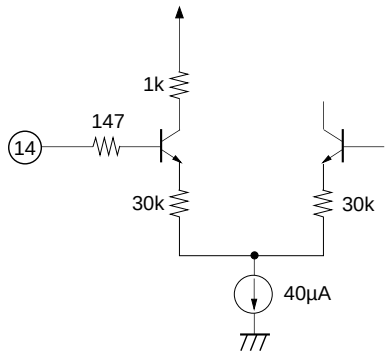
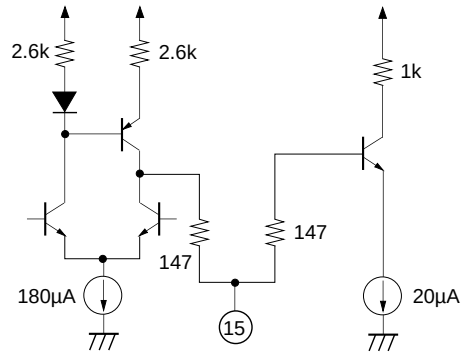
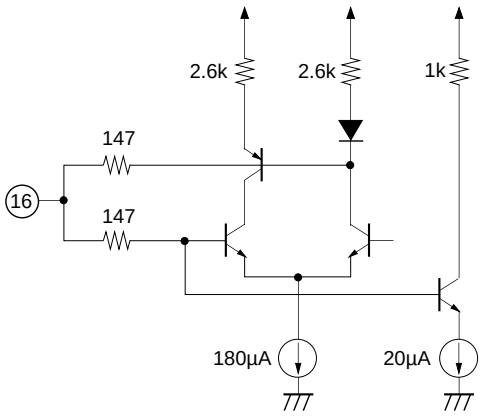
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CLP C Y_H	3 to 3.5V		Capacitor connecting pin for Y_H clamp (Clamp at CLP2)
2	DL Y_H IN	3.65V		DL Y_H signal input pin (Input from 1H delay line) Sig: Typ. 200mV (Positive polarity)
3	CLP C DL Y_H	2.6 to 3.8V		Capacitor connecting pin for DL Y_H clamp (Clamp at CLP4)
4	DL Y_H OUT	2.7 to 3.1V		DL Y_H signal output pin (To 1H delay line) Sig: Typ. 400mV Max. 600mV (Negative polarity)

Note) Pin voltage for input and output pins indicate black level.

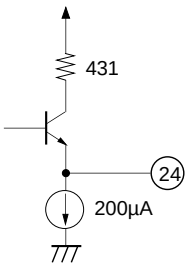
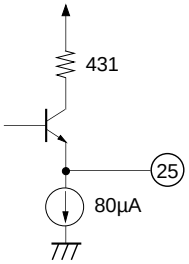
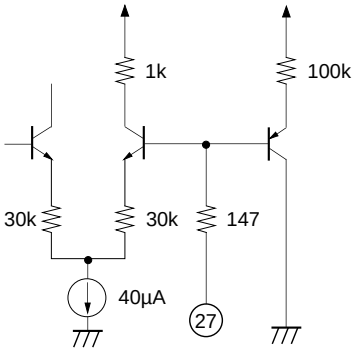
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
5	Y_H OUT1	1.9 to 2.3V		Y_H1 signal output pin Sig: Typ. 1V Max. 1.5V (Positive polarity)
6	Y_H OUT2	1.9 to 2.3V		Y_H2 signal output pin Sig: Typ. 1V Max. 1.5V (Positive polarity)
7	TP	2.6 to 3.0V (Y_H) 2.5 to 2.9V (G)		TP OUT (adjusting pin) 1H mode: Outputs Y_H1–Y_H0 0H mode: Outputs Gch C-slice OUT (Mode selection is executed through Pin 8)
8	DL Y_H GAIN	0V (0H Mode) 1.8 to 5V (1H Mode)		DL Y_H signal gain control pin (For 1H delay line gain compensation of Y_H) TP (Pin 7) mode selection 0H Mode: 0V 1H Mode: 1.8 to 5V
54	Y1 GAIN	0V: Common control by Pin 57 1.8 to 5V Independent control		DLY_1 signal gain control pin (1H delay line gain compensation) 0V: DLY_1 signal gain control is executed in common with DLY_2 signal gain control. 1.8 to 5V: DLY_1 signal gain control is executed independently from DLY_2 signal gain control.

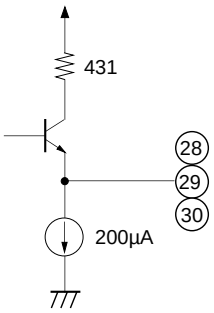
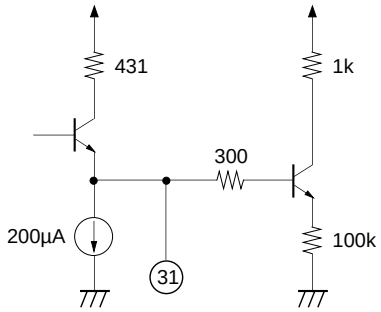
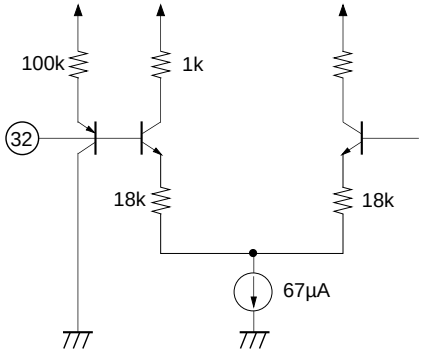
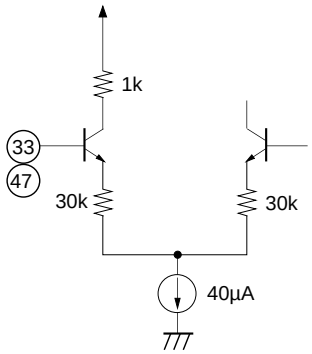
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
9	CLP4	5V 0		CLP4 pulse input pin (BLK clamp) (CMOS level input, V_{TH} = 2.5V)
10	CLP2	5V 0		CLP2 pulse input pin (OPB clamp) (CMOS level input, V_{TH} = 2.5V)
11	VAP OUT	2.6 to 3.0V		V-APCN signal output pin* Sig: Max. 1.2Vp-p
12	VAP GAIN	1.8 to 5V (Control)		V-APCN signal output level adjustment pin
13	CLP C VAP	3.4 to 3.8V		Capacitor connecting pin for VAP clamp (Clamp at CLP4)

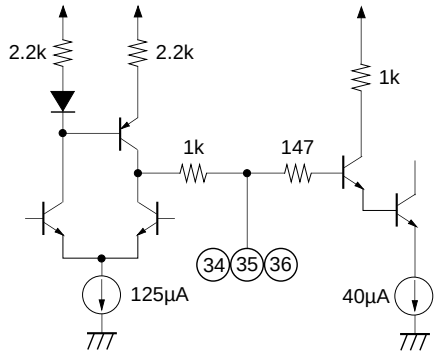
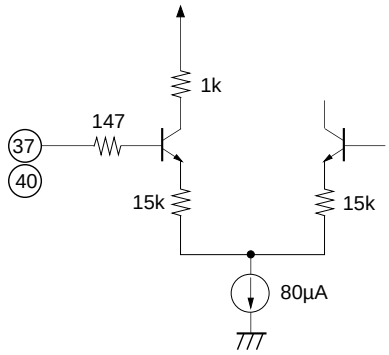
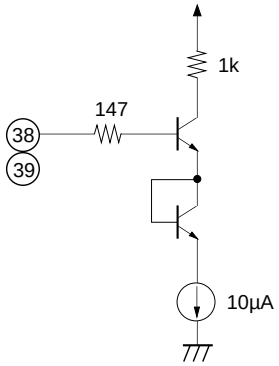
* V-APCN: Vertical Aperture Compensation

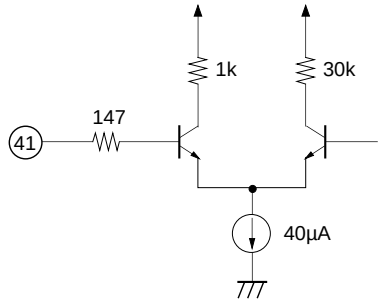
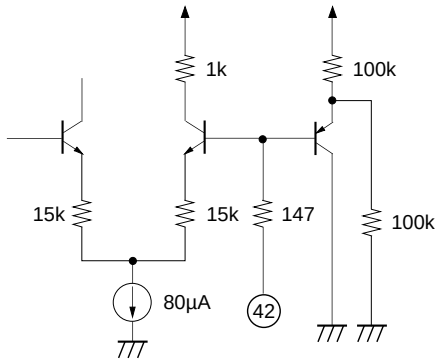
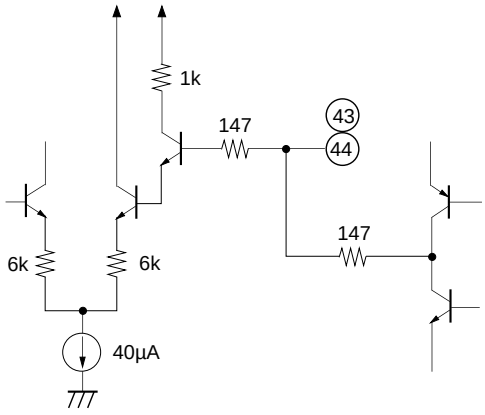
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
14	VAP SLICE	1.8 to 5V (Control)		V-APCN signal dark slice volume adjustment pin
15	CLP C CS	3.5 to 3.7V		Capacitor connecting pin for CS clamp (Clamp at CLP4)
16	CS IN	C-Couple input 2.9 to 3.3V		AGC CS signal input pin Sig: Max. 1V

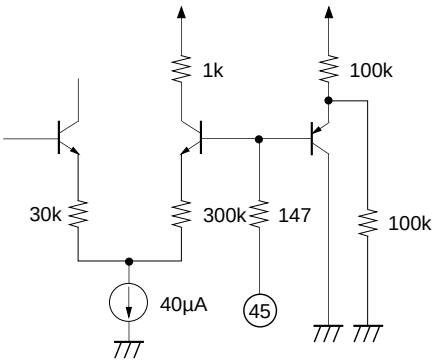
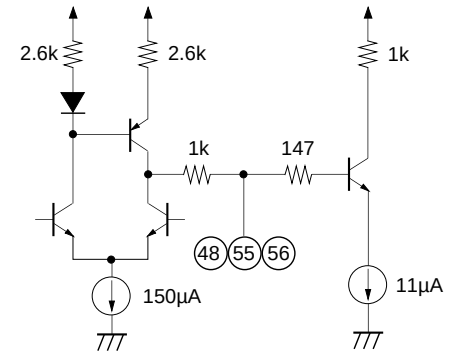
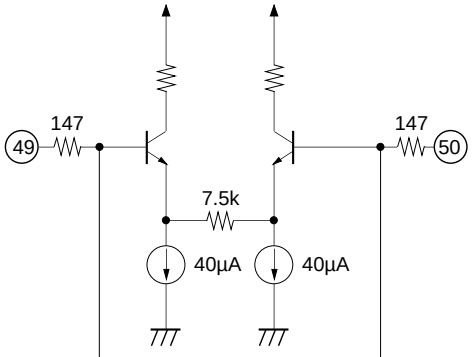
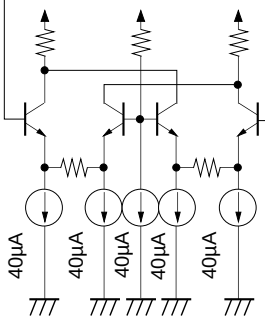
17	R–Y GAIN	0V: R–G output 1.8 to 5V: R–Y output		R–Y signal output level adjustment pin Pin 20 Mode select 0V: R–G output 1.8 to 5V: R–Y output
18	B–Y GAIN	0V: B–G output 1.8 to 5V: B–Y output		B–Y signal output level adjustment pin Pin 19 Mode select 0V: B–G output 1.8 to 5V: B–Y output
23	CS GAIN	1.8 to 5V (Control)		V-APCN CS signal gain control pin
19	B–Y OUT	2.75 to 3.15V (Hue OFF) 2.35 to 2.75V (Hue ON)		
20	R–Y OUT			
46	DLC_0 OUT	1.8 to 2.2V		
52	DLY_0 OUT	1.4 to 1.8V		
53	DLY_1 OUT	2.8 to 3.2V		
21	B–Y Hue	0V:		B–Y hue control pin
				R–Y hue control pin

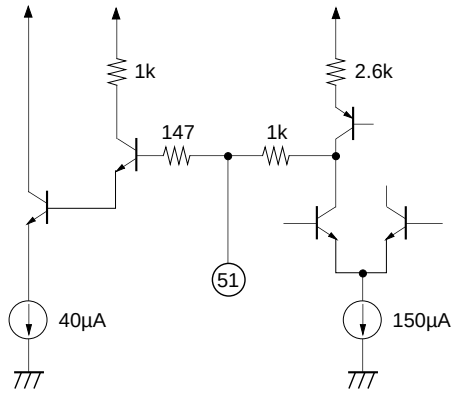
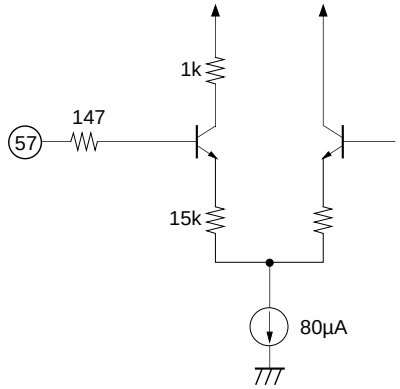
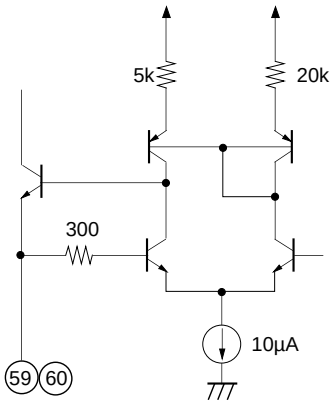
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
24	CS OUT	1.5 to 1.8V		CS signal output pin Sig: Max. 1V
25	Y_L OUT	1.9 to 2.3V		Y_L signal output pin
26	GND1			GND
27	C-γ CONT	0V: Typ. γ curve		Chroma (R.G.B) γ curve adjustment pin

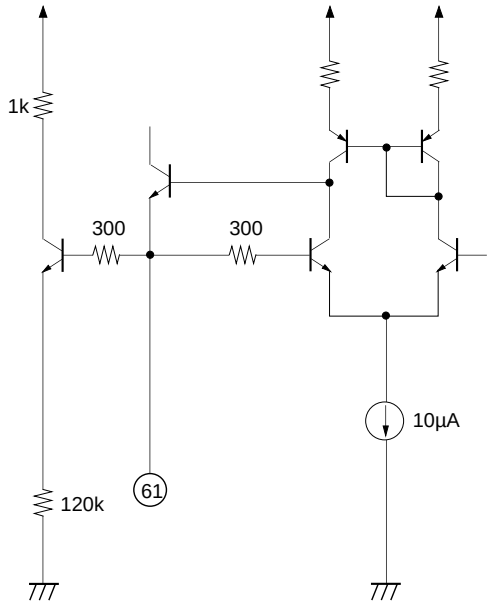
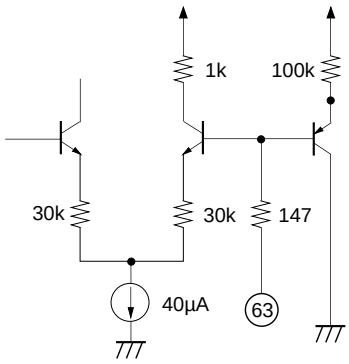
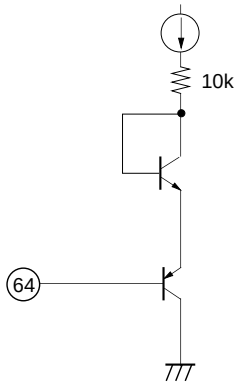
PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
28	WB R	1.4 to 2V		R signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
29	WB G	1.4 to 2V		G signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
30	WB B	1.4 to 2V		B signal output pin WB Mode: Sig: Typ. 400mV γ Mode: Sig: Typ. 500mV
31	WB DC	1.4 to 2V		When used as output pin, it is an Auto WB DC output pin. Pin 28, 29 and 30 turn to WB mode. When connected to Vcc: Pins 28, 29 and 30 turn to γ mode.
32	C SLICE	0V: Slice OFF		Chroma (R.G.B) signals dark slice level adjustment pin
33	C LEVEL	1.8 to 5V (Control)		Chroma (R.G.B) gain control pin (Chroma modulation factor control for all 3 channels)
47	C_1 GAIN	1.8 to 5V (Control)		DL C_1 signal gain control pin (1H delay line gain compensation)

PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
34	CLP C R	3.0 to 3.6V		Capacitor connecting pin for R WB amplifier clamp (Clamp at CLP2)
35	CLP C G	3.0 to 3.6V		Capacitor connecting pin for G WB amplifier clamp (Clamp at CLP2)
36	CLP C B	3.0 to 3.6V		Capacitor connecting pin for B WB amplifier clamp (Clamp at CLP2)
37	R GAIN	1.8 to 5V (Control)		Rch WB amplifier gain control pin (Pre-WB)
40	B GAIN	1.8 to 5V (Control)		Bch WB amplifier gain control pin (Pre-WB)
38	R CONT	2.5 to 4.6V		Rch WB amplifier gain control pin
39	B CONT	2.5 to 4.6V		Bch WB amplifier gain control pin

PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
41	ID	5V 0		ID pulse (color discrimination pulse) input pin (CMOS level V_{IH} = 2.5V) ID = L $C_0 \rightarrow C_R$ $C_1 \rightarrow C_B$ ID = H $C_0 \rightarrow C_B$ $C_1 \rightarrow C_R$
42	B MTX	1.8 to 5V (Control) 0V (Preset)		B signal operations MTX coefficient adjustment pin (Coefficient 0.22) Refer to Note 2.
43	CLP C MPX2	2.7 to 3.1V		Capacitor connecting pin for MPX clamp (Clamp at CLP2)
44	CLP C MPX1	2.7 to 3.1V		

PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
45	R MTX	1.8 to 5V (Control) 0V (Preset)		R signal operations MTX coefficient adjustment pin (Coefficient 0.617) Refer to Note 2.
48	DLC1 IN	C-Couple input 3.1 to 3.5V		DL C1 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
55	DLY1 IN	C-Couple input 3.6 to 4.0V		DL Y1 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
56	DLY2 IN	C-Couple input 3.6 to 4.0V		DL Y2 signal input pin Sig: Typ. 150mVp-p (Negative polarity)
49	S2 IN	1.9V		S2 signal input pin Sig: Typ. 500mV Max. 1500mV
50	S1 IN	1.9V		S1 signal input pin Sig: Typ. 500mV Max. 1500mV

PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
51	CLP C Y_0	3.3 to 3.7V		Capacitor connecting pin for Y_0 clamp (Clamp at CLP4)
57	Y_2 GAIN	1.8 to 5V (3H Mode) 0V (2H Mode)		DL Y_2 signal gain control pin (1H delay line gain compensation) V-APCON mode selection 0V: 2H Mode 1.8 to 5V: 3H Mode
58	GND2			GND
59	LPF Adj. 1	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the LPF for 1H DL. (External resistor in the range of 15 to 27kΩ)
60	LPF Adj. 2	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the chroma LPF (LPF for R, G, B, CS). (External resistor in the range of 15 to 62kΩ)

PIn No.	Symbol	Pin voltage	Equivalent circuit	Description
61	LPF Adj. 3	1.8 to 2.2V		Connecting pin of the external resistor that determines the characteristics of the LPF for V-APCN. (External resistor in the range of 15 to 62kΩ) When connected to Vcc, the LPF for V-APCN turns OFF.
62	Vcc			Power supply 5V (Typ.)
63	Y-γ CONT	0V (Typ. γ curve) 1.8 to 5V (Control)		Y_H γ curve adjustment
64	Y_H IN	0.95V		Y_H signal input Sig: Typ. 220mV Max. 660mV

Electrical Characteristics

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption		ID		25	34.5	43	mA
S2–S1 Amp Gain		SSG	Input: S1 IN = –62.5mV, S2 IN = 62.5mV Calculations: DLC_0 OUT/S1 IN	–3	–1.95	–1	dB
DLC_1 gain control	Max.	DLC_1H	Input: DLC_1IN = 100mV Conditions: C_1Gain = 5V C-level = 5V Calculations: (WB-R/DLC_1IN) –CG Note2)	6	7	9	dB
	Min.	DLC_1L	Conditions: C_1Gain = 0V (Others same as DLC_1H)	–2	–0.85	0	dB
S1+S2 Amp		SAG	Input: S1 IN = 500mV Calculations: DLY_0OUT/S1 IN	–15	–14	–13	dB
Chroma matrix (Gch) Note 3)	Gch Y	GY	Input: S1 IN = S2 IN = 300mV Conditions: C-level = 5V Calculations: WB-G (ID = H, L average)	80	100	120	mV
	C_R/Y	GC_R	Input: S1 IN = S2 IN = 62.5mV Conditions: C-level = 5V Calculations: WB-G/GY (ID = L)	0.9	1	1.1	—
	–C_B/Y	GC_B	ID = H (Others same as GC_R)	–1.1	–1	–0.9	—
Chroma matrix (Rch) Note 3)	Rch C_R	RC_R	Input: S1 IN = –62.5mV, S2 IN = 62.5mV Conditions: C-level = 5V Calculations: WB-R (ID = L)	70	85	100	mV
	Y (Preset)	RYP	Input: S1 IN = S2 IN = 500mV Conditions: C-level = 5V Calculations: WB-R/RC_R (ID = H)	0.15	0.168	0.186	—
	Y (Max.)	RYH	RMTX = 5V (Others same as RYP)	0.22	0.25	0.27	—
	Y (Min.)	RYL	RMTX = 1.8V (Others same as RYP)	0.11	0.125	0.14	—
Chroma matrix (Bch) Note 3)	Bch–C_B	BC_B	Input: S1 IN = 62.5mV, S2 IN = –62.5mV Conditions: C-level = 5V Calculations: WB-B (ID = H)	80	100	120	mV
	Y (Preset)	BYP	Input: S1 IN = S2 IN = 500mV Conditions: C-level = 5V Calculations: WB-B/BC_B (ID = H)	0.2	0.22	0.24	—
	Y (Max.)	BYH	BMTX = 5V (Others same as BYP)	0.31	0.34	0.37	—
	Y (Min.)	BYL	BMTX =1.8V (Others same as BYP)	0.13	0.15	0.17	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
WB GAIN	RCONT Max.	RCH	Input: DLC_1IN = –200mV Conditions: C-level = 5V RCONT = 4.6V (ID = H) Calculations: WB-R/WB-RTyp. Note 4) WB-R Typ. is the tested output of WB-R when RCONT is set to 4V (Other inputs, conditions same as RCH)	7.5	8.2	8.5	dB
	RCONT Min.	RCL	Test: RCONT = 2.5V (Others same as RCH)	–8.4	–7.9	–7.4	dB
	BCONT Max.	BCH	Input: DLC_1IN = 150mV Conditions: C-level = 5V BCONT = 4.6V (ID = L) Calculations: WB-B/WB-BTyp. Note 4) WB-B Typ. is the tested output of WB-B when BCONT is set to 4V (Other inputs, conditions same as BCH)	7.5	8.2	8.5	dB
	BCONT Min.	BCL	Test: BCONT = 2.5V (Others same as BCH)	–8.4	–7.9	–7.4	dB
	RGAIN Max.	RGH	Input: DLC_1IN = –200mV Conditions: RCONT = 2.5V RGAIN = 5V C-level = 5V (ID = H) Calculations: WB-R/WB-RMin. WB-R Min. is the tested WB-R, when tested under the same conditions as RCL.	8.6	9.2	—	dB
	BGAIN Max.	BGH	Input: DLC_1IN = 150mV Conditions: BCONT = 2.5V BGAIN = 5V C-level = 5V (ID = L) Calculations: WB-B/WB-BMin. WB-B Min. is the tested WB-B, when tested under the same conditions as BCL.	11.4	12.2	—	dB

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Bch color difference matrix Note 5)	R–G OUT/ WB-B	BMBY	Input: S1IN = 200mV S2IN = 160mV DLC1IN = 220mV Conditions: C-γ CONT = WB DC = C-Slice = C-level = 5V RCONT = 2.5V BCONT = 4.6V (ID = L) Calculations: B–Y OUT/WB-B	0.4	0.44	0.48	—
	R–Y OUT/ WB-B	BMRY	Conditions: R–Y GAIN = 1.8V Calculations: R–Y OUT/WB-B (Others same as BMBY)	–0.24	–0.21	–0.17	—
	B–Y GAIN Max.	BMG	Conditions: BCONT = 4V 1. B–Y OUT is tested when B–Y gain = 0V and taken as A. (Other conditions are the same as BMBY) 2. B–Y OUT is tested when B–Y gain = 5V and taken as B. (Other conditions are the same as BMBY) Calculations: B/A	3.0	3.3	—	—
	B–Y Hue Max.	BMHH	Conditions: B–Y HUE = 1.8V (Others same as BMBY) Calculations: R–Y OUT/B–Y Typ. B–Y Typ. is the value of the tested B–Y OUT when B–Y hue=0V (Other conditions are the same as BMBY). Note 6)	0.58	0.68	—	—
	B–Y Hue Min.	BMHL	B–Y HUE = 5V (Others same as BMHH)	—	–0.67	–0.58	—
Gch color difference matrix Note 5)	R–Y/R–G	GMR	Input: S1IN = 830mV S2IN = 660mV DLC1IN = –230mV Conditions: WB-DC = C-level = 5V RCONT = BCONT = 2.5V 1. R–Y OUT is tested when R–Y gain = 0V and taken as A. 2. R–Y OUT is tested when R–Y gain = 1.8V and taken as B. Calculations: B/A	0.81	0.85	0.89	—
	B–Y/B–G	GMB	Input: (The same as GMR) Conditions: 1. B–Y OUT is tested when B–Y gain = 0V and taken as A. 2. B–Y OUT is tested when R–Y gain = 1.8V and taken as B. (Others same as GMR) Calculations: B/A	0.63	0.66	0.7	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
C-Slice	Typ.–Min.	CSLL	Input: DLY1IN = –400mV Conditions: C-level = 5V Y1GAIN = 1.8V C-Slice = 1.8V (ID = H) Calculations: C-Slice Typ. -TP C-Slice Typ. is the TP output of C-Slice = 0V.	0	5	15	mV
	Typ.–Max.	CSLH	Conditions: C-Slice =5V (Others same as CSLL)	95	120	145	mV
Gch γ curve	C-γ CONT=0V Gch-WB=400mV	γTyp.	Input: DLY1IN = –200mV S1IN = S2IN = 500mV Conditions: Y1GAIN = 1.8V C-level is valied and adjusted to obtain 400mV at WB-G. After that C-level is fixed during test. WB-DC is set to OPEN during C-level adjusted and set to 5V during test. Calculations: WB-G is tested.	450	500	550	mV
	C-γ CONT=0V Gch-WB=800mV	γL8	Input: DLY1IN = –400mV S1IN = S2IN = 1000mV Conditions: Same as γ Typ. Calculations: WB-G/γ Typ.	1.13	1.2	1.25	—
	C-γ CONT=0V Gch-WB=100mV	γL1	Input: DLY1IN = –50mV S1IN = S2IN = 125mV (Others same as γL8)	0.36	0.4	0.44	—
	C-γ CONT=1.8V Gch-WB=400mV	γM4	Input: DLY1IN = –200mV S1IN = S2IN = 500mV Conditions: Cγ CONT = 1.8V Calculations: WB-G/γ Typ.	0.9	1	1.1	—
	C-γ CONT=1.8V Gch-WB=800mV	γM8	Input: DLY1IN = –400mV S1IN = S2IN = 1000mV (Others same as γM4)	1.13	1.2	1.25	—
	C-γ CONT=1.8V Gch-WB=100mV	γM1	Input: DLY1IN = –50mV S1IN = S2IN = 125mV (Others same as γM4)	0.45	0.5	0.55	—
	C-γ CONT=5V Gch-WB=400mV	γH4	Input: DLY1IN = –200mV S1IN = S2IN = 500mV Conditions: Cγ CONT = 1.8V Calculations: WB-G/γ Typ.	0.9	1	1.1	—
	C-γ CONT=5V Gch-WB=800mV	γH8	Input: DLY1IN = –400mV S1IN = S2IN = 1000mV (Others same as γH4)	1.13	1.2	1.25	—
	C-γ CONT=5V Gch-WB=100mV	γH1	Input: DLY1IN = –50mV S1IN = S2IN = 125mV (Others same as γH4)	0.26	0.3	0.35	—

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Yγ	Yγ1.0 (Typ.)	YγT	Input: Y_HIN = 220mV Calculations: DLY_HOUT	–440	–400	–360	mV
	Yγ2.0/Yγ1.0	Yγ2.0	Input: Y_HIN = 440mV Calculations: DLY_HOUT/YγT	1.23	1.37	1.51	—
	Yγ0.5/Yγ1.0	Yγ0.5	Input: Y_HIN = 110mV Calculations: DLY_HOUT/YγT	0.59	0.66	0.73	—
	Yγ0.5 (Max.)/ Yγ1.0	YγH	Input: Y_HIN = 110mV Conditions: Yγ CONT = 1.8V Calculations: DLY_HOUT/YγT	0.64	0.71	0.78	—
	Yγ0.5 (Min.)/ Yγ1.0	YγL	Input: Y_HIN = 110mV Conditions: Yγ CONT = 5V Calculations: DLY_HOUT/YγT	0.54	0.6	0.66	—
TP	TP (YH)	TPY	Input: Y_HIN = 220mV Conditions: DLY_HGAIN = 1.8V Calculations: TP/DLY_HOUT	–5	–4	–3	dB
	TP (DLY_H)	TPDY	Input: DLY_HIN = YγT × 0.7 Conditions: Same as TPY Calculations: TP/–DLY_HOUT Note 7)	–5	–4	–3	dB
	TP (GWBS)	TPG	Input: S1IN = S2IN = 500mV DLY1IN = 200mV Conditions: Y1GAIN = 1.8V Calculations: TP/WB-G	–2	0	2	dB
Y_H AMP	Min. Gain	YLG	Input: Y_HIN = 220mV DLY_HIN = – [YγT × –3.5dB] Conditions: DLY_HGAIN = 1.8V Calculations: TP is tested to check that the signal level is below 0mV in relation to black level. Note 8)	—	—	3.5	dB
	Max. Gain	YHG	Input: Y_HIN = 220mV DLY_HIN = – [YγT × –12dB] Conditions: DLY_HGAIN = 5V Calculations: TP_{TP} is tested to check that the signal level is over 0mV in relation to black level. Note 8)	12	—	—	dB
Chroma level Max./Min.		GCL	Input: DLC_1IN = 200mV Conditions: 1. WB-G is tested when C-level = 5V and taken as GC-level Min. 2. WB-G is tested when C-level = 1.8V and taken as GC-level Max. (Both 1 and 2 test at ID-H.) Calculations: GC-level Max. / GC-level Min.	1.55	1.65	1.75	—
WB DC		WDDC	Test: WB-DC	1.4	1.6	2	V

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Y_L Note 5)	Y_LOUT/ RγOUT	Y_LR	Input: S1IN = 150mV S2IN = 450mV Conditions: C-γ CONT = WB DC = C-Slice = C-level = 5V RCONT = 4.6V BCONT = 2.5V BGAIN = 1.8V (ID = L) Calculations: Y_LOUT/WB-R	0.27	0.3	0.34	—
	Y_LOUT/ BγOUT	Y_LB	Input: S1IN = 200mV S2IN = 160mV DLC_1IN = 220mV Conditions: C-γ CONT = WB DC = C-Slice = C-level = 5V RCONT = 2.5V BCONT = 4.6V (ID = L) Calculations: Y_LOUT/WB-B	0.08	0.1	0.12	—
	Y_LOUT/ GγOUT	Y_LG	Input: S1IN = 830mV S2IN = 660mV DLC_1IN = –230mV Conditions: WB-DC = C-level = 5V RCONT = BCONT = 2.5V Calculations: Y_LOUT/WB-G	0.54	0.6	0.66	—
Y_HOUT1 (OH mode)		YH1Z	Input: Y_HIN = 220mV Calculations: Y_HOUT1 is tested.	900	1000	1100	mV
Y_HOUT1 1H/0H		YH1O	Input: DLY_HIN = – (YγT × –4dB) Conditions: DLY_HGAIN = 1.8V Calculations: Y_HOUT1/YH1Z Note 8)	–1	0	1	dB
Y_HOUT2 (0H) /Y_HOUT1		YH2Z	Input: Y_HIN = 220mV Calculations: Y_HOUT2/YH1Z	–1	0	1	dB
Y_HOUT2 (1H) /Y_HOUT1		YH2O	Input: Y_HIN = 220mV Conditions: DLY_HGAIN = 1.8V Calculations: Y_HOUT2/Y_HOUT2Typ. Y_HOUT2Typ. is Y_HOUT2 output tested at YH2Z.	–6.5	–6	–5.5	dB
VAP Typ. Note 9)		VAPT	Input: S1IN = S2IN = 125mV Conditions: VAP GAIN = 1.8V VAP Slice = 1.8V Y_2 GAIN = 1.8V Calculations: VAP OUT is tested.	–250	–200	–150	mV
VAP Slice Note 9)		VS	Input: S1IN = S2IN = 1000mV Conditions: Y_2 GAIN = 1.8V 1. VAP OUT is tested when VAP Slice=1.8V and taken as SMin. 2. VAP OUT is tested when VAP Slice=5V and taken as SMax. Calculations: SMax.–SMin. Note 10)	256	320	384	mV

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
DLY_1 gain Note 11)	Min.	DY_1L	Input: S1IN = S2IN = 500mV DLY_1IN = –200mV Conditions: VAP GAIN = VAP Slice = Y_1GAIN = 1.8V Calculations: VAP-OUT is tested to check that the signal level is over 0mV in relation to black level.	—	—	0	dB
	Max.	DY_1H	Input: S1IN = S2IN = 500mV DLY_1IN = –110mV Conditions: VAP GAIN = VAP Slice = 1.8V Y_1GAIN = 5V Calculations: VAP-OUT is tested to check that the signal level is below 0mV in relation to black level.	5	—	—	dB
DLY_2 gain Note 11)	Min.	DY_2L	Input: S1IN = S2IN = –167mV DLY_2IN = –66.7mV Conditions: VAP GAIN = VAP Slice = Y_1GAIN = Y_2GAIN = 1.8V Calculations: VAP-OUT is tested to check that the signal level is over 0mV in relation to black level.	—	—	0	dB
	Max.	DY_2H	Input: S1IN = S2IN = –167mV DLY_2IN = –37.5mV Conditions: Y_2GAIN = 5V (Others same as DY_2L) Calculations: VAP-OUT is tested to check that the signal level is below 0mV in relation to black level.	5	—	—	dB
CS Note 12)	VCS Typ.	VCST	Input: S1IN = S2IN = 167mV Conditions: Y_1GAIN = Y_2GAIN = 1.8V CS GAIN = 5V Calculations: CS OUT is tested.	90	120	150	mV
	VCS Min.	VCSL	Conditions: CS GAIN = 0V (Others same as VCST) Calculations: CS OUT/VCST	—	0	0.05	—
	VCS Max.	VCSH	Conditions: CS GAIN = 1.8V (Others same as VCSL)	4.4		—	—
	VCS Typ.	CST	Input: CS-IN = 500mV	440	465	490	mV

Note 1) For pins without specific instructions regarding input, feed the DC value shown on the Test Circuit. Calculations are mentioned utilizing the pin name or the electrical characteristics symbols. Otherwise, for exceptional notations explanatory notes, are given with every case.

Note 2) In this item, the gain of DLC_1 amplifier exclusively is calculated. CG is the gain of the system from DLC_1 IN to WB-R from which DLC_1 GC amplifier gain has been excluded.

—CG calculating method—

In the actual calculation, the system on C_0 side is utilized.

Input: S1IN = –62.5mV S2IN = 62.5mV

Condition: Same as DLC_1H

Calculations: CG = 20log (WB-R/DLC_0OUT)

Note 3) Chroma matrix operations

$R = 2 [C_R + \alpha Y]$ α: Control with RMTX (Preset 0.167)

$G = Y – (C_R + C_B)$

$B = 2 [C_B + ß (Y – C)]$ ß: Control with BMTX (Preset 0.22)

Note 4) With the typical gain taken when R CONT is at 4V, compare with the gain during Max. and Min. The same for B CONT.

Note 5) Adjustment and testing is performed so that signals are output only for each of R, G, B channels respectively.

Note 6) Comparison with B–Y OUT when R–Y HUE = 0V (HUE OFF).
The same for B–Y HUE.

Note 7) The compensation of difference in gain of Y_H0 andY_H1 is as follows.

1) At DLY_H GAIN = 1.8V, DLY_H amplifier gain is 3dB.
2) Test DLY_H OUT (tested at YrT) when Y_H IN = 220mV signal is input.
3) The difference in gain between Y_H0 and Y_H1 is compensated by inputting the signal as –3dB to DLY_H IN.

Note 8) The amplifier input is varied and the gain confirmed.

Note 9) VAP (Vertical Aperture Compensation)

Note 10) Dark slice variable volume. (Output level difference between the value slice volume at Max. and slice volume at Min.)

Note 11) Utilizing V-APCN 2H mode, DLY_1 amplifier exclusive gain is obtained through operations. However, as the amplifier gain cannot be tested directly, only the upper and lower limits of the gain control are checked according to the following method.

(a) Lower limit check

S1 IN = S2 IN = 500mV (At that time KNEE circuit input turns to 200mV)

DLY_1 IN = –200mV (For others refer to the conditions chart)

In this condition, if we have VAP OUT ≥ 0, this indicates that DLY_1 amplifier is below 0dB.

(b) Upper limit check

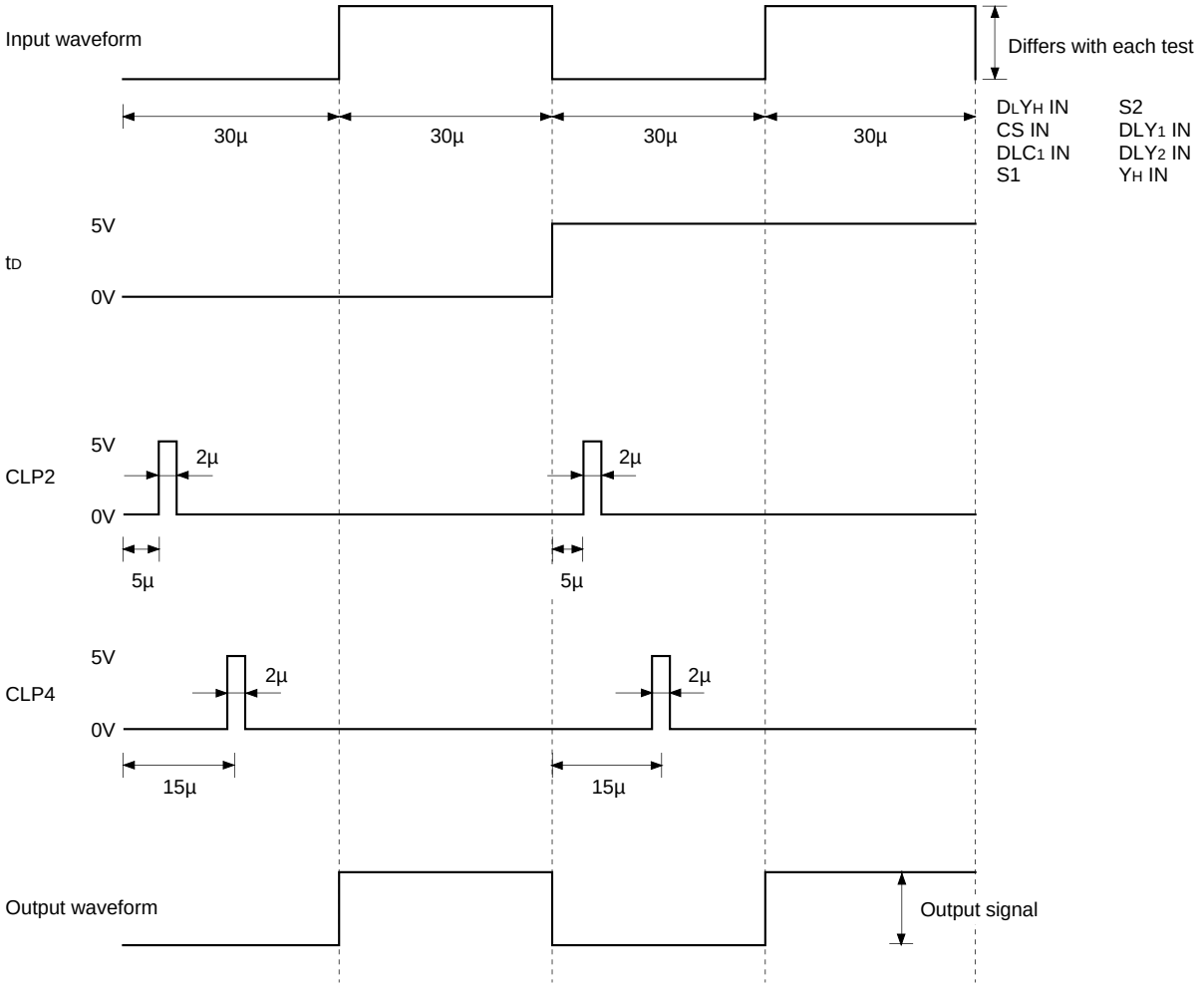
S1 IN = S2 IN = 500mV

DLY_1 IN = –110mV (in (a) the –5dB of –200mV)

In this condition, if we have VAP OUT ≤ 0, this indicates that DLY_1 amplifier is above 5dB.

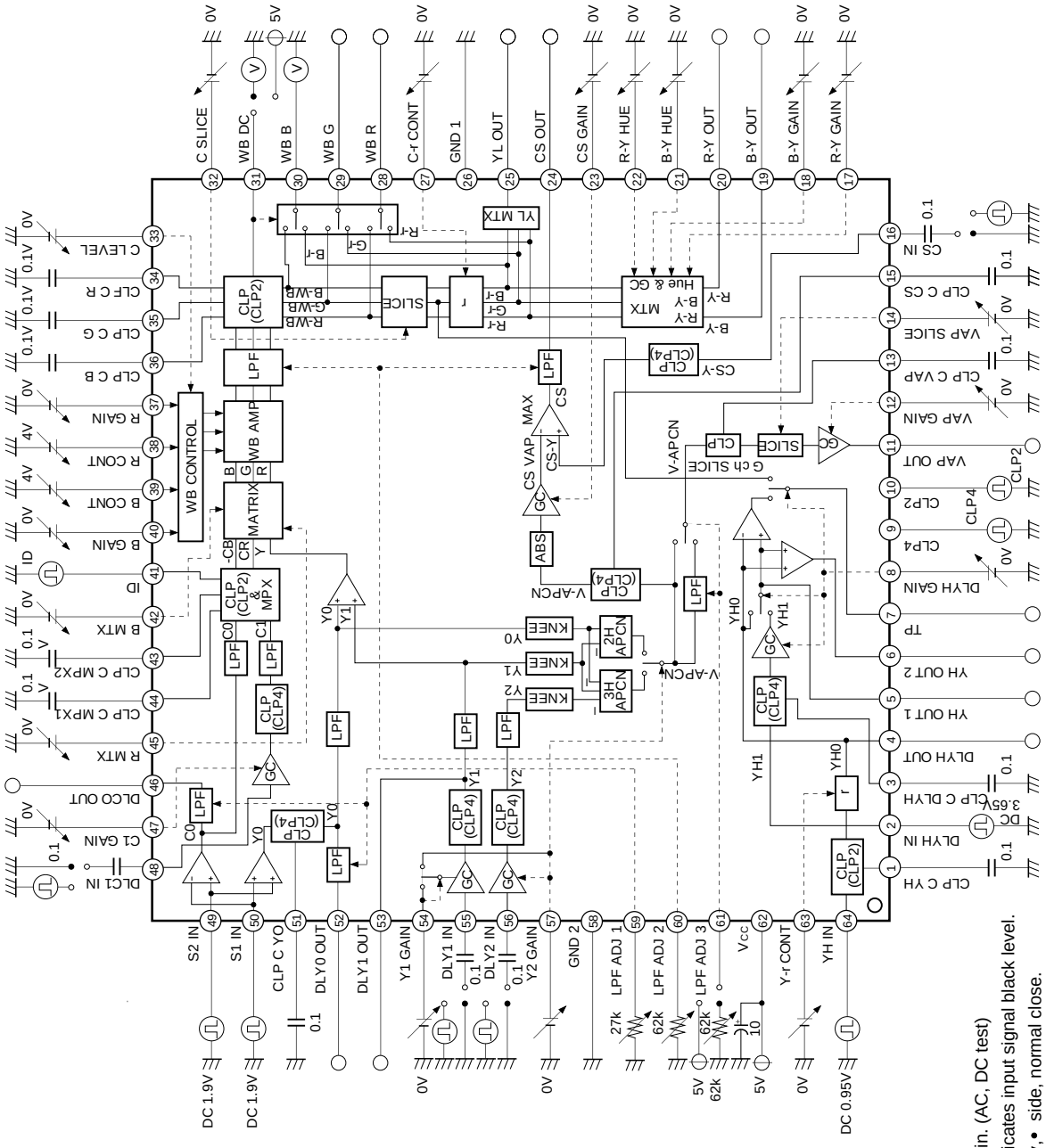
Note 12) CS (Chroma Suppress)

Timing Chart for Testing



DLYH OUT	B – Y OUT	WB_G
YH OUT1	R – Y OUT	WB_B
YH OUT2	CS OUT	DLC0 OUT
TP	YL OUT	DLY0 OUT
VAP_OUT	WB_R	DLY1 OUT

Test Circuit (Typ. setting)



Note 1) µF is unit of capacitor

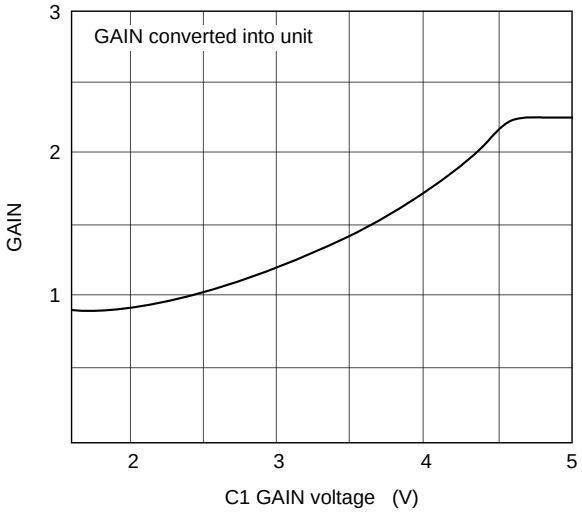
Note 2) —○ indicates testing pin. (AC, DC test)

Note 3) Input pin DC value indicates input signal black level.

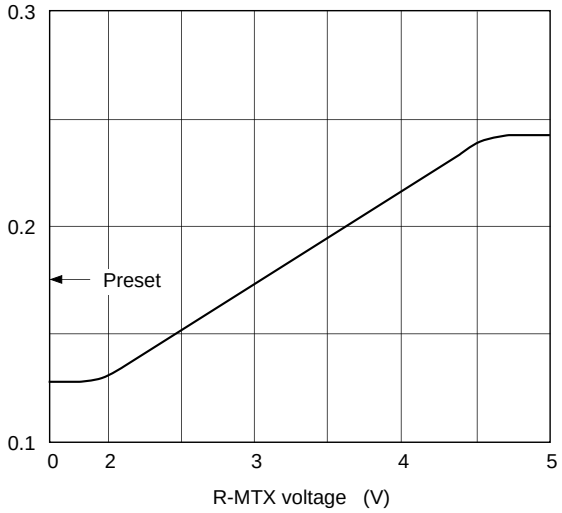
Note 4) —○•— indicate relay, • side, normal close.

Standard Control Characteristics (Vcc = 5V, Ta = 25°C)

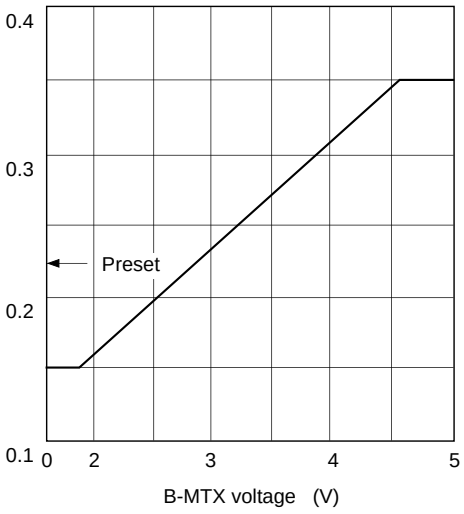
C1 GAIN control characteristics



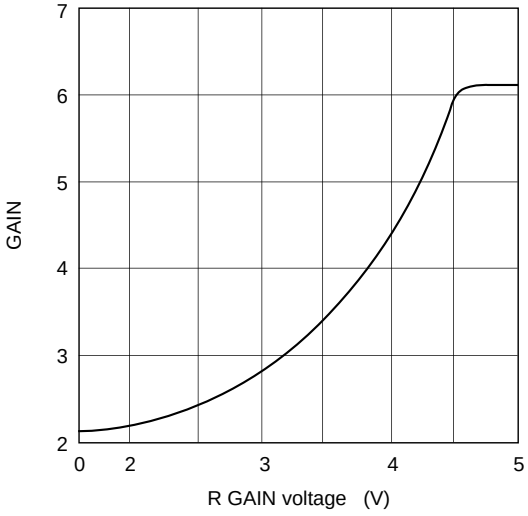
R-MTX coefficient



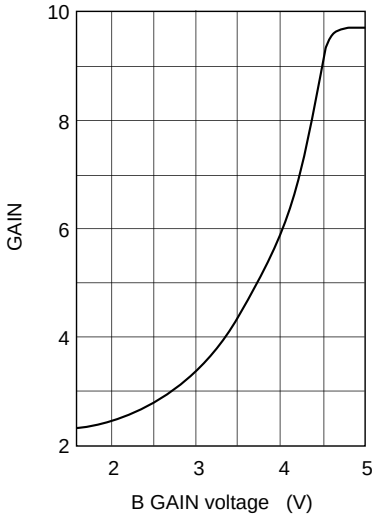
B-MTX coefficient



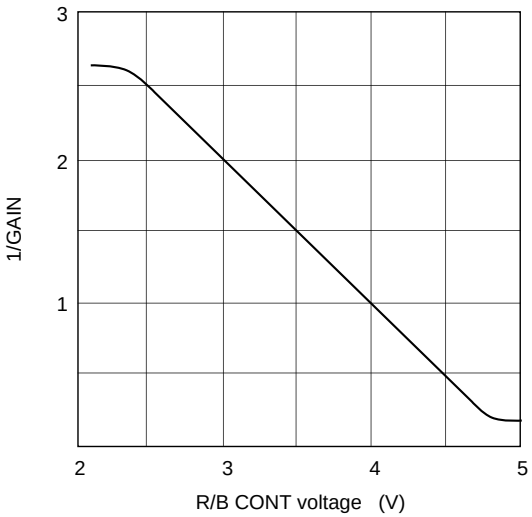
R GAIN control characteristics



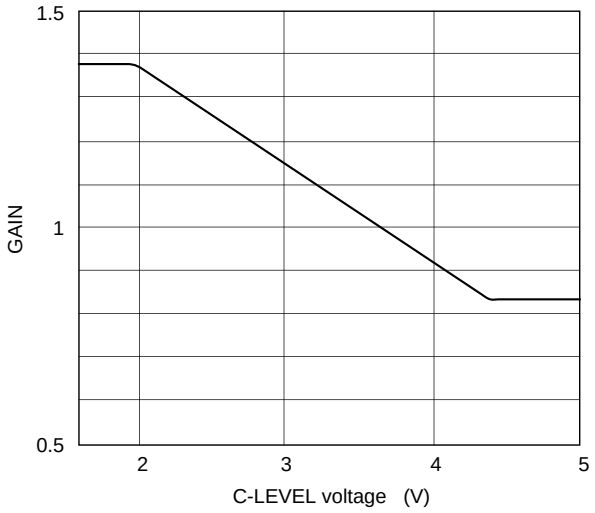
B GAIN control characteristics



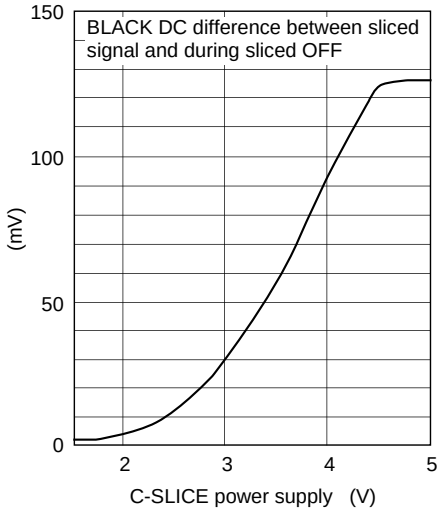
R/B CONT control characteristics



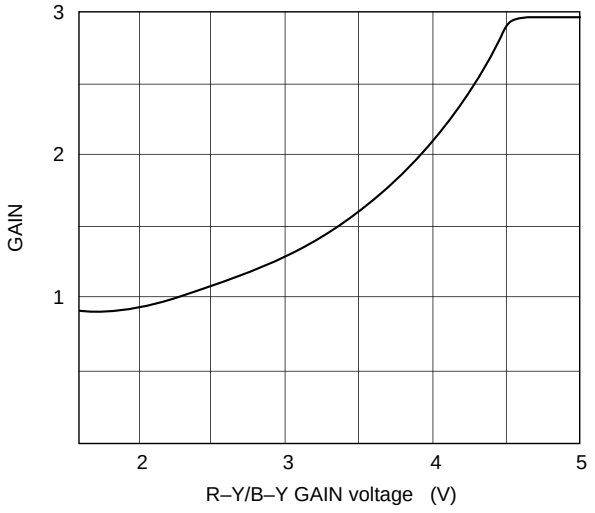
C-SLICE control characteristics



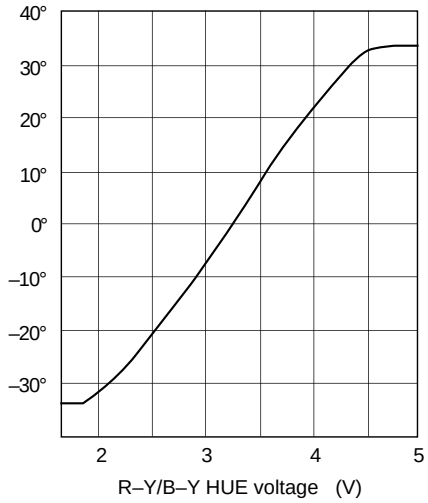
C-SLICE control characteristics



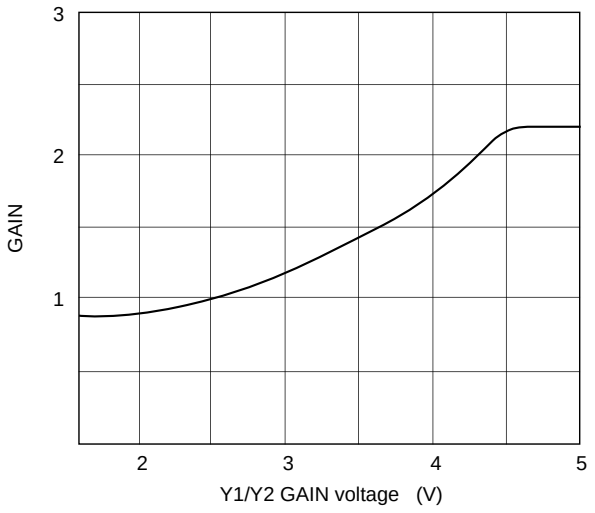
R–Y/B–Y GAIN control characteristics



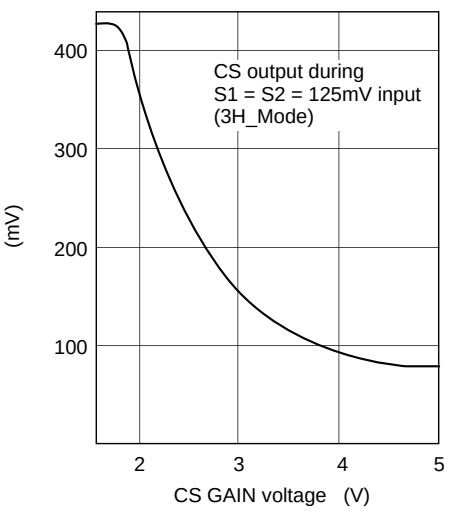
R–Y/B–Y HUE control characteristics



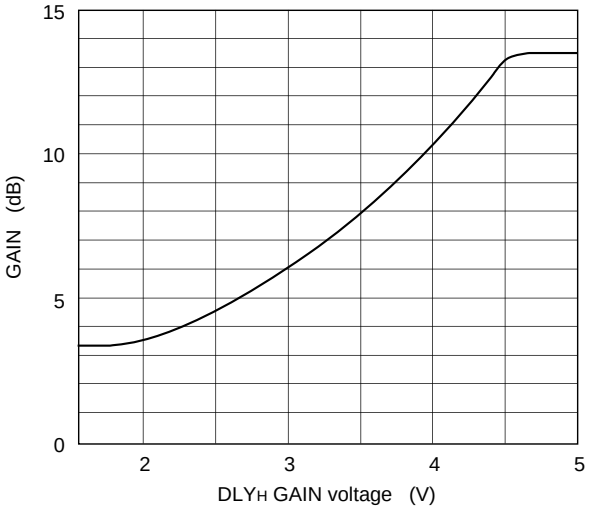
Y1/Y2 GAIN control characteristics



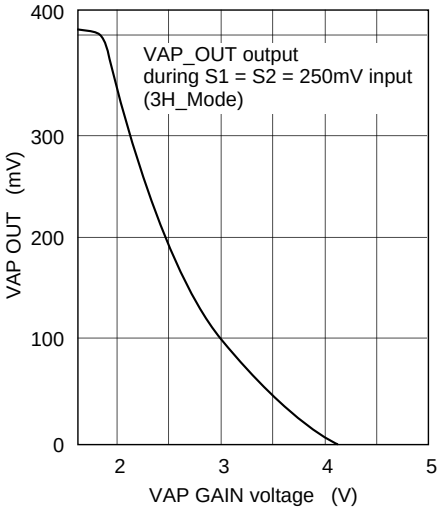
CS GAIN control characteristics



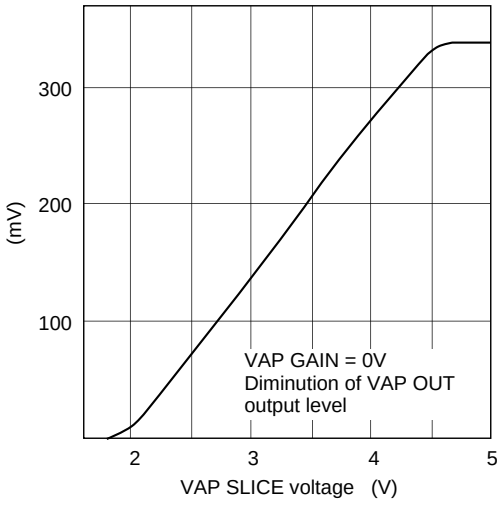
DLYH GAIN control characteristics



VAP control characteristics

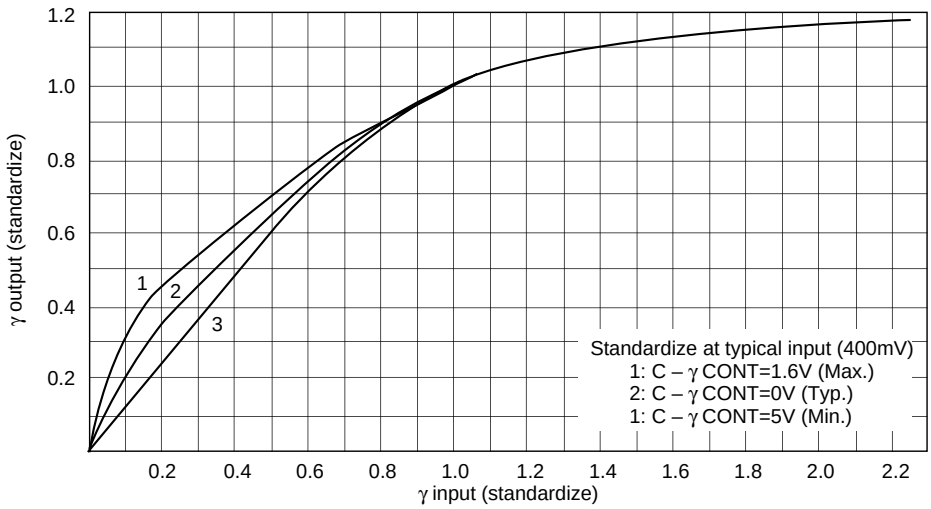


VAP SLICE control characteristics

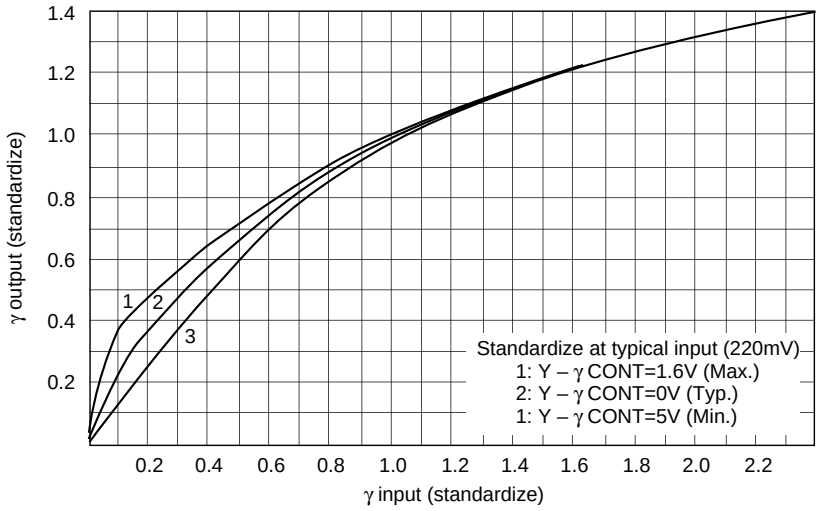


Standard Design Data

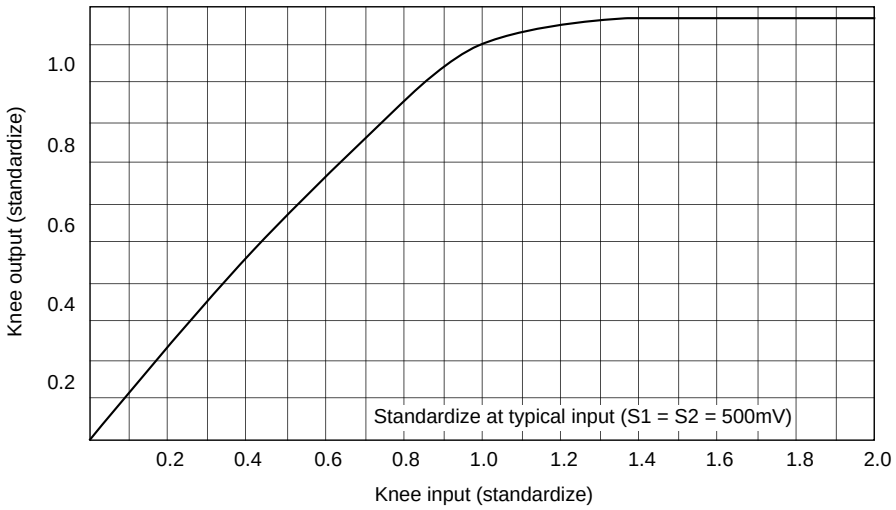
Chroma γ curve (standardize)



Y_H γ curve (standardize) (mV)

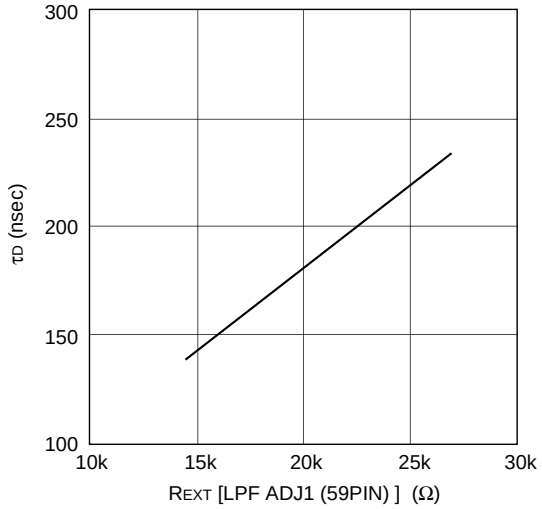


V-APCN Knee (standardize) (mV)

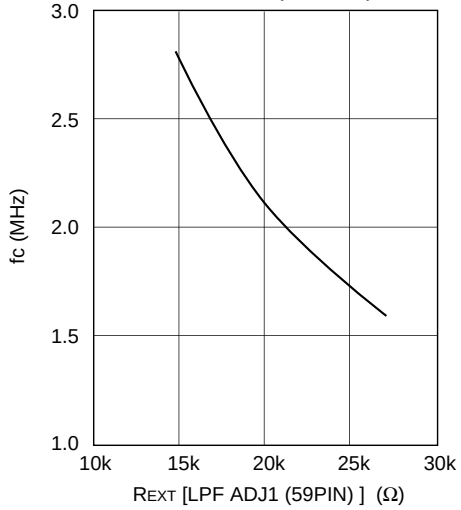


Pre-Filter Adjust characteristics ⟨S1, S2 → DL Y0 out / DL C0 out⟩

<Group Delay>



<Cut Off> (fc: –3dB)



Chroma Adjust characteristics ⟨S1, S2 → R–Y out / B–Y out⟩

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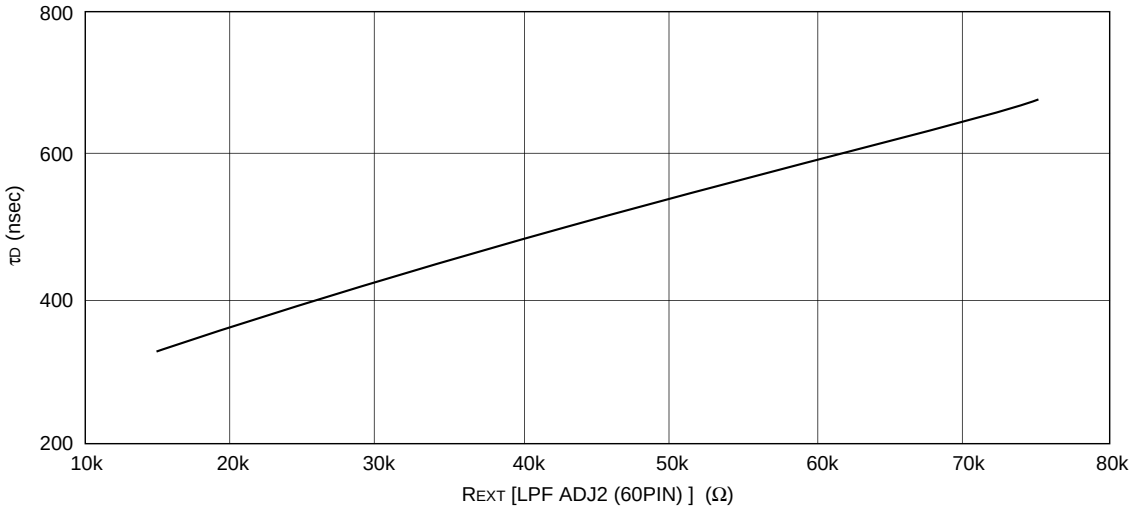

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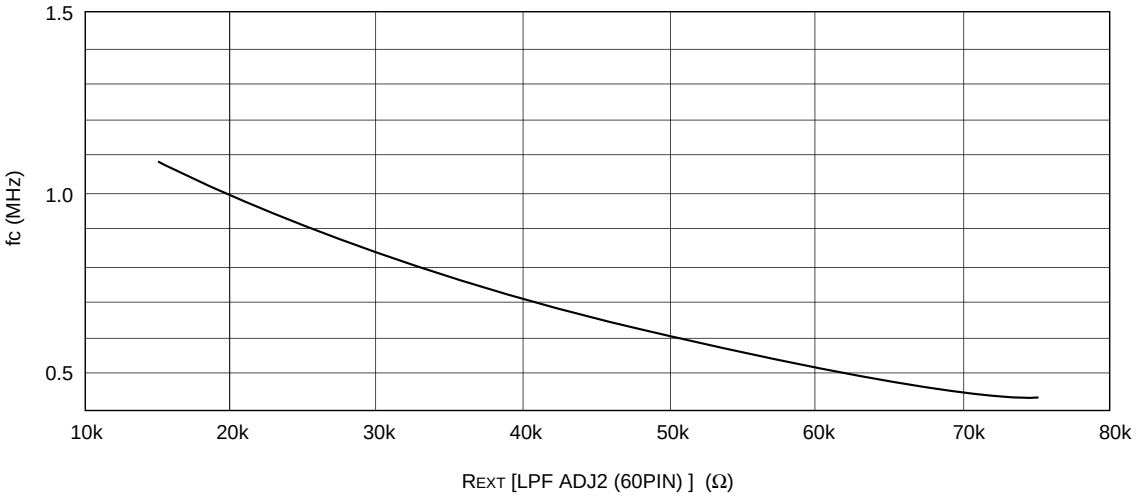

CS-VAP Adjust characteristics (S1, S2 → CS OUT)
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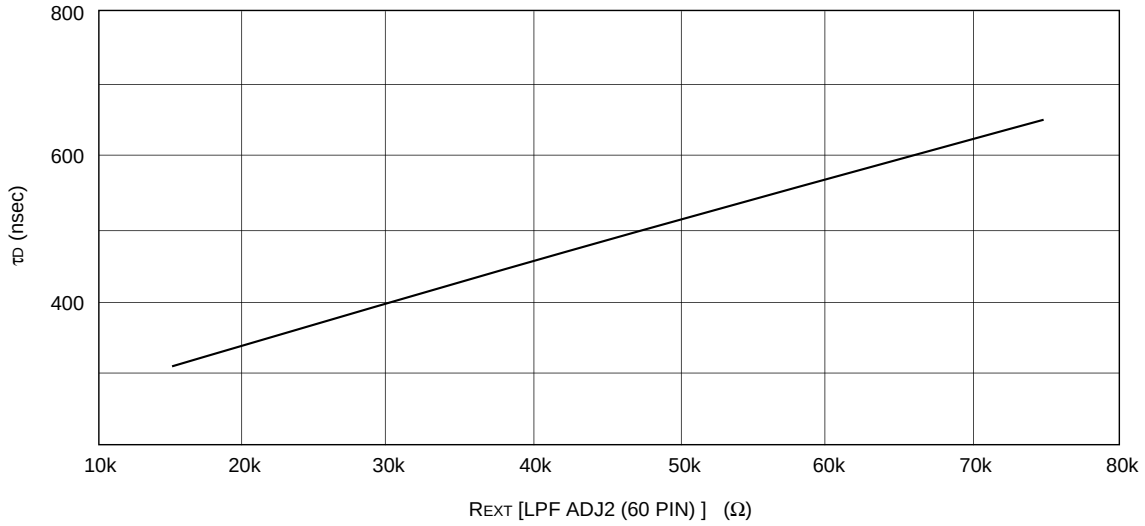

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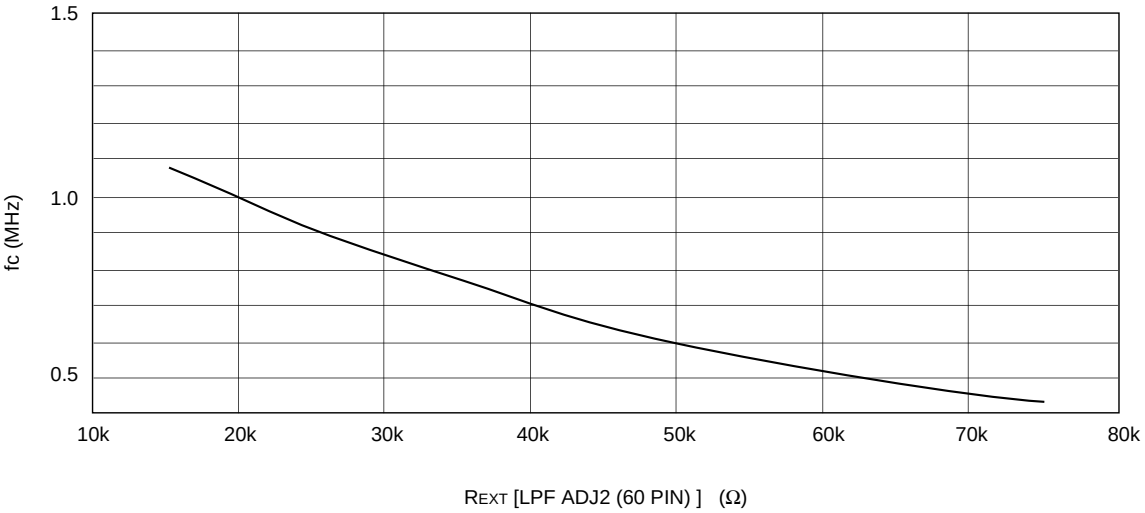

CS-Y LPF Adjust characteristics (CS IN → CS OUT)
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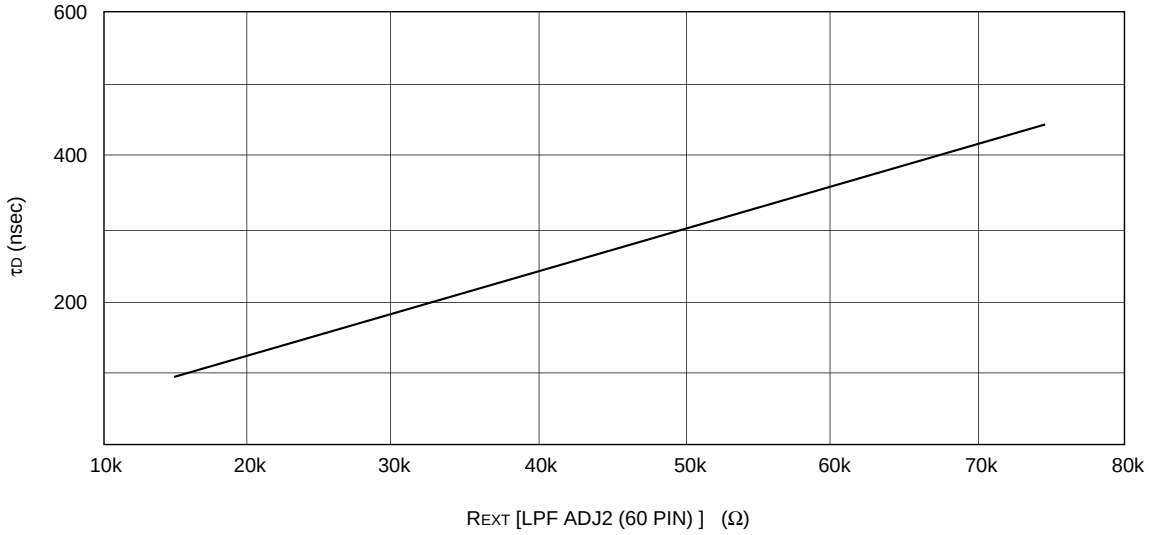

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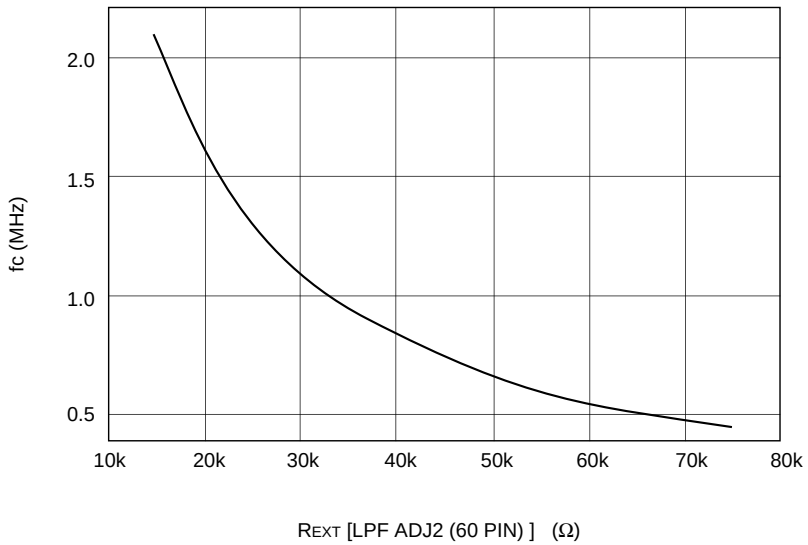
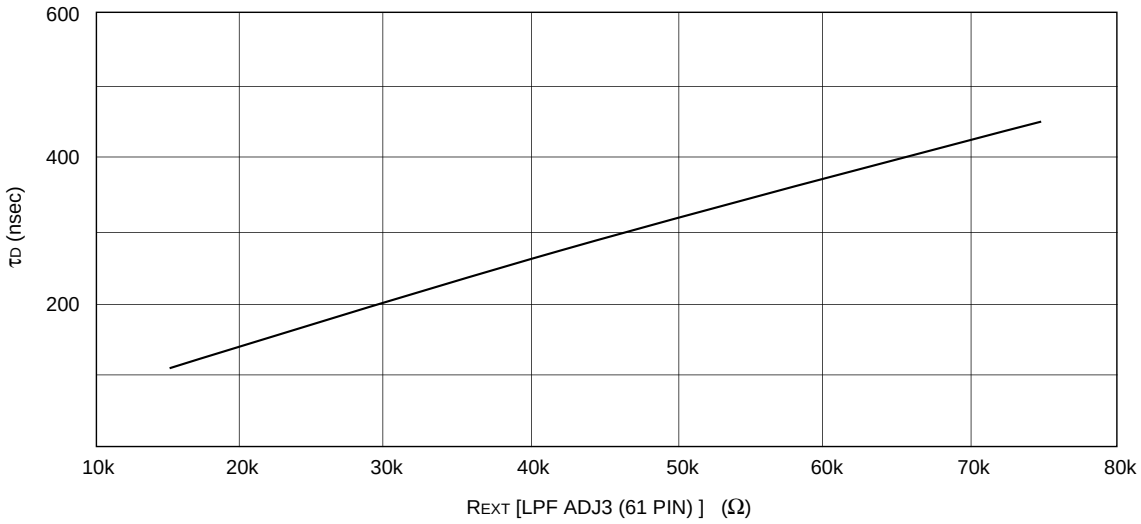


VAP LPF Adjust characteristics

VAP LPF Adjust characteristics (S1, S2 → VAP OUT)
<Group Delay>



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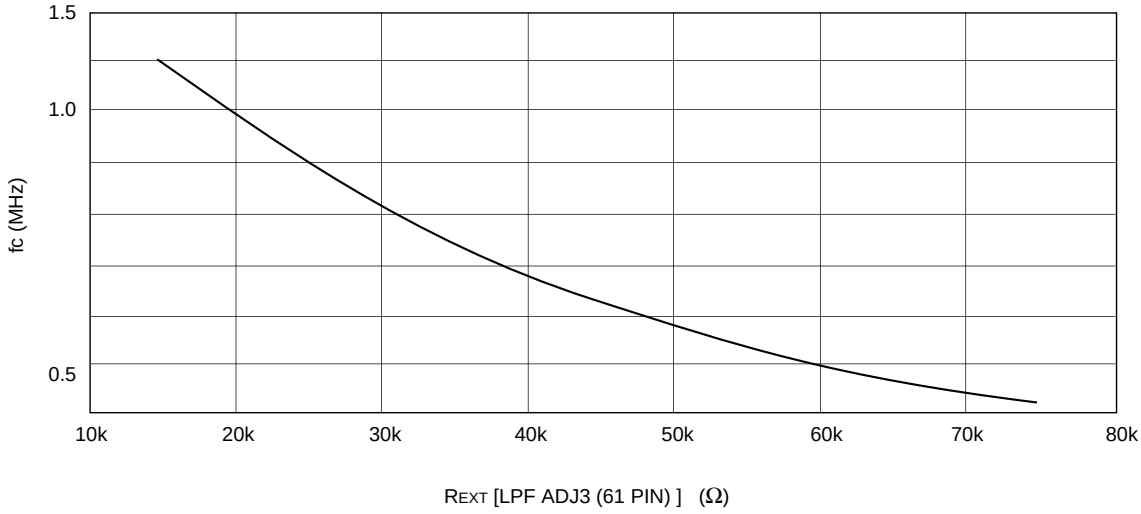
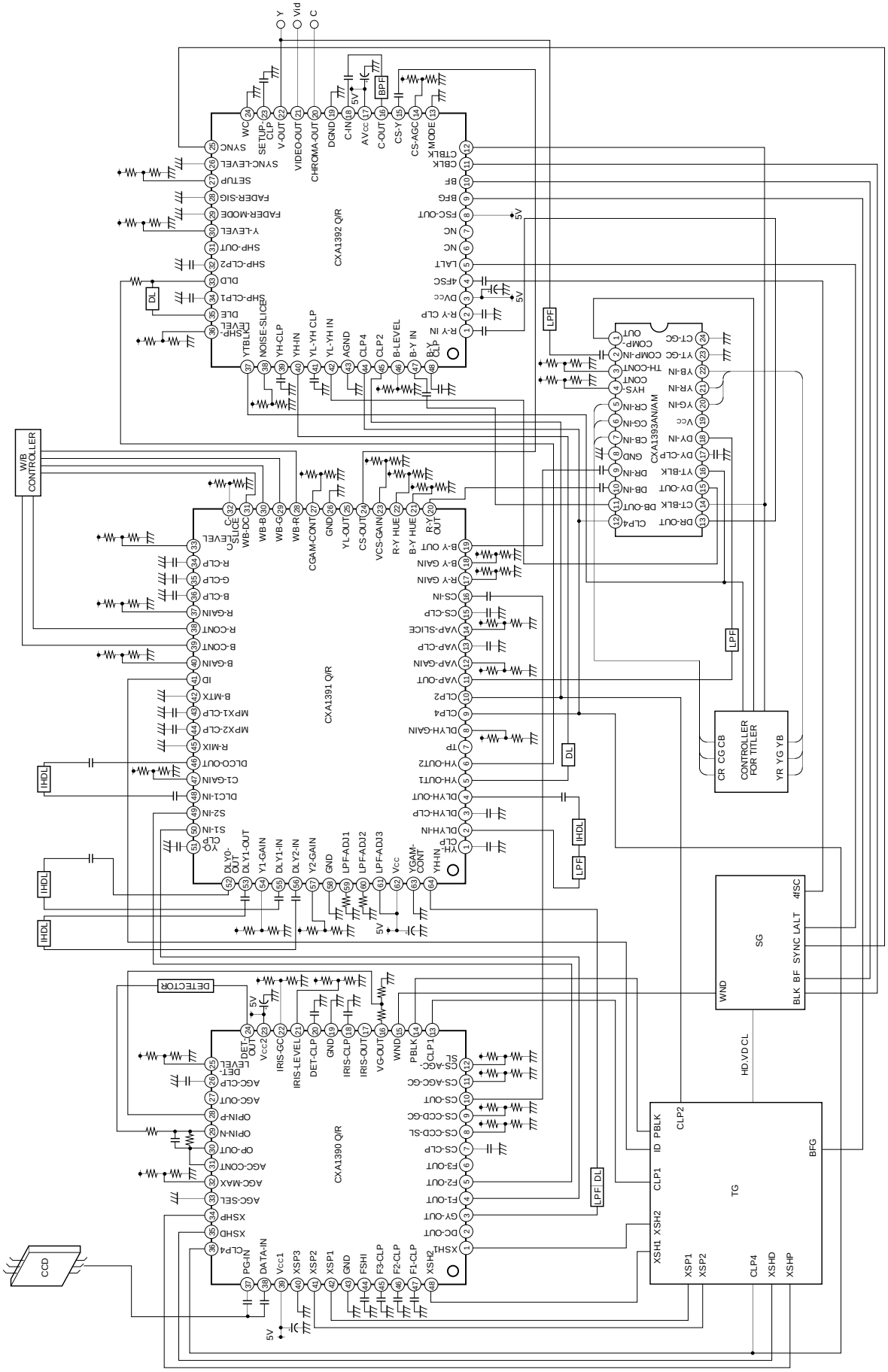


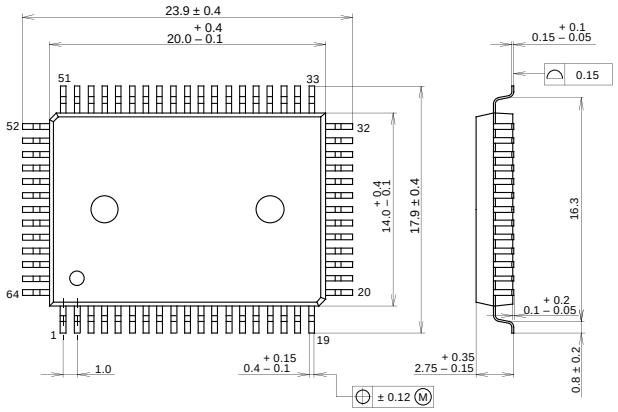
CXA Series System Diagram



Package Outline Unit: mm

CXA1391Q

64PIN QFP(PLASTIC)



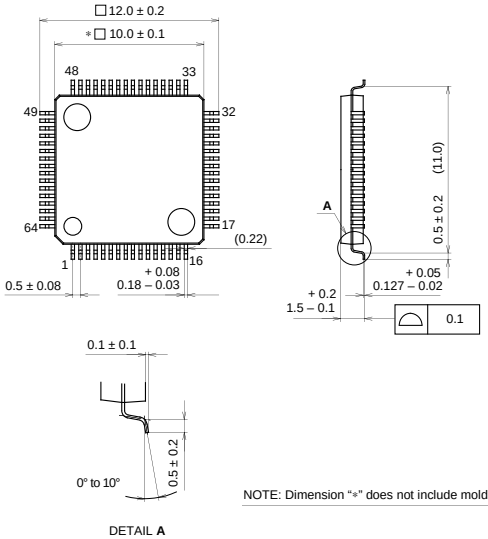
SONY CODE	QFP–64P–L01
EIAJ CODE	*QFP064–P–1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g

CXA1391R

64PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-64P-L01
EIAJ CODE	*QFP064-P-1010-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g