

## 8-bit 35 MSPS High-Speed D/A Converter

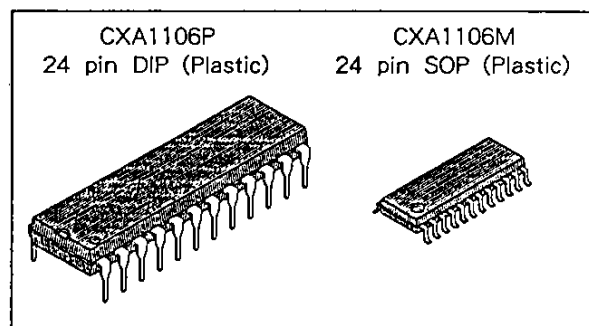
### Description

CXA1106P/M is an 8-bit 35MSPS high-speed D/A converter IC. Summing type current for the upper 2-bits and ladder type resistance for the lower 6-bits, ensure a low power consumption of 200 mW (Single power supply). This IC is suitable for digital TV's, graphic displays and other applications.

### Features

- Resolution 8-bit
- High speed operation  
35MSPS (Max. conversion speed)
- Non linear error  
less than  $\pm 1/2\text{LSB}$
- Low glitch
- TTL compatible input
- +5V single power supply or  $\pm 5\text{V}$  dual power supply
- Low power consumption
 

+5V single power supply	200 mW (Typ.)
$\pm 5\text{V}$ dual power supply	400 mW (Typ.)



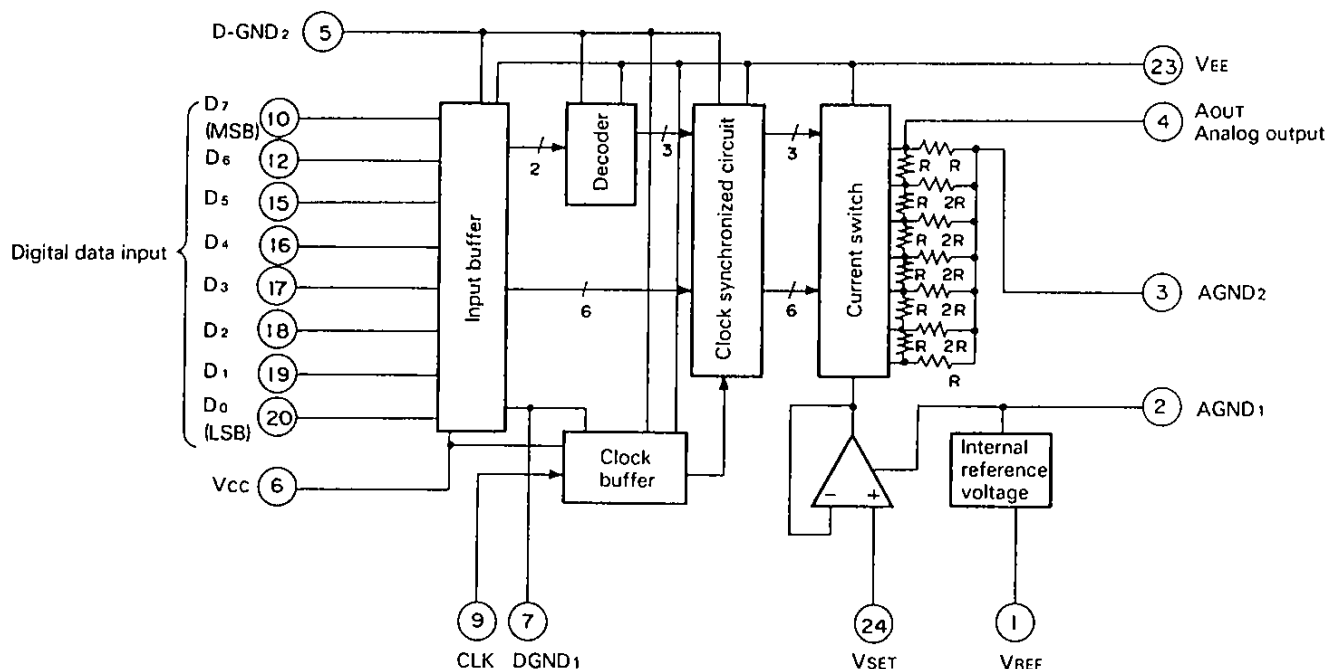
### Function

8-bit 35 MSPS D/A converter

### Structure

Bipolar silicon monolithic IC

### Block Diagram



**Absolute Maximum Ratings (Ta = 25°C)**

• Supply voltage	VCC-DGND1	0 to 6	V
	VEE-AGND1,2	-6 to 0	V
	DGND2-DGND1	0 to 6	V
• Digital input voltage	VI	DGND1-0.3 to VCC+0.3	V
	VCLK	DGND1-0.3 to VCC+0.3	V
• Input voltage (VSET pin)	VSET	VEE-0.3 to VEE+2.7	V
• Output current (VREF pin)	IREF	-5 to 0	mA
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-55 to +150	°C
• Allowable power dissipation	PD	1.27	W

**Recommended Operating Conditions****Single power supply**

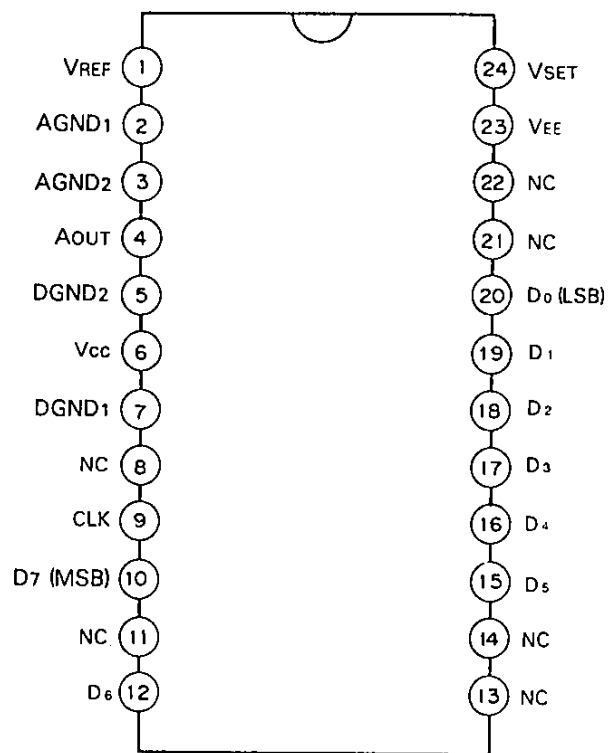
Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		VCC, DGND2 AGND1, AGND2	4.75	5.00	5.25	V
		DGND2-AGND1 DGND2-AGND2	-0.2	0	0.2	V
		AGND1-AGND2	-0.1	0	0.1	V
Digital input voltage	H level	VIH, VCLKH	2.0		VCC	V
	L level	VIL, VCLKL	DGND1		1.0	V
VSET input voltage		VSET	0.70	0.84	1.0	V
VREF pin current		IREF	-3.0		-0.4	mA
Clock pulse width*		TPW1	10			ns
		TPW0	10			ns

\*Note) See Fig. 6. Timing chart

**Dual power supply**

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		VCC	4.75	5.00	5.25	V
		VEE	-5.5	5.00	-4.75	V
		DGND2-AGND1 DGND2-AGND2	-0.2	0	-0.2	V
		AGND1-AGND2	-0.1	0	0.1	V
Digital input voltage	H level	VIH, VCLKH	2.0		VCC	V
	L level	VIL, VCLKL	DGND1		1.0	V
VSET input voltage		VSET	-4.30	-4.16	-4.00	V
VREF pin current		IREF	-3.0		-0.4	mA
Clock pulse width		TPW1	10			ns
		TPW0	10			ns

Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Description
1	VREF		Internal reference voltage output pin 1.2 V (Typ.) An external pull down resistance is necessary. For reference see Notes on Application 1 on page 15.
2	AGND1		Set to Analog Vcc for single power supply and to Analog GND for dual power supply. Connect to AGND2 and use.
3	AGND2		Connect to AGND1
4	AOUT		Analog output pin
5	DGND2		Set to Digital Vcc for single power supply and to Digital GND for dual power supply.
6	Vcc		Digital Vcc
7	DGND1		Digital GND
8	NC		Non-connection
9	CLK		Clock input pin

No.	Symbol	Equivalent circuit	Description
10, 12, 15 to 20	D7, D6, D5 to D0		Digital input pin D1 to MSB, D8 to LSB
11, 13, 14	NC		Non-connection
21, 22	NC		Non connection pin. But connect to AGND or VEE
23	VEE		Set to Analog GND for single power supply and to VEE for dual power supply.
24	VSET		Bias input pin Normally set VSET - VEE to 0.84V. For reference see Notes on Application 1.

See the Application Circuit for reference.

## Electrical Characteristics (Ta = 25°C)

## Single power supply

$$V_{CC} = DGND2 = AGND1 = AGND2 = 5V, DGND1 = V_{EE} = 0, V_{SET} = 0.84V$$

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution	n			8		bit
Maximum conversion speed	f <sub>MAX</sub>	R <sub>L</sub> > 10kΩ, C <sub>L</sub> < 20pF	35			MSPS
Linearity error	E <sub>L</sub>	R <sub>L</sub> > 10 KΩ	-0.5		+0.5	LSB
Differential linear error	E <sub>D</sub>		-0.5		+0.5	LSB
Full scale output voltage	V <sub>FS</sub>	R <sub>L</sub> > 10KΩ	0.9	1.0	1.1	V
Offset voltage*	V <sub>OS</sub>	R <sub>L</sub> > 10KΩ	0	4	10	mV
Output resistance	R <sub>O</sub>		290	350	410	Ω
Power supply current	I <sub>CC</sub>	R <sub>L</sub> > 10KΩ I <sub>REF</sub> = -400μA	32	40	48	mA
Digital input current	H level	I <sub>IH</sub>	0		5	μA
	L level	I <sub>IL</sub>	-400		0	μA
V <sub>SET</sub> input current	I <sub>SET</sub>		-3		0	μA
Internal reference output voltage	V <sub>REF</sub>	I <sub>REF</sub> = -400μA	1.17	1.25	1.33	V
Accuracy output voltage range	V <sub>OC</sub>	R <sub>L</sub> > 10KΩ	0.5	1.0	1.5	V
Set up time	t <sub>s</sub>		10			ns
Hold time	t <sub>h</sub>		2			ns
Propagation delay time	t <sub>PD</sub>	R <sub>L</sub> > 10KΩ		11		ns
Glitch energy	GE	R <sub>L</sub> > 10KΩ f <sub>CLK</sub> = 1 MHz Digital lamp output		30		pV-s

\*Note) V<sub>OS</sub> = AGND2 - V<sub>255</sub> (V<sub>255</sub> is the output voltage when full input is at high level)

## Dual power supply

 $V_{CC} = 5V, DGND1 = DGND2 = AGND1 = AGND2 = 0, V_{EE} = -5V, V_{SET} - V_{EE} = 0.84V$ 

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution	n			8		bit
Maximum conversion speed	f <sub>MAX</sub>	R <sub>L</sub> > 10kΩ, C <sub>L</sub> < 20pF	35			MSPS
Linearity error	E <sub>L</sub>	R <sub>L</sub> > 10KΩ	-0.5		+0.5	LSB
Differential linear error	E <sub>D</sub>		-0.5		+0.5	LSB
Full scale output voltage	V <sub>FS</sub>	R <sub>L</sub> > 10KΩ	0.9	1.0	1.1	V
Offset voltage	V <sub>OS</sub>	R <sub>L</sub> > 10KΩ	0	4	10	mV
Output resistance	R <sub>O</sub>		290	350	410	Ω
Power supply current	I <sub>CC</sub>	R <sub>L</sub> > 10KΩ I <sub>REF</sub> = -400μA	24	30	36	mA
	I <sub>EE</sub>		40	50	60	mA
Digital input current	H level	I <sub>IH</sub>	0		5	μA
	L level	I <sub>IL</sub>	-400		0	μA
V <sub>SET</sub> input current	I <sub>SET</sub>		-3		0	μA
Internal reference output voltage	V <sub>REF</sub>	I <sub>REF</sub> = -400μA	-3.83	-3.75	-3.67	V
Accuracy output voltage range	V <sub>OC</sub>	R <sub>L</sub> > 10KΩ	0.5	1.0	1.5	V
Set up time	t <sub>s</sub>		10			ns
Hold time	t <sub>h</sub>		2			ns
Propagation delay time	t <sub>PD</sub>	R <sub>L</sub> > 10KΩ		11		ns
Glitch energy	GE	R <sub>L</sub> > 10KΩ f <sub>CLK</sub> = 1 MHz Digital lamp output		30		pV-s

Input/Output Chart (when output full scale voltage at 1.00 V)

Table 1

Input code								Output voltage (Single supply)	Output voltage (dual supply)
MSB							LSB		
1	1	1	1	1	1	1	1	Vcc	-0V
1	0	0	0	0	0	0	0	Vcc -0.5V	-0.5V
0	0	0	0	0	0	0	0	Vcc -1.0V	-1.0V

Electrical Characteristics Test Circuit

DC characteristics

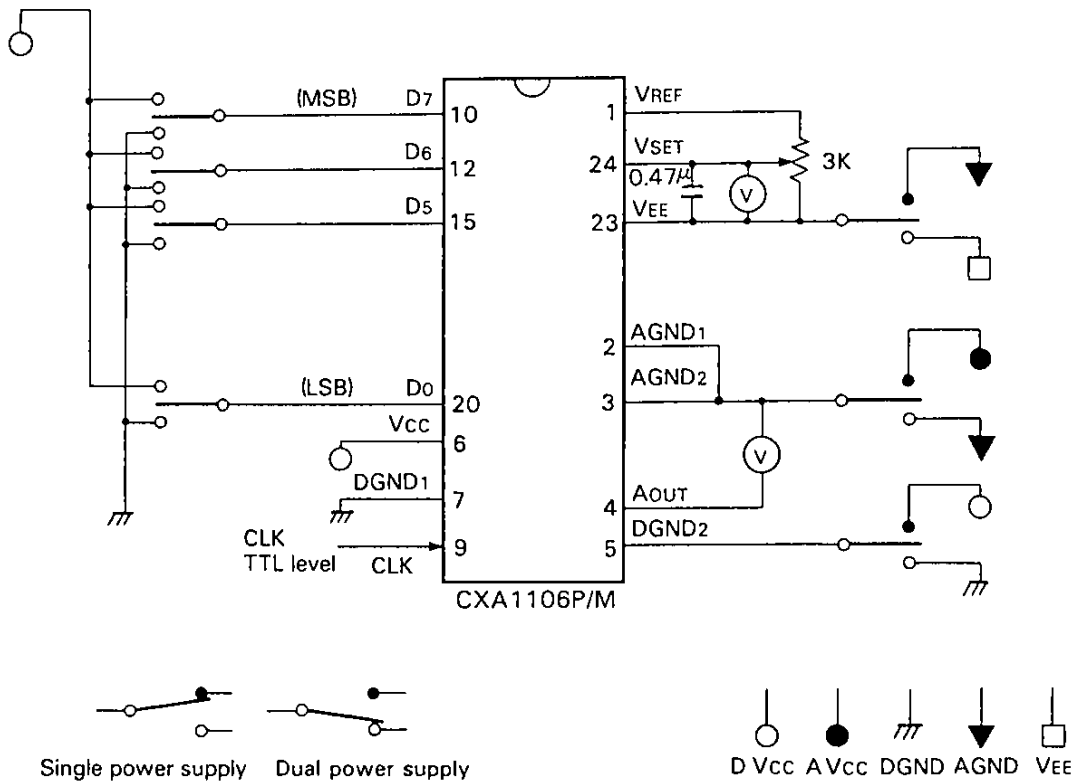
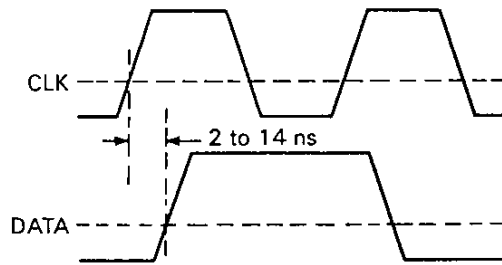
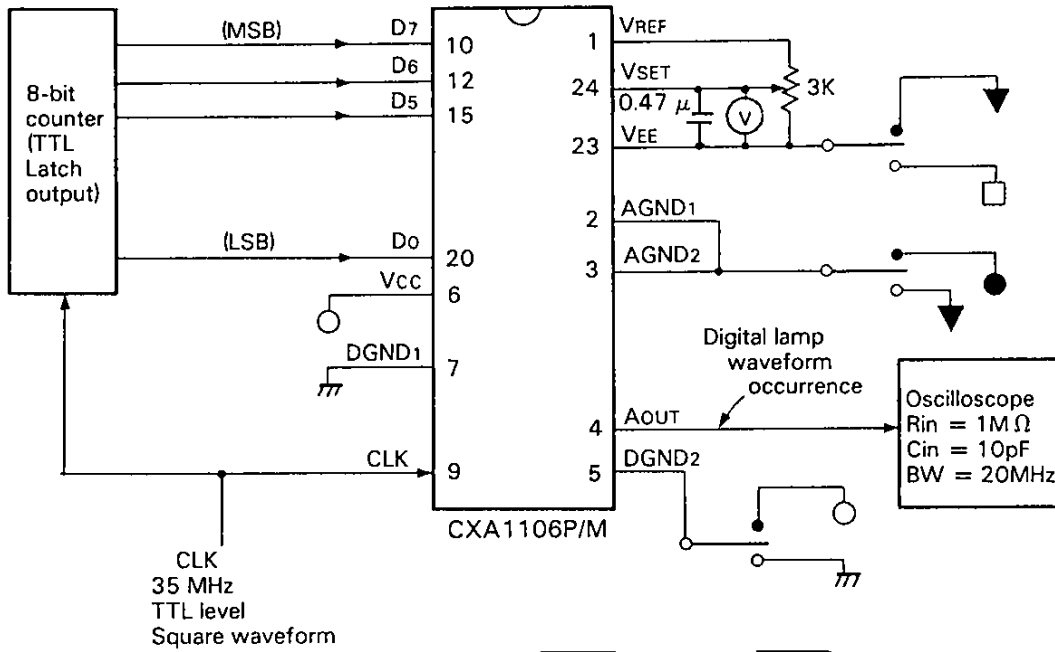


Fig. 1



Test Circuit for Maximum Conversion Speed



Timing between CLK and Data

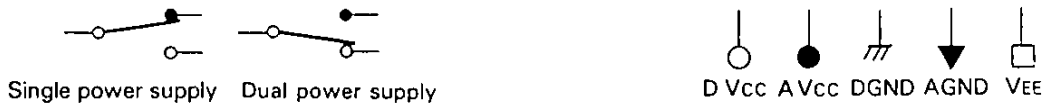


Fig. 2

Test Circuit for Set-up Time, Hold Time

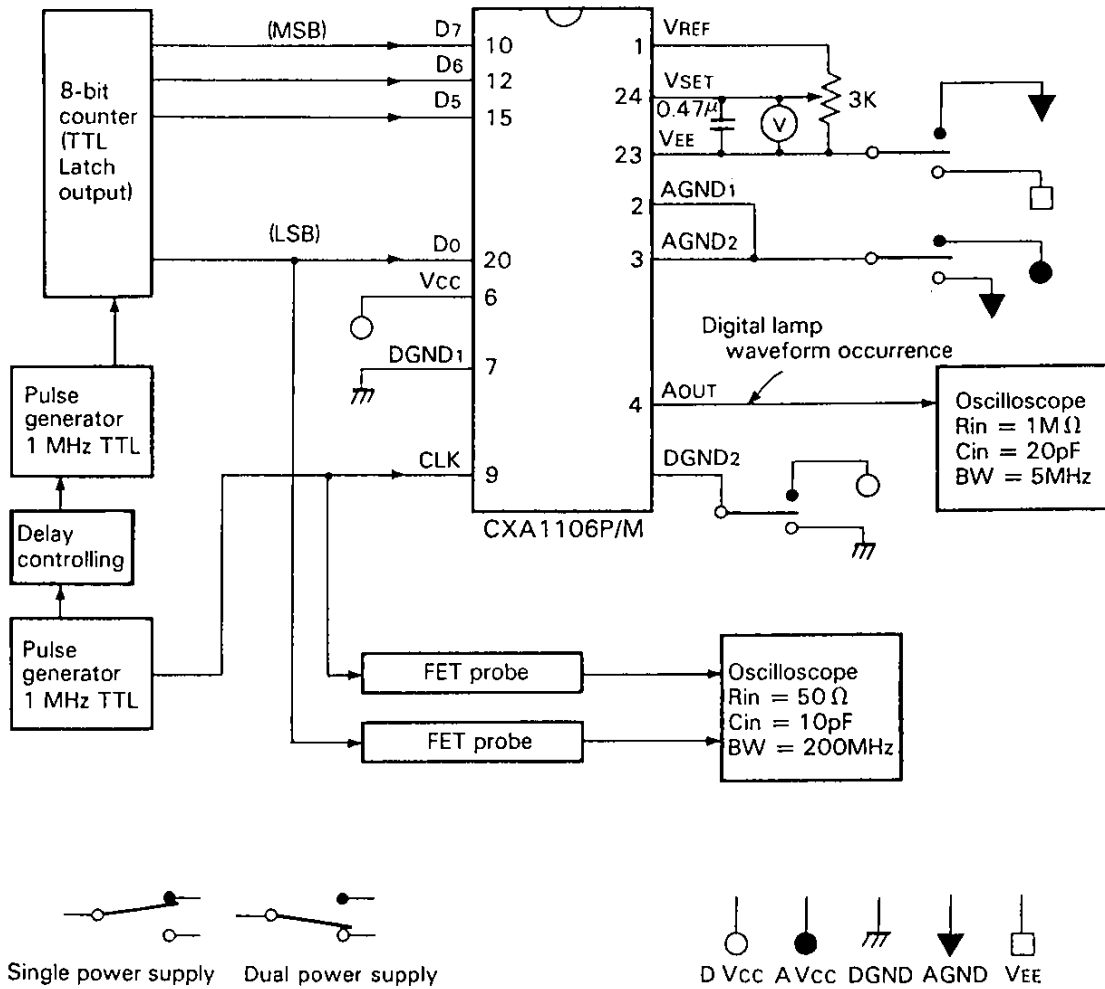


Fig. 3

Test Circuit for Glitch Energy

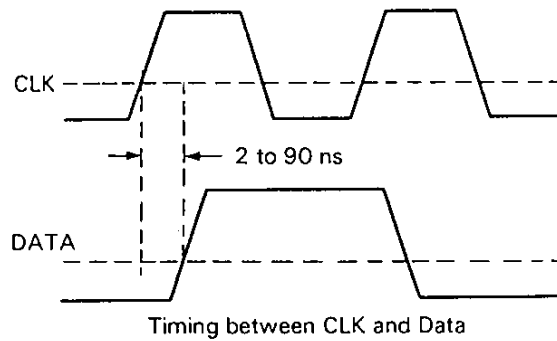
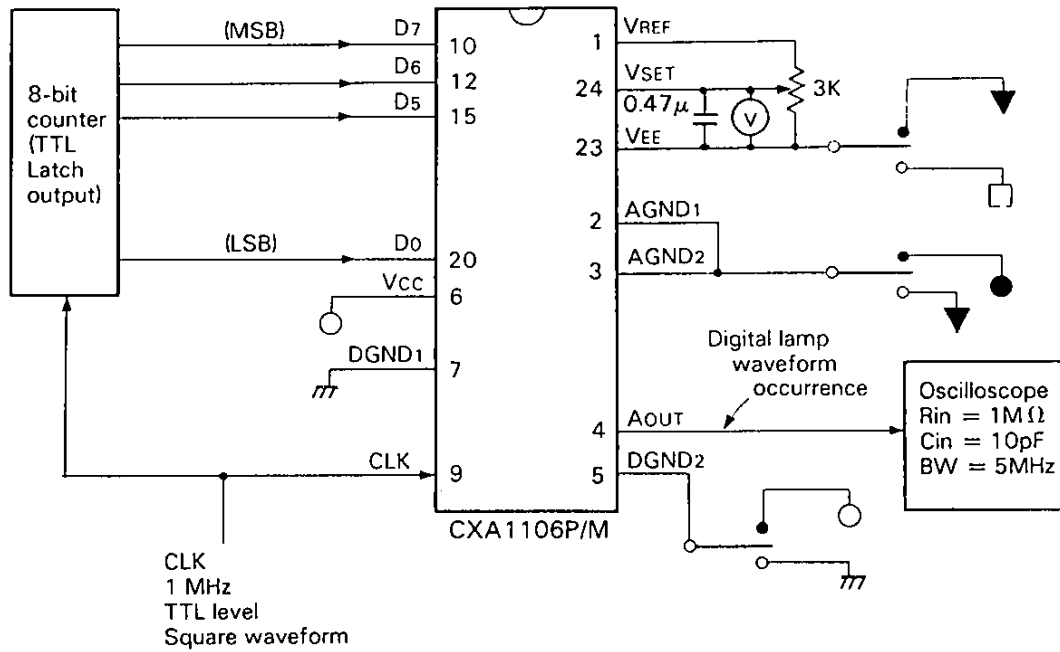
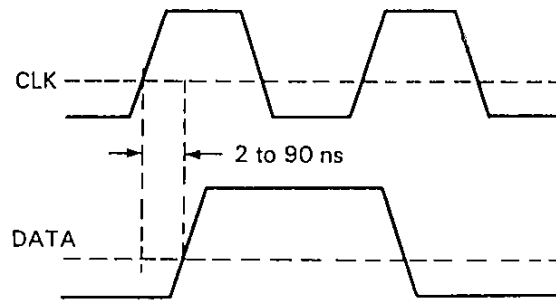
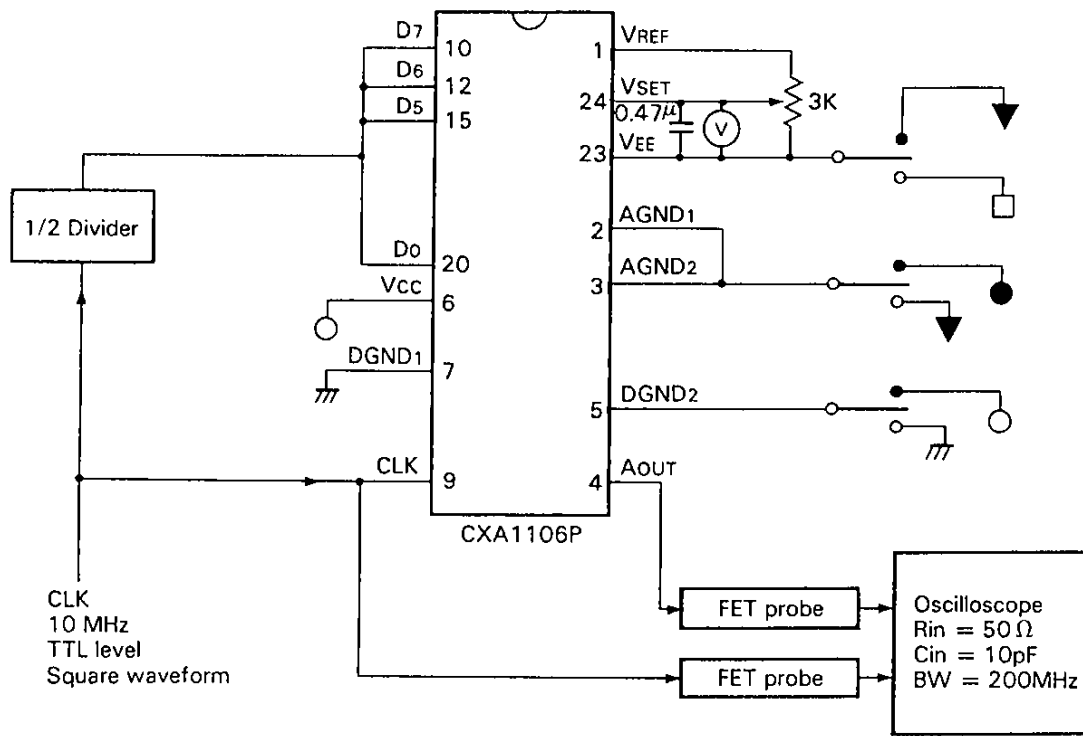


Fig. 4

Test Circuit for Propagation Delay Time



Timing between CLK and Data



Fig. 5

Operation

Timing chart

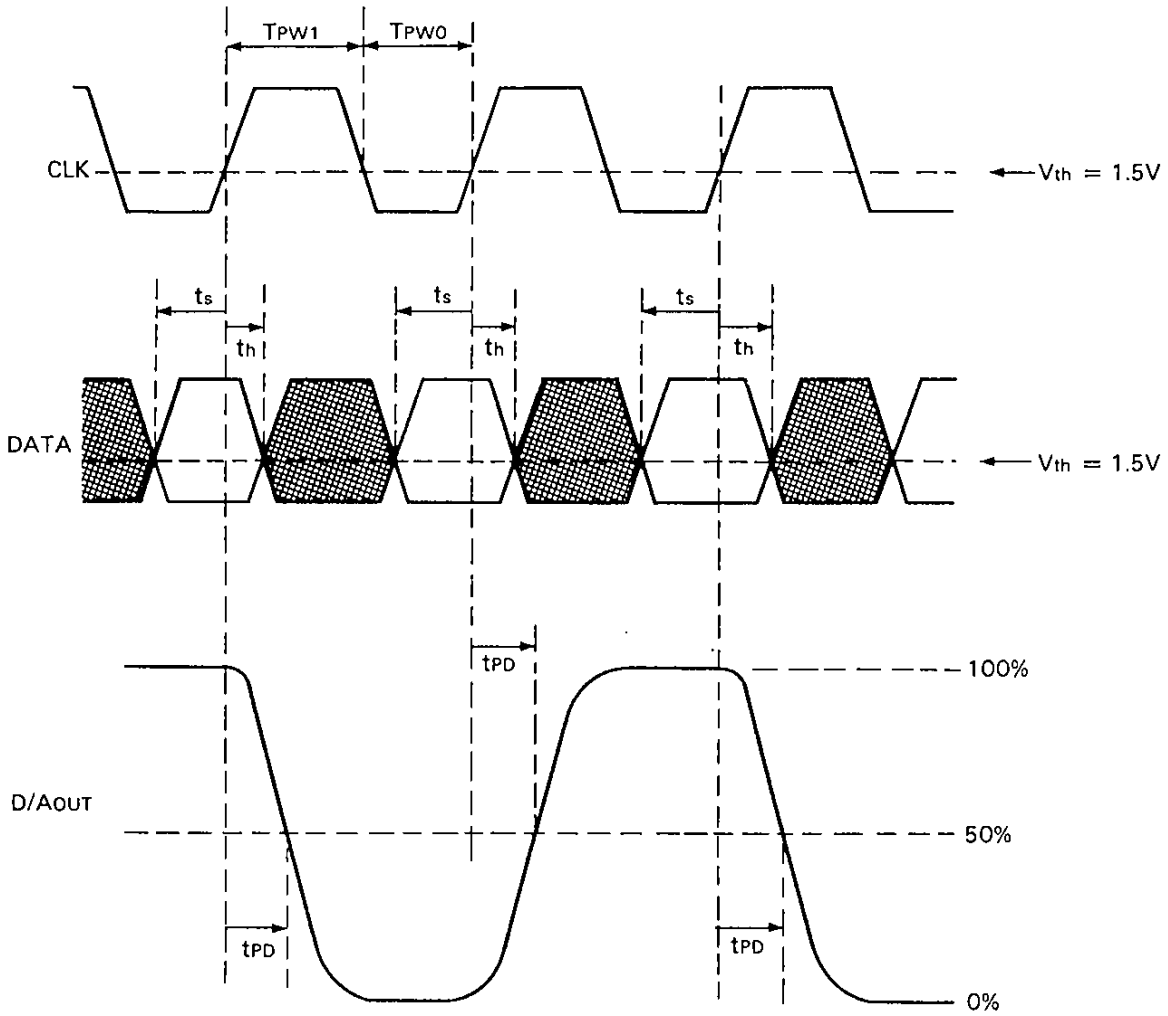
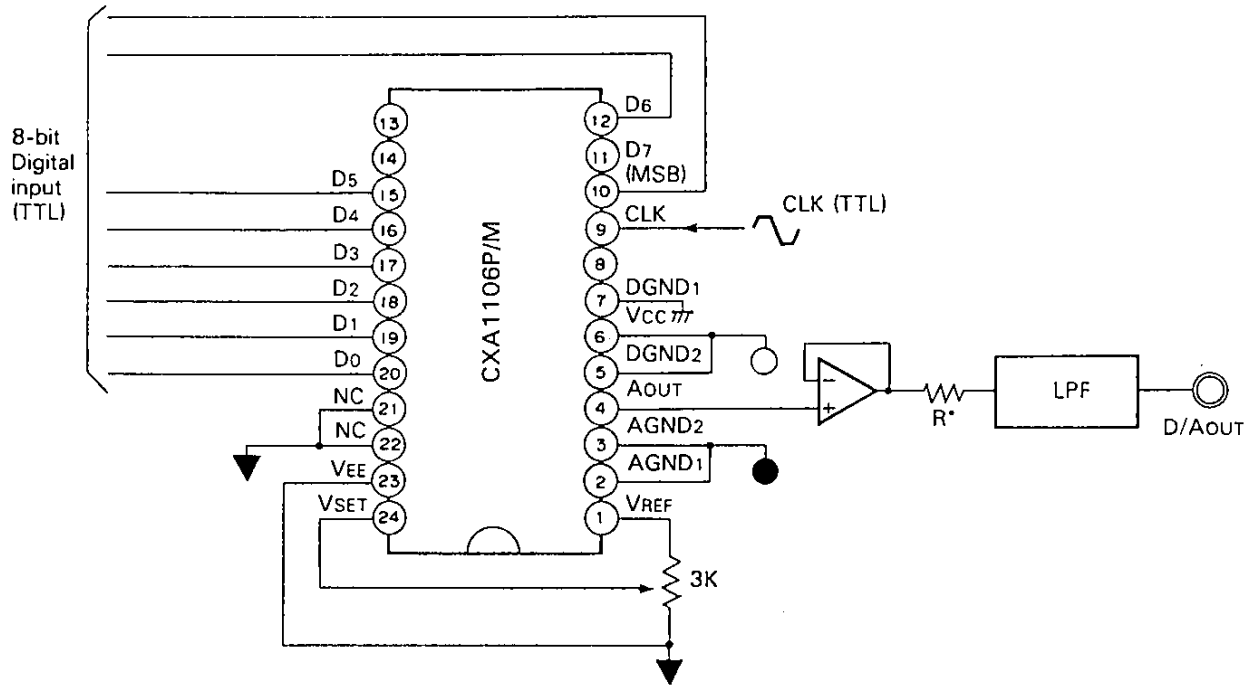


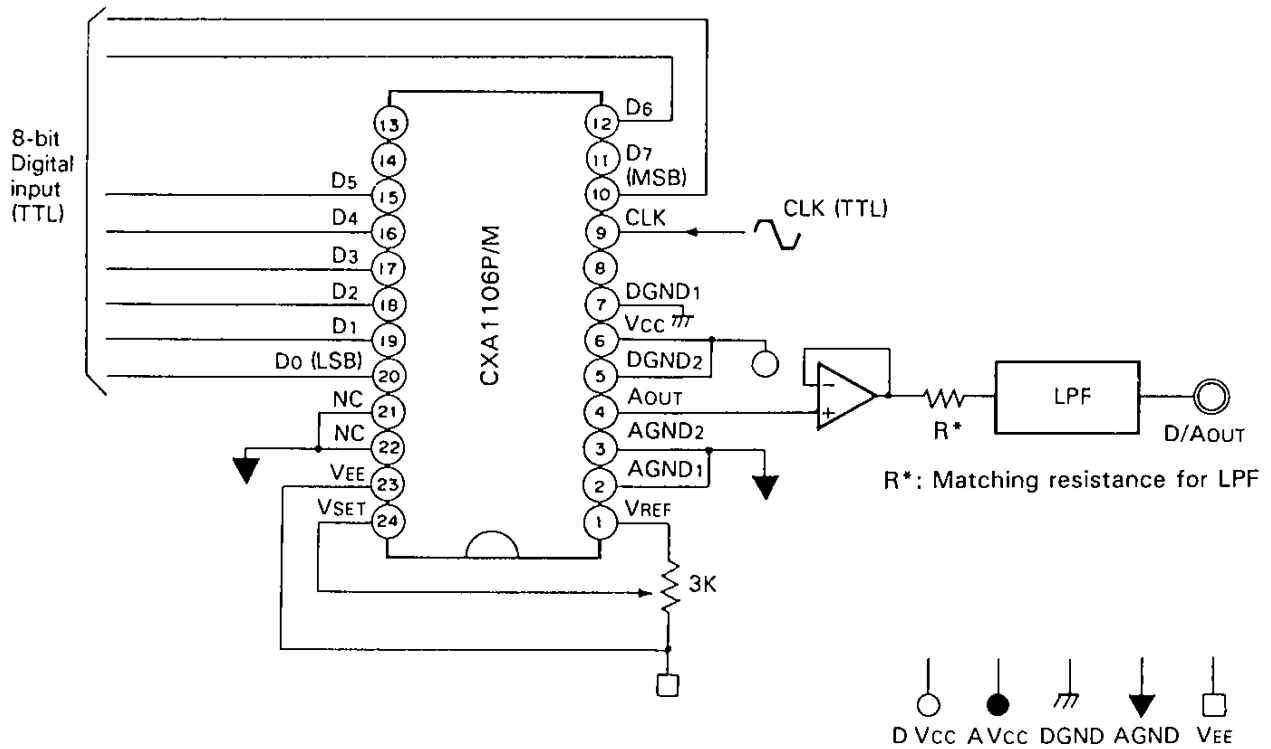
Fig. 6

Application Circuits

Single power supply



Dual power supply



## Notes on Application

### 1. Setting of VSET Pin (Pin 24)

The full-scale voltage of the D/A output is determined by VSET input voltage. As about (1.2V - VEE) DC voltage is generated at VREF pin (Pin 1) by connecting an external resistor from VREF pin to VEE pin (Pin 23), divide this voltage using resistors and apply it to VSET pin as Fig. 7.

(Example of usage)

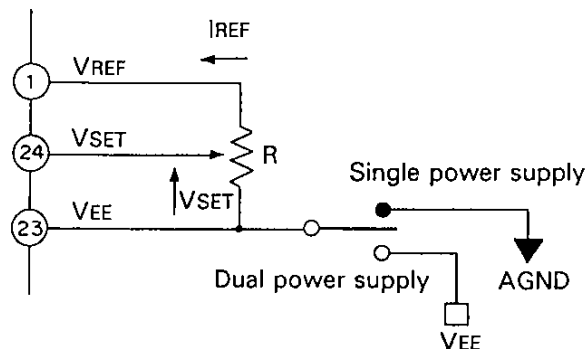


Fig. 7

The full-scale voltage of the D/A output can be determined from the following equation.

$$V_{FS} = 1.2 (V_{SET} - V_{EE}) \quad (R_L > 10K\Omega, 0.4V \leq V_{SET} \leq 1.2V)$$

Select an external resistor R (Connected to VREF pin) so that IREF (current of an external resistor) is within the value indicated as the Recommended Operational Conditions ( $-3 \text{ mA} < I_{REF} < -0.4 \text{ mA}$ ).

### 2. Phase relation between Data and Clock

To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set.

Set up time ( $t_s$ ) and Hold time ( $t_h$ ) should be as indicated in the Electrical characteristics. For  $t_s$  and  $t_h$  refer to Fig. 6 in the Timing Chart.

Also, set the clock pulse width according to the Recommended Operating Conditions.

### 3. D/A output pin Load

Receive the D/A output stage at high impedance, so as to obtain

$$R_L > 10K\Omega$$

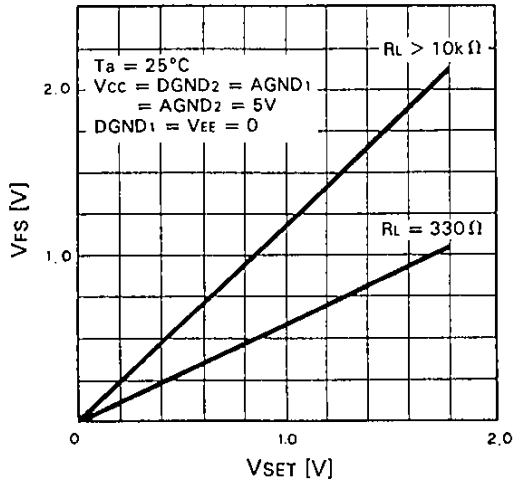
$$C_L < 20pF$$

### 4. Noise reduction

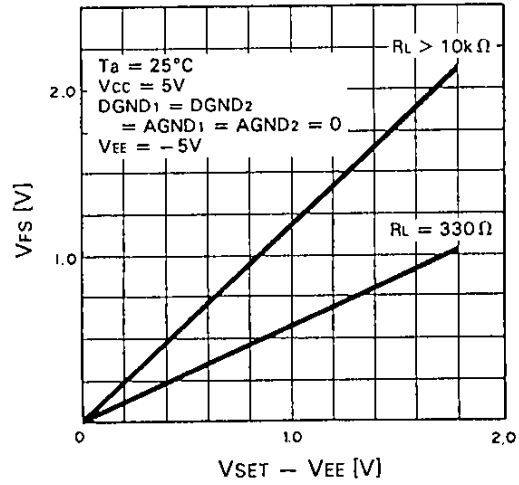
Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penetrates D/A output.

- The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
- Connected a bypass capacitor between each of DVCC (Pin 6) and DGND1 (Pin 7); AGND1,2 (Pins 2, 3) and VEE (Pin 23); VSET (Pin 24) and VEE (Pin 23), respectively.

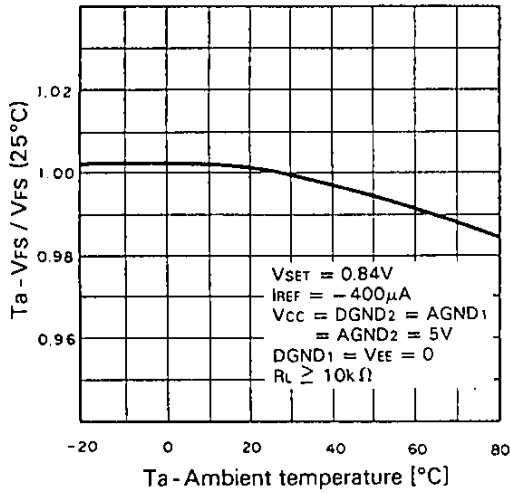
Full-scale output voltage  $V_{FS}$  and  $V_{SET}$   
(Single power supply)



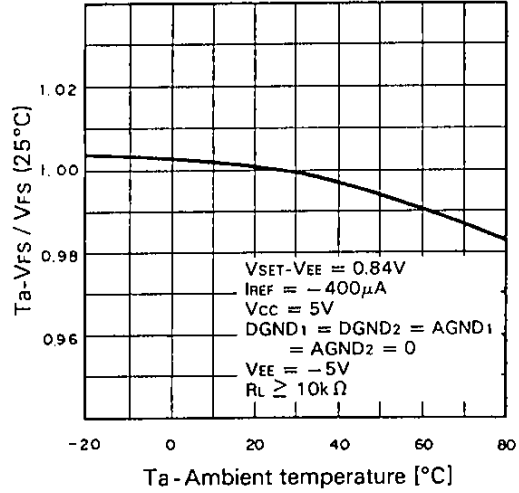
Full-scale output voltage  $V_{FS}$  and  $V_{SET-VEE}$   
(Dual power supply)



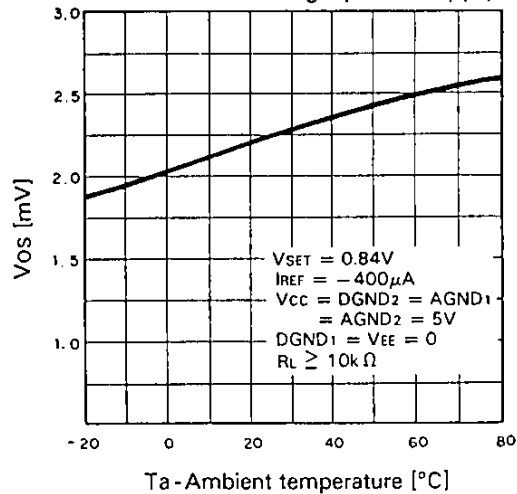
Full-scale output voltage  $V_{FS}$  temperature characteristics  
(Single power supply)



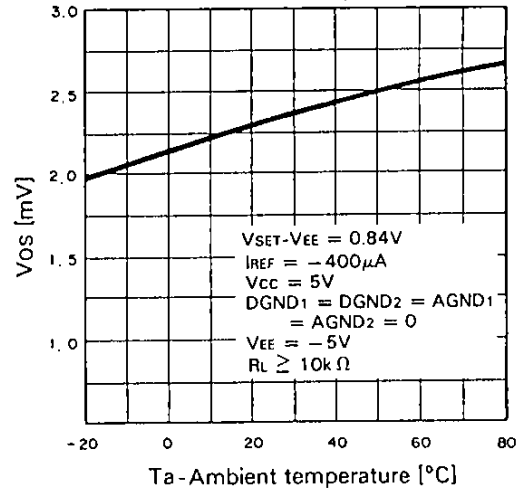
Full-scale output voltage  $V_{FS}$  temperature characteristics  
(Dual power supply)



Output offset voltage  $V_{OS}$  temperature characteristics  
(Single power supply)

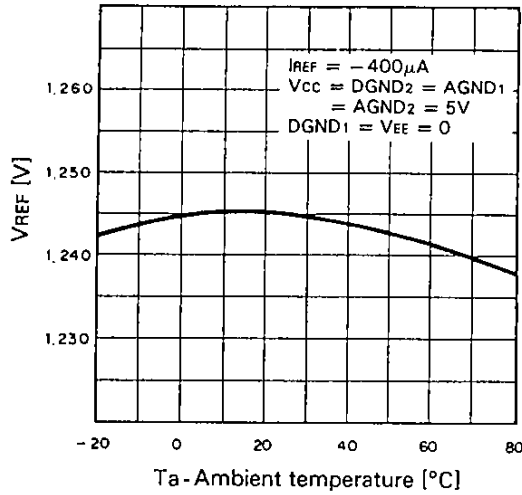


Output offset voltage  $V_{OS}$  temperature characteristics  
(Dual power supply)

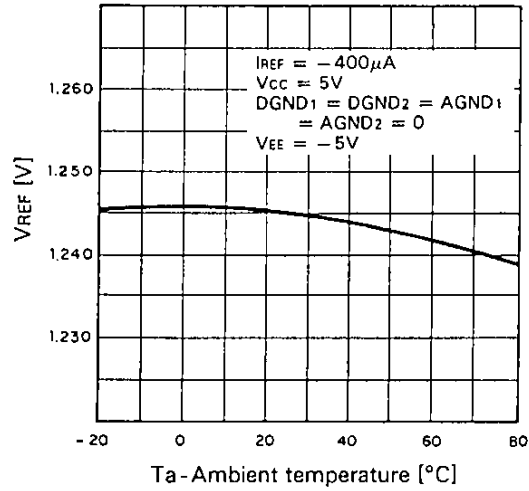




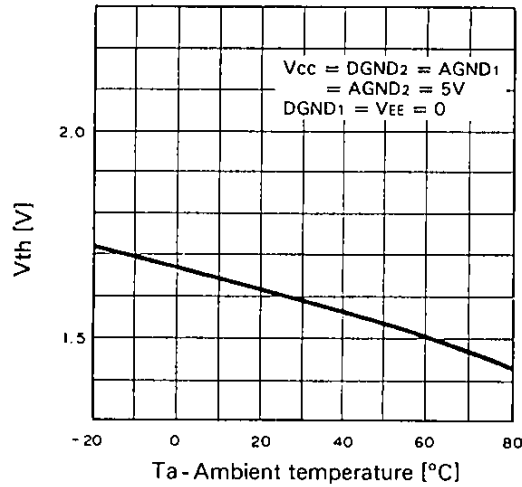
Internal reference voltage  $V_{REF}$  temperature characteristics (Single power supply)



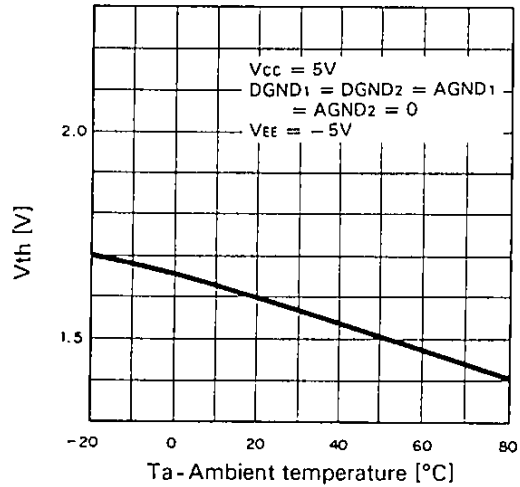
Internal reference voltage  $V_{REF}$  temperature characteristics (Dual power supply)



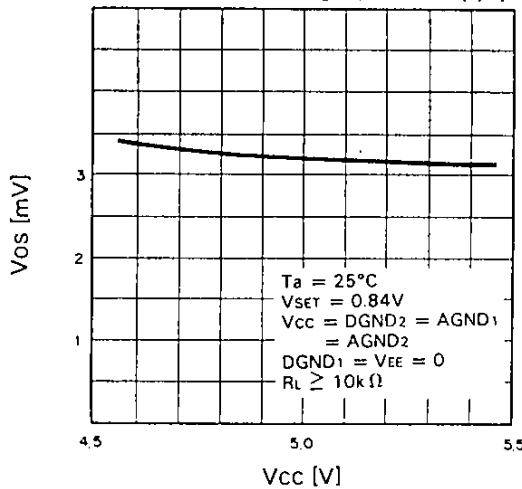
Threshold voltage  $V_{th}$  of digital input temperature characteristics (Single power supply)



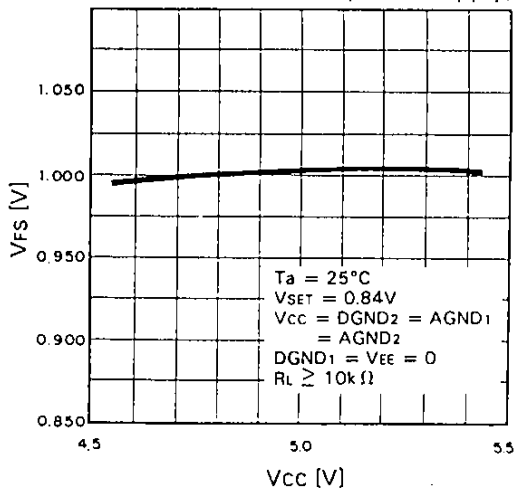
Threshold voltage  $V_{th}$  of digital input temperature characteristics (Dual power supply)



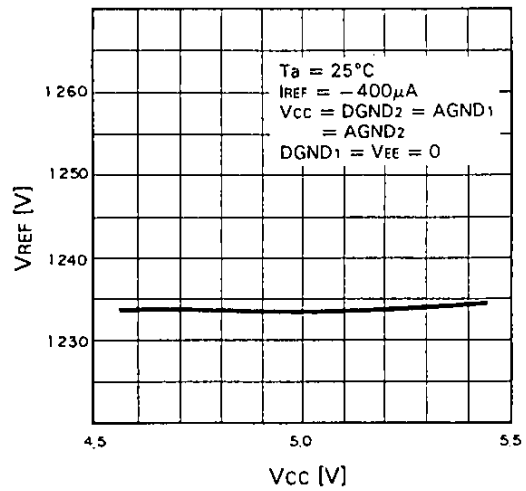
Output offset voltage  $V_{OS}$  to Supply voltage (Single power supply)



Output full-scale voltage  $V_{FS}$  to Supply voltage (Dual power supply)

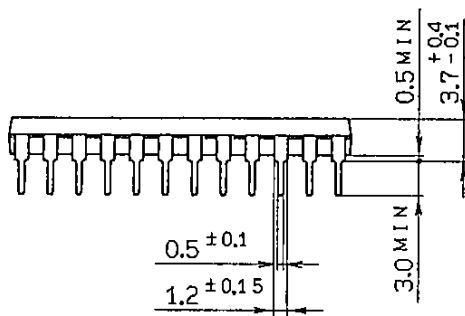
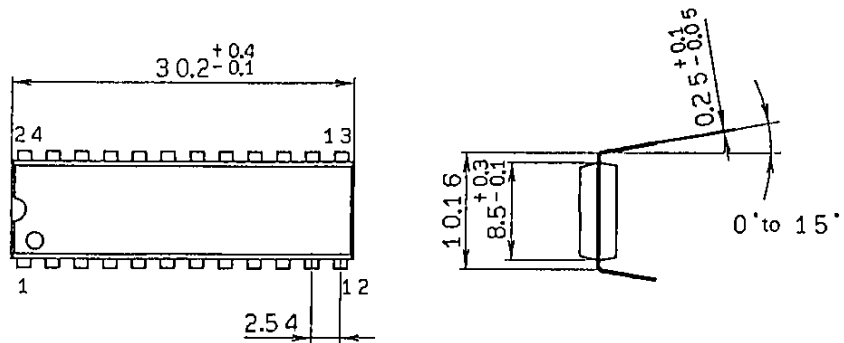


Internal reference voltage  $V_{REF}$  to supply voltage  
(Single power supply)



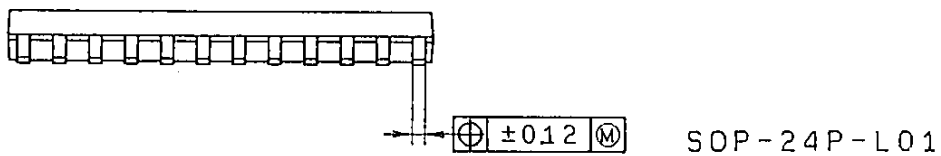
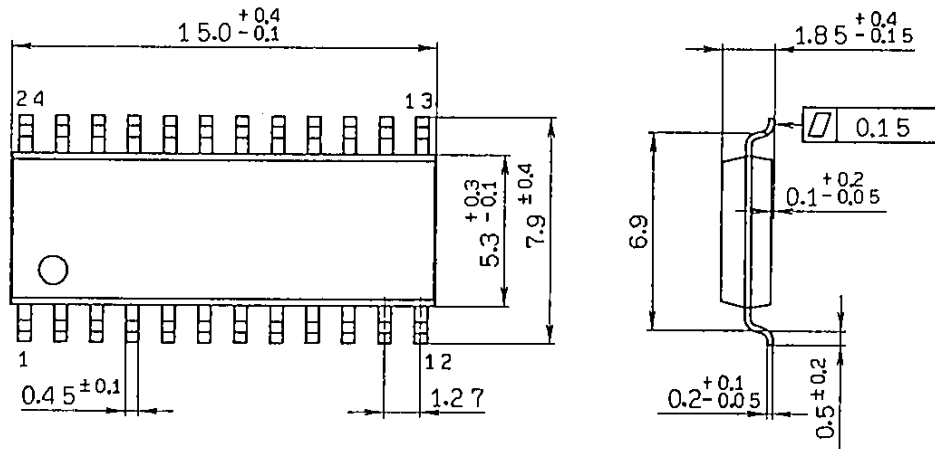
Package Outline Unit : mm

CXA1106P 24 pin DIP (Plastic) 400mil 2.0g



DIP-24P-01

CXA1106M 24 pin SOP (Plastic) 300mil 0.3g



SOP-24P-L01