82526
CONTROLLER AREA NETWORK CHIP

Automotive

- **On-Board "MOTEL"**
- **Multimaster Architecture**
- **Bus Access Priority by Message**
- **2032 Different Message Objects**
- **Guaranteed Latency Time for High Priority Messages**
- **Powerful Error Handling**
- **Data Length to 8 Bytes**
- **Message Configuration Flexibility**
- **Broadcast Message Transfer**
- **Ready Output**
- **Global Interrupt Disable**
- **Non-Destructive Bitwise Arbitration**
- **Two 8-Bit I/O Ports**
- **NRZ Coding/Decoding with Bit Stuffing**
- **Programmable Transfer Rate to 1 MBit/Sec**
- **Programmable Output Driver Configuration**
- **Programmable Clock Output**
- **44-Pin PLCC**
- **Three Additional $\overline{CS}$ Outputs**

The 82526 Communication Controller is a highly integrated VLSI device which implements the CAN (Controller Area Network) Protocol. Included on the chip are an Interface Management Processor (IMP), Bit Stream Processor (BSP), Bus Timing Logic (BTL), Transceiver Control Logic (TCL), Processor Interface Unit (PIU), Error Management Logic (EML), Clock Generator and a pseudo Dual Port RAM (DPRAM). These hardware modules implement all necessary features of a high performance serial communication protocol. When connected to a microprocessor, the 82526 performs the principal functions of the physical and data link layer. Figure 1 shows a block diagram of the 82526.

The 82526 uses an 8-bit multiplexed address and data bus optimized for operating with Intel's microcontrollers and microprocessors. Other architectures may also be used with the direct connect on board "MOTEL" circuitry.

As shown in Figure 1, the BSP, TCL, BTL and EML are related with Bus Line Logic. The IMP, RAM and PIU are related to the CPU Interface Logic. The logic blocks BSP, BTL, TCL and EML are referred to as the "Serial Interface Unit".

The CPU communicates with the 82526 through the on-chip pseudo dual port RAM which includes global status and control registers. The on-chip memory serves as the communication buffer interface between the CPU and the IMP. The CPU initializes the global status and control registers and creates a data structure (Communication Objects) within the communication buffer for reception and transmission of defined messages.

Commands, data and status transfers take place over the 8-bit parallel bus. The CPU writes data to the 82526 using $\overline{CS}$, ALE and $\overline{WR}$ signals and reads the 82526 received data and status information using the $\overline{CS}$, ALE and $\overline{RD}$ signals. The 82526 uses the interrupt line to alert the CPU of errors or data received.

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Order Number: 270573-005

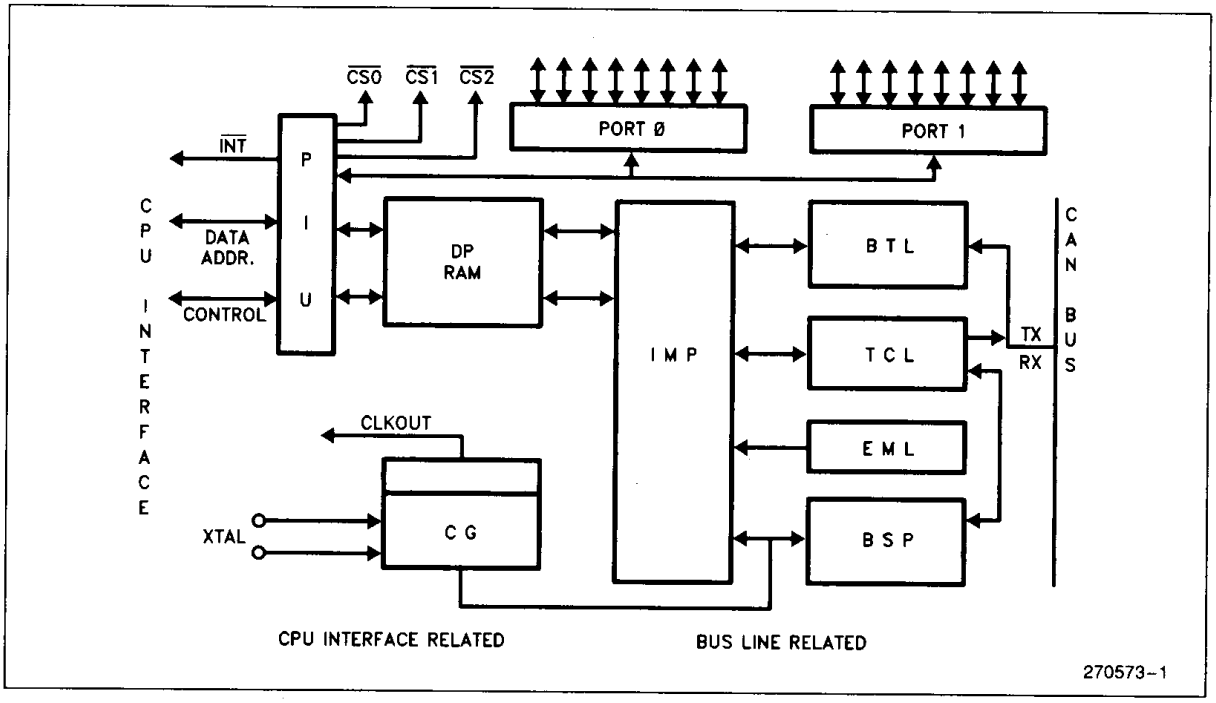


Figure 1. 82526 Block Diagram

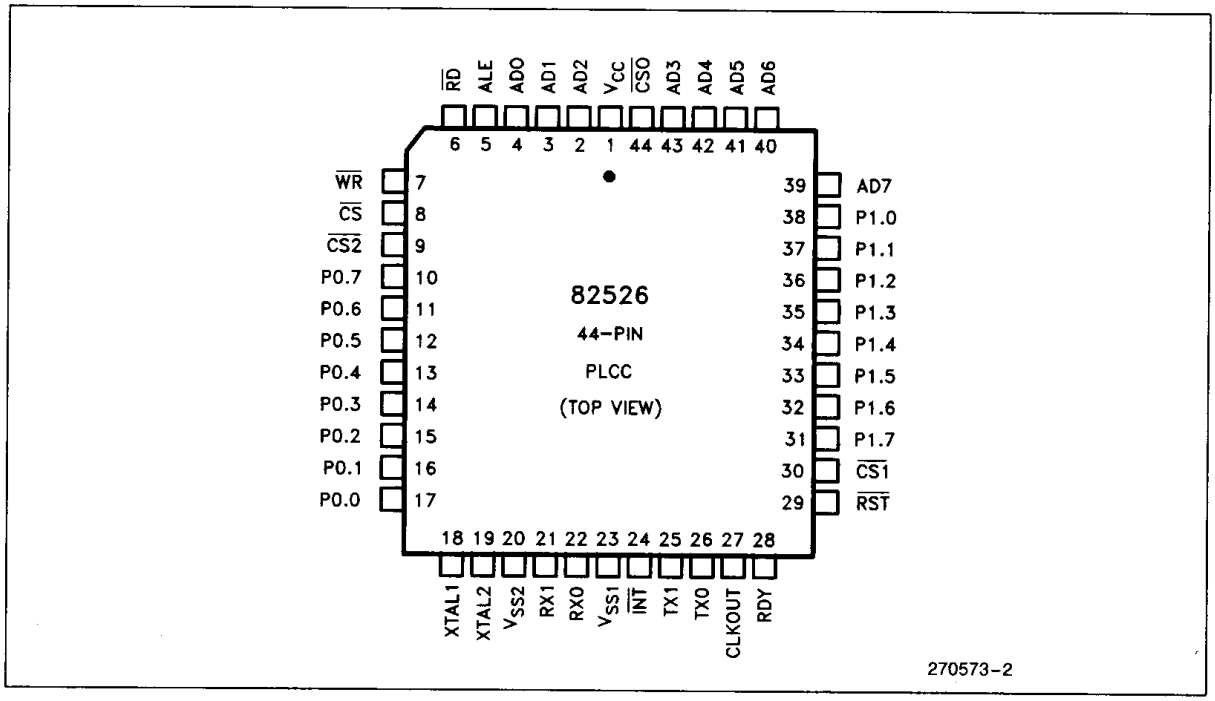


Figure 2. 44-PIN PLCC Package

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias . . . . . −40°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS V_{CC} = 4.5V to +5.5V; T_A = −40°C to +125°C

Symbol	Parameter	Min	Typ	Max	Conditions
V_{IL}	Input Low Voltage (All except XTAL1)	$V_{SS}-0.5V$		0.8V	
V_{IL1}	Input Low Voltage (XTAL1)	$V_{SS}-0.5V$		$0.2V_{CC}-0.1$	
V_{IH}	Input High Voltage (All except XTAL1, $\overline{RST}$, ALE, $\overline{CS}$)	2.0V		V_{CC} + 0.5	
V_{IH1}	Input High Voltage ($\overline{RST}$)	3.5V		V_{CC} + 0.5	
	Hysteresis on $\overline{RST}$	200 mV			
V_{IH2}	Input High Voltage (ALE, $\overline{CS}$)	0.5 V_{CC}		V_{CC} + 0.5	
V_{IH3}	Input High Voltage (XTAL1)	0.7 V_{CC}		V_{CC} + 0.5	
V_{OL}	Output Low Voltage (All Outputs except AD0–7, $\overline{INT}$, RDY, CLKOUT, TX0, TX1)			0.4V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (AD0–7)			0.4	I_{OL} = 3.2 mA
V_{OL2}	Output Low Voltage (RDY, $\overline{INT}$)			0.4V	I_{OL} = 5 mA
V_{OH}	Output High Voltage (All Outputs except AD0–7, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, TX0, TX1, CLKOUT)	2.5V			I_{OH} = −80 μA
V_{OH1}	Output High Voltage (AD0–7, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$)	0.6 V_{CC}			I_{OH} = −400 μA
		0.7 V_{CC}			I_{OH} = −80 μA
I_{LK}	Input Leakage Current (Except Port0/Port1)			±10 μA	$V_{SS} < V_{IN} < V_{CC}$
I_{IL}	Low Level Input Current (Port0/Port1)			−50 μA	V_{IN} = 0.4V
I_{TL}	Logical 1 to 0 Transition Current (Port0/Port1)			−750 μA	V_{IN} = 2V
I_{LT}	Latch-up Trigger Current			±80 mA	
C_{IO}	Pin Capacitance			10 pF	@1 MHz, 25°C
I_{CC}	Supply Current		22 mA	33 mA	F_{XTAL} = 16 MHz
ISM	Sleep Mode Supply Current		1.2 mA 5.5 mA	2.2 mA 8.5 mA	F_{XTAL} = 1 MHz F_{XTAL} = 16 MHz
I_{OC}	Comparator Offset Current			±1 μA	
I_{BC}	Comparator Bias Current			±1 μA	

AC CHARACTERISTICS

Conditions: $T_A = -40°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, Port 2 outputs: CL = 150 pF, All other outputs: CL = 80 pF

Symbol	Parameter	Min	Typ	Max
$1/T_{XTAL}$	Oscillator Frequency	1 MHz		16 MHz
T_{AVLL}	Address Valid to ALE Low	20 ns		
T_{LLAX}	Address Hold after ALE Low	12 ns		
T_{LLDV}	ALE or $\overline{CS}$(1) Low to Valid Data Out			$5\ T_{XTAL} + 80$ ns(8)
T_{RHDZ}	Data Float after $\overline{RD}$ High	6 ns		50 ns
T_{RLDV}	Valid Data Out Delay from Read Control			80 ns
T_{QVWH}	Input Data Setup to $\overline{WR}$ High	20 ns		
T_{WHQX}	Input Data Hold after $\overline{WR}$ High	18 ns		
T_{WHDV}	$\overline{WR}$ High to Output Data Valid on Port 0 or Port 1			$4\ T_{XTAL} + 70$ ns
T_{WHLL}	$\overline{WR}$ High to Next ALE or $\overline{CS}$ Low(1, 2)	$2\ T_{XTAL} + 5$ ns		
T_{WHWL}	Time between Writes	$4\ T_{XTAL} + 5$ ns		
T_{LLWH}	ALE or $\overline{CS}$(1) Low to $\overline{WR}$ High	$4\ T_{XTAL} + 10$ ns		
T_{ALAL}	Time between ALE Falling Edges (or $\overline{CS}$)(1)	$8\ T_{XTAL} + 5$ ns		
T_{LLYV}	End of ALE to RDY Setup			65 ns
T_{LLYH}	End of ALE to RDY High(4) (with 1k External Pull-Up)	$4\ T_{XTAL} + 65$ ns		$6\ T_{XTAL} + 65$ ns
T_{LCSL}	ALE or $\overline{CS}$ Low to $\overline{CS0}$-1-2 Low(1, 5)			45 ns
T_{HCSH}	$\overline{CS0}$-1-2 High after ALE or $\overline{CS}$ High(3, 5)			70 ns
T_{AVCS}	Address Valid to $\overline{CS0}$-1-2 Low(6)			40 ns
T_{CSHH}	$\overline{CS}$ Active Hold after $\overline{RD}$ or $\overline{WR}$ High(7)	0 ns		

NOTES:
1. Whichever falling edge is last.
2. Some pipe-lining of the write accesses is possible. This spec is important mainly when processor speed is higher than 82526 speed (use of the RDY output . . .).
3. Whichever rising edge comes first.
4. RDY is an open drain output (so is $\overline{INT}$).
5. Timings valid on ALE falling or rising edges only if ALE is used to strobe the $\overline{CS0}$-1-2 outputs (default mode). If the other mode is programmed by writing 1 to bit 7 of address 253, the new state starts propagating to the $\overline{CS0}$-1-2 outputs as soon as a stable address has been decoded (providing that $\overline{CS}$ is also valid).
6. Timing valid only when ALE is not used to strobe the $\overline{CS0}$-1-2 outputs. In this mode, T_{HCSH} also applies on $\overline{CS}$ rising edge and T_{LCSL} on $\overline{CS}$ falling edge.
7. $\overline{CS}$ must be active low with $\overline{RD}$ or $\overline{WR}$ rising edge for proper completion of the read or write access.
8. If t_{LLDV} is too slow for the host microcontroller, a double read mechanism can be implemented. For details, contact an Intel representative.

Physical Layer Specifications Load Condition: 80 pF

RX0/RX1	Min	Max	Conditions
Input Voltage	V_{SS} − 0.5V	V_{CC} + 0.5V	
Common Mode Range	V_{SS} + 1.0V	V_{CC} − 1.0V	(1)
Differential Input Threshold	±50 mV		(1)

TX0/TX1(5)	Min	Max	Conditions
Source Current	−3.0 mA		$V_{OUT} = V_{CC} - 0.4V$
	−6.0 mA		$V_{OUT} = V_{CC} - 1.0V$
Sink Current	10.0 mA		$V_{OUT} = 0.4V$
	20.0 mA		$V_{OUT} = 1.0V$
Maximum Permitted Source Current (TX0, TX1 Together)		−8.0 mA	
Maximum Permitted Sink Current (TX0, TX1 Together)		22.0 mA	
Rise Time		20 ns	(4)
Fall Time		15 ns	(4)

CLKOUT Specifications

CL = 50 pF	Min	Max	Conditions
CLKOUT frequency (1/T)	fXTAL/30(3)	16 MHz	
Rise Time(4)		15 ns	
Fall Time(4)		15 ns	
Output Low Voltage		0.2 V_{CC} − 0.1	
Output High Voltage	0.7 V_{CC}		
Output Duty Cycle is 50% if Clock Divider Register Not Equal	0FH		
Output Duty Cycle Equal XTAL If Clock Divider Register Equal	0FH		

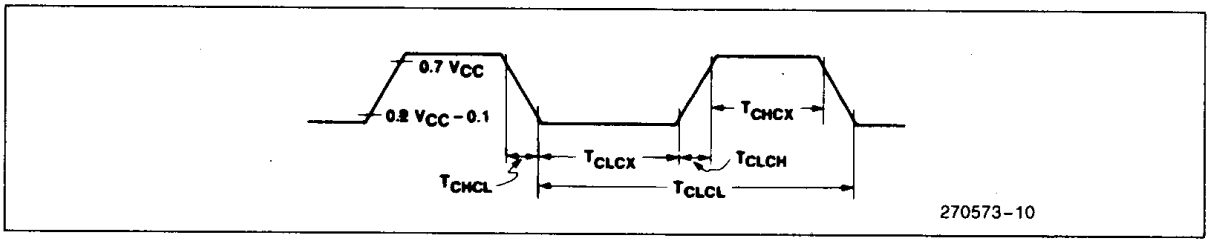
Internal Delay Time(2, 6)	Min	Max	Minimum Differential Input Threshold	Common Mode Range
$t_{(IN1)}$		187 ns	50 mV	V_{SS} + 1.0V to V_{CC} − 1.0V
$t_{(IN2)}$		137 ns	100 mV	V_{SS} + 1.0V to V_{CC} − 1.0V
$t_{(IN3)}$		127 ns	100 mV	V_{SS} + 1.5V to V_{CC} − 1.0V

NOTES:
1. See Internal Delay Times.
2. The Internal Delay Time is given by the sum: $t_{(internal\ logic)} + t_{(internal\ output\ driver)} + t_{(internal\ comparator)}$.
3. $F_{OUT} = F_{XTAL/R}$ with R = 1,2,4,6,8, . . . 2 × r and $r_{MAX} = 15$.
4. Measured between 0.2 V_{CC} − 0.1 and 0.7 V_{CC}.
5. Push-pull mode.
6. The total delay time from transmit to sample point = $t_{(total\ delay)} = t_{(internal\ delay)} + t_{(external\ logic)} + t_{(propagation\ delay)}$.

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency	1	16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



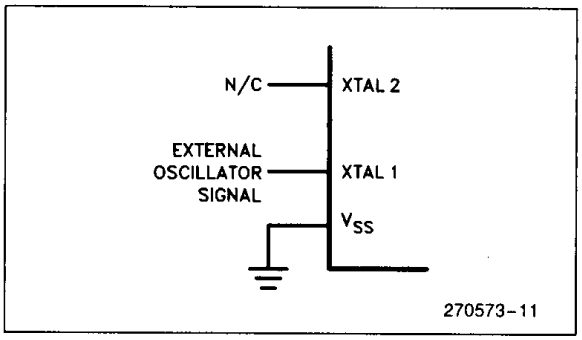
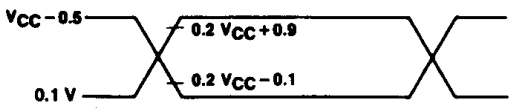


Figure 1. External Clock Drive Configuration

AC TESTING INPUT, OUTPUT WAVEFORMS

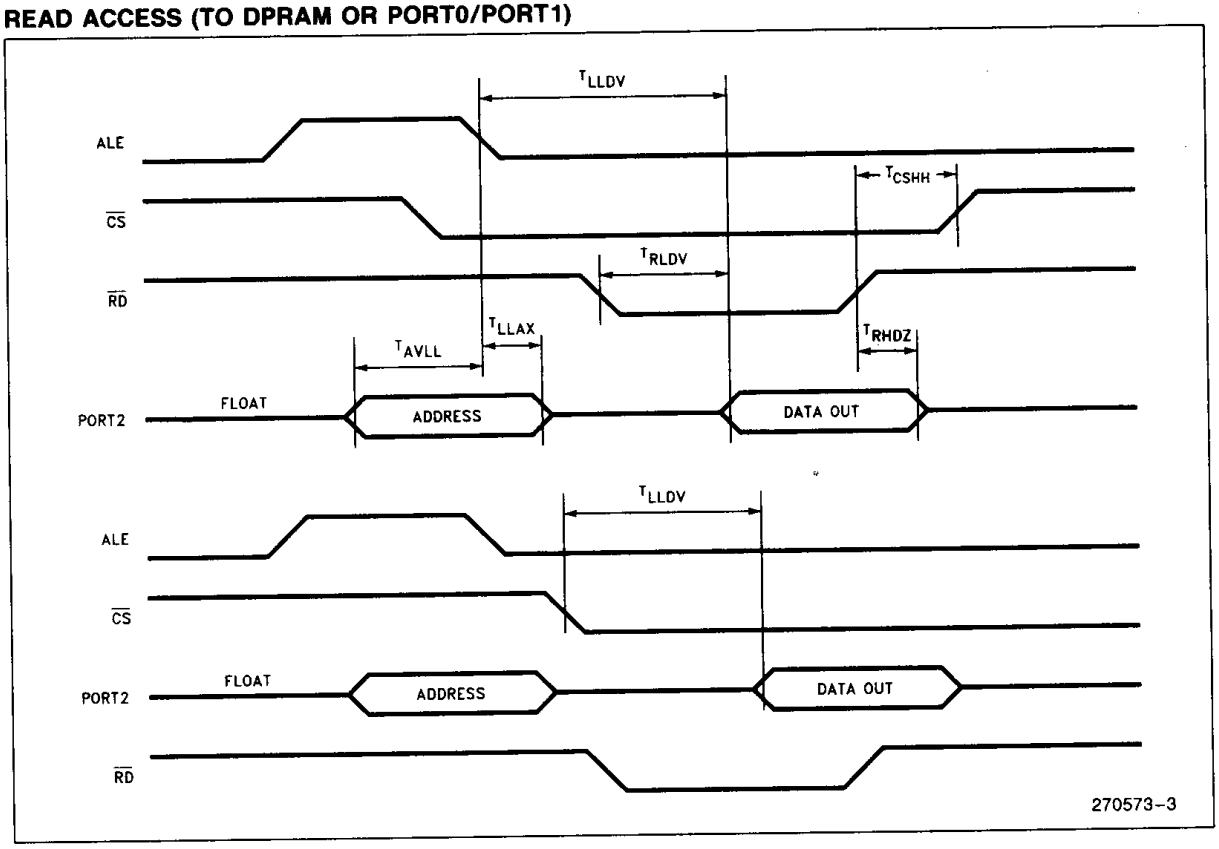


AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a Logic "1" and 0.1V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

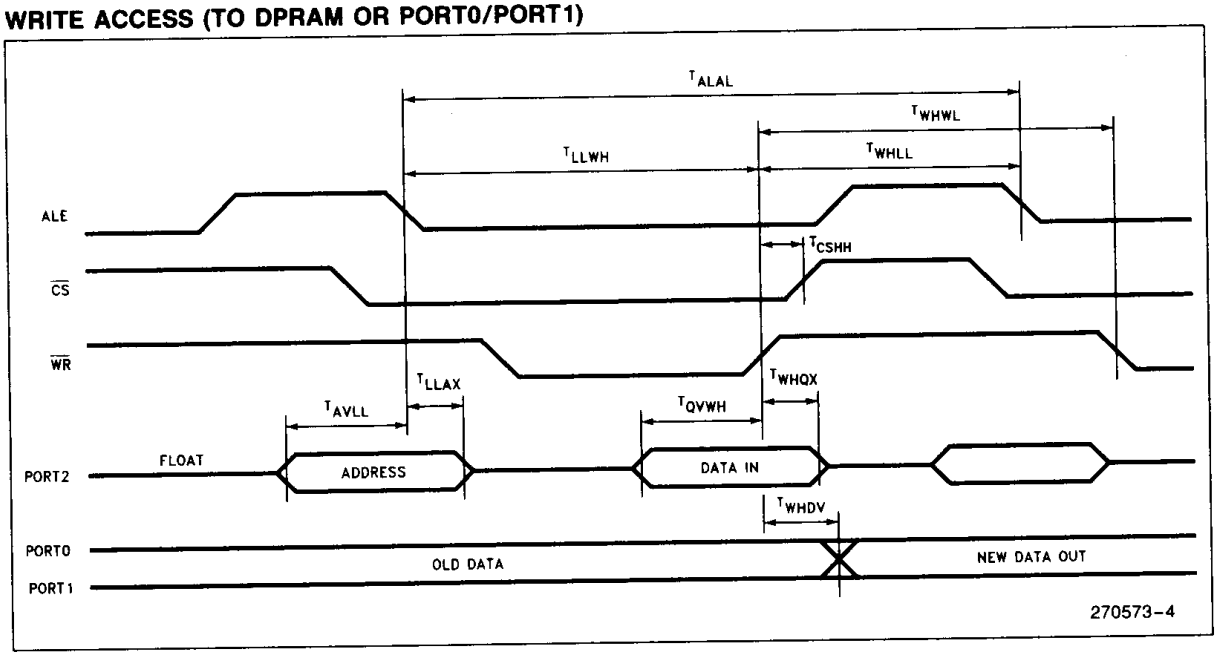
FLOAT WAVEFORMS

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

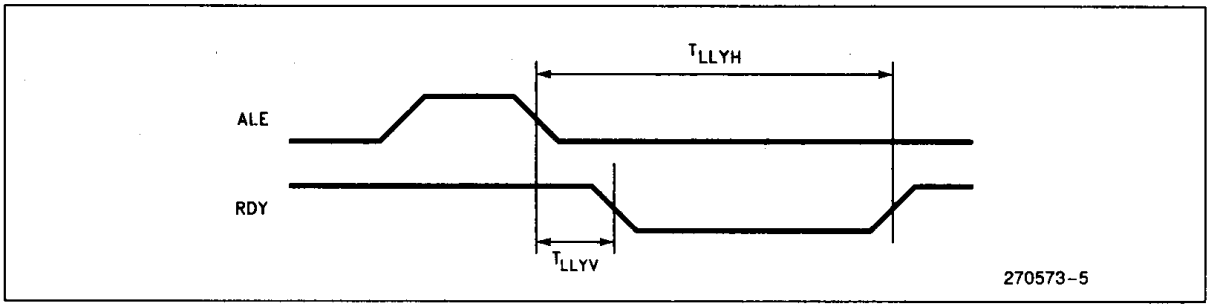
READ ACCESS (TO DPRAM OR PORT0/PORT1)



WRITE ACCESS (TO DPRAM OR PORT0/PORT1)

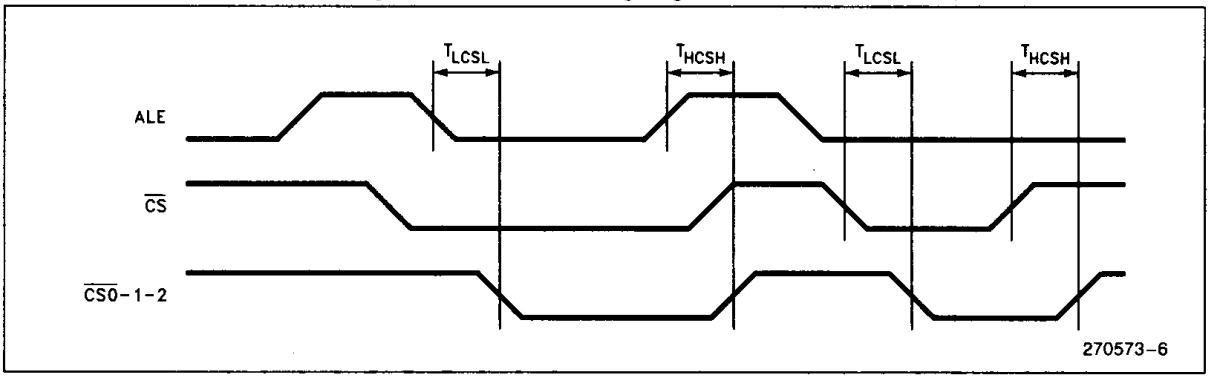


READY (RDY) OUTPUT TIMING



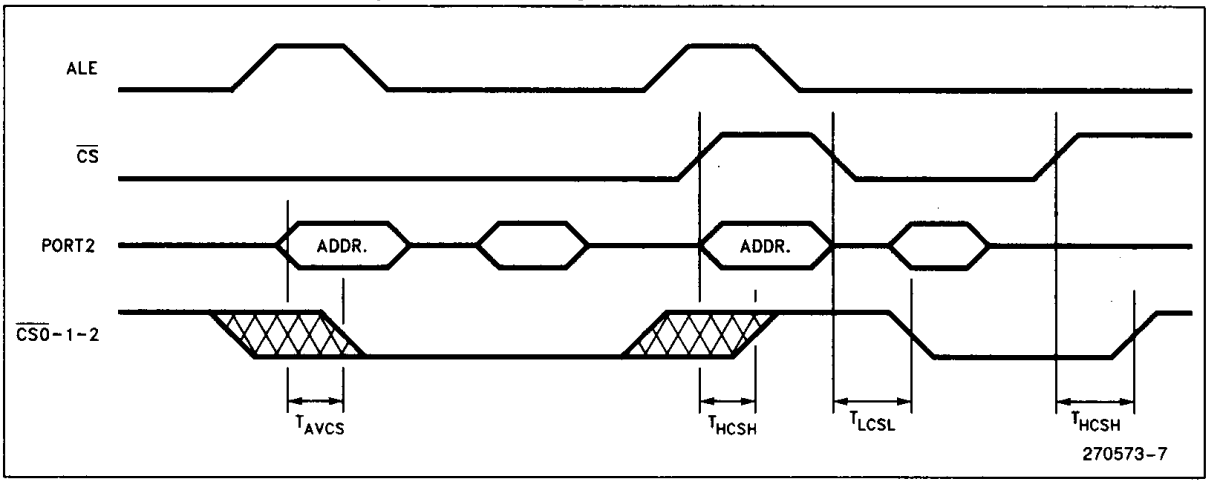
$\overline{CS0}$-1-2 OUTPUTS TIMING

Mode programmed: outputs change on ALE or $\overline{CS}$ falling edge (whichever comes last).

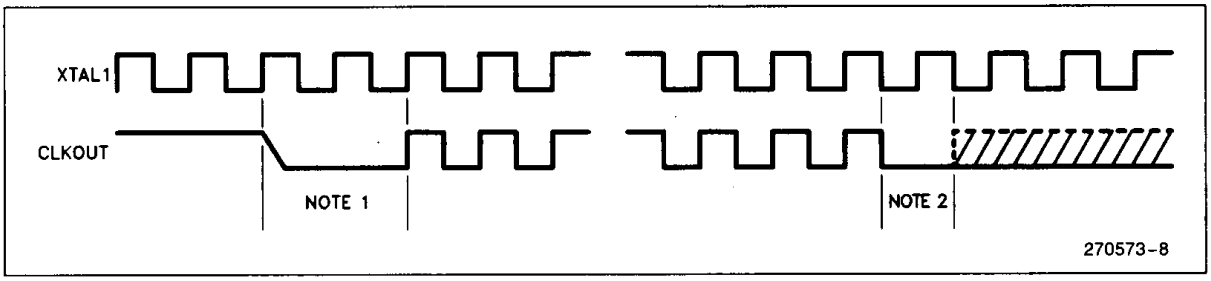


$\overline{CS0}$-1-2 OUTPUTS TIMING

Mode programmed: outputs change when ALE is high.

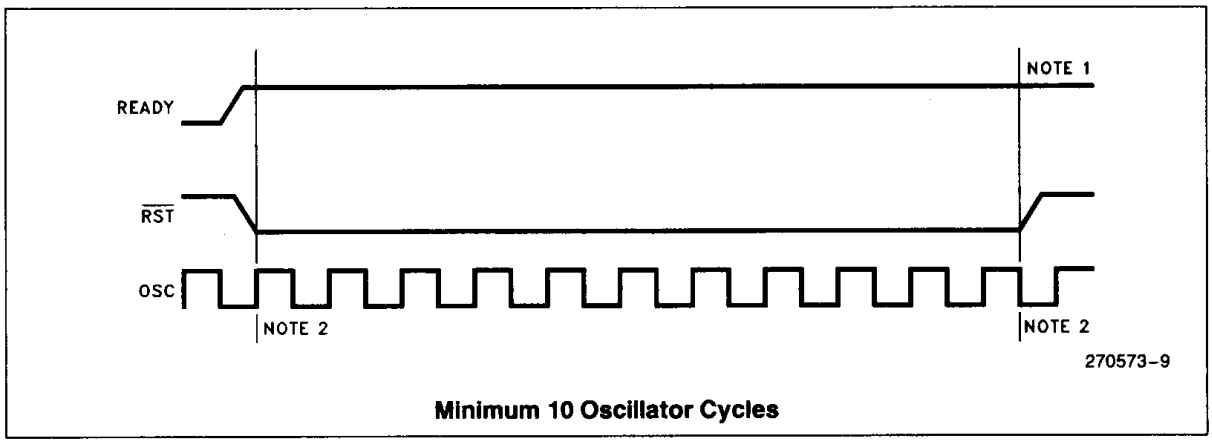


FREQUENCY TRANSITION TIME FOR CLOCKOUT LOGIC "0"



NOTES:
1. $F_{OUT} = F_{XTAL}$/Divider Register $\rightarrow$ $F_{OUT} = F_{XTAL}$ max Logic "0" = 2 T_{XTAL}
2. $F_{OUT} = F_{XTAL} \rightarrow F_{OUT} = F_{XTAL}$/Divider Register
max Logic "0" = 1.5 T_{XTAL} If Divider Register = 2
max Logic "0" = (Divider Register − 1) XTAL if Divider Register > 2

RESET TIMING



NOTES:
1. Ready must not be pulled low during reset.
2. Reset timing measure from rising edge to rising edge of OSC.

DATA SHEET REVISION SUMMARY

The following are the differences between the previous 82526 data sheet and this new data sheet (rev. -003):

1. I_{OC} and I_{BC} added to page 3-42.