Dual Bootstrapped, 12 V MOSFET Driver with Output Disable

ADP3418

FEATURES

All-in-one synchronous buck driver
Bootstrapped high-side drive
1 PWM signal generates both drives
Anticross-conduction protection circuitry
Output disable control turns off both MOSFETs to float the output per Intel® VR 10 and AMD Opteron™ specifications

APPLICATIONS

Multiphase desktop CPU supplies
Single-supply synchronous buck converters

GENERAL DESCRIPTION

The ADP3418 is a dual, high voltage MOSFET driver optimized for driving two N-channel MOSFETs, the two switches in a nonisolated, synchronous, buck power converter. Each of the drivers is capable of driving a 3000 pF load with a 30 ns transition time. One of the drivers can be bootstrapped and is designed to handle the high voltage slew rate associated with floating high-side gate drivers. The ADP3418 includes overlapping drive protection to prevent shoot-through current in the external MOSFETs. The $\overline{OD}$ pin shuts off both the high-side and the low-side MOSFETs to prevent rapid output capacitor discharge during system shutdowns.

The ADP3418 is specified over the commercial temperature range of 0°C to 85°C and is available in an 8-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM

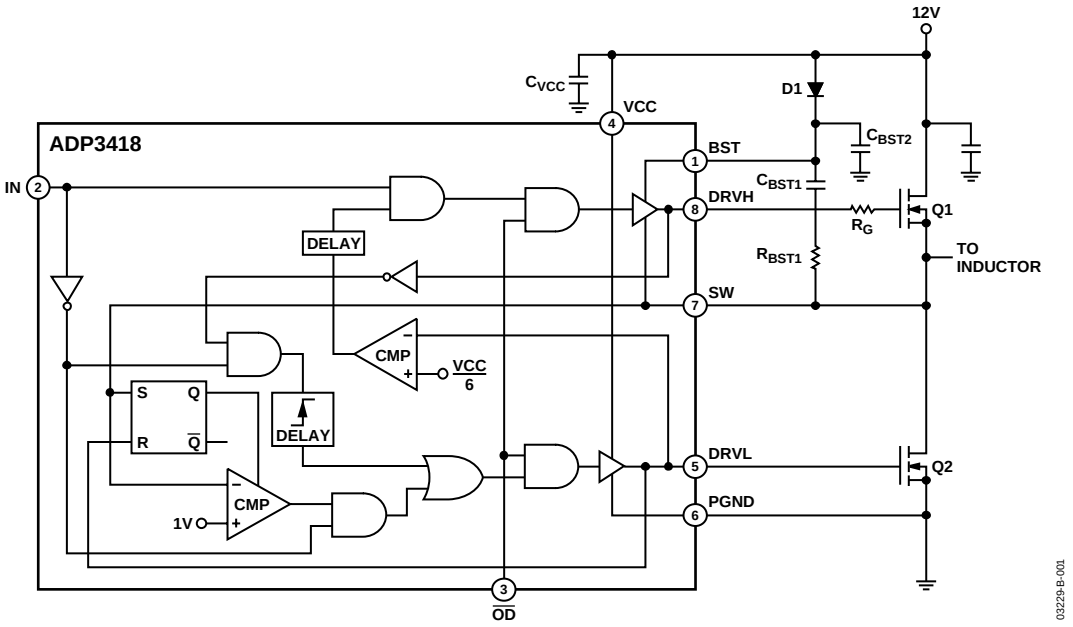

Figure 1.

Rev. D

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3/03—Revision 0: Initial Version

SPECIFICATIONS[1]

V_{CC} = 12 V, BST = 4 V to 26 V, T_A = 0°C to 85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	V_{CC}		4.15		13.2	V
Supply Current	I_{SYS}	BST = 12 V, IN = 0 V		3	6	mA
$\overline{OD}$ INPUT						
Input Voltage High			2.6			V
Input Voltage Low					0.8	V
Input Current			−1		+1	µA
Propagation Delay Time	$t_{pdh\overline{OD}}$	See Figure 3		25	40	ns
	$t_{pdl\overline{OD}}$	See Figure 3		20	40	ns
PWM INPUT						
Input Voltage High			3.0			V
Input Voltage Low					0.8	V
Input Current			−1		+1	µA
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		$V_{BST} - V_{SW}$ = 12 V		1.8	3.0	Ω
Output Resistance, Sinking Current		$V_{BST} - V_{SW}$ = 12 V		1.0	2.5	Ω
Transition Times	t_{rDRVH}	See Figure 4, $V_{BST} - V_{SW}$ = 12 V, C_{LOAD} = 3 nF		35	45	ns
	t_{fDRVH}	See Figure 4, $V_{BST} - V_{SW}$ = 12 V, C_{LOAD} = 3 nF		20	30	ns
Propagation Delay[2]	$t_{pdhDRVH}$	See Figure 4, $V_{BST} - V_{SW}$ = 12 V	10	40	65	ns
	$t_{pdlDRVH}$	$V_{BST} - V_{SW}$ = 12 V		20	35	ns
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current				1.8	3.0	Ω
Output Resistance, Sinking Current				1.0	2.5	Ω
Transition Times	t_{rDRVL}	See Figure 4, C_{LOAD} = 3 nF		25	35	ns
	t_{fDRVL}	See Figure 4, C_{LOAD} = 3 nF		21	30	ns
Propagation Delay[2]	$t_{pdhDRVL}$	See Figure 4	5	30	60	ns
	$t_{pdlDRVL}$	See Figure 4		10	20	ns
Timeout Delay		SW = 5 V		240		ns
		SW = PGND	90	120		ns

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] For propagation delays, t_{pdh} refers to the specified signal going high, and t_{pdl} refers to it going low.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
BST	
DC	−0.3 V to V_{CC} + 15 V
<200 ns	−0.3 V to +36 V
BST to SW	−0.3 V to +15 V
SW	
DC	−5 V to +15 V
<200 ns	−10 V to +25 V
DRVH (DC)	SW − 0.3 V to BST + 0.3 V
DRVH (<200 ns)	SW − 2 V to BST + 0.3 V
DRVL (DC)	−0.3 V to V_{CC} + 0.3 V
DRVL (<200 ns)	−2 V to V_{CC} + 0.3 V
IN, $\overline{OD}$	−0.3 V to +6.5 V
Operating Ambient Temperature Range	0°C to 85°C
Operating Junction Temperature Range	0°C to 150°C
Storage Temperature Range	−65°C to +150°C
Junction-to-Air Thermal Resistance (θ_{JA})	
2-Layer Board	123°C/W
4-Layer Board	90°C/W
Lead Temperature (Soldering, 10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to PGND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

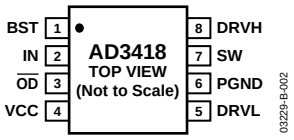


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high-side MOSFET as it is switched. The capacitor should be between 100 nF and 1 µF.
2	IN	Logic Level Input. This pin has primary control of the drive outputs.
3	$\overline{OD}$	Output Disable. When low, this pin disables normal operation, forcing DRVH and DRVL low.
4	VCC	Input Supply. This pin should be bypassed to PGND with a ~1 µF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SW	This pin is connected to the buck switching node, close to the upper MOSFET's source. It is the floating return for the upper MOSFET drive signal.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.

TIMING CHARACTERISTICS

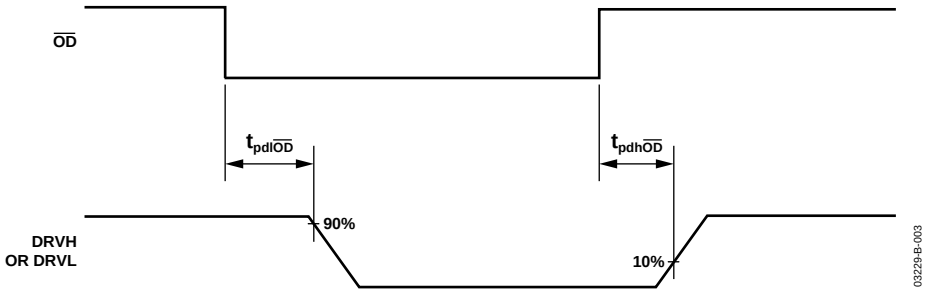


Figure 3. Output Disable Timing Diagram

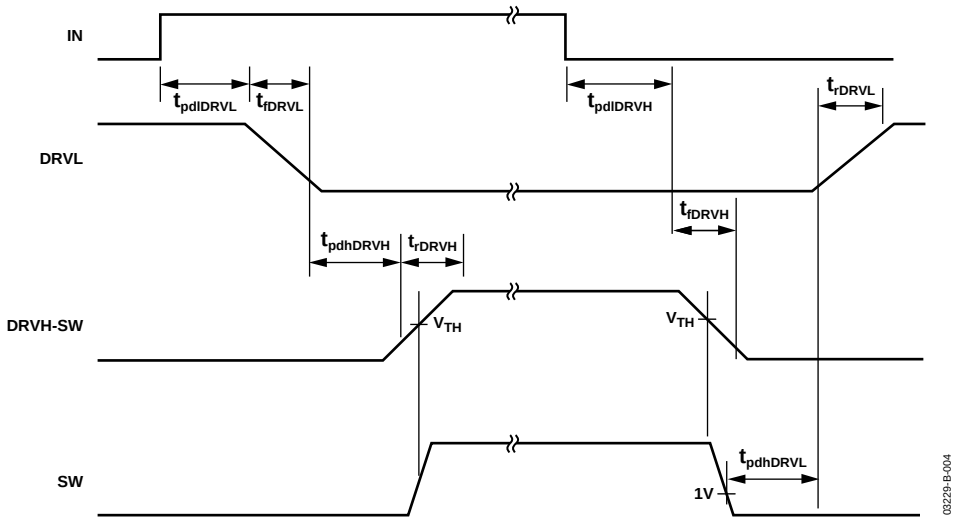


Figure 4. Timing Diagram—Timing Is Referenced to the 90% and 10% Points, Unless Otherwise Noted

TYPICAL PERFORMANCE CHARACTERISTICS

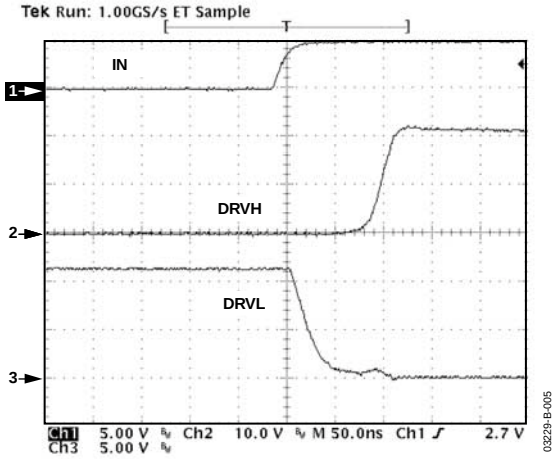


Figure 5. DRVH Rise and DRVL Fall Times

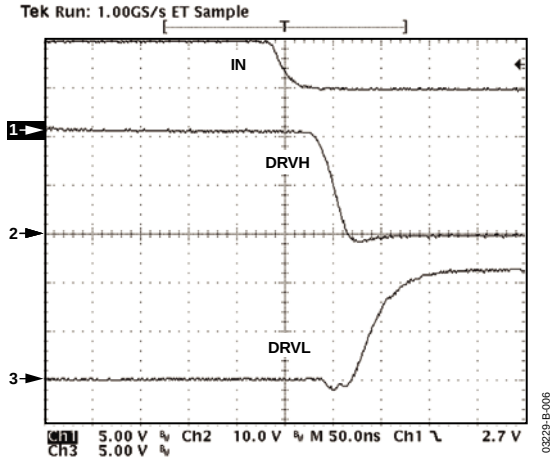


Figure 6. DRVH Fall and DRVL Rise Times

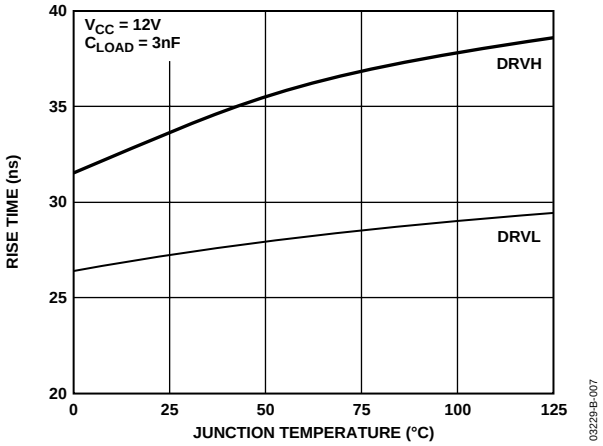


Figure 7. DRVH and DRVL Rise Times vs. Junction Temperature

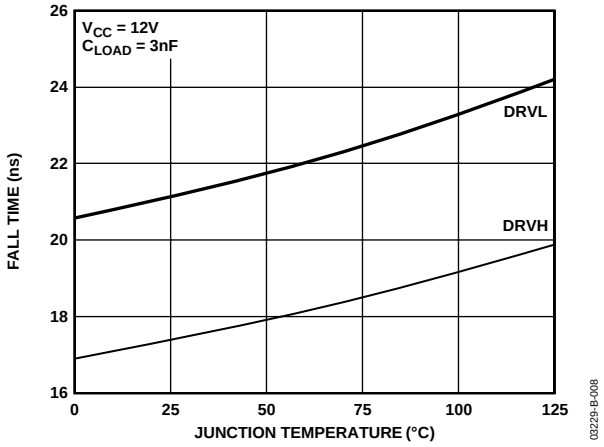


Figure 8. DRVH and DRVL Fall Times vs. Junction Temperature

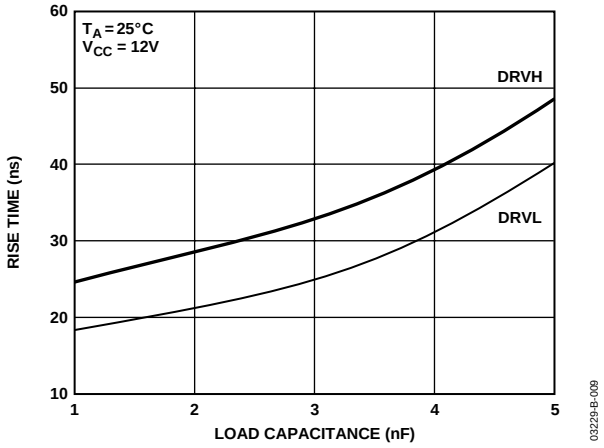


Figure 9. DRVH and DRVL Rise Times vs. Load Capacitance

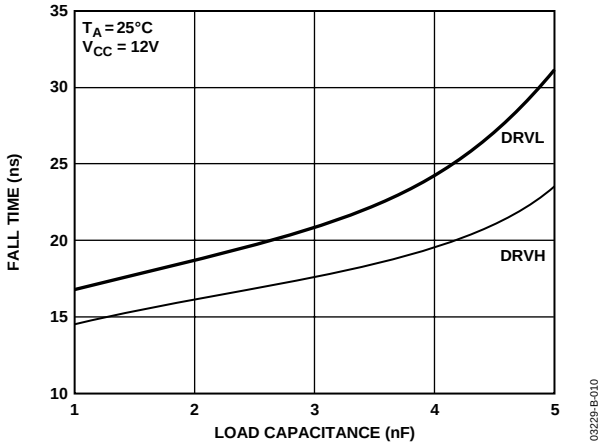


Figure 10. DRVH and DRVL Fall Times vs. Load Capacitance

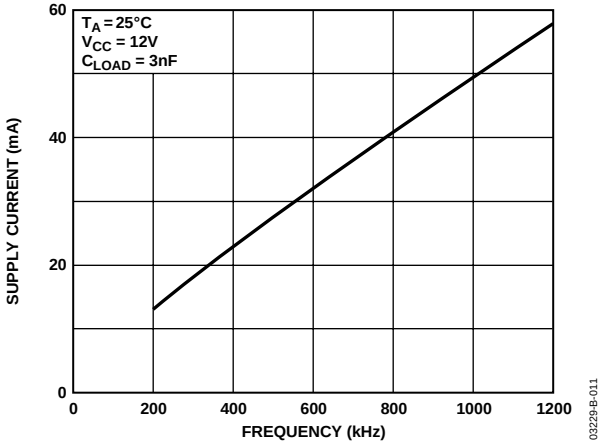


Figure 11. Supply Current vs. Frequency

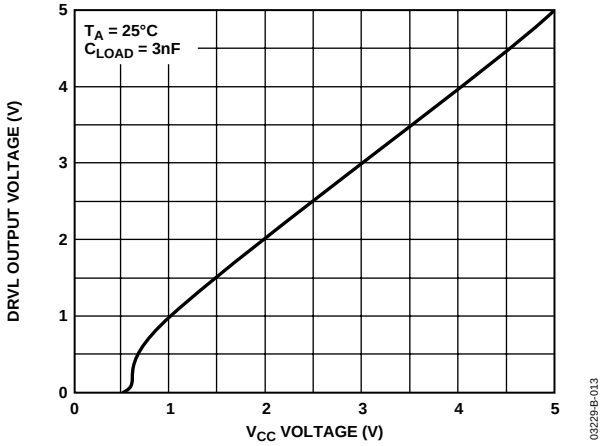


Figure 13. DRVL Output Voltage vs. Supply Voltage

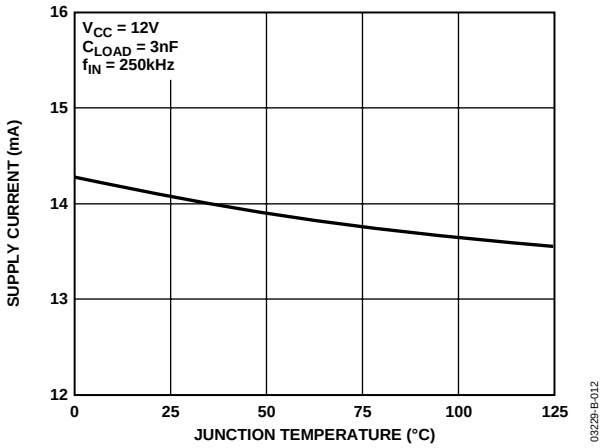


Figure 12. Supply Current vs. Junction Temperature

THEORY OF OPERATION

The ADP3418 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 500 kHz.

A more detailed description of the ADP3418 and its features follows. Refer to Figure 1.

LOW-SIDE DRIVER

The low-side driver is designed to drive a ground-referenced N-channel MOSFET. The bias to the low-side driver is internally connected to the V_{CC} supply and PGND.

When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the ADP3418 is disabled, the low-side gate is held low.

HIGH-SIDE DRIVER

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the BST and SW pins.

The bootstrap circuit comprises a diode, D1, and bootstrap capacitor, C_{BST1}. C_{BST2} and R_{BST} are included to reduce the high-side gate drive voltage and limit the switch node slew rate (referred to as a Boot-Snap™ circuit, see the Application Information section for more details). When the ADP3418 starts up, the SW pin is at ground; therefore, the bootstrap capacitor charges up to V_{CC} through D1. When the PWM input goes high, the high-side driver begins to turn on the high-side MOSFET, Q1, by pulling charge out of C_{BST1} and C_{BST2}. As Q1 turns on, the SW pin rises up to V_{IN}, forcing the BST pin to $V_{IN} + V_{C\,(BST)}$, which is enough gate-to-source voltage to hold Q1 on. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET, Q2, turns on, the SW pin pulls to ground. This allows the bootstrap capacitor to charge up to V_{CC} again.

The high-side driver's output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

OVERLAP PROTECTION CIRCUIT

The overlap protection circuit prevents both of the main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on/off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from the Q1 turn off to the Q2 turn on, and by internally setting the delay from the Q2 turn off to the Q1 turn on.

To prevent the overlap of the gate drives during the Q1 turn off and the Q2 turn on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 begins to turn off (after propagation delay). Before Q2 can turn on, the overlap protection circuit ensures that SW has first gone high and then waits for the voltage at the SW pin to fall from V_{IN} to 1 V. Once the voltage on the SW pin falls to 1 V, Q2 begins to turn on. If the SW pin had not gone high first, the Q2 turn on is delayed by a fixed 120 ns. By waiting for the voltage on the SW pin to reach 1 V or for the fixed delay time, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, input pulse width, gate charge, and drive current. If SW does not go below 1 V after 240 ns, DRVL turns on. This can occur if the current flowing in the output inductor is negative and is flowing through the high-side MOSFET body diode.

To prevent the overlap of the gate drives during the Q2 turn off and the Q1 turn on, the overlap circuit provides an internal delay that is set to 40 ns. When the PWM input signal goes high, Q2 begins to turn off (after a propagation delay), but before Q1 can turn on, the overlap protection circuit waits for the voltage at DRVL to drop to approximately one sixth of V_{CC}. Once the voltage at DRVL has reached this point, the overlap protection circuit waits for the 40 ns internal delay time. Once the delay period has expired, Q1 turns on.

APPLICATION INFORMATION

SUPPLY CAPACITOR SELECTION

For the supply input (V_{CC}) of the ADP3418, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn, such as a 4.7 µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the ADP3418.

BOOTSTRAP CIRCUIT

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a diode, as shown in Figure 1. These components can be selected after the high-side MOSFET is chosen. The bootstrap capacitor must have a voltage rating that is able to handle twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitor values are determined by:

$$C_{BST1} + C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} \quad (1)$$

$$\frac{C_{BST1}}{C_{BST1} + C_{BST2}} = \frac{V_{GATE}}{V_{CC} - V_D} \quad (2)$$

where:

Q_{GATE} is the total gate charge of the high-side MOSFET at V_{GATE}.

V_{GATE} is the desired gate drive voltage (usually in the 5 V to 10 V range, 7 V being typical).

V_D is the voltage drop across D1.

Rearranging Equation 1 and Equation 2 to solve for C_{BST1} yields

$$C_{BST1} = 10 \times \frac{Q_{GATE}}{V_{CC} - V_D}$$

C_{BST2} can then be found by rearranging Equation 1 as

$$C_{BST2} = 10 \times \frac{Q_{GATE}}{V_{GATE}} - C_{BST1}$$

For example, an NTD60N02 has a total gate charge of approximately 12 nC at V_{GATE} = 7 V. Using V_{CC} = 12 V and V_D = 1 V, one finds C_{BST1} = 12 nF and C_{BST2} = 6.8 nF. Good quality ceramic capacitors should be used.

R_{BST} is used for slew rate limiting to minimize the ringing at the switch node. It also provides peak current limiting through D1. An R_{BST} value of 1.5 Ω to 2.2 Ω is a good choice. The resistor needs to be able to handle at least 250 mW due to the peak currents that flow through it.

A small signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15 V rating to withstand the maximum supply voltage. The average forward current is estimated by

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \quad (3)$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating is calculated by

$$I_{F(PEAK)} = \frac{V_{CC} - V_D}{R_{BST}} \quad (4)$$

MOSFET SELECTION

When interfacing the ADP3418 to external MOSFETs, there are a few considerations that the designer should be aware of. These help make a more robust design that minimizes stresses on both the driver and MOSFETs. These stresses include exceeding the short-time duration voltage ratings on the driver pins as well as the external MOSFET.

It is also highly recommended to use the Boot-Snap circuit to improve the interaction of the driver with the characteristics of the MOSFETs. If a simple bootstrap arrangement is used, make sure to include a proper snubber network on the SW node.

HIGH-SIDE (CONTROL) MOSFETS

The high-side MOSFET is usually high speed to minimize switching losses (see any ADI Flex-Mode™[1] controller data sheet for more details on MOSFET losses). This usually implies a low gate resistance and a low input capacitance/charge device. Yet, there is also a significant source lead inductance that can exist. This depends mainly on the MOSFET package; it is best to contact the MOSFET vendor for this information.

The ADP3418 DRVH output impedance and the input resistance of the MOSFETs determine the rate of charge delivery to the gate's internal capacitance, which determines the speed at which the MOSFETs turn on and off. However, due to potentially large currents flowing in the MOSFETs at the on and off times (this current is usually larger at turn off due to ramping up of the output current in the output inductor), the source lead inductance generates a significant voltage across it when the high-side MOSFETs switch off. This creates a significant drain-source voltage spike across the internal die of the MOSFETs and can lead to a catastrophic avalanche. The mechanisms involved in this avalanche condition can be referenced in literature from the MOSFET suppliers.

[1] Flex-Mode is protected by U.S. Patent 6,683,441.

The MOSFET vendor should provide a maximum voltage slew rate at the drain current rating such that this can be designed around. Once this specification is had, the next step is to determine the maximum current expected to be seen in the MOSFET. This can be done by

$$I_{MAX} = I_{DC}(per\ phase) + (V_{CC} - V_{OUT}) \times \frac{D_{MAX}}{f_{MAX} \times L_{OUT}} \quad (5)$$

where:

D_{MAX} is determined for the VR controller being used with the driver. Note that this current is divided roughly equally between MOSFETs if more than one is used (assume a worst-case mismatch of 30% for design margin).

L_{OUT} is the output inductor value.

When producing the design, there is no exact method for calculating the dV/dt due to the parasitic effects in the external MOSFETs as well as the PCB. However, it can be measured to determine if it is safe. If it appears the dV/dt is too fast, an optional gate resistor can be added between DRVH and the high-side MOSFETs. This resistor slows down the dV/dt, but it also increases the switching losses in the high-side MOSFETs. The ADP3418 has been optimally designed with internal drive impedance that works with most MOSFETs to switch them efficiently while minimizing dV/dt. However, some high speed MOSFETs can require this external gate resistor, depending on the currents being switched in the MOSFET.

LOW-SIDE (SYNCHRONOUS) MOSFETS

The low-side MOSFETs are usually selected to have a low on resistance to minimize conduction losses. This usually implies a large input gate capacitance and gate charge. The first concern is to make sure the power delivery from the ADP3418's DRVL does not exceed the thermal rating of the driver (see any ADI Flex-Mode controller data sheet for details).

The next concern for the low-side MOSFETs is based on preventing them from inadvertently being switched on when the high-side MOSFET turns on. This occurs due to the drain-gate (Miller, also specified as C_{rss}) capacitance of the MOSFET. When the drain of the low-side MOSFET is switched to V_{CC} by the high-side turning on (at a rate dV/dt), the internal gate of the low-side MOSFET is pulled up by an amount roughly equal to $V_{CC} \times (C_{rss}/C_{iss})$. It is important to make sure this does not put the MOSFET into conduction.

Another consideration is the nonoverlap circuitry of the ADP3418, which attempts to minimize the nonoverlap period. During the state of the high-side turning off to low-side turning on, the SW pin is monitored (as well as the conditions of SW prior to switching) to adequately prevent overlap.

However, during the low-side turn off to high-side turn on, the SW pin does not contain information for determining the proper switching time; therefore, the state of the DRVL pin is monitored to go below one sixth of V_{CC} and then a delay is added. However, due to the Miller capacitance and internal delays of the low-side MOSFET gate, one must ensure that the Miller to input capacitance ratio is low enough, and that the low-side MOSFET internal delays are not large enough, to allow accidental turn on of the low-side when the high-side turns on.

A spreadsheet is available from ADI to assist designers with the proper selection of low-side MOSFETs.

PC BOARD LAYOUT CONSIDERATIONS

Use the following general guidelines when designing printed circuit boards:

- Trace out the high current paths and use short, wide (>20 mil) traces to make these connections.
- Connect the PGND pin of the ADP3418 as close as possible to the source of the lower MOSFET.
- The V_{CC} bypass capacitor should be located as close as possible to the VCC and PGND pins.
- Use vias to other layers when possible to maximize thermal conduction away from the IC.

The circuit in Figure 15 shows how four drivers can be combined with the ADP3188 to form a total power conversion solution for generating $V_{CC\,(CORE)}$ for an Intel CPU that is VR 10.x-compliant.

Figure 14 shows an example of the typical land patterns based on the guidelines given previously. For more detailed layout guidelines for a complete CPU voltage regulator subsystem, refer to the ADP3188 data sheet.

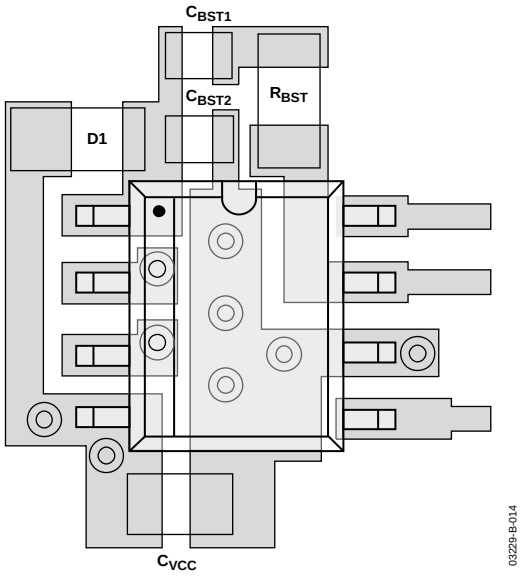


Figure 14. External Component Placement Example for the ADP3418 Driver

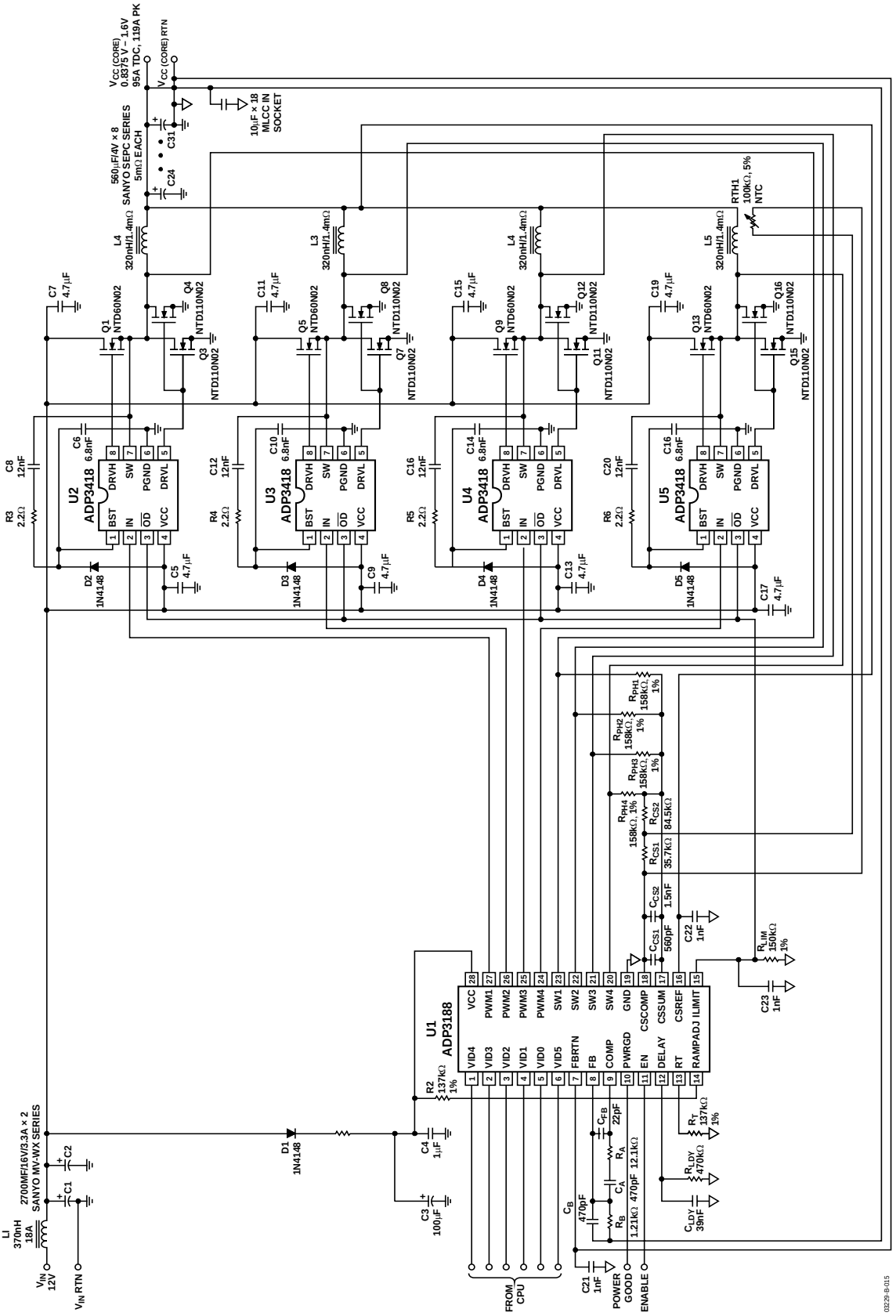
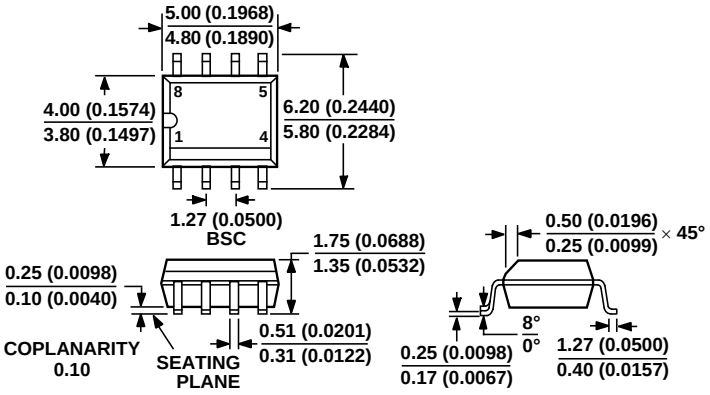


Figure 15. VR 10.x-Compliant Intel CPU Supply Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 16. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3418KRZ[1]	0°C to 85°C	8-Lead SOIC_N	R-8
ADP3418KRZ-REEL[1]	0°C to 85°C	8-Lead SOIC_N	R-8

[1] Z = Pb-free part.

NOTES

NOTES

C03229–0–3/06(D)