TOSHIBA

TX System RISC™ Product Selection Guide

TX19™ Core Features

The TX19 is an exceptionally compact, high-performance processor at 20Mips and is available as an ASIC-ready core as well as a standard product. Based on MIPS® I ISA and supporting the MIPS 16 ASE, TX19 offers the performance of a 32-bit RISC processor while delivering the compact code size associated with a 16-bit instruction set. Using an optimized interrupt circuitry, the TX19 is ideal for embedded applications requiring real-time interrupt response.

- 5-Stage Pipeline
- MIPS 32-/16-Based
- Non-Blocking Load
- Data Cache: 1Kbyte, 2-Way S/A, Write-Thru
- Instruction Cache: 4Kbyte, 2-Way S/A
- 4-Cycle MAC
- Direct Segment Mapping MMU
- DRAM, ROM, DMA and Interrupt Controller

TX39™ Core Features

TX39 offers many enhancements over the TX19 family, such as various low power modes, one-cycle MAC, register score-boarding and high-performance cache.

- 5-Stage Pipeline
- MIPS I ISA as well as some MIPS II & III Instructions
- Non-Blocking Load
- Data Cache: 4Kbyte, 2-Way S/A, Write Back/Write-Thru (3912/22)
- Instruction Cache: 8Kbyte, 2-Way S/A (3912/22)
- 1-Cycle MAC
- 64-Entry MMU/TLB, 4K to 4M (3912/22)

TX49™ Core Features

TX49 is a true 64-bit processor for high-end embedded applications. The efficient pipe line design and the register score-boarding of this family allows for reaching very high performances.

- Optimized 5-Stage Pipeline
- MIPS ISA III Plus PREF Instruction
- Non-Blocking Load
- Data Cache: 16Kbyte, 4-Way S/A, Write Back/Write-Thru
- Instruction Cache: 16Kbyte, 4-Way S/A
- 4-Cycle MAC
- 48-Entry MMU/TLB

TX System RISC Product Selection Guide

Processor	CPU Clock (MHz)	ALU Bus	Ext. Bus	ISA	I Cache	D Cache	MAC Cycles	DSU	DMAC	Memory Controller	MMU	PCI Cont.	SIO	Timer	IRC	LCD	I/O	Package FQFP Pins	Windows CE	Companion Chips
TMPR1904AF	20	32	32	I	4	1	4	●	2 Ch	ROM, DRAM	–	–	2 UART	3 Ch, WD	●	–	24	160	–	–
TMPR3904AF	50	32	32	I	4	1	1	●	4 Ch	ROM, DRAM	–	–	2 UART	3 Ch, WD	●	–	24	208	–	–
TMPR3907F	66	32	32	I	4	1	1	●	4 Ch	ROM, DRAM	–	●	1 UART	3 Ch, WD	●	–	–	208	–	–
TMPR3912AU	75/92	32	32	I	8	4	1	●	4 Ch	ROM, SDRAM	●	–	2 UART	3 Ch, WD	●	1Kx1K	39	208 [1]	●	TC35143F
TMPR3922U	148	32	32	I	8	4	1	●	4 Ch	ROM, SDRAM	●	–	2 UART	3 Ch, WD	●	–	39	208 [1]	●	TC6358
*TMPR4951U-133	133	64	32	III [2]	16	16	1	–	–	–	●	–	2 UART	3 Ch, WD	●	–		240 120	–	Note [3]

Notes

1) Chip Scale Packaging under development
2) Includes Prefetch
3) Contact www.Galileot.com
* Under development

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TX System RISC Tools Support

Tools	TX19	TX39
C/C++ Compiler	Toshiba, GHS, Cygnus (GNUPro), Metro Werks [1]	GHS, Cygnus (GNUPro), Metro Werks [1]
Assembler	Toshiba, GHS, Cygnus (GNUPro), Metro Werks [1]	GHS, Cygnus (GNUPro), Metro Werks [1]
Linker	Toshiba, GHS, Cygnus (GNUPro), Metro Werks [1]	GHS, Cygnus (GNUPro), Metro Werks [1]
Simulator	GHS, Cygnus (GNUPro), Metro Werks [1]	GHS, Cygnus (GNUPro), Metro Werks [1]
RTOS [3]	Toshiba (µITRON), CMX, ISI (pSOS), WRS (VxWorks)	Toshiba (µITRON), WRS, ISI, JMI
DSU ICE	HP, YDC	HP
Evaluation Board	Cogent, Densan	Cogent, Midas, Densan
Full ICE	Toshiba, YDC	
Windows CE		Pallas Board (3912), Juno Board (3922)

Notes
1) Under development
2) R4000 based
3) CMX, ISI, WRS under development

Companion Chips

Toshiba has developed a series of companion chips for TX System RISC products targeted for Windows CE applications. The TC35143F analog front-end is designed to operate with the TMPR3912AU in PDA applications. The TC35143F analog front-end and TC6358TB CMOS companion IC are designed to operate with the TMPR3922U in high-end Windows CE applications.

TC35143F

The TC35143F provides the analog interfaces required to complete a Windows CE PDA using a TX System RISC processor.
Specific features include:
- 14-bit Audio Codec for Recording and Playing Quality Audio Sound
- 10-bit 4-wire Resistive Touch Panel I/F
- 16-bit Telecom Codec Supporting V.90 Softmodem

TC6358TB

The TC6358TB companion IC provides the LCD driver and peripheral support required with the TMPR3922U in high-end Windows CE applications.
Specific features include:
- LCD Panel Interface
- CRT Display Interface
- PCMCIA Interface
- USB Interface
- I/O Bus Interface

One additional correction to the 16-bit selection guide.
2nd part in the OTP column should be TMP95PW64F, not TMP95PS64F.

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