FAIRCHILD SEMICONDUCTOR®

April 1988
Revised March 2005

74F245
Octal Bidirectional Transceiver with 3-STATE Outputs

General Description

The 74F245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at the A Ports and 64 mA at the B Ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A Ports to B Ports; Receive (active LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a High Z condition.

Features

- Non-inverting buffers
- Bidirectional data path
- A outputs sink 24 mA
- B outputs sink 64 mA

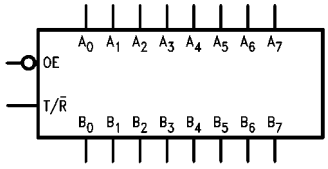
Ordering Code:

Order Number	Package Number	Package Description
74F245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F245SC_NL (Note 1)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F245SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74F245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74F245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74F245PC_NL (Note 1)	N20A	Pb-Free 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

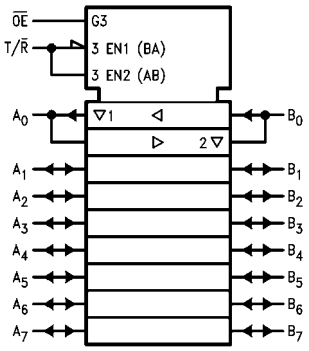
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Please use order number as indicated.

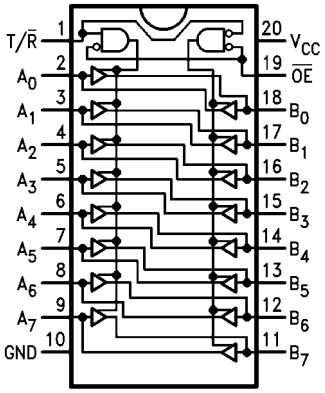
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 μA/−1.2 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/2.0	20 μA/−1.2 mA
A_0–A_7	Side A Inputs or	3.5/1.083	70 μA/−0.65 mA
	3-STATE Outputs	150/40(38.3)	−3 mA/24 mA (20 mA)
B_0–B_7	Side B Inputs or	3.5/1.083	70 μA/−0.65 mA
	3-STATE Outputs	600/106.6(80)	−12 mA/64 mA (48 mA)

Truth Table

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

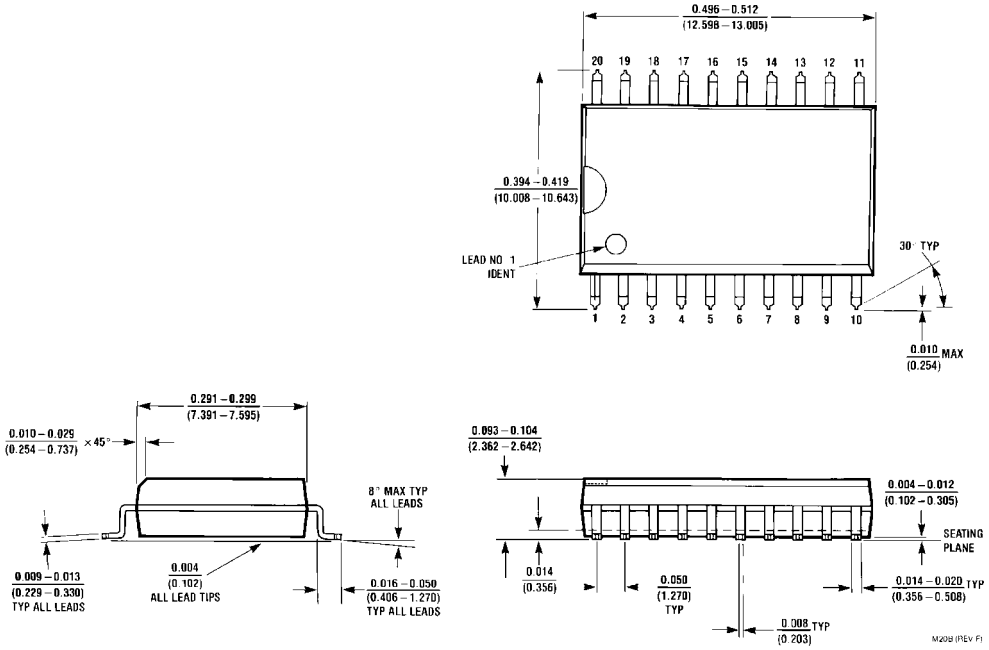
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.4			V	Min	I_{OH} = −3 mA (A_n)
		10% V_{CC}	2.0					I_{OH} = −15 mA (B_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (A_n)
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA (A_n)
		10% V_{CC}			0.55			I_{OL} = 64 mA (B_n)
I_{IH}	Input HIGH Current				5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	μA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
I_{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	V_{IN} = 5.5 V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−1.2	mA	Max	V_{IN} = 0.5V (T/$\overline{R}$, $\overline{OE}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V (A_n)
			−100		−225			V_{OUT} = 0V (B_n)
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V(A_n, B_n)
I_{CCH}	Power Supply Current			70	90	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			95	120	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			85	110	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

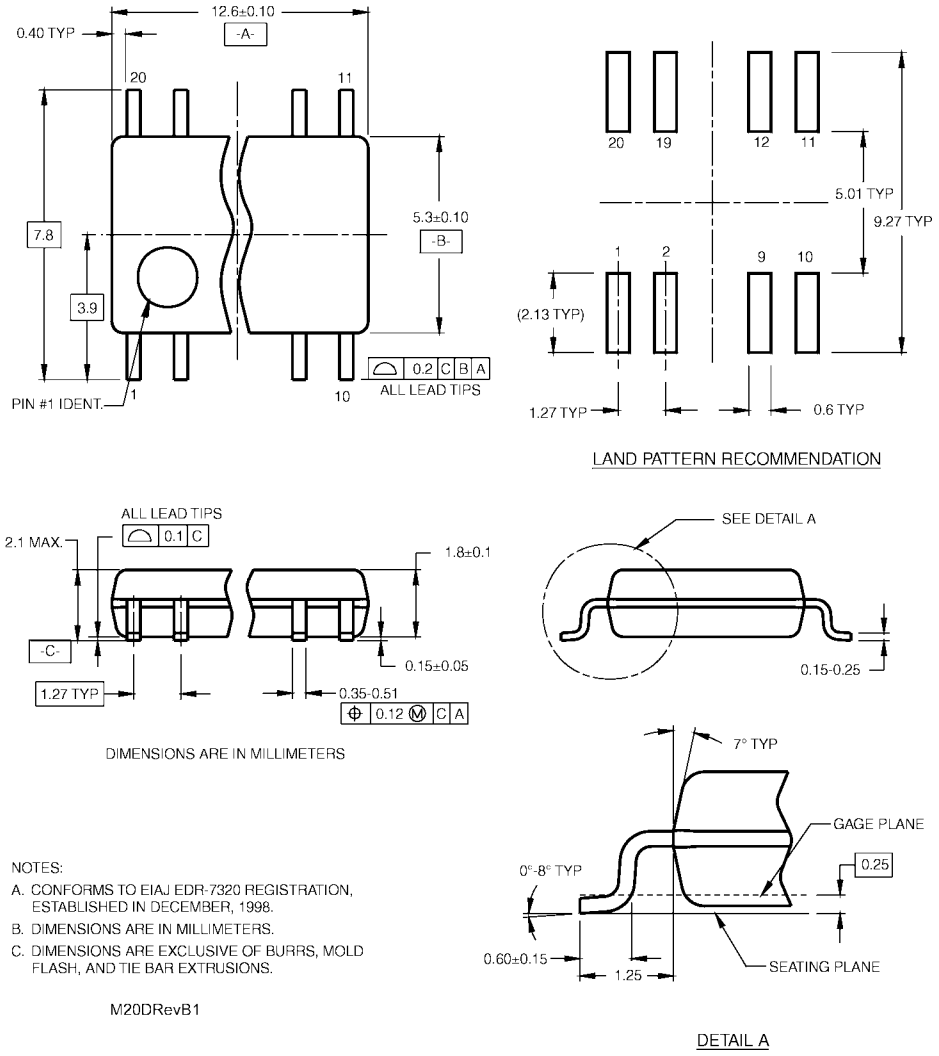
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.0	7.0	ns
t_{PHL}	A_n to B_n or B_n to A_n	2.5	4.2	6.0	2.0	7.5	2.0	7.0	
t_{PZH}	Output Enable Time	3.0	5.3	7.0	2.5	9.0	2.5	8.0	ns
t_{PZL}		3.5	6.0	8.0	3.0	10.0	3.0	9.0	
t_{PHZ}	Output Disable Time	2.0	5.0	6.5	2.0	9.0	2.0	7.5	
t_{PLZ}		2.0	5.0	6.5	2.0	10.0	2.0	7.5	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

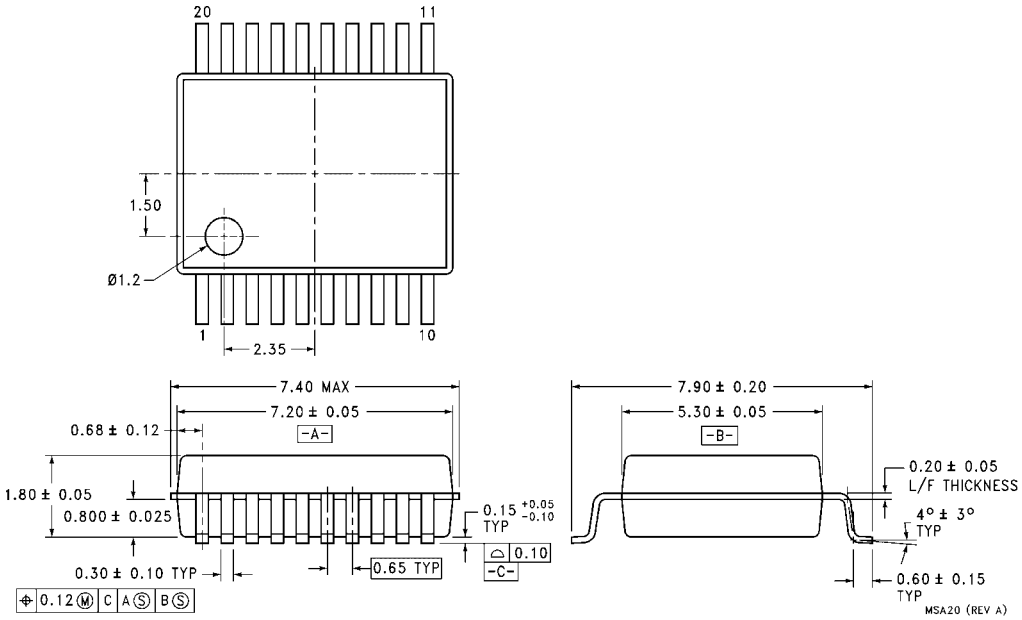
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

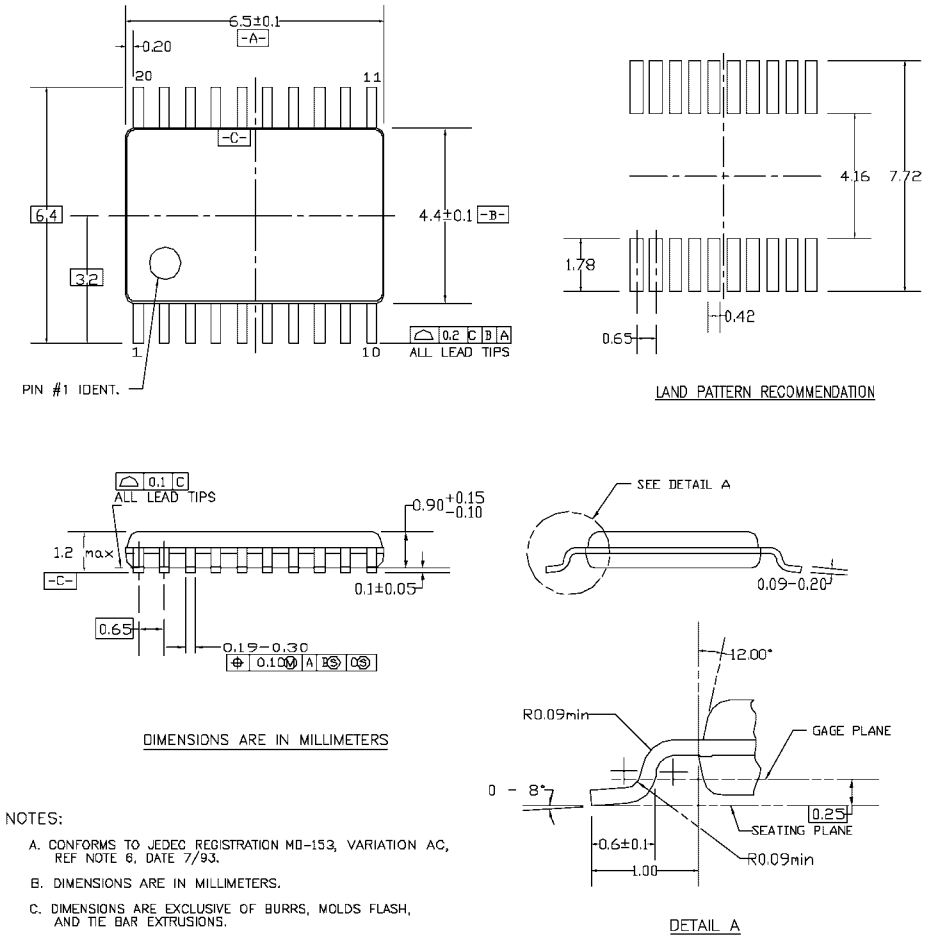
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

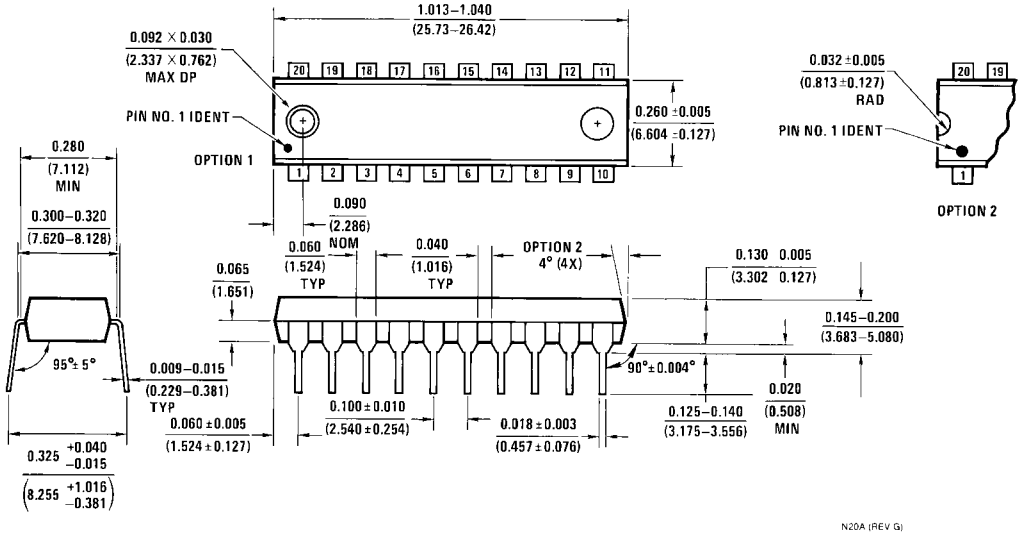
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com