28F016XS
16-MBIT (1 MBIT x 16, 2 MBIT x 8) SYNCHRONOUS FLASH MEMORY

- **Effective Zero Wait-State Performance up to 33 MHz**
  - **Synchronous Pipelined Reads**
- **SmartVoltage Technology**
  - **User-Selectable 3.3V or 5V V_{CC}**
  - **User-Selectable 5V or 12V V_{PP}**
- **0.33 MB/sec Write Transfer Rate**
- **Configurable x8 or x16 Operation**
- **56-Lead TSOP and SSOP Type I Package**
- **Backwards-Compatible with 28F008SA Command-Set**
- **2 µA Typical Deep Power-Down**
- **1 mA Typical Active I_{CC} Current in Static Mode**
- **16 Separately-Erasable/Lockable 128-Kbyte Blocks**
- **1 Million Erase Cycles per Block**
- **State-of-the-Art 0.6 µm ETOX™ IV Flash Technology**

Intel's 28F016XS 16-Mbit flash memory is a revolutionary architecture which is the ideal choice for designing truly revolutionary high-performance products. Combining very high read performance with the intrinsic nonvolatility of flash memory, the 28F016XS eliminates the traditional redundant memory paradigm of shadowing code from a slow nonvolatile storage source to a faster execution memory, such as DRAM, for improved system performance. The innovative capabilities of the 28F016XS enable the design of direct-execute code and mass storage data/file flash memory systems.

The 28F016XS is the highest performance high-density nonvolatile read/program flash memory solution available today. Its synchronous pipelined read interface, flexible V_{CC} and V_{PP} voltages, extended cycling, fast program and read performance, symmetrically-blocked architecture, and selective block locking provide a highly flexible memory component suitable for resident flash component arrays on the system board or SIMMs. The synchronous pipelined interface and x8/x16 architecture of the 28F016XS allow easy interface with minimal glue logic to a wide range of processors/buses, providing effective zero wait-state read performance up to 33 MHz. The 28F016XS's dual read voltage allows the same component to operate at either 3.3V or 5.0V V_{CC}. Programming voltage at 5V V_{PP} minimizes external circuitry in minimal-chip, space critical designs, while the 12.0V V_{PP} option maximizes program/erase performance. Its high read performance combined with flexible block locking enable both storage and execution of operating systems/application software and fast access to large data tables. The 28F016XS is manufactured on Intel's 0.6 µm ETOX IV process technology.

November 1996

Order Number: 290532-004

CONTENTS

REVISION HISTORY

Number	Description
-001	Original Version
-002	Removed support of the following features: • All page buffer operations (read, write, programming, Upload Device Information) • Command queuing • Software Sleep and Abort • Erase all Unlocked Blocks and Two-Byte Write • RY/BY# Configuration as part of the Device Configuration command Changed definition of "NC." Removed "No internal connection to die" from description. Added "xx" to Upper Byte of Command (Data) Definition in Sections 4.3 and 4.4. Modified parameters "V" and "I" of Section 5.1 to apply to "NC" pins. Increased I_{PPR} (V_{PP} Read Current) for $V_{PP} > V_{CC}$ to 200 µA at V_{CC} = 3.3V/5.0V. Changed V_{CC} = 5.0V DC Characteristics (Section 5.5) marked with Note 1 to indicate that these currents are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns. Corrected t_{PHCH} (RP# High to CLK) to be a "Min" specification at V_{CC} = 3.3V/5.0V. Corrected the graphical representation of t_{WHCH} and t_{EHCH} in Figures 15 and 16. Increased Typical "Byte/Word Program Times" (t_{WHRH1A}/t_{WHRH1B}) for V_{PP} = 5.0V (Sec. 5.13): t_{WHRH1A} from 16.5 µs to 29.0 µs and t_{WHRH1B} from 24.0 µs to 35.0 µs at V_{CC} = 3.3V t_{WHRH1A} from 11.0 µs to 20.0 µs and t_{WHRH1B} from 16.0 µs to 25.0 µs at V_{CC} = 5.0V. Increased Typical "Block Program Times" (t_{WHRH2}/ t_{WHRH3}) for V_{PP} = 5.0V (Section 5.13): t_{WHRH2} from 2.2 sec to 3.8 sec and t_{WHRH3} from 1.6 sec to 2.4 sec at V_{CC} = 3.3V t_{WHRH2} from 1.6 sec to 2.8 sec and t_{WHRH3} from 1.2 sec to 1.7 sec at V_{CC} = 5.0V. Changed "Time from Erase Suspend Command to WSM Ready" spec name to "Erase Suspend Latency Time to Read;" Modified typical values and Added Min/Max values at V_{CC} =3.3/5.0V and V_{PP} =5.0/12.0V (Section 5.13). Minor cosmetic changes throughout document.
-003	Added 3/5# pin to Pinout Configuration (Figure 2), Product Overview (Section 1.1) and Lead Descriptions (Section 2.1) Modified Block Diagram (Figure 1): Removed Address Counter; Added 3/5# pin Added 3/5# pin to Test Conditions of I_{CCS} Specifications Added 3/5# pin (Y) to Timing Nomenclature (Section 5.6) Removed Note 7 of Section 5.7 Modified Device Configuration Code: Incorporated RY/BY# Configuration (Level Mode support ONLY) Modified Power-Up and Reset Timings (Section 5.10) to include 3/5# pin: Removed t_{5VPH} and t_{3VPH} specifications; Added t_{PLYL}, t_{PLYH}, t_{YLPH}, and t_{YHPH} specifications Added SSOP pinout (Figure 2) and Mechanical Specifications Corrected TSOP Mechanical Specification A1 from 0.50 mm to 0.050 mm (Section 6.0) Minor cosmetic changes throughout document.

REVISION HISTORY (Continued)

Number	Description
-004	Require all V_{CC} Tolerences to be within 5% of Operational Voltage I_{PPES} Is Pushed to 200 µA from 50 Max I_{CCD} Is Pushed to 10 µA from 5 Max Updated t_{AVAV} at 3.3V Updated t_{ELEH} at 3.3V and 5.0V

This page intentionally left blank

1.0 INTRODUCTION

The documentation of the Intel 28F016XS Flash memory device includes this datasheet, a detailed user's manual, a number of application notes and design tools, all of which are referenced in Appendix B.

The datasheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications. The *16-Mbit Flash Product Family User's Manual* provides complete descriptions of the user modes, system interface examples and detailed descriptions of all principles of operation. It also contains the full list of software algorithm flowcharts, and a brief section on compatibility with the Intel 28F008SA.

Significant 28F016XS feature revisions occurred between datasheet revisions 290532-001 and 290532-002. These revisions center around removal of the following features:

- All page buffer operations (read, write, programming, Upload Device Information)
- Command queuing
- Software Sleep and Abort
- Erase all Unlocked Blocks and Two-Byte Write
- RY/BY# Configuration options

In addition, a significant 28F016XS change occurred between datasheet revisions 290532-002 and 290532-003. This change centers around the addition of a 3/5# pin to the device's pinout configuration. Figures 2 and 3 show the 3/5# pin assignment for the TSOP and SSOP Type I packages.

Intel recommends that all customers obtain the latest revisions of 28F016XS documentation.

1.1 Product Overview

The 28F016XS is a high-performance, 16-Mbit (16,777,216-bit) block erasable nonvolatile random access memory organized as either 1 Mword x 16 or 2 Mbyte x 8, subdivided into even and odd banks. Address A_1 makes the bank selection. The 28F016XS includes sixteen 128-Kbyte (131,072 byte) blocks or sixteen 64-Kword (65,536 word) blocks. Chip memory maps for x8 and x16 modes are shown in Figures 4 and 5.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and result in greater product reliability and ease-of-use as compared to other flash memories. Significant features of the 28F016XS as compared to previous asynchronous flash memories include:

- Synchronous Pipelined Read Interface
- Significantly Improved Read and Program Performance
- SmartVoltage Technology
  - — Selectable 3.3V or 5.0 V_{CC}
  - — Selectable 5.0V or 12.0 V_{PP}
- Block Program/Erase Protection

The 28F016XS's synchronous pipelined interface dramatically raises read performance far beyond previously attainable levels. Addresses are synchronously latched and data is read from a 28F016XS bank every 30 ns (5V V_{CC}, SFI Configuration = 2). This capability translates to zero wait-state reads at clock rates up to 33 MHz at 5V V_{CC}, after an initial address pipeline fill delay and assuming even and odd banks within the flash memory are alternately accessed. Data is latched and driven valid 20 ns (t_{CHQV}) after a rising CLK edge. The 28F016XS is capable of operating up to 50 MHz (5V V_{CC}); its programmable SFI Configuration enables system design flexibility, optimizing the 28F016XS to a specific system clock frequency. See Section 4.9, SFI Configuration Table, for specific SFI Configurations for given operating frequencies.

The SFI Configuration optimizes the 28F016XS for a wide range of system operating frequencies. The default SFI Configuration is 4, which allows system boot from the 28F016XS at any frequency up to 50 MHz at 5V V_{CC}. After initiating an access, data is latched and begins driving on the data outputs after a CLK count corresponding to the SFI Configuration has elapsed. The 28F016XS will hold data valid until CE# or OE# is deactivated or a CLK count corresponding to the SFI Configuration for a subsequent access has elapsed.

The CLK and ADV# inputs, new to the 28F016XS in comparison to previous flash memories, control address latching and device synchronization during read operations. The CLK input controls the device latencies, times out the SFI Configuration counter and synchronizes data outputs. ADV# indicates the presence of a valid address on the 28F016XS

address inputs. During read operations, addresses are latched and accesses are initiated on a rising CLK edge in conjunction with ADV# low. Both CLK and ADV# are ignored by the 28F016XS during command/data write sequences.

The 28F016XS incorporates SmartVoltage technology, providing V_{CC} operation at both 3.3V and 5.0V and program and erase capability at V_{PP} = 12.0V or 5.0V. Operating at V_{CC} = 3.3V, the 28F016XS consumes less than one half the power consumption at 5.0V V_{CC}, while 5.0V V_{CC} provides highest read performance capability. V_{PP} operation at 5.0V eliminates the need for a separate 12.0V converter, while the V_{PP} = 12.0V option maximizes program/erase performance. In addition to the flexible program and erase voltages, the dedicated V_{PP} gives complete code protection with $V_{PP} \leq V_{PPLK}$.

A 3/5# input pin configures the device's internal circuitry for optimal 3.3V or 5.0V read/program operation.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows program and block erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the 28F008SA 8-Mbit FlashFile™ memory.

Software locking of memory blocks is an added feature of the 28F016XS as compared to the 28F008SA. The 28F016XS provides selectable block locking to protect code or data such as direct-executable operating systems or application code. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the 28F016XS has a master Write Protect pin (WP#) which prevents any modifications to memory blocks whose lock-bits are set.

Writing of memory data is performed in either byte or word increments, typically within 6 µs at 12.0V V_{PP}, which is a 33% improvement over the 28F008SA. A block erase operation erases one of the 16 blocks in typically 1.2 sec, independent of the other blocks.

Each block can be written and erased a minimum of 100,000 cycles. Systems can achieve one million Block Erase Cycles by providing wear-leveling algorithms and graceful block retirement. These techniques have already been employed in many flash file systems and hard disk drive designs.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later in this datasheet) and a RY/BY# output pin provide information on the progress of the requested operation.

The following Status Registers are used to provide device and WSM operation information to the user:

- A Compatible Status Register (CSR) which is 100% compatible with the 28F008SA FlashFile memory Status Register. The CSR, when used alone, provides a straightforward upgrade capability to the 28F016XS from a 28F008SA-based design.
- A Global Status Register (GSR) which also informs the system of overall Write State Machine (WSM) status.
- 16 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 5 and 6.

The 28F016XS incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

The 28F016XS also incorporates a dual chip-enable function with two input pins, CE_0# and CE_1#. These pins have exactly the same functionality as the regular chip-enable pin, CE#, on the 28F008SA. For minimum chip designs, CE_1# may be tied to ground and system logic may use CE_0# as the chip enable input. The 28F016XS uses the logical combination of these two signals to enable or disable the entire chip. Both CE_0# and CE_1# must be active low to enable the device. If either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 16-Mbit devices.

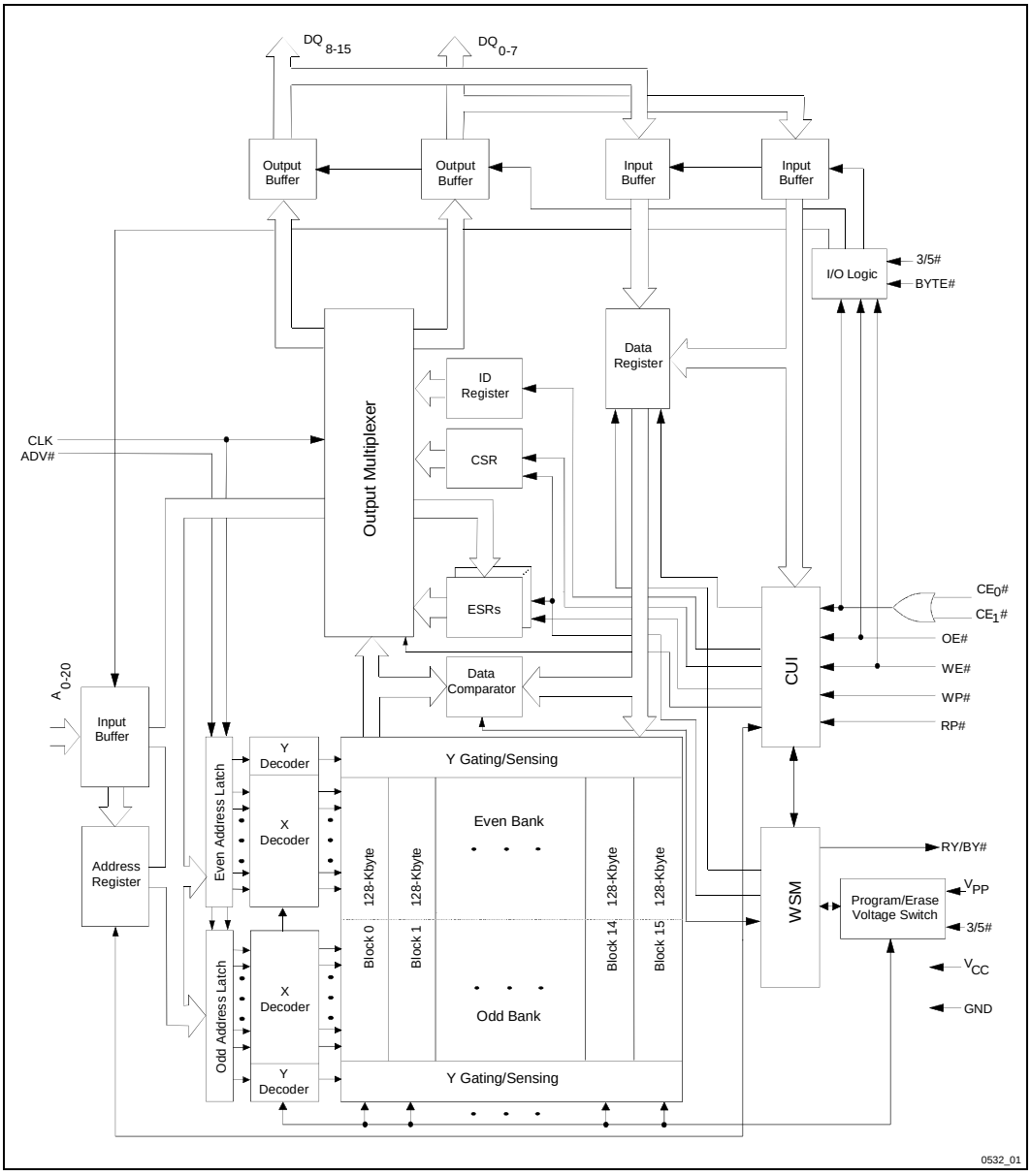


Figure 1. 28F016XS Block Diagram
Architectural Evolution Includes Synchronous Pipelined Read Interface, SmartVoltage Technology, and Extended Status Registers

The BYTE# pin allows either x8 or x16 read/programs to the 28F016XS. BYTE# at logic low selects 8-bit mode with address A_0 selecting between low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A_1 becoming the lowest order address and address A_0 is not used (don't care). A device block diagram is shown in Figure 1.

The 28F016XS incorporates an Automatic Power Saving (APS) feature, which substantially reduces the active current when the device is in static mode of operation (addresses not switching). In APS mode, the typical I_{CC} current is 1 mA at 5.0V (3 mA at 3.3V).

A deep power-down mode of operation is invoked when the RP# (called PWD# on the 28F008SA) pin transitions low. This mode brings the device power consumption to less than 2.0 µA, typically, and provides additional write protection by acting as a device reset pin during power transitions. A reset time of 300 ns (5V V_{CC}) is required from RP# switching high before latching an address into the 28F016XS. In the deep power-down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS standby mode of operation is enabled when either CE_0# or CE_1# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I_{CC} standby current of 70 µA at 5V V_{CC}.

The 28F016XS is available in 56-Lead, 1.2 mm thick, 14 mm x 20 mm TSOP and 1.8 mm thick, 16 mm x 23.7 mm SSOP Type I packages. The form factor and pinout of these two packages allow for very high board layout densities.

2.0 DEVICE PINOUT

The 28F016XS is pinout compatible with the 28F016SA/SV 16-Mbit FlashFile memory components, providing a performance upgrade path to the 28F016XS. The 28F016XS 56-Lead TSOP and SSOP pinout configurations are shown in Figures 2 and 3.

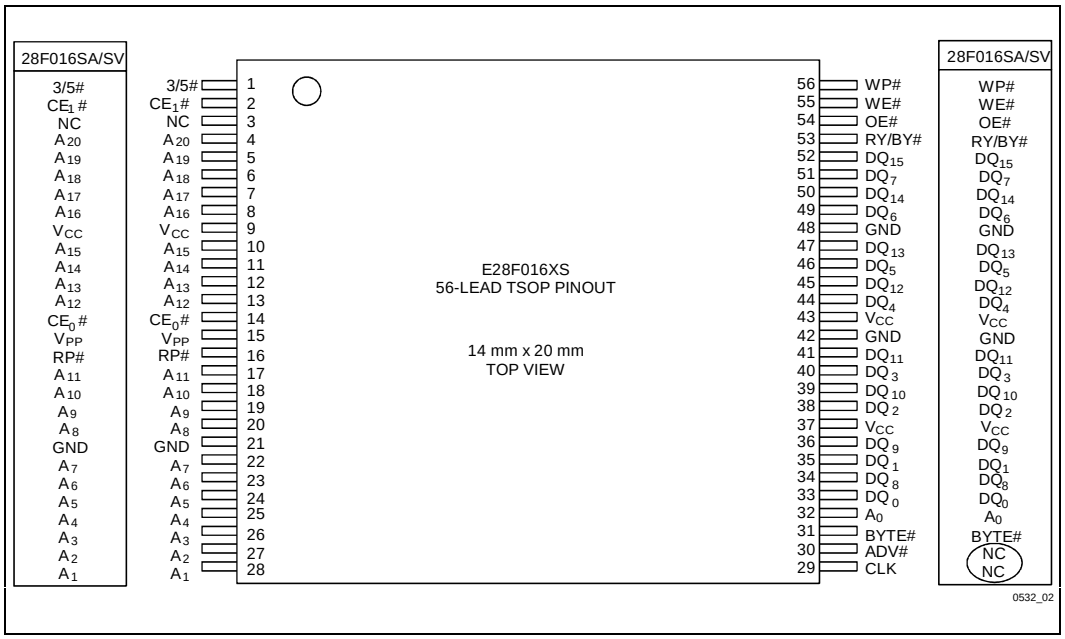


Figure 2. 28F016XS 56-Lead TSOP Pinout Configuration Shows Compatibility with the 28F016SA/SV, Allowing for Easy Performance Upgrades from Existing 16-Mbit Designs

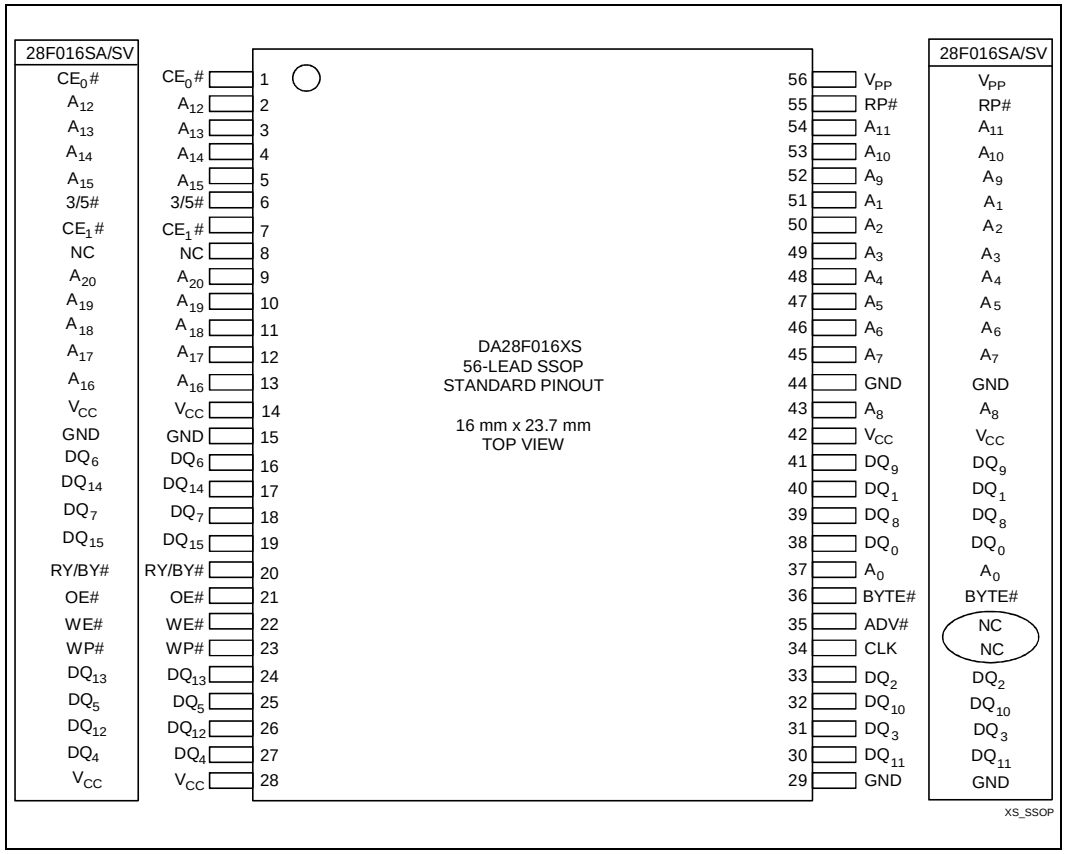


Figure 3. 28F016XS 56-Lead SSOP Pinout Configuration Shows Compatibility with the 28F016SA/SV, Allowing for Easy Performance Upgrades from Existing 16-Mbit Designs

2.1 Lead Descriptions

Symbol	Type	Name and Function
A_0	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 data programs and ignored in x16 mode (i.e., the A_0 input buffer is turned off when BYTE# is high).
A_1	INPUT	**BANK-SELECT ADDRESS:** Selects an even or odd bank in a selected block. A 128-Kbyte block is subdivided into an even and odd bank. A_1 = 0 selects the even bank and A_1 = 1 selects the odd bank, in both byte-wide mode and word-wide mode device configurations.
A_2–A_{16}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 128-Kbyte block. Address A_1 and $A_{7–16}$ select 1 of 2048 rows, and $A_{2–6}$ select 16 of 512 columns. These addresses are latched during both data reads and programs.
A_{17}–A_{20}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 16 erase blocks. These addresses are latched during data programs, erase and lock-block operations.
DQ_0–DQ_7	INPUT/ OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, identifier or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/ OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 data program operations. Outputs array or identifier data in the appropriate read mode; not used for Status Register reads. Outputs floated when the chip is de-selected, the outputs are disabled (OE# = V_{IH}) or BYTE# is driven active.
CE_0#, CE_1#	INPUT	**CHIP ENABLE INPUTS:** Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE_0# or CE_1# high, the device is de-selected and power consumption reduces to standby levels upon completion of any current data program or erase operations. Both CE_0# and CE_1# must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE_0# or CE_1#. The first rising edge of CE_0# or CE_1# disables the device.
RP#	INPUT	**RESET/POWER-DOWN:** RP# low places the device in a deep power-down state. All circuits that consume static power, even those circuits enabled in standby mode, are turned off. When returning from deep power-down, a recovery time of t_{PHCH} is required to allow these circuits to power-up. When RP# goes low, the current WSM operation is terminated, and the device is reset. All Status Registers return to ready, clearing all status flags. Exit from deep power-down places the device in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Drives device data through the output buffers when low. The outputs float to tri-state off when OE# is high. CE_X# overrides OE#, and OE# overrides WE#.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Data Register and Address Latch. WE# is active low, and latches both address and data (command or array) on its rising edge.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
CLK	INPUT	**CLOCK:** Provides the fundamental timing and internal operating frequency. CLK latches input addresses in conjunction with ADV#, times out the desired output SFI Configuration as a function of the CLK period, and synchronizes device outputs. CLK can be slowed or stopped with no loss of data or synchronization. CLK is ignored during program operations.
ADV#	INPUT	**ADDRESS VALID:** Indicates that a valid address is present on the address inputs. ADV# low at the rising edge of CLK latches the address on the address inputs into the flash memory and initiates a read access to the even or odd bank depending on the state of A_1. ADV# is ignored during program operations.
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# high indicates that the WSM is ready for new operations, erase is suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE_0#, CE_1# are high).
WP#	INPUT	**WRITE PROTECT:** Erase blocks can be locked by writing a nonvolatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent data programs or erases. When WP# is high, all blocks can be written or erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on $DQ_{0–7}$, and $DQ_{8–15}$ float. Address A_0 selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_0 input buffer. Address A_1 then becomes the lowest order address.
3/5#	INPUT	**3.3/5.0 VOLT SELECT:** 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. **NOTE:** Reading the array with 3/5# high in a 5.0V system could damage the device. Reference the power-up and reset timings (Section 5.10) for 3/5# switching delay to valid data.
V_{PP}	SUPPLY	**PROGRAM/ERASE POWER SUPPLY (12.0V ± 0.6V, 5.0V ± 0.5V) :** For erasing memory array blocks or writing words/bytes into the flash array. V_{PP} = 5.0V ± 0.5V eliminates the need for a 12.0V converter, while the 12.0V ± 0.6V option maximizes program/erase performance. Successful completion of program and erase attempts is inhibited with V_{PP} at or below 1.5V. Program and erase attempts with V_{PP} between 1.5V and 4.5V, between 5.5V and 11.4V, and above 12.6V produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 5%, 5.0V ± 5%):** To switch 3.3V to 5.0V (or vice versa), first ramp V_{CC} down to GND, and then power to the new V_{CC} voltage. Do not leave any power pins floating.

2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** Lead may be driven or left floating.

3.0 MEMORY MAPS

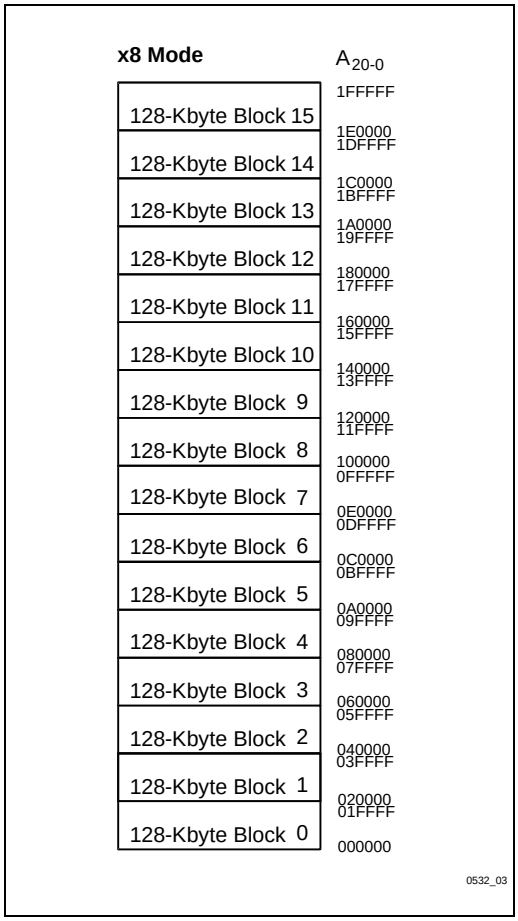


Figure 4. 28F016XS Memory Map (Byte-Wide Mode)

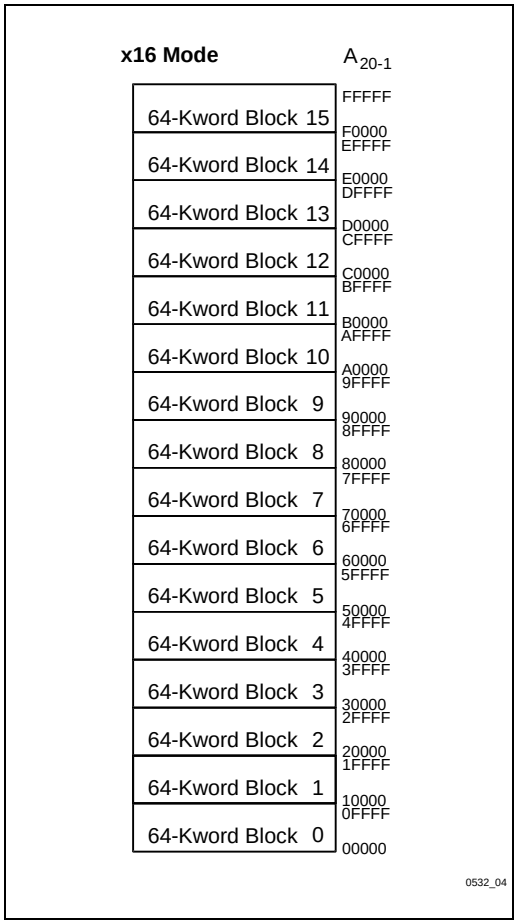


Figure 5. 28F016XS Memory Map (Word-Wide Mode)

3.1 Extended Status Register Memory Map

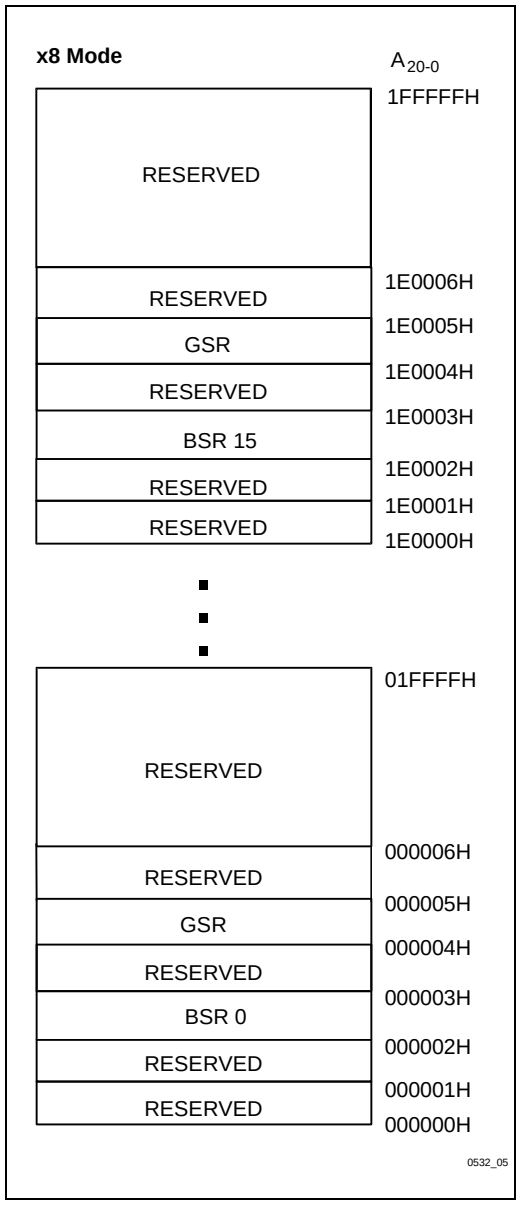


Figure 6. Extended Status Register Memory Map (Byte-Wide Mode)

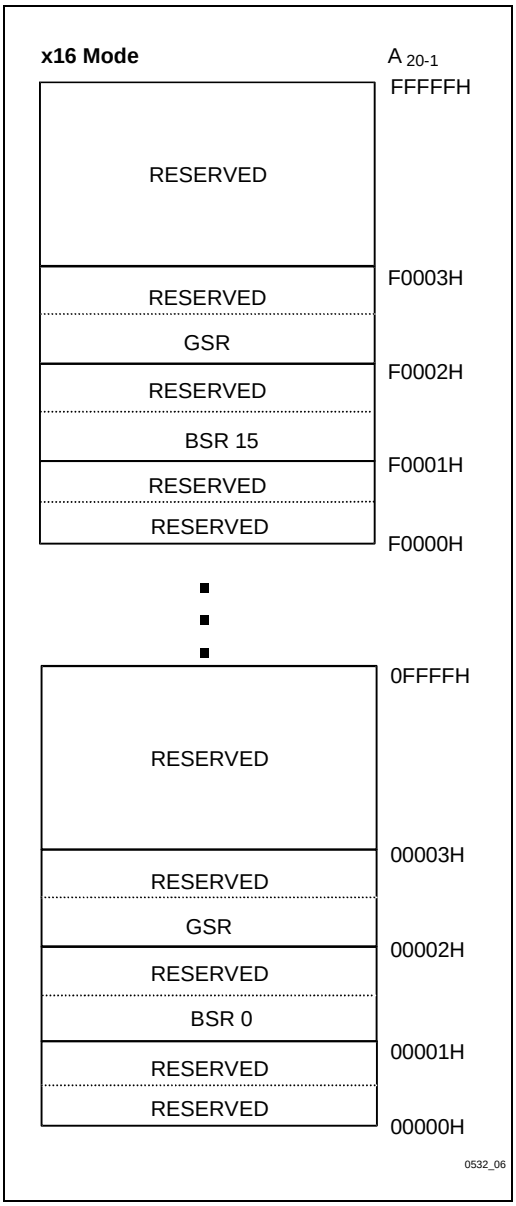


Figure 7. Extended Status Register Memory Map (Word-Wide Mode)

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (BYTE# = V_{IH})

Mode	Notes	RP#	CE_{0-1}#	OE#	WE#	ADV#	CLK	A_1	DQ_{0-15}	RY/BY#
Latch Read Address	1,9,10	V_{IH}	V_{IL}	X	V_{IH}	V_{IL}	↑	X	X	X
Inhibit Latching Read Address	1,9	V_{IH}	V_{IL}	X	V_{IH}	V_{IH}	↑	X	X	X
Read	1,2,7,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	X	D_{OUT}	X
Output Disable	1,6,7,9	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z	X
Standby	1,6,7,9	V_{IH}	V_{IL}	X	X	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	1,4,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	V_{IL}	0089H	V_{OH}
Device ID	1,4,8,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	V_{IH}	66A8H	V_{OH}
Write	1,5,6,9	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}, or High Z or D_{OUT} for data pins depending on whether or not OE# is active.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended, or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide device manufacturer codes in x8 and x16 modes respectively. A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for erase, data program, or lock-block operations can only be completed successfully when $V_{PP} = V_{PPH1}$ or $V_{PP} = V_{PPH2}$.
6. While the WSM is running, RY/BY# stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations (for example, a Status Register read during a write operation).
8. The 28F016XS shares an identical device identifier with the 28F016XD.
9. CE_{0-1}# at V_{IL} is defined as both CE_0# and CE_1# low, and CE_{0-1}# at V_{IH} is defined as either CE_0# or CE_1# high.
10. Addresses are latched on the rising edge of CLK in conjunction with ADV# low. Address $A_1 = 0$ selects the even bank and $A_1 = 1$ selects the odd bank, in both byte-wide mode and word-wide mode device configurations.

4.2 Bus Operations for Byte-Wide Mode (BYTE# = V_{IL})

Mode	Notes	RP#	CE_{0-1}#	OE#	WE#	ADV#	CLK	A_0	DQ_{0-7}	RY/BY#
Latch Read Address	1,9,10	V_{IH}	V_{IL}	X	V_{IH}	V_{IL}	↑	X	X	X
Inhibit Latching Read Address	1,9	V_{IH}	V_{IL}	X	V_{IH}	V_{IH}	↑	X	X	X
Read	1,2,7,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	X	D_{OUT}	X
Output Disable	1,6,7,9	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z	X
Standby	1,6,7,9	V_{IH}	V_{IH}	X	X	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	X	X	High Z	V_{OH}
Manufacturer ID	1,4,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	V_{IL}	89H	V_{OH}
Device ID	1,4,8,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	↑	V_{IH}	A8H	V_{OH}
Write	1,5,6,9	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}, or High Z or D_{OUT} for data pins depending on whether or not OE# is active.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended, or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. RY/BY# at V_{OH} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 and A_1 at V_{IL} provide device manufacturer codes in x8 and x16 modes respectively. A_0 and A_1 at V_{IH} provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
5. Commands for erase, data program, or lock-block operations can only be completed successfully when $V_{PP} = V_{PPH1}$ or $V_{PP} = V_{PPH2}$.
6. While the WSM is running, RY/BY# stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations (for example, a Status Register read during a program operation).
8. The 28F016XS shares an identical device identifier with the 28F016XD.
9. CE_{0-1}# at V_{IL} is defined as both CE_0# and CE_1# low, and CE_{0-1}# at V_{IH} is defined as either CE_0# or CE_1# high.
10. Addresses are latched on the rising edge of CLK in conjunction with ADV# low. Address $A_1 = 0$ selects the even bank and $A_1 = 1$ selects the odd bank, in both byte-wide mode and word-wide mode device configurations.

4.3 28F008SA—Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data[4]	Oper	Addr	Data[4]
Read Array		Write	X	xxFFH	Read	AA	AD
Intelligent Identifier	1	Write	X	xx90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	xx70H	Read	X	CSRD
Clear Status Register	3	Write	X	xx50H			
Program		Write	X	xx40H	Write	PA	PD
Alternate Program		Write	X	xx10H	Write	PA	PD
Block Erase/Confirm		Write	X	xx20H	Write	BA	xxD0H
Erase Suspend/Resume		Write	X	xxB0H	Write	X	xxD0H

ADDRESS

AA = Array Address

BA = Block Address

IA = Identifier Address

PA = Program Address

X = Don't Care

DATA

AD = Array Data

CSRD = CSR Data

ID = Identifier Data

PD = Program Data

NOTES:

1. Following the Intelligent Identifier command, two read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters data program, erase, or suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5, BSR.4 and BSR.2 bits. See Status Register definitions.
4. The upper byte of the data bus (D_{8-15}) during command writes is a "Don't Care" in x16 operation of the device.

4.4 28F016XS—Enhanced Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data[4]	Oper	Addr	Data[4]
Read Extended Status Register	1	Write	X	xx71H	Read	RA	GSRD BSRD
Lock Block/Confirm		Write	X	xx77H	Write	BA	xxD0H
Upload Status Bits/Confirm	2	Write	X	xx97H	Write	X	xxD0H
Device Configuration	3	Write	X	xx96H	Write	X	DCCD

ADDRESS	DATA
BA = Block Address	AD = Array Data
RA = Extended Register Address	BSRD = BSR Data
PA = Program Address	GSRD = GSR Data
X = Don't Care	DCCD = Device Configuration Code Data

NOTES:

1. RA can be the GSR address or any BSR address. See Figures 5 and 6 for Extended Status Register memory maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3. This command sets the SFI Configuration allowing the device to be optimized for the specific sytem operating frequency.
4. The upper byte of the Data bus ($D_{8–15}$) during command writes is a "Don't Care" in x16 operation of the device.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

NOTES:
RY/BY# output or WSMS bit must be checked to determine completion of an operation (erase, erase suspend, or data program) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

CSR.6 = ERASE-SUSPEND STATUS
1 = Erase Suspended
0 = Erase In Progress/Completed

CSR.5 = ERASE STATUS
1 = Error In Block Erasure
0 = Successful Block Erase

If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

CSR.4 = DATA WRITE STATUS
1 = Error in Data Program
0 = Data Program Successful

CSR.3 = V_{PP} STATUS
1 = V_{PP} Error Detect, Operation Abort
0 = V_{PP} OK

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max).

CSR.2–0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the CSR.

4.6 Global Status Register

WSMS	OSS	DOS	R	R	R	R	R
7	6	5	4	3	2	1	0

GSR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

NOTES:
RY/BY# output or WSMS bit must be checked to determine completion of an operation (block lock, suspend, Upload Status Bits, erase or data program) before the appropriate Status bit (OSS or DOS) is checked for success.

GSR.6 = OPERATION SUSPEND STATUS
1 = Operation Suspended
0 = Operation in Progress/Completed

GSR.5 = DEVICE OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

GSR.4–0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the GSR.

4.7 Block Status Register

BS	BLS	BOS	R	R	VPPS	VPPL	R
7	6	5	4	3	2	1	0

BSR.7 = BLOCK STATUS
1 = Ready
0 = Busy

BSR.6 = BLOCK LOCK STATUS
1 = Block Unlocked for Program/Erase
0 = Block Locked for Program/Erase

BSR.5 = BLOCK OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Currently Running

BSR.2 = V_{PP} STATUS
1 = V_{PP} Error Detect, Operation Abort
0 = V_{PP} OK

BSR.1 = V_{PP} LEVEL
1 = V_{PP} Detected at 5.0V ± 10%
0 = V_{PP} Detected at 12.0V ± 5%

BSR.4,3,0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use; mask them out when polling the BSRs.

NOTES:

RY/BY# output or BS bit must be checked to determine completion of an operation (block lock, suspend, erase or data program) before the appropriate Status bits (BOS, BLS) is checked for success.

BSR.1 is not guaranteed to report accurate feedback between the V_{PPH1} and V_{PPH2} voltage ranges. Programs and erases with V_{PP} between V_{PPLK}(max) and V_{PPH1} (min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max) produce spurious results and should not be attempted.

4.8 Device Configuration Code

R	R	SFI2	SFI1	SFI0	R	R	RB
7	6	5	4	3	2	1	0

NOTES:

DCC.5–DCC.3 = SFI CONFIGURATION (SFI2-SFI0)
001 = SFI Configuration 1
010 = SFI Configuration 2
011 = SFI Configuration 3
100 = SFI Configuration 4 (Default)

Default SFI Configuration on power-up or return from deep power-down mode is 4, allowing system boot from the 28F016XS at any frequency up to the device's maximum frequency. Undocumented combinations of SFI2-SFI0 are reserved by Intel Corporation for future implementations and should not be used.

DCC.0 = RY/BY# CONFIGURATION (RB)
1 = Level Mode (Default)

Undocumented combinations of RB are reserved by Intel Corporation for future implementations and should not be used.

DCC.7–DCC.6, DCC.2–DCC.1 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use. Set these bits to “0” when modifying the Device Configuration Code.

4.9 SFI Configuration Table

SFI Configuration	Notes	28F016XS-15 Frequency (MHz)	28F016XS-20 Frequency (MHz)	28F016XS-25 Frequency (MHz)
4	1	50 (and below)	50 (and below)	40 (and below)
3		50 (and below)	37.5 (and below)	30 (and below)
2		33 (and below)	25 (and below)	20 (and below)
1		16.7 (and below)	12.5 (and below)	10 (and below)

NOTE:
1. Default SFI Configuration after power-up or return from deep power-down mode via RP#low.

5.0 ELECTRICAL SPECIFICATIONS

NOTICE: This is a production datasheet. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

5.1 Absolute Maximum Ratings*

Temperature Under Bias .....0°C to +80°C

Storage Temperature .....–65°C to +125°C

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CC} = 3.3V ± 5% Systems

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–0.5	V_{CC} + 0.5	V	
I	Current into any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

V_{CC} = 5.0V ± 5% Systems

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	–0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2,3	–0.2	14.0	V	
V	Voltage on any Pin (except V_{CC},V_{PP}) with Respect to GND	2,5	–2.0	7.0	V	
I	Current into any Non-Supply Pin	5		± 30	mA	
I_{OUT}	Output Short Circuit Current	4		100	mA	

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} +0.5V which may overshoot to V_{CC} +2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. This specification also applies to pins marked "NC."

5.2 Capacitance

For a 3.3V ± 5% System:

Symbol	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1, 2		50	pF	For the 28F016XS-20 and 28F016XS-25

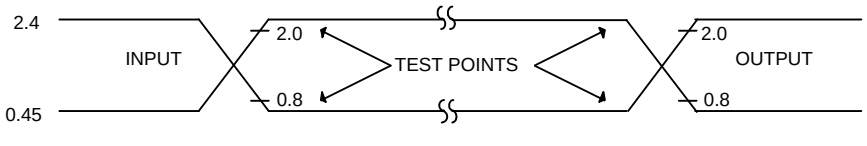
For 5.0V ± 5% System:

Symbol	Parameter	Notes	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T_A = +25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	8	12	pF	T_A = +25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1, 2		100	pF	For the 28F016XS-20
				30	pF	For the 28F016XS-15

NOTE:

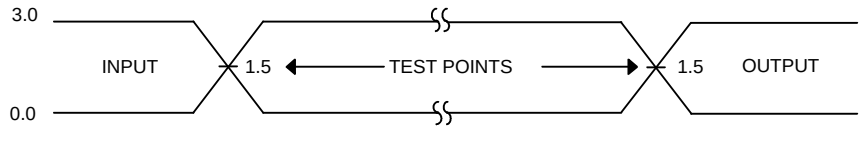
1. Sampled, not 100% tested. Guaranteed by design.
2. To obtain iBIS models for the 28F016XS, please contact your local Intel/Distribution Sales Office.

5.3 Transient Input/Output Reference Waveforms



AC test inputs are driven at V_{OH} (2.4 VTTL) for a Logic "1" and V_{OL} (0.45 VTTL) for a Logic "0." Input timing begins at V_{IH} (2.0 VTTL) and V_{IL} (0.8 VTTL). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 8. Transient Input/Output Reference Waveform (V_{CC} = 5.0V ± 5%) for Standard Testing Configuration(1)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 9. Transient Input/Output Reference Waveform (V_{CC} = 3.3V ± 5%) High Speed Reference Waveform(2) (V_{CC} = 5.0V ± 5%)

NOTES:

1. Testing characteristics for 28F016XS-20 at 5V V_{CC}.
2. Testing characteristics for 28F016XS-15 at 5V V_{CC} and 28F016XS-20/28F016XS-25 at 3.3V V_{CC}.

5.4 DC Characteristics

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Load Current	1			± 1	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5		70	130	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				1	4	mA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	5	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCR}[1]	V_{CC} Word/Byte Read Current	1,4,5		65	85	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0# ,CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V 4-Location Access Sequence: 3-1-1-1 (clocks) f = 25 MHz, I_{OUT} = 0 mA
I_{CCR}[2]	V_{CC} Word/Byte Read Current	1,4, 5,6		60	75	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V 4-Location Access Sequence: 3-1-1-1 (clocks) f = 16 MHz, I_{OUT} = 0 mA

5.4 DC Characteristics (Continued)

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{CCW}	V_{CC} Program Current	1,6		8	12	mA	V_{PP} = 12.0V ± 5% Program in Progress
				8	17	mA	V_{PP} = 5.0V ± 10% Program in Progress
I_{CCE}	V_{CC} Block Erase Current	1,6		6	12	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				9	17	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read Current	1		± 1	± 10	µA	$V_{PP} \le V_{CC}$
I_{PPR}				30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Program Current	1,6		10	15	mA	V_{PP} = 12.0V ± 5% Program in Progress
				15	25	mA	Program in Progress
I_{PPE}	V_{PP} Erase Current	1,6		4	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				14	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		30	200	µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase Suspended
V_{IL}	Input Low Voltage	6	–0.3		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC} +0.3	V	
V_{OL}	Output Low Voltage	6			0.4	V	V_{CC} = V_{CC} Min I_{OL} = 4 mA
$V_{OH}1$	Output High Voltage	6	2.4			V	V_{CC} = V_{CC} Min I_{OH} = –2.0 mA
$V_{OH}2$			V_{CC} –0.2			V	V_{CC} = V_{CC} Min I_{OH} = –100 µA

5.4 DC Characteristics (Continued)

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
V_{PPLK}	V_{PP} Erase/Program Lock Voltage	3,6	0.0		1.5	V	
V_{PPH1}	V_{PP} during Program/Erase Operations	3	4.5	5.0	5.5	V	
V_{PPH2}	V_{PP} during Program/Erase Operations	3	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Program Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 12.0V or 5.0V, T = +25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, programs and lock block operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1} (max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Savings (APS) reduces I_{CCR} to 3 mA typical in static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, but not 100% tested. Guaranteed by design.

5.5 DC Characteristics

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5.0V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Load Current	1			± 1	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1			± 10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,5		70	130	µA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{CC} ± 0.2V BYTE#, WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
				2	4	mA	$V_{CC} = V_{CC}$ Max CE_0#, CE_1#, RP# = V_{IH} BYTE#, WP#, 3/5# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		2	5	µA	RP# = GND ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
I_{CCR}[1]	V_{CC} Read Current	1,4,5		120	175	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0# ,CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V 4-Location Access Sequence: 3-1-1-1 (clocks) f = 33 MHz, I_{OUT} = 0 mA
I_{CCR}[2]	V_{CC} Read Current	1,4, 5,6		105	150	mA	$V_{CC} = V_{CC}$ Max CMOS: CE_0#, CE_1# = GND ± 0.2V, BYTE# = GND ± 0.2V, or V_{CC} ± 0.2V, Inputs = GND ± 0.2V or V_{CC} ± 0.2V 4-Location Access Sequence: 3-1-1-1 (clocks) f = 20 MHz, I_{OUT} = 0 mA

5.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5.0V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{CCW}	V_{CC} Program Current	1,6		25	35	mA	V_{PP} = 12.0V ± 5% Program in Progress
				25	40	mA	V_{PP} = 5.0V ± 10% Program in Progress
I_{CCE}	V_{CC} Erase Suspend Current	1,6		18	25	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				20	30	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Block Erase Current	1,2		5	10	mA	CE_0#, CE_1# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read Current	1		± 1	± 10	µA	$V_{PP} \leq V_{CC}$
I_{PPR}				30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V
I_{PPW}	V_{PP} Program Current	1,6		7	12	mA	V_{PP} = 12.0V ± 5% Program in Progress
				17	22	mA	V_{PP} = 5.0V ± 10% Program in Progress
I_{PPE}	V_{PP} Block Erase Current	1,6		5	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
				16	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		30	200	µA	V_{PP} = V_{PPH1} or V_{PPH2} Block Erase Suspended
V_{IL}	Input Low Voltage	6	–0.5		0.8	V	
V_{IH}	Input High Voltage	6	2.0		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	6			0.45	V	V_{CC} = V_{CC} Min I_{OL} = 5.8 mA
$V_{OH}1$	Output High Voltage	6	0.85 V_{CC}			V	V_{CC} = V_{CC} Min I_{OH} = –2.5 mA
$V_{OH}2$			V_{CC} –0.4				V_{CC} = V_{CC} Min I_{OH} = –100 µA

5.5 DC Characteristics (Continued)

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5.0V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
V_{PPLK}	V_{PP} Program/Erase Lock Voltage	3,6	0.0		1.5	V	
V_{PPH1}	V_{PP} during Program/Erase Operations		4.5	5.0	5.5	V	
V_{PPH2}	V_{PP} during Program/Erase Operations		11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Program/Erase Lock Voltage		2.0			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V or 5.0V, T = +25°C. These currents are valid for all product versions (package and speeds) and are specified for a CMOS rise/fall time (10% to 90%) of <5 ns and a TTL rise/fall time of <10 ns.
2. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases, programs and lock block operations are inhibited when $V_{PP} \le V_{PPLK}$ and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1} (max) and V_{PPH2}(min) and above V_{PPH2}(max).
4. Automatic Power Saving (APS) reduces I_{CCR} to 1 mA typical in static operation.
5. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
6. Sampled, but not 100% tested. Guaranteed by design.

5.6 Timing Nomenclature

All 3.3V system timings are measured from where signals cross 1.5V.

For 5.0V systems, use the standard JEDEC cross point definitions (standard testing) or from where signals cross 1.5V (high speed testing).

Each timing parameter consists of five characters. Some common examples are defined below:

t_{ELCH} time(t) from CE# (E) going low (L) to CLK (C) going high (H)

t_{AVCH} time(t) from address (A) valid (V) to CLK (C) going high (H)

t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
C	CLK (Clock)	L	Low
D	Data Inputs	V	Valid
Q	Data Outputs	X	Driven, but Not Necessarily Valid
E	CE# (Chip Enable)	Z	High Impedance
F	BYTE# (Byte Enable)	L	Latched
G	OE# (Output Enable)		
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready Busy)		
V	ADV# (Address Valid)		
Y	3/5# Pin		
5V	V_{CC} at 4.5V Minimum		
3V	V_{CC} at 3.0V Minimum		

5.7 AC Characteristics—Read Only Operations[1]

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C

Versions[3]			28F016XS-20		28F016XS-25		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	CLK Frequency			50		40	MHz
t_{CLK}	CLK Period		20		25		ns
t_{CH}	CLK High Time		6		8.5		ns
t_{CL}	CLK Low Time		6		8.5		ns
t_{CLCH}	CLK Rise Time			4		4	ns
t_{CHCL}	CLK Fall Time			4		4	ns
t_{ELCH}	CE_X# Setup to CLK	6	25		35		ns
t_{VLCH}	ADV# Setup to CLK		20		25		ns
t_{AVCH}	Address Valid to CLK		20		25		ns
t_{CHAX}	Address Hold from CLK		0		0		ns
t_{CHVH}	ADV# Hold from CLK		0		0		ns
t_{GLCH}	OE# Setup to CLK		20		25		ns
t_{CHQV}	CLK to Data Delay			30		35	ns
t_{PHCH}	RP# High to CLK		480		480		ns
t_{CHQX}	Output Hold from CLK	2	6		6		ns
t_{ELQX}	CE_X# to Output Low Z	2,6	0		0		ns
t_{EHQZ}	CE_X# High to Output High Z	2,6		30		30	ns
t_{GLQX}	OE# to Output Low Z	2	0		0		ns
t_{GHQZ}	OE# High to Output High Z	2		30		30	ns
t_{OH}	Output Hold from CE_X# or OE# Change, Whichever Occurs First	6	0		0		ns

5.7 AC Characteristics—Read Only Operations[1] (Continued)

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C

Versions[3]			28F016XS-15[4]		28F016XS-20[5]		
Symbol	**Parameter**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CLK}	CLK Frequency			66		50	MHz
t_{CLK}	CLK Period		15		20		ns
t_{CH}	CLK High Time		3.5		6		ns
t_{CL}	CLK Low Time		3.5		6		ns
t_{CLCH}	CLK Rise Time			4		4	ns
t_{CHCL}	CLK Fall Time			4		4	ns
t_{ELCH}	CE_X# Setup to CLK	6	25		30		ns
t_{VLCH}	ADV# Setup to CLK		15		20		ns
t_{AVCH}	Address Valid to CLK		15		20		ns
t_{CHAX}	Address Hold from CLK		0		0		ns
t_{CHVH}	ADV# Hold from CLK		0		0		ns
t_{GLCH}	OE# Setup to CLK		15		20		ns
t_{CHQV}	CLK to Data Delay			20		30	ns
t_{PHCH}	RP# High to CLK		300		300		ns
t_{CHQX}	Output Hold from CLK	2	5		5		ns
t_{ELQX}	CE_X# to Output Low Z	2,6	0		0		ns
t_{EHQZ}	CE_X# High to Output High Z	2,6		30		30	ns
t_{GLQX}	OE# to Output Low Z	2	0		0		ns
t_{GHQZ}	OE# High to Output High Z	2		30		30	ns
t_{OH}	Output Hold from CE_X# or OE# Change, Whichever Occurs First	6	0		0		ns

NOTES:

1. See AC Input/Output Reference Waveforms for timing measurements.
2. Sampled, not 100% tested. Guaranteed by design.
3. Device speeds are defined as:
   15 ns at V_{CC} = 5.0V equivalent to 20 ns at V_{CC} = 3.3V
   20 ns at V_{CC} = 5.0V equivalent to 25 ns at V_{CC} = 3.3V
4. See the high speed AC Input/Output Reference Waveforms.
5. See the standard AC Input/Output Reference Waveforms.
6. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.

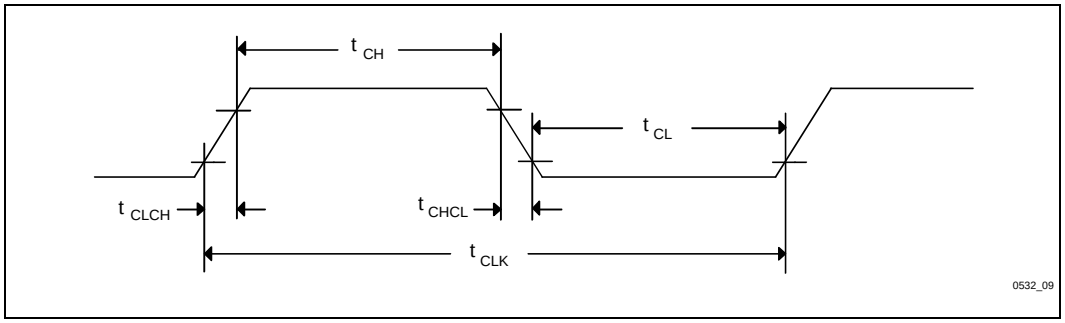
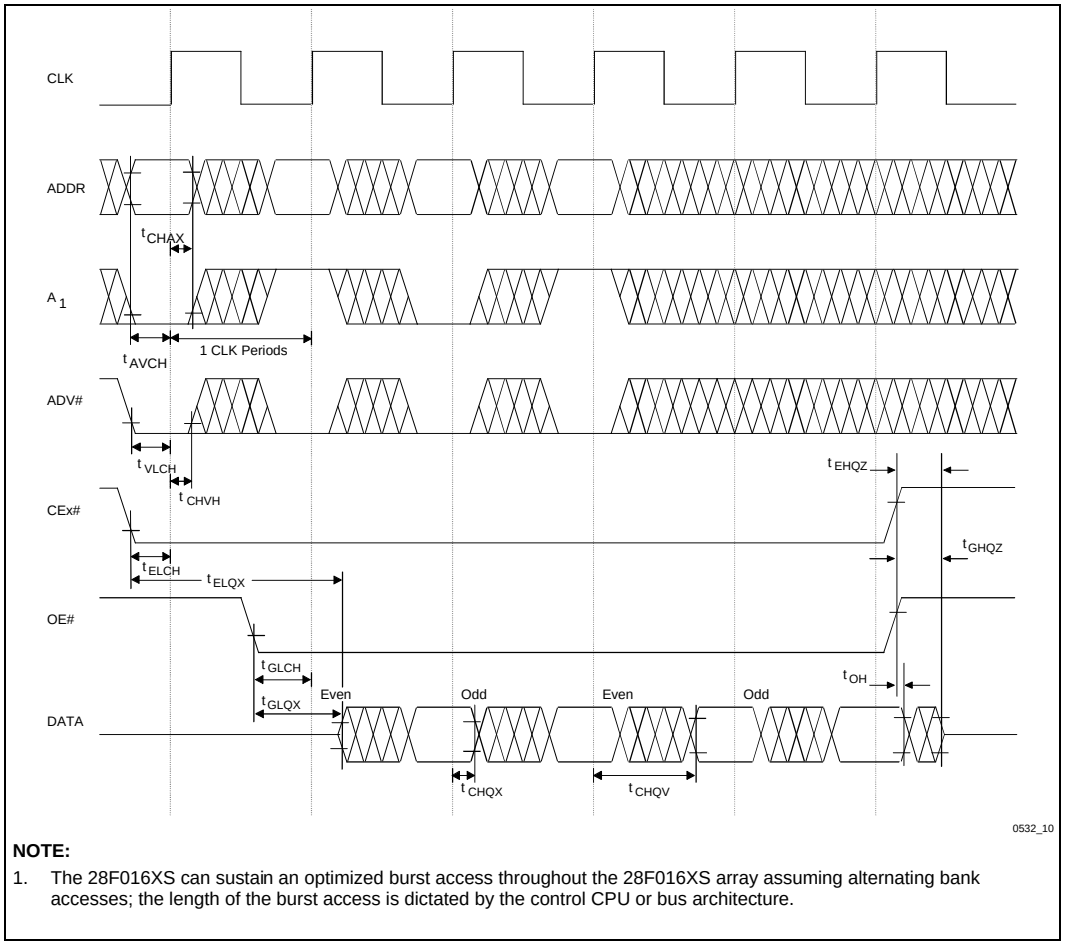


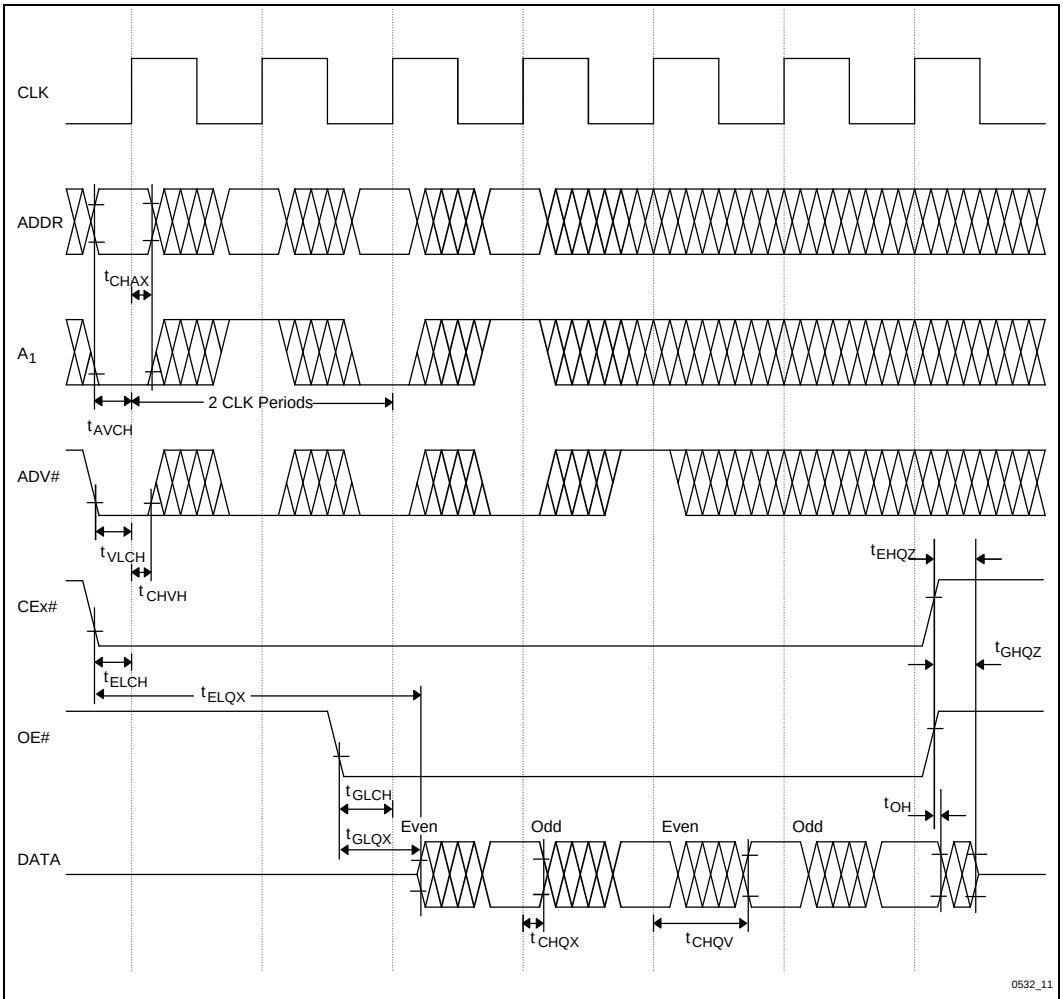
Figure 10. CLK Waveform



NOTE:

1. The 28F016XS can sustain an optimized burst access throughout the 28F016XS array assuming alternating bank accesses; the length of the burst access is dictated by the control CPU or bus architecture.

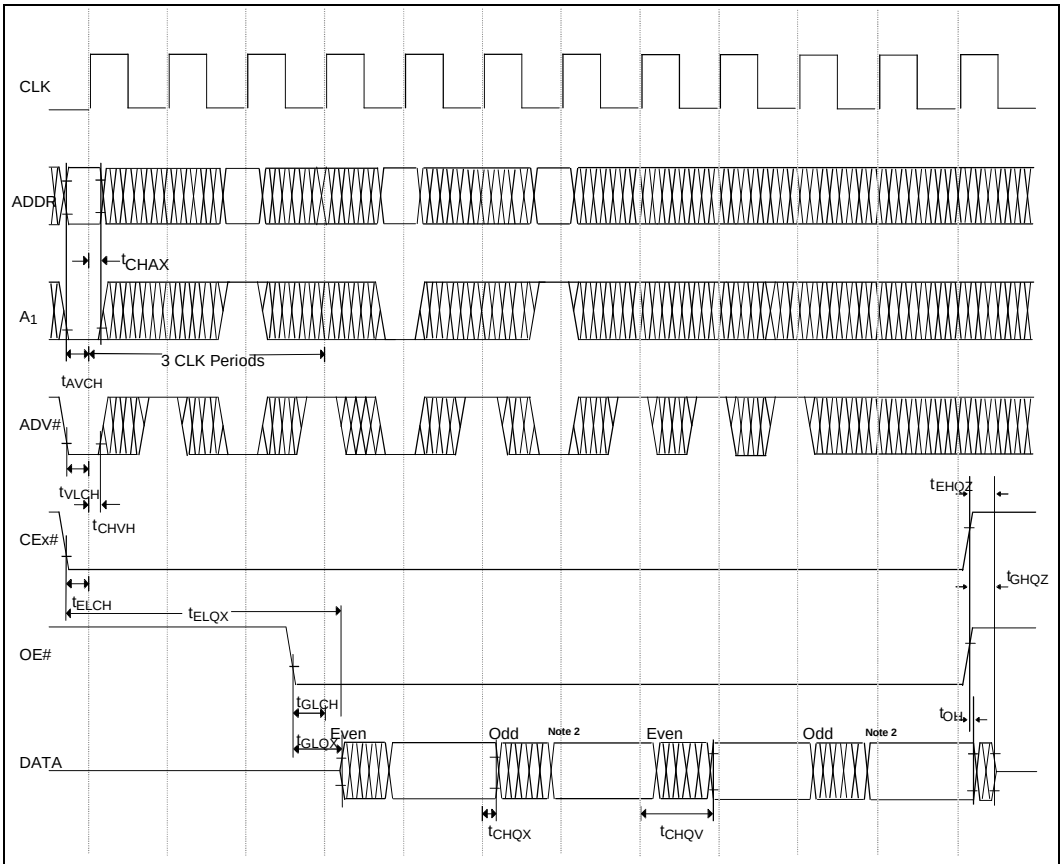
Figure 11. Read Timing Waveform(1)
(SFI Configuration = 1, Alternate-Bank Accesses)



NOTE:

1. The 28F016XS can sustain an optimized burst access throughout the 28F016XS array assuming alternating bank accesses; the length of the burst access is dictated by the control CPU or bus architecture.

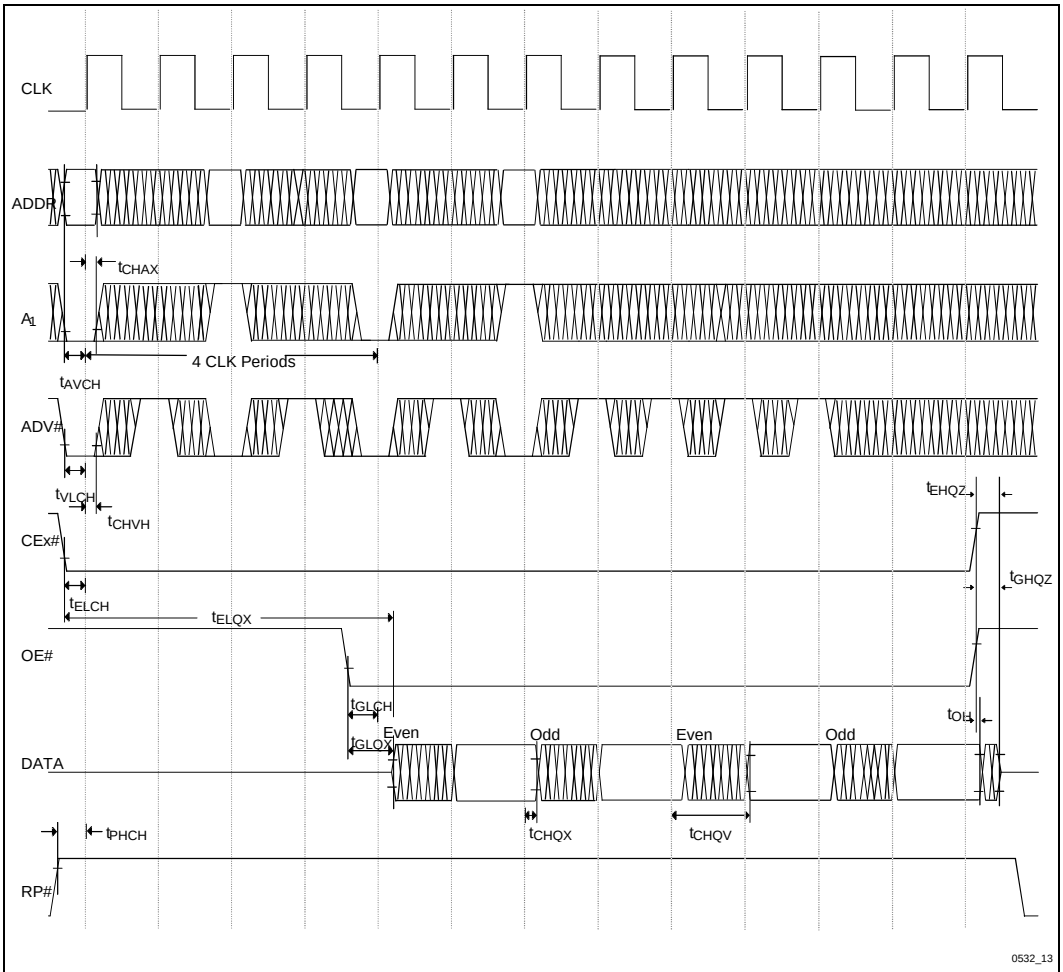
Figure 12. Read Timing Waveform(1)
(SFI Configuration = 2, Alternate-Bank Accesses)



NOTES:

1. The 28F016XS can sustain an optimized burst access throughout the 28F016XS array assuming alternating bank accesses; the length of the burst access is dictated by the control CPU or bus architecture.
2. Depending on the actual operation frequency, a consecutive alternating bank access can be initiated one clock period earlier. See *AP-398 Designing with the 28F016XS* for further information.

Figure 13. Read Timing Waveform(1)
(SFI Configuration = 3, Alternate-Bank Accesses)



NOTE:

1. The 28F016XS can sustain an optimized burst access throughout the 28F016XS array assuming alternating bank accesses; the length of the burst access is dictated by the control CPU or bus architecture.

Figure 14. Read Timing Waveform(1)
(SFI Configuration = 4, Alternating Bank Accesses)

5.8 AC Characteristics for WE#—Controlled Write Operations(1)

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C

Versions			28F016XS-20			28F016XS-25			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		75			75			ns
t_{VPWH}1,2	V_{PP} Setup to WE# Going High	3	100			100			ns
t_{PHEL}	RP# Setup to CE_X# Going Low	3,7	480			480			ns
t_{ELWL}	CE_X# Setup to WE# Going Low	3,7	0			0			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	60			60			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	60			60			ns
t_{WLWH}	WE# Pulse Width		60			60			ns
t_{WHDX}	Data Hold from WE# High	2	5			5			ns
t_{WHAX}	Address Hold from WE# High	2	5			5			ns
t_{WHEH}	CE_X# hold from WE# High	3,7	5			5			ns
t_{WHWL}	WE# Pulse Width High		15			15			ns
t_{GHWL}	Read Recovery before Write	3	0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low	3			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) data and RY/BY# High	3	0			0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low	3	480			480			ns
t_{WHCH}	Write Recovery before Read		20			20			ns
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			µs
t_{WHQV}1	Duration of Program Operation	3,4, 5,8	5	9	TBD	5	9	TBD	µs
t_{WHQV}2	Duration of Block Erase Operation	3,4	0.6	1.6	20	0.6	1.6	20	sec

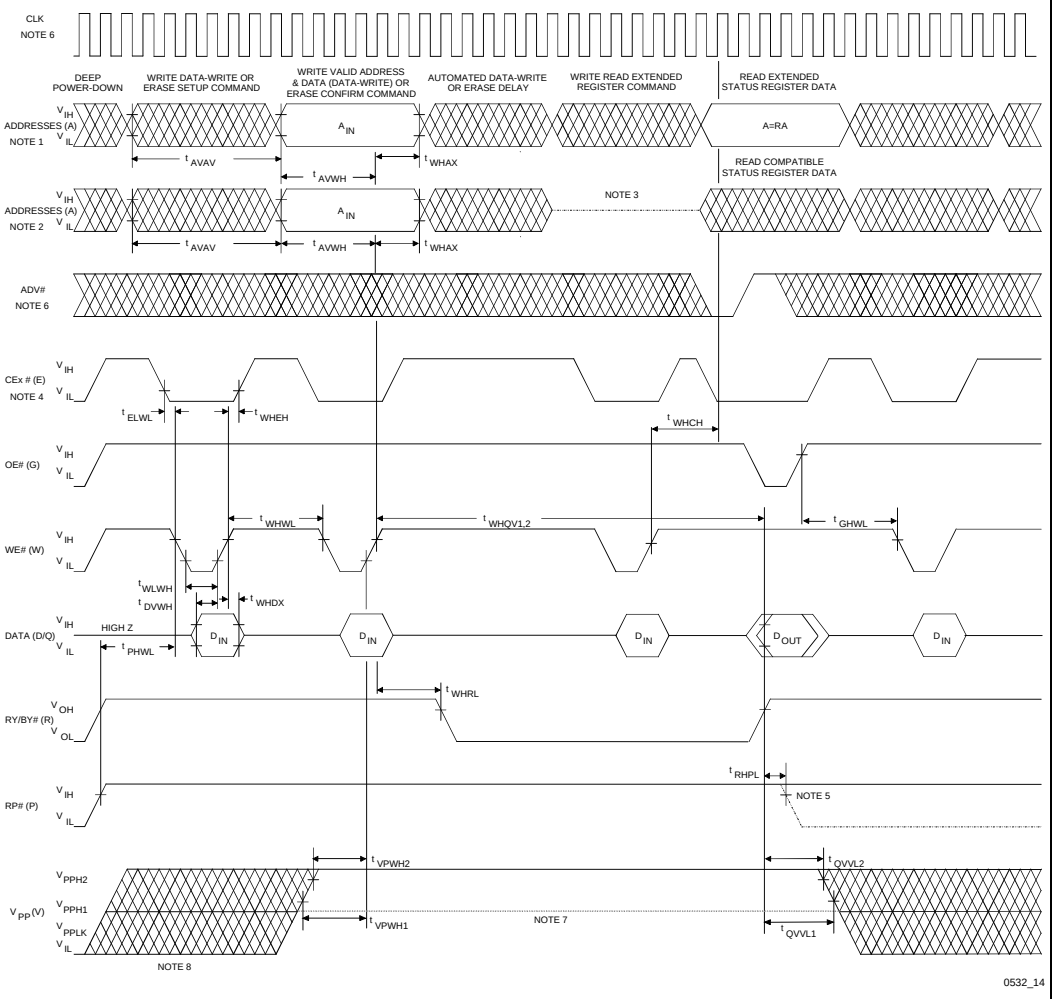
5.8 AC Characteristics for WE#—Controlled Write Operations(1) (Continued)

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C

Versions			28F016XS-15			28F016XS-20			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		65			65			ns
t_{VPWH}1,2	V_{PP} Setup to WE# Going High	3	100			100			ns
t_{PHEL}	RP# Setup to CE_X# Going Low	3,7	300			300			ns
t_{ELWL}	CE_X# Setup to WE# Going Low	3,7	0			0			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	50			50			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	50			50			ns
t_{WLWH}	WE# Pulse Width		50			50			ns
t_{WHDX}	Data Hold from WE# High	2	0			0			ns
t_{WHAX}	Address Hold from WE# High	2	5			5			ns
t_{WHEH}	CE_X# hold from WE# High	3,7	5			5			ns
t_{WHWL}	WE# Pulse Width High		15			15			ns
t_{GHWL}	Read Recovery before Write	3	0			0			ns
t_{WHRL}	WE# High to RY/BY# Going Low	3			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) data and RY/BY# High	3	0			0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low	3	300			300			ns
t_{WHCH}	Write Recovery before Read		20			20			ns
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			µs
t_{WHQV}1	Duration of Program Operation	3,4, 5,8	4.5	6	TBD	4.5	6	TBD	µs
t_{WHQV}2	Duration of Block Erase Operation	3,4	0.6	1.2	20	0.6	1.2	20	sec

NOTES:

1. Read timings during program and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested. Guaranteed by design.
4. Program/erase durations are measured to valid Status Register (CSR) Data.
5. Program operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all command program operations.
7. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Please contact Intel's Application Hotline or your local sales office for current TBD information.



NOTES:

1. This address string depicts data program/erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/erase operations.
4. CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above read and program cycles.
6. Data program/erase cycles are asynchronous; CLK and ADV# are ignored.
7. V_{PP} voltage during data program/erase operations valid at both 12.0V and 5.0V.
8. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 15. AC Waveforms for WE#—Command Write Operations, Illustrating a Two Command Write Sequence Followed by an Extended Status Register Read

5.9 AC Characteristics for CE_X#—Controlled Write Operations(1)

V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C

Versions			28F016XS-20			28F016XS-25			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		80			75			ns
t_{VPEH}1,2	V_{PP} Setup to CE_X# Going High	3,7	100			100			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480			480			ns
t_{WLEL}	WE# Setup to CE_X# Going Low	3,7	0			0			ns
t_{AVEH}	Address Setup to CE_X# Going High	2,6,7	60			60			ns
t_{DVEH}	Data Setup to CE_X# Going High	2,6,7	60			60			ns
t_{ELEH}	CE_X# Pulse Width	7	65			60			ns
t_{EHDX}	Data Hold from CE_X# High	2,7	10			10			ns
t_{EHAX}	Address Hold from CE_X# High	2,7	10			10			ns
t_{EHWH}	WE hold from CE_X# High	3,7	5			5			ns
t_{EHEL}	CE_X# Pulse Width High	7	15			15			ns
t_{GHEL}	Read Recovery before Write	3	0			0			ns
t_{EHRL}	CE_X# High to RY/BY# Going Low	3,7			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t_{PHEL}	RP# High Recovery to CE_X# Going Low	3,7	480			480			ns
t_{EHCH}	Write Recovery before Read		20			20			ns
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			µs
t_{EHQV}1	Duration of Program Operation	3,4,5,8	5	9	TBD	5	9	TBD	µs
t_{EHQV}2	Duration of Block Erase Operation	3,4	0.6	1.6	20	0.6	1.6	20	sec

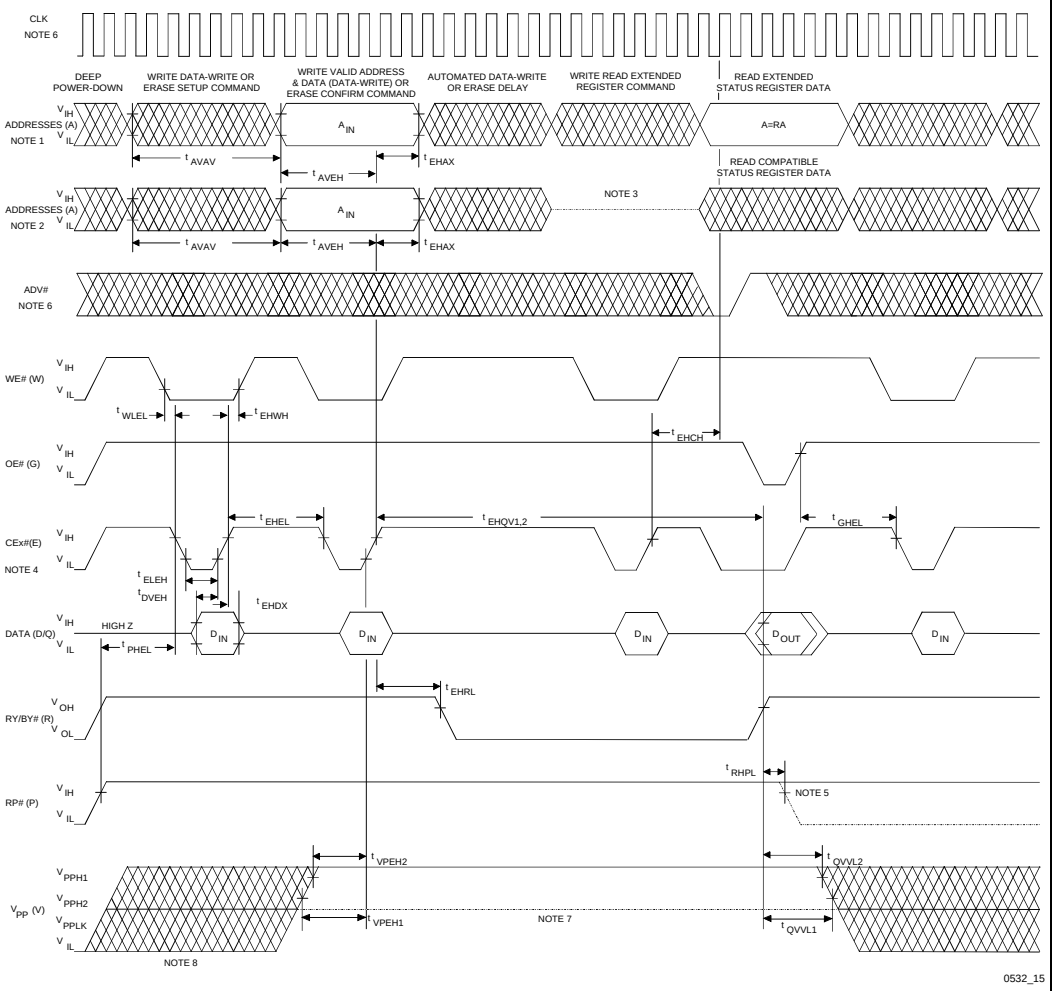
5.9 AC Characteristics for CE_X#—Controlled Write Operations(1) (Continued)

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C

Versions			28F016XS-15			28F016XS-20			
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{AVAV}	Write Cycle Time		60			60			ns
t_{VPEH}1,2	V_{PP} Setup to CE_X# Going High	3,7	100			100			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	300			300			ns
t_{WLEL}	WE# Setup to CE_X# Going Low	3,7	0			0			ns
t_{AVEH}	Address Setup to CE_X# Going High	2,6,7	45			45			ns
t_{DVEH}	Data Setup to CE_X# Going High	2,6,7	45			45			ns
t_{ELEH}	CE_X# Pulse Width	7	50			50			ns
t_{EHDX}	Data Hold from CE_X# High	2,7	0			0			ns
t_{EHAX}	Address Hold from CE_X# High	2,7	5			5			ns
t_{EHWH}	WE hold from CE_X# High	3,7	5			5			ns
t_{EHEL}	CE_X# Pulse Width High	7	15			15			ns
t_{GHEL}	Read Recovery before Write	3	0			0			ns
t_{EHRL}	CE_X# High to RY/BY# Going Low	3,7			100			100	ns
t_{RHPL}	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			ns
t_{PHEL}	RP# High Recovery to CE_X# Going Low	3,7	300			300			ns
t_{EHCH}	Write Recovery before Read		20			20			ns
t_{QVVL}1,2	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			0			µs
t_{EHQV}1	Duration of Program Operation	3,4,5,8	4.5	6	TBD	4.5	6	TBD	µs
t_{EHQV}2	Duration of Block Erase Operation	3,4	0.6	1.2	20	0.6	1.2	20	sec

NOTES:

1. Read timings during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested. Guaranteed by design.
4. Program/erase durations are measured to valid Status Register (CSR) Data.
5. Program operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all command write operations.
7. CE_X# is defined as the latter of CE_0# or CE_1# going low, or the first of CE_0# or CE_1# going high.
8. Please contact Intel's Application Hotline or your local sales office for current TBD information.

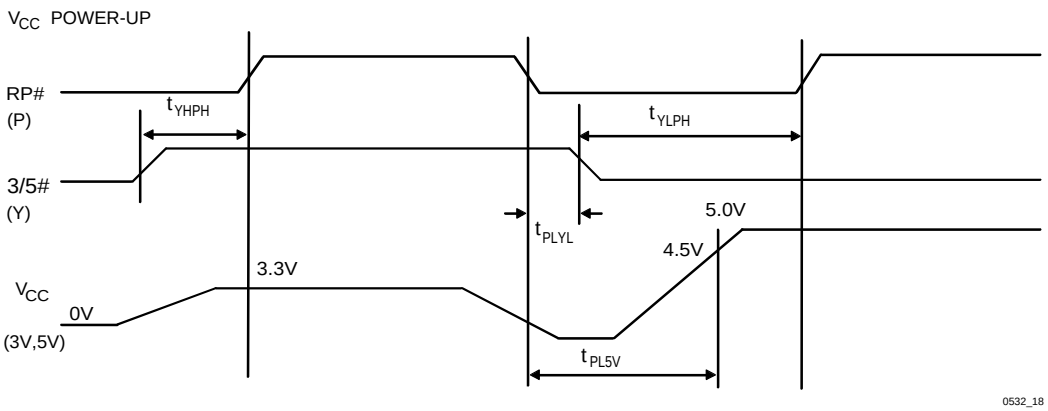


NOTES:

1. This address string depicts data program/erase cycles with corresponding verification via ESRD.
2. This address string depicts data program/erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during data program/erase operations.
4. CE_X# is defined as the latter of CE_0# or CE_1# going low or the first of CE_0# or CE_1# going high.
5. RP# low transition is only to show t_{RHPL}; not valid for above read and program cycles.
6. Data program/erase cycles are asynchronous; CLK and ADV# are ignored.
7. V_{PP} voltage during data program/erase operations valid at both 12.0V and 5.0V.
8. V_{PP} voltage equal to or below V_{PPLK} provides complete flash memory array protection.

Figure 16. AC Waveforms for CE_X#—Controlled Write Operations, Illustrating a Two Command Write Sequence Followed by an Extended Status Register Read

5.10 Power-Up and Reset Timings



NOTE:
For read timings following reset see Section 5.7.

Figure 17. V_{CC} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Notes	Min	Max	Unit
t_{PLYL} t_{PLYH}	RP# Low to 3/5# Low (High)		0		µs
t_{YLPH} t_{YHPH}	3/5# Low (High) to RP# High		0		µs
t_{PL5V} t_{PL3V}	RP# Low to V_{CC} at 4.5V (Minimum) RP# Low to V_{CC} at 3V (Min) or 3.6V (Max)	2	0		µs

NOTES:
1. The t_{YLPH} and/or t_{YHPH} times must be strictly followed to guarantee all other read and program specifications for the 28F016XS.
2. The power supply may start to switch concurrently with RP# going low.

5.11 Erase and Program Performance(3,4)

V_{CC} = 3.3V ± 5%, V_{PP} = 5.0V ± 5%, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1A$	Byte Program Time	2,5	TBD	29	TBD	µs	
$t_{WHRH}1B$	Word Program Time	2,5	TBD	35	TBD	µs	
$t_{WHRH}2$	Block Program Time	2,5	TBD	3.8	TBD	sec	Byte Program Mode
$t_{WHRH}3$	Block Program Time	2,5	TBD	2.4	TBD	sec	Word Program Mode
	Block Erase Time	2,5	TBD	2.8	TBD	sec	
	Erase Suspend Latency Time to Read		1.0	12	75	µs	

V_{CC} = 3.3V ± 5%, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Program Time	2,5	5	9	TBD	µs	
$t_{WHRH}2$	Block Program Time	2,5	TBD	1.2	4.2	sec	Byte Program Mode
$t_{WHRH}3$	Block Program Time	2,5	TBD	0.6	2.0	sec	Word Program Mode
	Block Erase Time	2	0.6	1.6	20	sec	
	Erase Suspend Latency Time to Read		1.0	9	55	µs	

5.11 Erase and Program Performance(3,4) (Continued)

V_{CC} = 5.0V ± 5%, V_{PP} = 5.0V ± 5%, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1A$	Byte Program Time	2,5	TBD	20	TBD	µs	
$t_{WHRH}1B$	Word Program Time	2,5	TBD	25	TBD	µs	
$t_{WHRH}2$	Block Program Time	2,5	TBD	2.8	TBD	sec	Byte Program Mode
$t_{WHRH}3$	Block Program Time	2,5	TBD	1.7	TBD	sec	Word Program Mode
	Block Erase Time	2,5	TBD	2.0	TBD	sec	
	Erase Suspend Latency Time to Read		1.0	9	55	µs	

V_{CC} = 5.0V ± 5%, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Program Time	2,5	4.5	6	TBD	µs	
$t_{WHRH}2$	Block Program Time	2,5	TBD	0.8	4.2	sec	Byte Program Mode
$t_{WHRH}3$	Block Program Time	2,5	TBD	0.4	2.0	sec	Word Program Mode
	Block Erase Time	2	0.6	1.2	20	sec	
	Erase Suspend Latency Time to Read		1.0	7	40	µs	

NOTES:

1. +25°C, and nominal voltages.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled, but not 100% tested. Guaranteed by design.
5. Please contact Intel's Application Hotline or your local sales office for current TBD information.

6.0 MECHANICAL SPECIFICATIONS

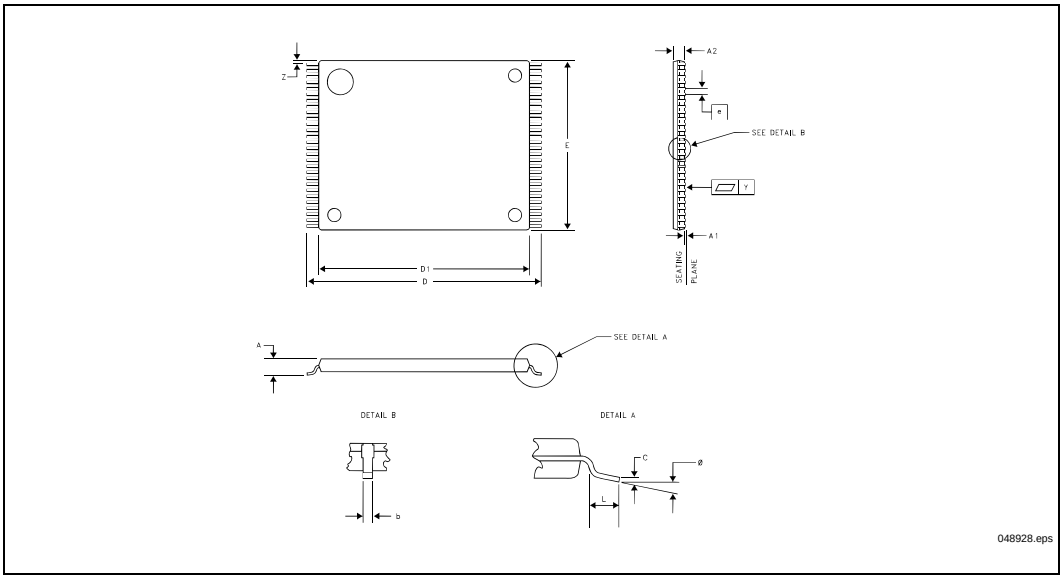


Figure 18. Mechanical Specifications of the 28F016XS 56-Lead TSOP Type I Package

Family: Thin Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A			1.20	
A_1	0.050			
A_2	0.965	0.995	1.025	
b	0.100	0.150	0.200	
c	0.115	0.125	0.135	
D_1	18.20	18.40	18.60	
E	13.80	14.00	14.20	
e		0.50		
D	19.80	20.00	20.20	
L	0.500	0.600	0.700	
N		56		
∅	0°	3°	5°	
Y			0.100	
Z	0.150	0.250	0.350	

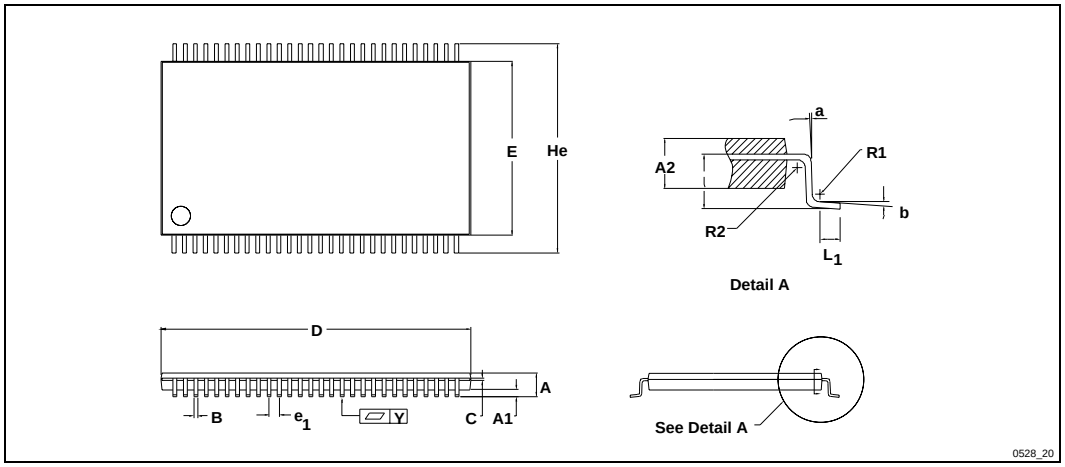
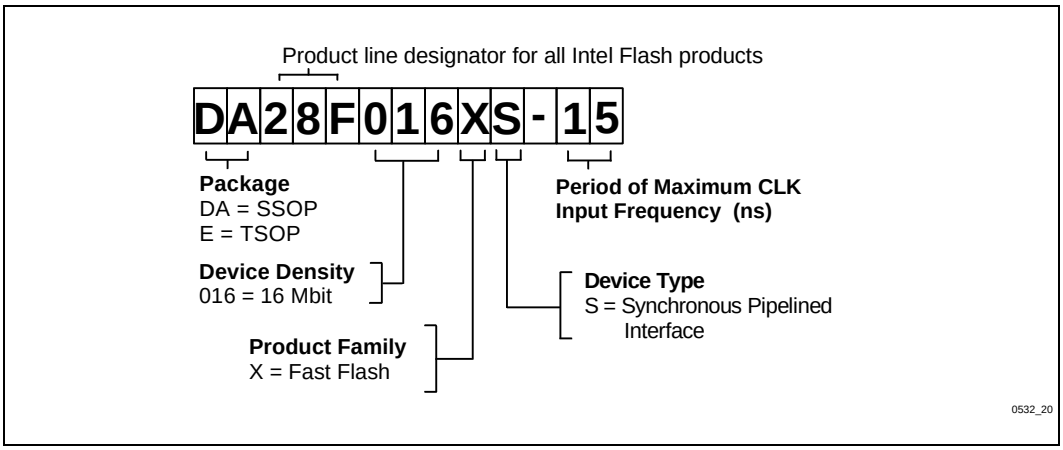


Figure 19. Mechanical Specifications of the 28F016SV 56-Lead SSOP Type I Package

Family: Shrink Small Out-Line Package				
Symbol	**Millimeters**			**Notes**
	Minimum	**Nominal**	**Maximum**	
A		1.80	1.90	
A1	0.47	0.52	0.57	
A2	1.18	1.28	1.38	
B	0.25	0.30	0.40	
C	0.13	0.15	0.20	
D	23.40	23.70	24.00	
E	13.10	13.30	13.50	
e_1		0.80		
He	15.70	16.00	16.30	
N		56		
L_1	0.45	0.50	0.55	
Y			0.10	
a	2°	3°	4°	
b	3°	4°	5°	
R1	0.15	0.20	0.25	
R2	0.15	0.20	0.25	

APPENDIX A
DEVICE NOMENCLATURE AND ORDERING INFORMATION



Option	Order Code	Valid Combinations		
		V_{CC} = 3.3V ± 5%, 50 pF load, 1.5V I/O Levels(1)	V_{CC} = 5.0V ± 5%, 100 pF load TTL I/O Levels(1)	V_{CC} = 5.0V ± 5%, 30 pF load 1.5V I/O Levels(1)
1	E28F016XS15	28F016XS-20		28F016XS-15
2	E28F016XS20	28F016XS-25	28F016XS-20	
3	DA28F016XS15	28F016XS-20		28F016XS-15
4	DA28F016XS20	28F016XS-25	28F016XS-20	

NOTE:

1. See Section 5.3 for Transient Input/Output Reference Waveforms.

APPENDIX B
ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
297372	*16-Mbit Flash Product Family User's Manual*
292147	*AP-398 Designing with the 28F016XS*
292146	*AP-600 Performance Benefits and Power/Energy Savings of 28F016XS-Based System Designs*
292163	*AP-610 Flash Memory In-System Code and Data Update Techniques*
292165	*AB-62 Compiled Code Optimizations for Flash Memories*
297500	*Interfacing the 28F016XS to the i960® Microprocessor Family*
297504	*Interfacing the 28F016XS to the Intel486™ Microprocessor Family*
294016	*ER-33 ETOX™ Flash Memory Technology—Insight to Intel's Fourth Generation Process Innovation*
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XS Benchmark Utility
Contact Intel/Distribution Sales Office	Flash Cycling Utility
Contact Intel/Distribution Sales Office	28F016XS iBIS Model
Contact Intel/Distribution Sales Office	28F016XS VHDL Model
Contact Intel/Distribution Sales Office	28F016XS TimingDesigner* Library Files
Contact Intel/Distribution Sales Office	28F016XS Orcad/Viewlogic Schematic Symbols

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.