NEC

MOS INTEGRATED CIRCUIT

μPD42280

2 M-BIT FIELD BUFFER

The μPD42280 is a high-speed field buffer equipped with a memory of 256K words × 8bit (262, 224 × 8bit) configuration. The high-speed and the low power consumption are realized in CMOS dynamic circuit.

The μPD42280 consists of FIFO (First In First Out) configuration, and the write/read operations are possible asynchronously and simultaneously.

Because it has refresh circuit internally, 1 field delay line and time axis conversion etc. are realized easily. Therefore it is suitable for YC separation between frames, interpolation between fields, reproduction of freeze picture and frame synchronizer in the digital TV, VCR systems.

FEATURES

- 256K words × 8 bit FIFO configuration
- Write/read operations are possible asynchronously and simultaneously
- Reset is possible apart from write/read address (real time reset)
- Serial read cycle time : 30 ns/60 ns (MIN.)
- Serial read access time : 25 ns/40 ns (MAX.)
- Serial write cycle time : 30 ns/60 ns (MIN.)
- Self refresh function incorporated
- Output enable
- All I/O TTL compatible
- CMOS low power consumption : (t_{RCK}, t_{WCK} = 30 ns) I_{CC} = 50 mA (TYP.)
- 28-pin plastic SOP (450 mil) μPD42280GU
- 28-pin plastic ZIP (400 mil) μPD42280V

ORDERING INFORMATION

Part number	Package	Read cycle time (ns)	Access time (ns)	Write cycle time (ns)
μPD42280GU-30	28-pin plastic SOP (450 mil)	30	25	30
μPD42280GU-60	28-pin plastic SOP (450 mil)	60	40	60
μPD42280V-30	28-pin plastic ZIP (400 mil)	30	25	30
μPD42280V-60	28-pin plastic ZIP (400 mil)	60	40	60

The information in this document is subject to change without notice.

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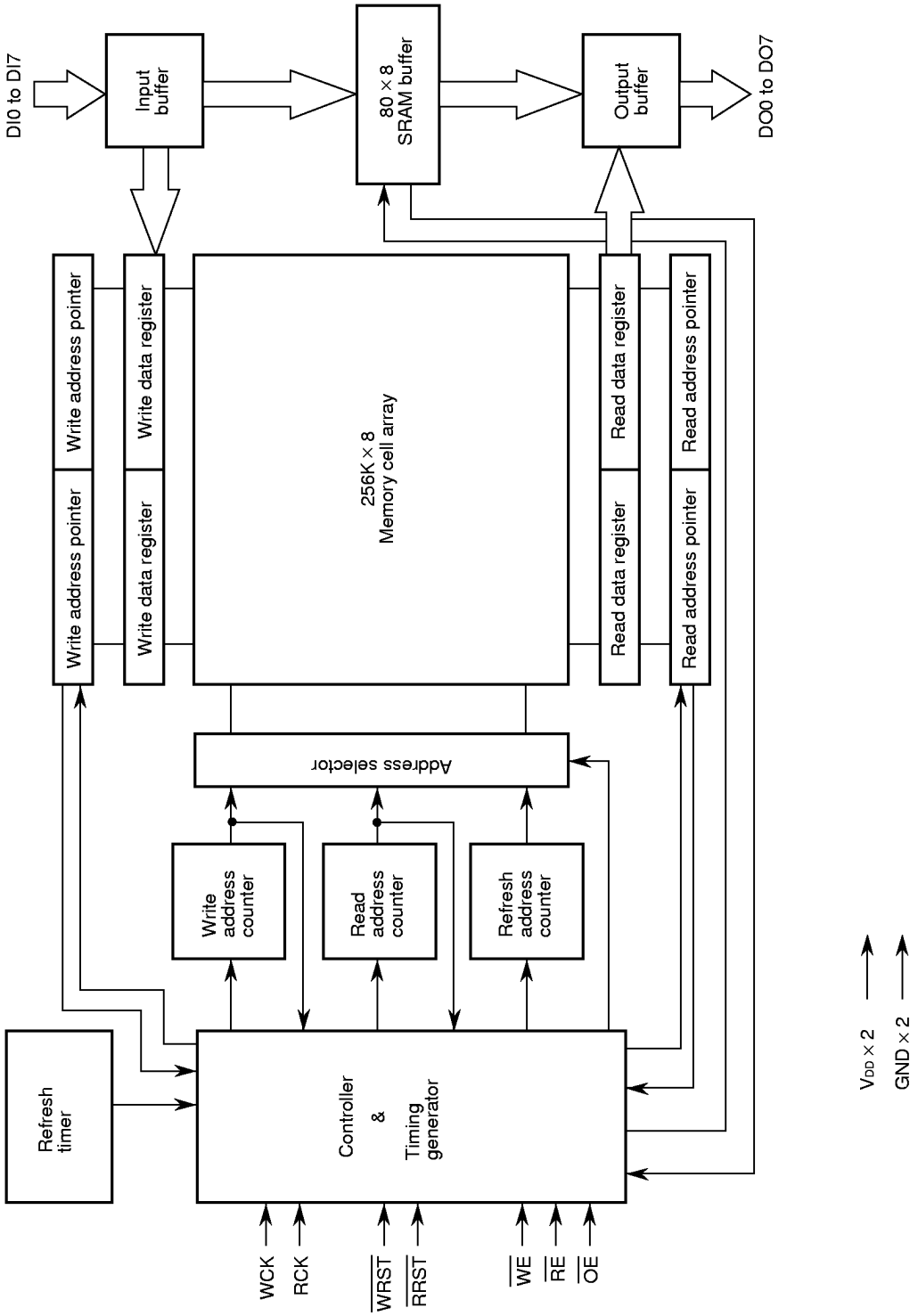
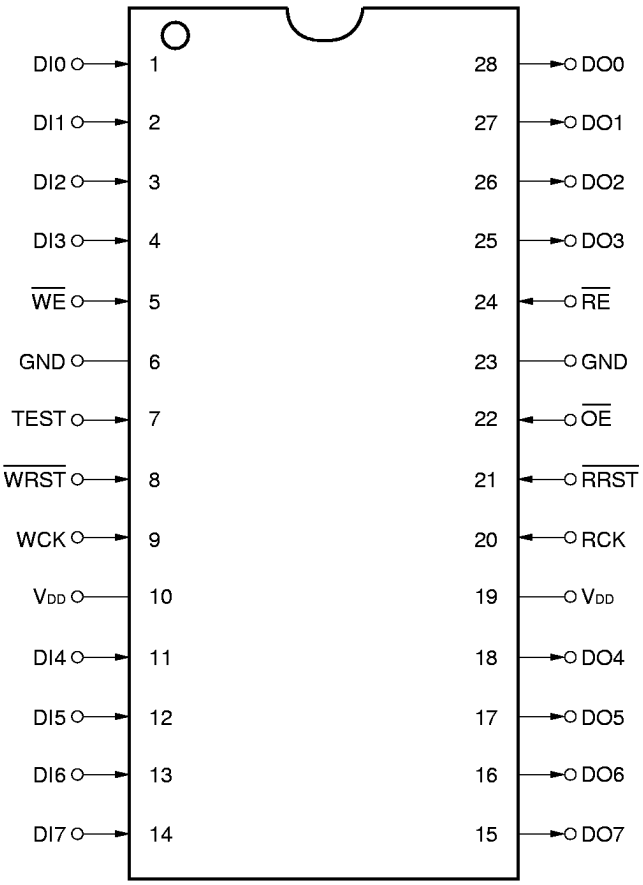
The mark ★ shows major reviced points.

BLOCK DIAGRAM

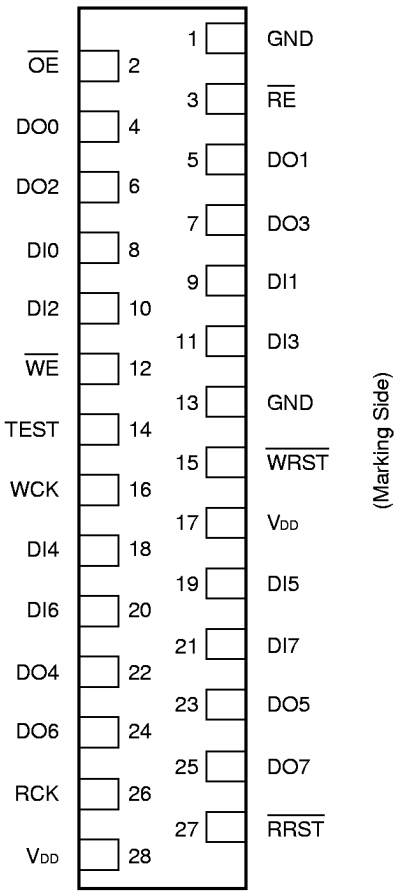


PIN CONFIGURATION

28-pin plastic SOP (450 mil)
(Top View)
μPD42280GU-xx



28-pin plastic ZIP (400 mil)
(Bottom View)
μPD42280V-xx



Pin name

DI0 to DI7	:	Data input
DO0 to DO7	:	Data output
WCK	:	Write clock input
RCK	:	Read clock input
$\overline{WE}$	:	Write enable input
$\overline{RE}$	:	Read enable input
$\overline{OE}$	:	Output enable input
$\overline{WRST}$	:	Write reset input
$\overline{RRST}$	:	Read reset inputt
TEST	:	Test pin
V_{DD}	:	+5 V power source
GND	:	Ground

1. PIN FUNCTION

Pin name	Input/Output	Function
DI0 to DI7	I	This is a write data input. Fetching data is executed on the back rise up edge of WCK input cycle, and the setup/hold time (t_{DS}, t_{DH}) are specified against the edge.
DO0 to DO7	O (3-state)	This is a read data output. The access time is specified from the front rise up edge of RCK cycle and determined by t_{AC}. It is 3 state output.
$\overline{WRST}$	I	This is a reset input for initializing a write address. Fetching reset signals is executed on the front rise up edge of WCK input cycle, and the setup/hold time (t_{RS}, t_{RH}) are specified against the edge.
$\overline{RRST}$	I	This is a reset input for initializing a read address. Fetching reset signals is executed on the front rise up edge of RCK input cycle, and the setup/hold time (t_{RS}, t_{RH}) are specified against the edge.
$\overline{WE}$	I	This is a write operation control input. In case of high level, the internal write operation is prohibited, and the write address pointer is also stopped at the present position. $\overline{WE}$ signal is fetched on the front rise up edge of WCK input cycle.
$\overline{RE}$	I	This is a read operation control input. In case of high level, the internal read operation is executed, and the read address pointer is stopped at the present position. $\overline{RE}$ signal is fetched on the front rise up edge of RCK input cycle.
$\overline{OE}$	I	This is a read data control input. In case of high-level, DO0 to DO7 will be high impedance. In the read address pointer an increment is executed synchronously for RCK, not depending on the $\overline{OE}$ signal input level. $\overline{OE}$ signal is fetched on the front rise up edge of RCK input cycle.
WCK	I	This is a write clock input. The write operation is executed synchronously for the write clock when $\overline{WE}$ is in low level, and in the write address pointer, the increment is executed at the same time.
RCK	I	This is a read clock input. The read operation is done synchronously for the read clock, and when $\overline{RE}$ is in low level, in the read address pointer the increment is executed at the same time.
TEST	I	This is a pin for testing. It is to be fixed on low level on the practical operation.

2. EXPLANATION FOR THE MEMORY AND FUNCTION BLOCK

2.1 Memory Cell Array

This is a memory cell array in this product consisting of dynamic memory cells, with 256K × 8 (2M bit) configuration.

2.2 Input Buffer

This is a buffer to input the signals of DI0 to DI7 to the write data register or SRAM buffer.

2.3 Output Buffer

This is a buffer to output the data from the read data register or SRAM buffer to DO0 to DI7.

2.4 Write Data Register/Write Address Pointer

This is a register to temporarily store the data input to DI0 to DI7. The input data is stored in the address directed by the write address pointer. In the write address pointer, its content increases every WCK input. When the write data register is filled with data, the data are transferred to the memory cell array together, and the write address pointer is reset to the 0 address. The data are transferred by 64 words unit.

2.5 Read Data Register/Read Address Pointer

This is a register to temporarily store the data transferred together from the memory cell array. The data in the register directed by the read address pointer is output to DO0 to DO7. In the read address pointer, its content increases every RCK input. When the read data register is emptied, the data read from the memory cell array is transferred together to the register, and the read address pointer is reset to the 0 address. The data are transferred by 64 words unit.

2.6 SRAM Buffer

This is a buffer to store the data for 80 words after the write address is reset by $\overline{\text{WRST}}$. Also, when a read address is reset by the input of $\overline{\text{RRST}}$ signals, the data for 80 words after the reset is output (to DO0 to DO7) from SRAM buffer.

2.7 Write Address Counter

This is a counter to direct the row address of the write data. When the data is transferred to memory cell array from the write data register, the content of the counter increases. When input of the last address is attained, the content of the counter is reset to the 0 address.

2.8 Read Address Counter

This is a counter to direct the row address of the read data. When the data is transferred to the read data register from memory cell array, the content of the counter increases. When input of $\overline{\text{RRST}}$ signals or the last address is attained, the content of the counter is reset to the 0 address.

2.9 Refresh Address Counter/Refresh Timer

This is a counter to direct the refresh address. Its content is increased one by one by the refresh timer. Because self refresh function is incorporated, the refresh operation is executed automatically.

2.10 Address Selector

This is a selector which selects one of the addresses directed by the address counter, read address counter and refresh address counter as the row address of memory cell array.

2.11 Controller/Timing Generator

Each block is controlled by the control signals from the input pins of this block.

3. MEMORY OPERATION

3.1 Write Operation

When $\overline{WE}$ input is in low level, the data input to DI0 to DI7 is written into the write data register every 8 bits together synchronizing with WCK input.

The write data should be input to meet the setup time and the hold time for the back rise up edge of WCK input cycle.

When $\overline{WE}$ input is attained to a high level, the write operation is prohibited. The write address pointer is stopped at the position of high level input state. When the low level is input again, the operation is started from the stopped address.

Though the write operation is prohibited at any time, $\overline{WE}$ signal should be input to meet the set up time and the hold time for the rise up edge of WCK.

3.2 Read Operation

When $\overline{RE}$ input and $\overline{OE}$ input are in low level, the data is output to DO0 to DO7 from the read data register every 8 bits together synchronizing with RCK input.

The read data is output after access time (t_{AC}) from the rise up edge of RCK input cycle.

When $\overline{RE}$ input is attained to a high level, the read address pointer is stopped at the position of the high level input state. When inputting a low level again, the operation is started from the stopped address.

When $\overline{OE}$ input is attained to a high level, the output will be a high impedance. The content of the read address pointer increases synchronously with RCK input, not depending on the input level of $\overline{OE}$ signal.

Though the read operation can be prohibited at any time, $\overline{RE}$ signal/$\overline{OE}$ signal should be input to meet the setup time and hold time for the rise up edge of RCK.

When the new data is read, the write address should be preceded 200 to 262, 223 or less cycles than the read address.

When the old data is read, the difference between the write address and the read address should be 0 cycle (the read address and the write address are the same).

When the read address and the write address compete with each other by double speed conversion etc. in the same field, in the data of the last 192 words the old data (the data prior to 1 field) may be output.

3.3 Reset Operation

The reset signal can be input any time, without depending on $\overline{WE}$, $\overline{RE}$ and $\overline{OE}$ signals. $\overline{WRST}$ and $\overline{RRST}$ signals should be input to meet the setup time and the hold time for the rise up edge of WCK, RCK inputs. When the reset signal is input in disable cycles, the reset operation is executed after the disable cycles.

The output and input of data are possible from the cycle (0 address) where low level is input to $\overline{WRST}$, $\overline{RRST}$.

3.4 Initialize

Following initializing should be taken when the power supply is ON.

(1) Stand-by period should be taken more than 100 μs.

(2) $\overline{WRST}$ and $\overline{RRST}$ signals should be input for initializing of the write address and read address.

(3) More than 82 dummy cycles should be taken where low level is input to $\overline{RE}$ and $\overline{WE}$.

(4) Ordinary operation is executed after next low level is input to $\overline{WRST}$ and $\overline{RRST}$.

Remark New data : Data written latest,
Old data : Stored data just before write operation

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

Parameter	Symbol	Conditions	Ratings	Unit
Operational Power Supply	V_{DD}		–1.0 to +7.0	V
Pin Voltage	V_T		–1.0 to V_{DD} +0.5 (7.0 V or less)	V
Output Current	I_O		±20	mA
Operating Ambient Temperature	T_A		–20 to +70	°C
Storage Temperature	T_{stg}		–55 to +125	°C

Caution Exposure to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

Recommended Operation Range

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage 1	V_{DD}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{DD} + 0.5	V
Low Level Input Voltage	V_{IL}		–1.0		+0.8	V
Operating Ambient Temperature	T_A		–20		+70	°C

DC Characteristics (Recomended Operation Range unless otherwise noted)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating Current 1	I_{CC1}	t_{WCK}, t_{RCK} = 30 ns		50	90	mA
Operating Current 2	I_{CC2}	t_{WCK}, t_{RCK} = 60 ns		33	60	mA
Standby Current	I_{CCS}	WCK, RCK = 'L' (TTL input)		4	10	mA
Input Leak Current	I_I	V_I = 0 to V_{DD} Other input: 0 V	–10		+10	μA
Output Leak Current	I_O	V_O = 0 to V_{DD} Do: High impedance	–10		+10	μA
High Level Output Voltage	V_{OH}	I_{OH} = –1 mA	2.4			V
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA			0.4	V

Input/Output Capacitance (T_A = +25 °C, f = 1 MHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I				5	pF
Output Capacitance	C_O				7	pF

AC Characteristics (Recommended Operating Range unless otherwise noted) Note 1, 2, 3, 5

Parameter	Symbol	μPD42280-30		μPD42280-60		Unit
		MIN.	MAX.	MIN.	MAX.	
Write Clock (WCK) Cycle Time	t_{WCK}	30		60		ns
Write Clock Active Time	t_{WCW}	12		20		ns
Write Clock Precharge Period	t_{WCP}	12		20		ns
Read Clock (RCK) Cycle Time	t_{RCK}	30		60		ns
Read Clock Active Time	t_{RCW}	12		20		ns
Read Clock Precharge Period	t_{RCP}	12		20		ns
Access Time	t_{AC}		25		40	ns
Output Hold Time	t_{OH}	5		5		ns
Output Low Impedance Time from RCK Rise Note 4	t_{LZ}	5	25	5	40	ns
Output High Impedance Time from RCK Rise Note 4	t_{HZ}	5	25	5	40	ns
Input Data, Setup Time	t_{DS}	7		12		ns
Input Data, Hold Time	t_{DH}	3		3		ns
Reset Setup Time from WCK or RCK Rise Note 6	t_{RS}	7		12		ns
Reset Hold Time from WCK or RCK Rise Note 6	t_{RH}	3		3		ns
Reset Non Selection Time 1 from WCK or RCK Rise Note 7	t_{RN1}	3		3		ns
Reset Non Selection Time 2 from WCK or RCK Rise Note 7	t_{RN2}	7		12		ns
$\overline{WE}$ Setup Time from WCK Rise Note 8	t_{WES}	7		12		ns
$\overline{WE}$ Hold Time from WCK Rise Note 8	t_{WEH}	3		3		ns
$\overline{WE}$ Non Selection Time 1 from WCK Rise Note 9	t_{WEN1}	3		3		ns
$\overline{WE}$ Non Selection Time 2 from WCK Rise Note 9	t_{WEN2}	7		12		ns
$\overline{RE}$ Setup Time from RCK Rise Note 8	t_{RES}	7		12		ns
$\overline{RE}$ Hold Time from RCK Rise Note 8	t_{REH}	3		3		ns
$\overline{RE}$ Non Selection Time 1 from RCK Rise Note 9	t_{REN1}	3		3		ns
$\overline{RE}$ Non Selection Time 2 from RCK Rise Note 9	t_{REN2}	7		12		ns
$\overline{OE}$ Setup Time from RCK Rise Note 10	t_{OES}	7		12		ns
$\overline{OE}$ Hold Time from RCK Rise Note 10	t_{OEH}	3		3		ns
$\overline{OE}$ Non Selection Time 1 from RCK Rise Note 11	t_{OEN1}	3		3		ns
$\overline{OE}$ Non Selection Time 2 from RCK Rise Note 11	t_{OEN2}	7		12		ns

Parameter	Symbol	μPD42280-30		μPD42280-60		Unit
		MIN.	MAX.	MIN.	MAX.	
$\overline{WE}$ High Level Period	t_{WEW}	0		0		ns
$\overline{RE}$ High Level Period	t_{REW}	0		0		ns
$\overline{OE}$ High Level Period	t_{OEW}	0		0		ns
$\overline{WRST}$ Low Level Period (Write Reset Period)	t_{WRST}	0		0		ns
$\overline{RRST}$ Low Level Period (Read Reset Period)	t_{RRST}	0		0		ns
Rise Up, Fall Down Time	t_T	3	35	3	35	ns

Notes

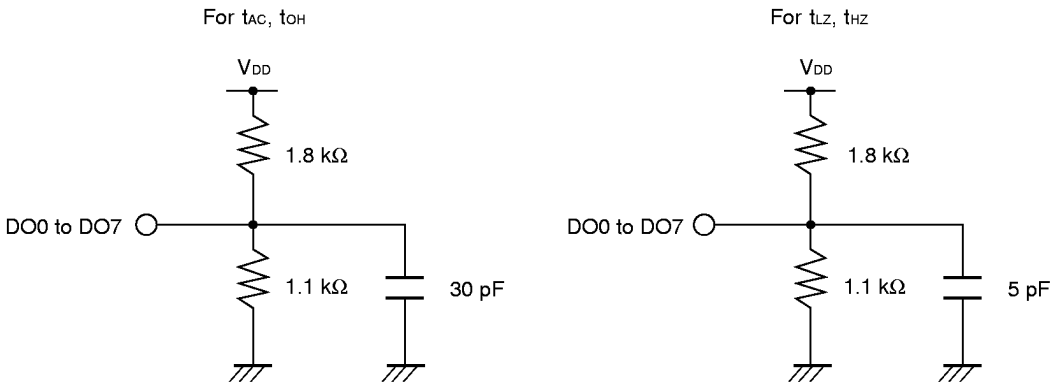
1. All voltages are determined by referring to the ground level.
2. Measurement by t_T = 5 ns.
3. Input voltage standard levels in the timing specification are V_{IH} = 2.4 V and V_{IL} = 0.4 V. Transferring time t_T is determined between V_{IH} = 2.4 V and V_{IL} = 0.4 V.
4. t_{LZ}, t_{HZ} are measured by ±200 mV from a stationary state. And t_{LZ} is equal to, or more than t_{HZ}.
5. The reference level of input signals is 1.5 V.
6. When the reset pulse which does not meet t_{RS}, t_{RH} is input, the reset operation is not assured.
7. When the reset pulse which does not meet t_{RN1}, t_{RN2} is input, the reset operation may effect the cycles before and after.
8. When $\overline{WE}$ ($\overline{RE}$) pulse which does not meet t_{WES}, t_{WEH} (or t_{RES}, t_{REH}) is input, the write (read) disable operation is not assured.
9. When $\overline{WE}$ ($\overline{RE}$) pulse which does not meet t_{WEN1}, t_{WEN2} (or t_{REN1}, t_{REN2}) is input, the write (read) disable operation may effect the cycles before and after.
10. When $\overline{OE}$ pulse which does not meet t_{OES}, t_{OEH} is input, the output disable operation is not assured.
11. When $\overline{OE}$ pulse which does not meet t_{OEN1}, t_{OEN2} is input, the output disable operation may effect the cycles before and after.

AC Characteristics Measurement Condition

Input timing specification

Output timing specification

DO external load



★ Restrictions

The μPD42280 has the following restrictions. When using the μPD42280, be very careful to observe these restrictions.

(1) To read new data, the write address must precede the read address by 200 cycles or more and less than 262,224 cycles. To read old data, there must be 0 cycle difference between the write address and the read address.

(2) The μPD42280 performs data transfer between the data registers and memory cell array in 64-word units. Therefore, when a low-level $\overline{WRST}$ signal is input to an address n higher than address 80, the old data of addresses higher than address n and up to address m indicated in the formula below is not guaranteed.

$$m = 143 + \text{int}\left[\frac{n - 80}{64}\right] \times 64$$

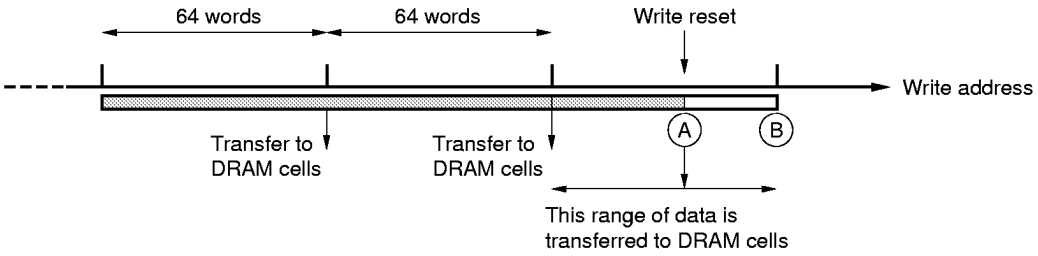
Remark $\text{int}\left[\frac{n - 80}{64}\right]$: Indicates only the integral part of the result of n – 80 divided by 64.

Example: If n = 280 → 3

Therefore, m = 335 and old data from address 280 to address 335 is not guaranteed.

This restriction applies to internal operation during write reset. When write reset is executed by inputting a low level to $\overline{WRST}$, the contents of the write data register at that moment are transferred to DRAM cells. Figure 4 -1 shows the data transmission from the write data register to DRAM chronologically. Data transfer from the write data register to DRAM is performed in units of 64 words.

Figure 4-1 Data Transfer During Write Reset



In Figure 4-1, when write reset is applied at point A, the data after point A up to point B is also transferred to DRAM. In other words, the old data stored in the transfer destination of this portion of data is overwritten by this portion of data.

(3) After write is started by inputting a low-level $\overline{WRST}$ signal, input the next low-level $\overline{WRST}$ signal 82 or more addresses apart.

Although this is highly improbable in actual practice, if no reset is executed but the operation transits from address 262,223 to address 0, this will be interpreted as a reset.

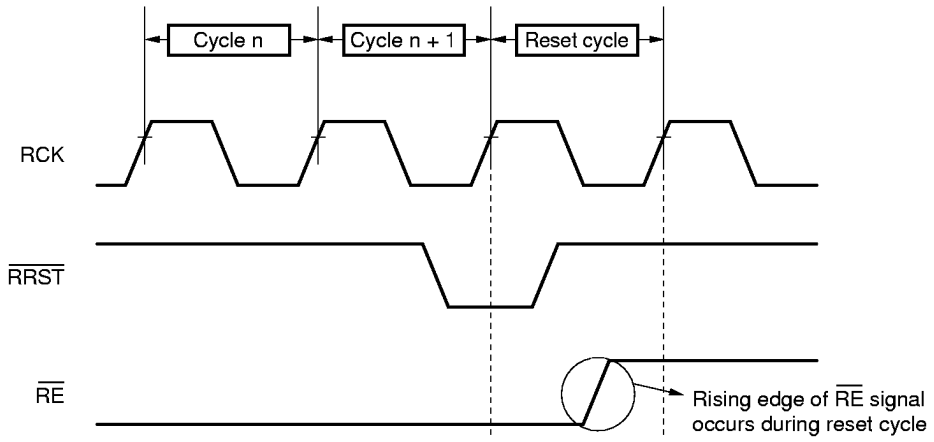
(4) After read is started by inputting a low-level $\overline{RRST}$ signal, input the next low-level $\overline{RRST}$ signal 82 or more addresses apart.

At the same time as (3) above, if no reset is executed but the operation transits from address 262,223 to address 0, this will be interpreted as a reset.

(5) Do not raise the $\overline{RE}$ signal from low level to high level at address 0 or during a reset cycle.

This is a restriction particular to internal device operation. Be sure not to perform the operation described in Figure 4-2.

Figure 4-2 Violation of Restriction (5)

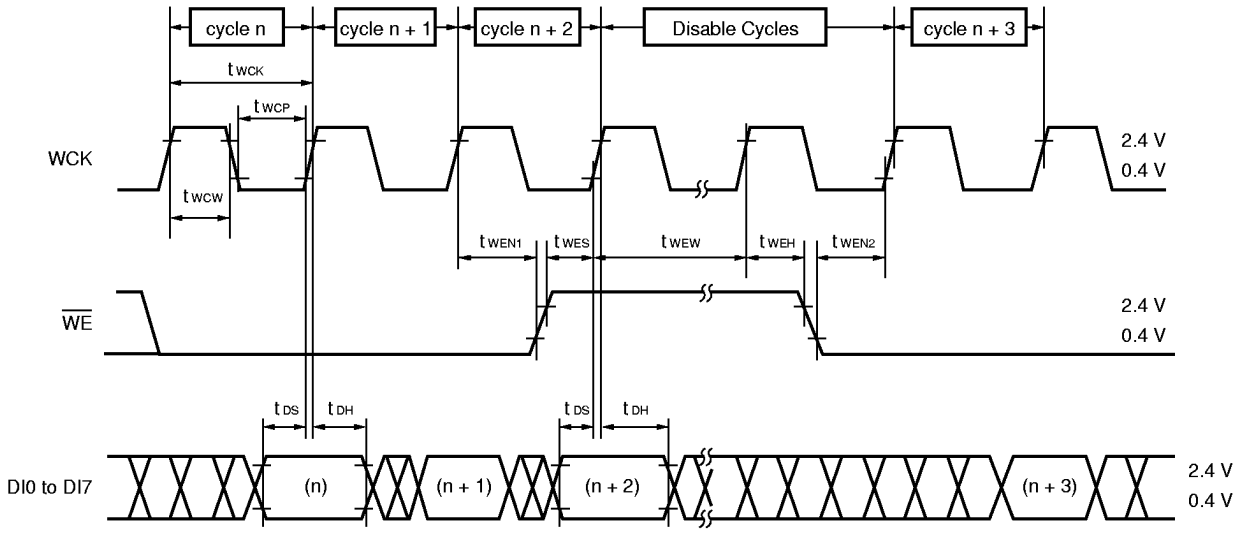


Thus it can be seen that due to restriction (5), it is not possible to use $\overline{RE}$ to stop the read address at address 0 using $\overline{RE}$.

To stop the read address at address 0, continue inputting low levels to $\overline{RRST}$. However, in this case, the data of address 0 is newly output each time RCK is input. Therefore, when new data is written to address 0 on the write side, and the written data becomes readable, new data is read.

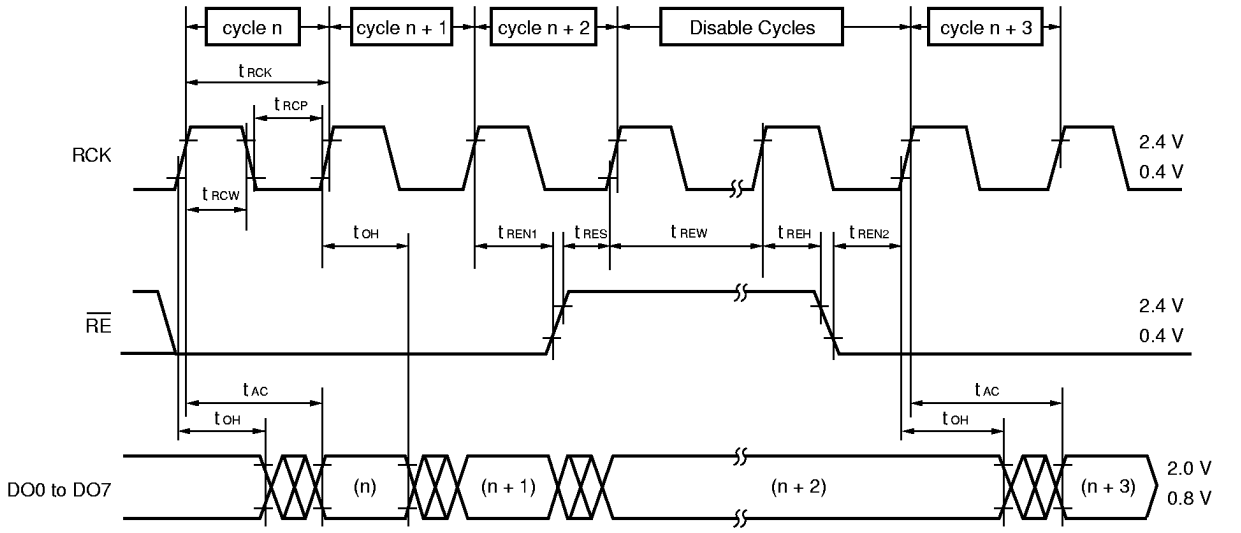
Timing Diagram

Write cycle ($\overline{WE}$ control)



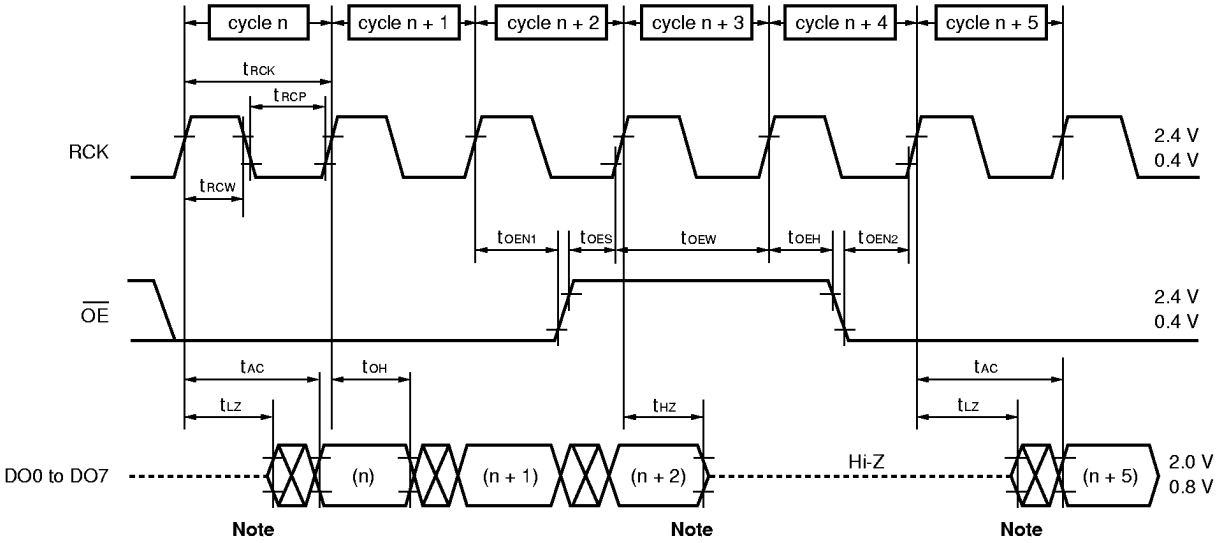
Remark $\overline{WRST}$ = "H" level

Read cycle ($\overline{RE}$ control)



Remark $\overline{RRST}$ = "H" level, $\overline{OE}$ = "L" level

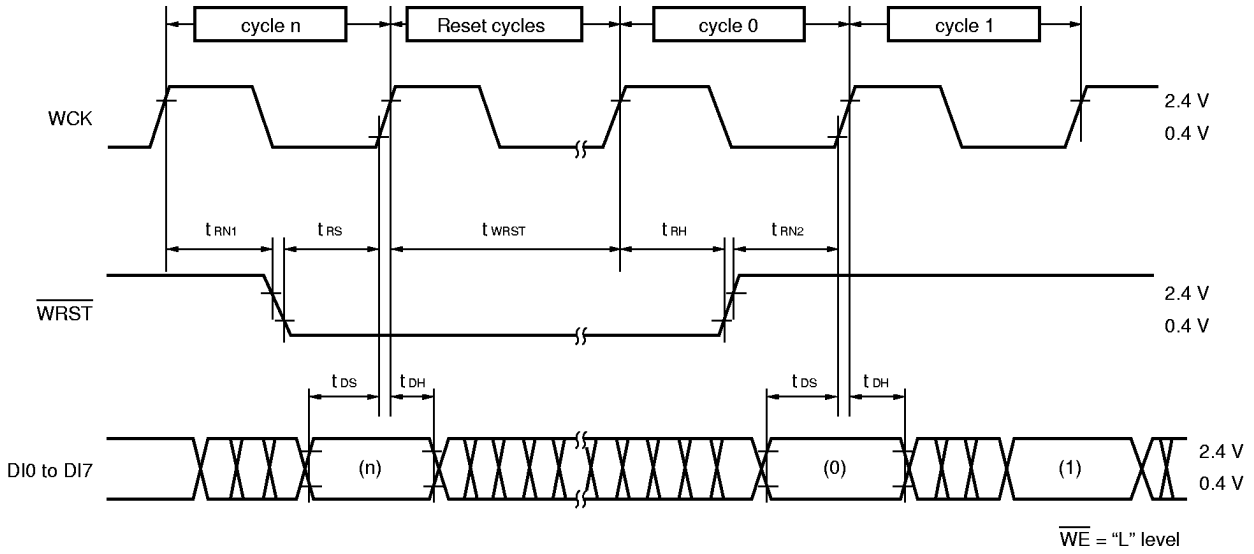
Read cycle ($\overline{OE}$ control)



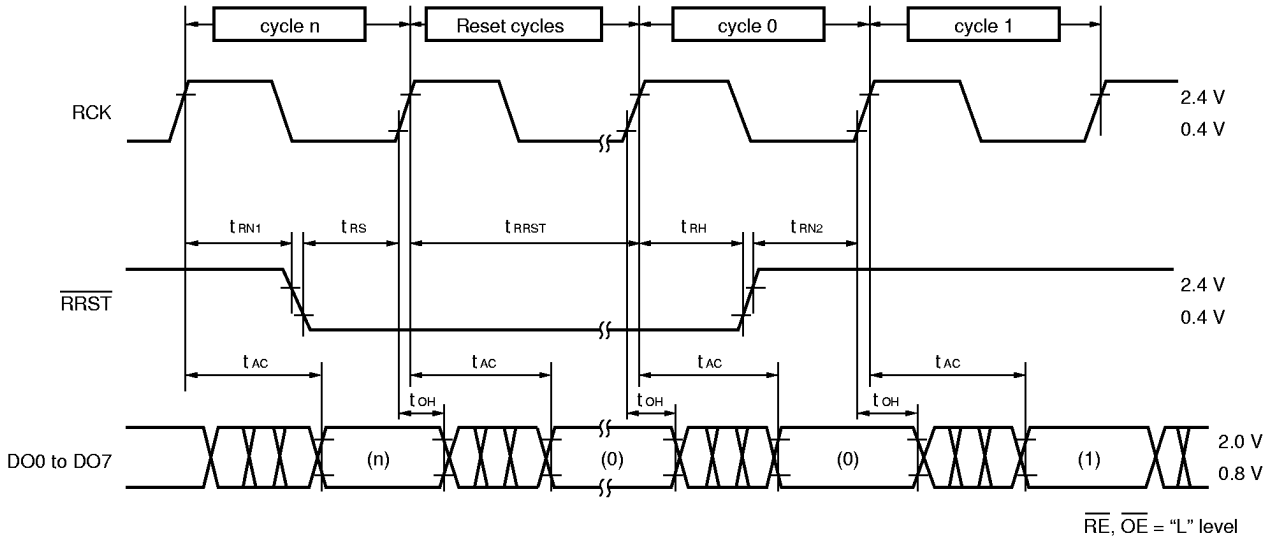
Note t_{LZ} and t_{HZ} are measured in ±200 mV point from the steady state of DO.

Remark $\overline{RRST}$ = "H" level, $\overline{RE}$ = "L" level

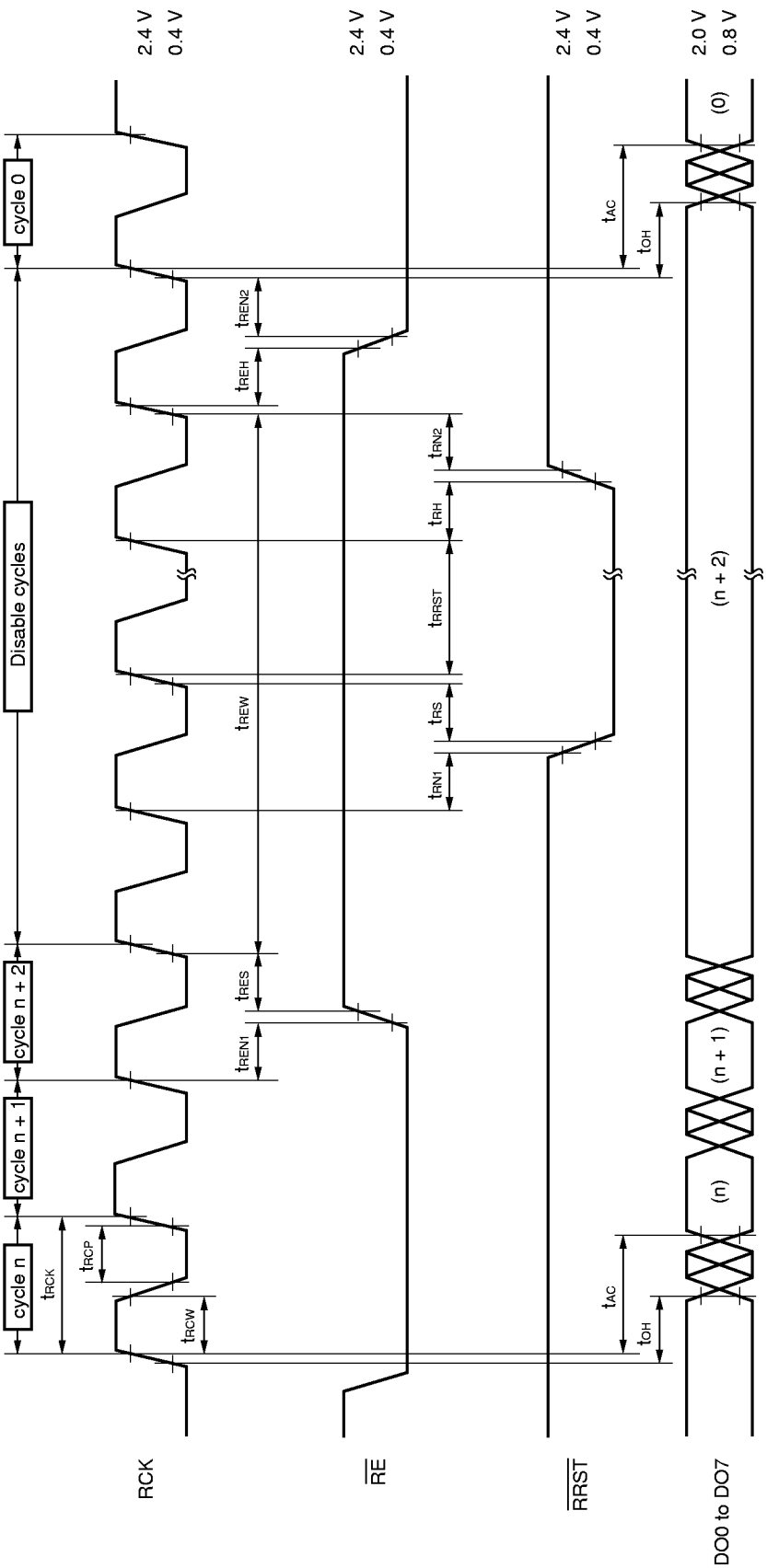
Write reset cycle



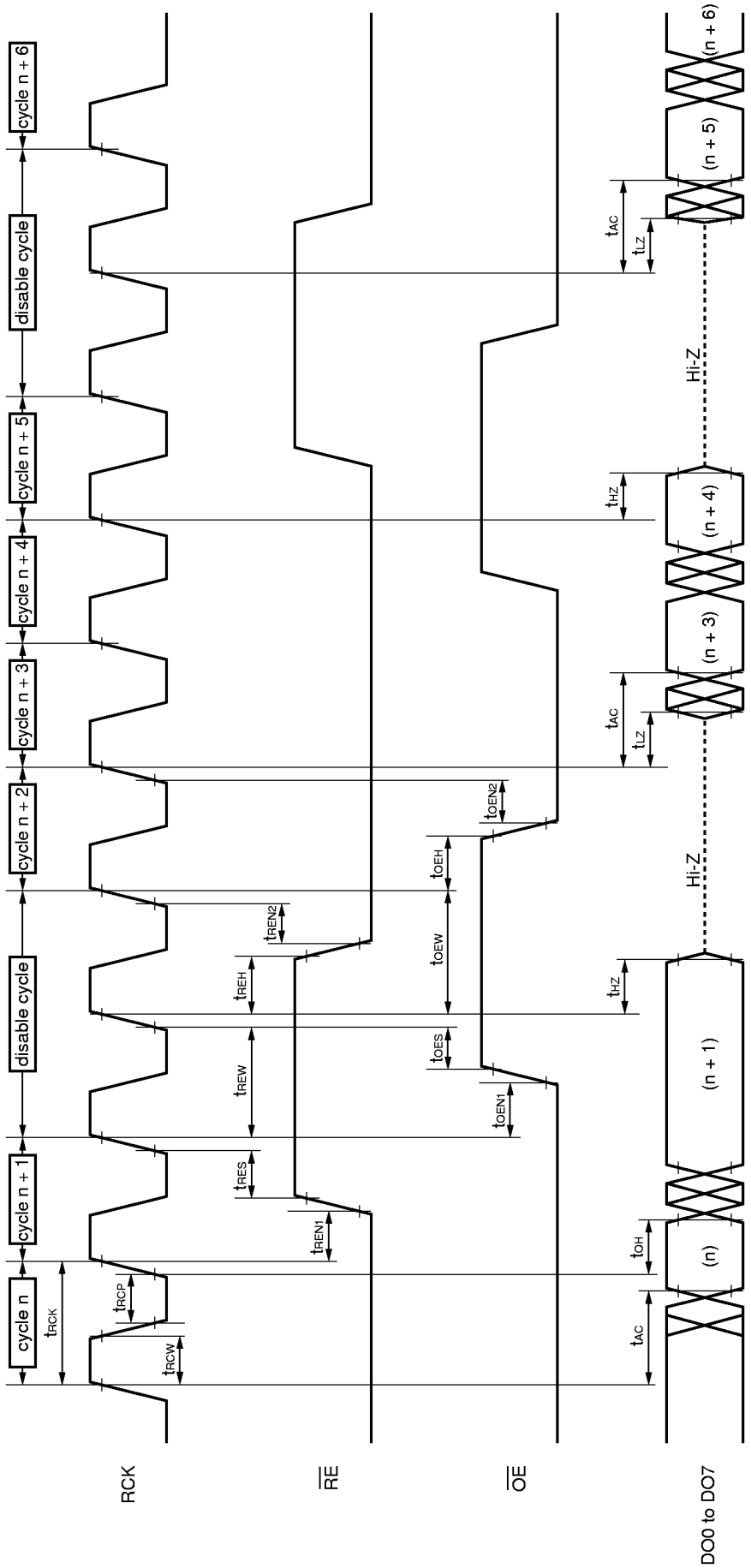
Read reset cycle



Read cycle ($\overline{RE}$, $\overline{RRST}$ control)



Read cycle ($\overline{RE}$, $\overline{OE}$ control)

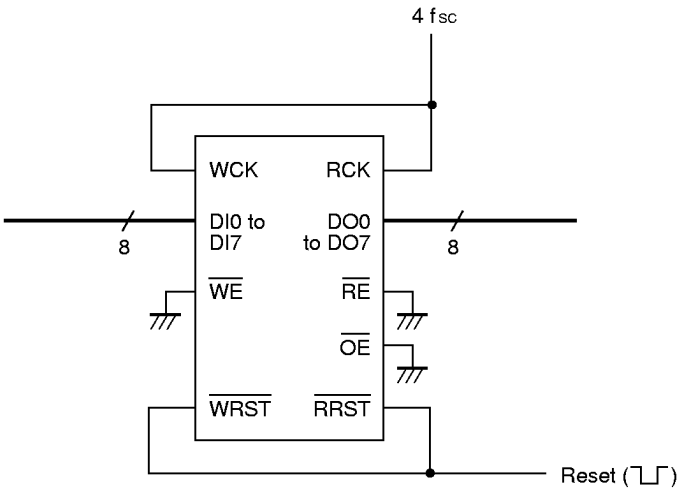


5. APPLICATION EXAMPLE

(1) 1 field delay line (the old data read)

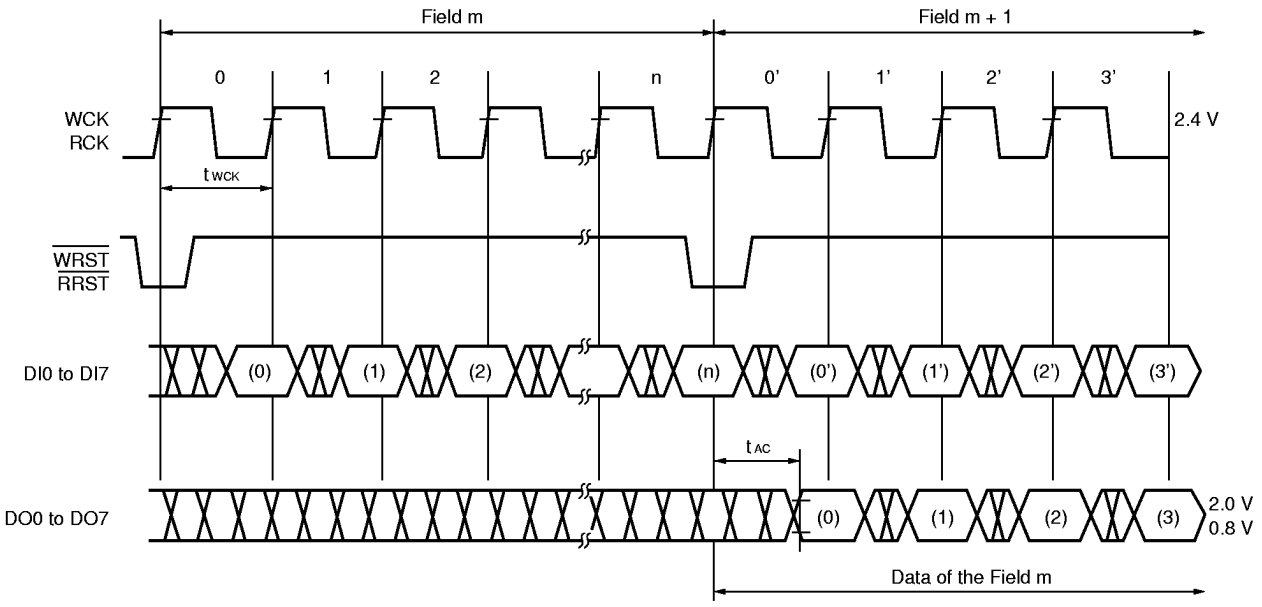
With connection as shown in Figure 5-1 by inputting the reset every 1 field cycle (in common with $\overline{WRST}$ and $\overline{RRST}$), 1 field delay line is realized easily (See Figure 5-2). When the difference between the write address and the read address is 0 (the read address and the write address are same), the old data is read as shown in Figure 5-2.

Figure 5-1 Circuit of 1 field delay line



fSC: Color subcarrier frequency

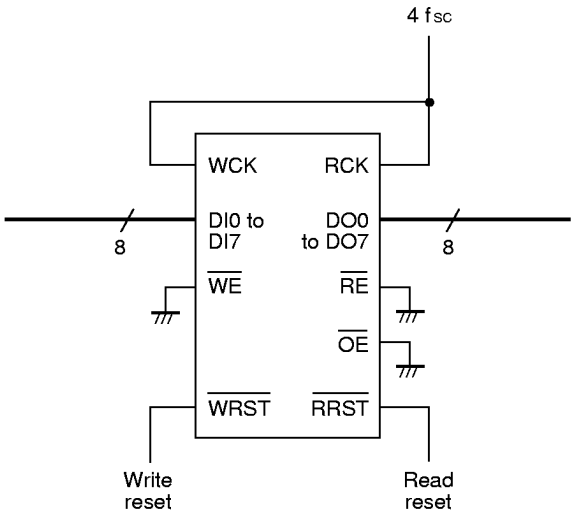
Figure 5-2 1 field delay line timing diagram



(2) The new data read

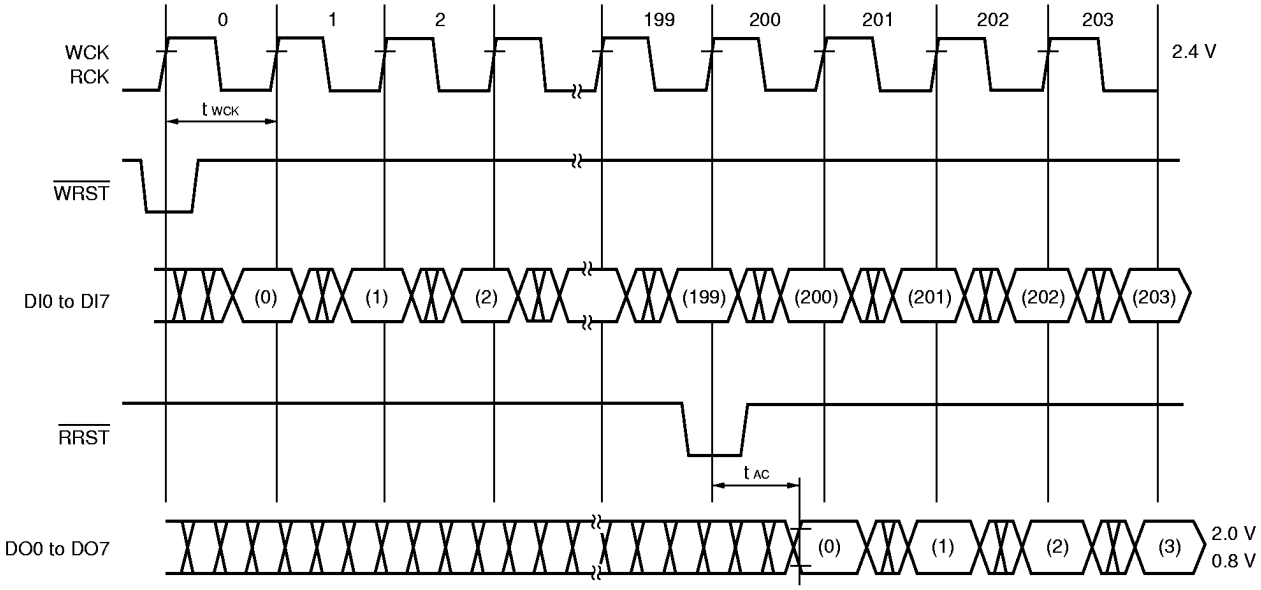
With connection as shown in Figure 5-3 by inputting $\overline{\text{RRST}}$ 200 cycle after $\overline{\text{WRST}}$, new data (the latest written data) can be read. (See Figure 5-4)

Figure 5-3 Circuit of new data read



fSC: Color subcarrier frequency

Figure 5-4 New data read timing diagram

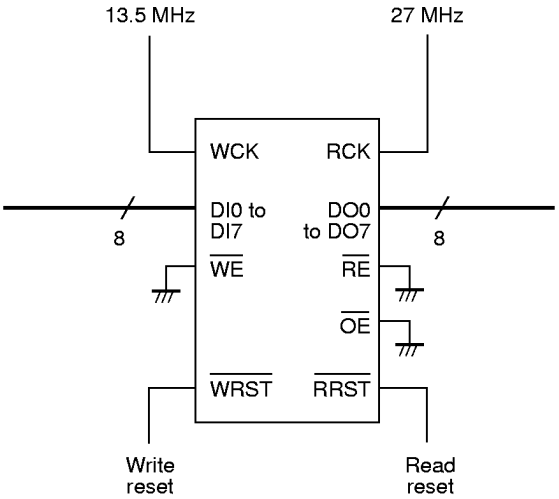


(3) Double speed conversion

By reading with double cycles for the write cycle, the double speed conversion can be done. Figure 5-5 shows an example circuit in which the data is written by 13.5 MHz and the data is read by 27 MHz. In this example, the same field is read 2 times (Timing Figure 5-6).

Caution Note that when the read and the write compete each other in the same field like this application, in the last 192 words, the data before 1 field may be output.

Figure 5-5 Circuit of double speed conversion



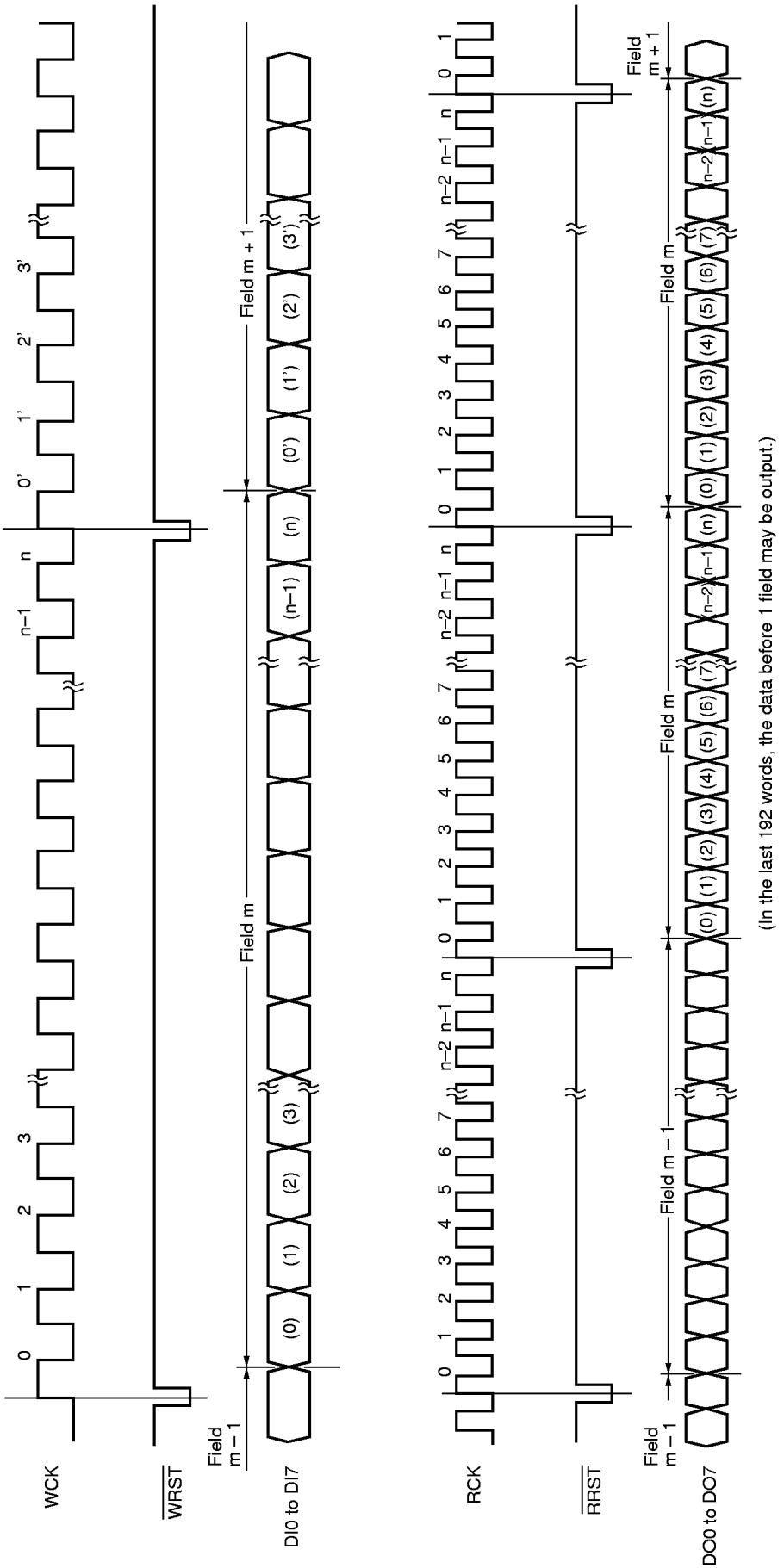
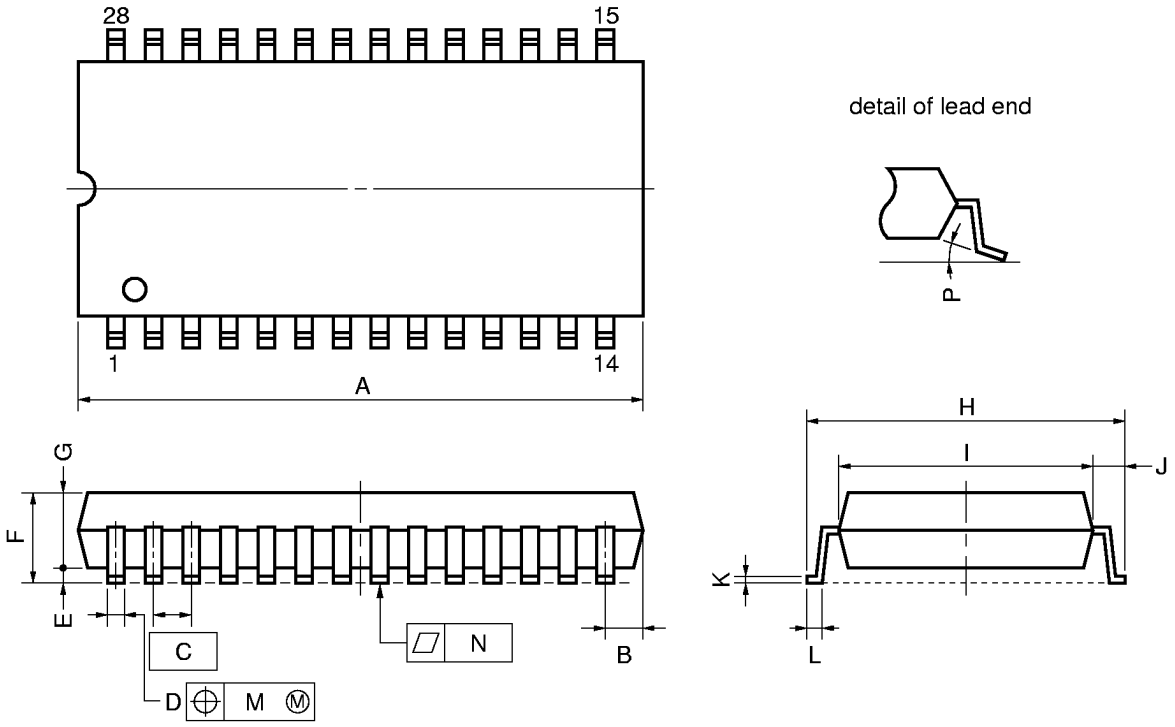


Figure 5-6 Double speed conversion timing diagram

6. PACKAGE DRAWINGS

28 PIN PLASTIC SOP (450 mil)



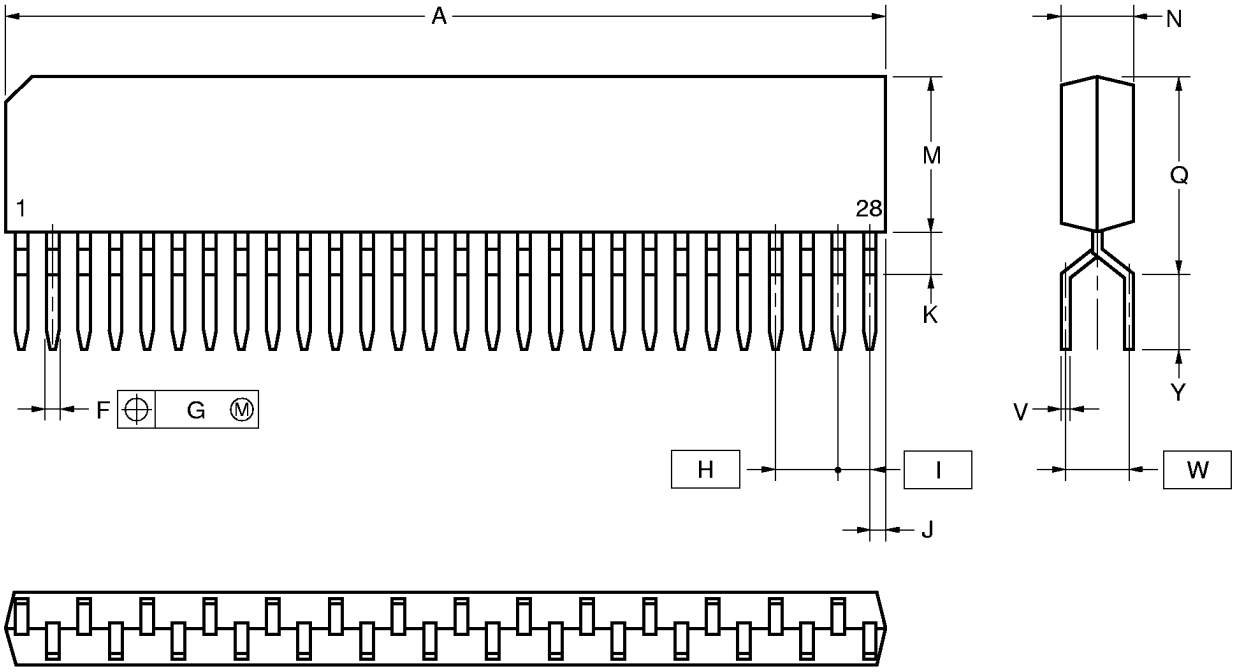
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	19.05 MAX.	0.750 MAX.
B	1.27 MAX.	0.050 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
E	0.2±0.1	0.008±0.004
F	3.0 MAX.	0.119 MAX.
G	2.55±0.1	$0.100^{+0.005}_{-0.004}$
H	11.8±0.3	$0.465^{+0.012}_{-0.013}$
I	8.4±0.1	$0.331^{+0.004}_{-0.005}$
J	1.7±0.2	0.067±0.008
K	$0.20^{+0.07}_{-0.03}$	$0.008^{+0.003}_{-0.002}$
L	0.7±0.2	$0.028^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	5°±5°	5°±5°

P28GU-50-450A-1

28 PIN PLASTIC ZIP (400mil)



NOTE

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	36.83 MAX.	1.050 MAX.
F	0.5±0.1	$0.020^{+0.004}_{-0.005}$
G	ϕ0.25	ϕ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	2.8±0.2	$0.110^{+0.009}_{-0.008}$
Q	10.16 MAX.	0.400 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	3.3±0.5	0.130±0.02

P28V-254-400A-1

7. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

★ **Type of Surface Mount Device**

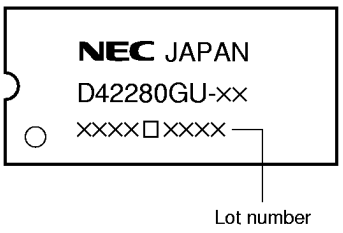
μPD42280GU-xx: 28-pin plastic SOP (450 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below, (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times, Exposure limit Note : 7 days (20 hours pre-baking is required at 125 °C afterwards).	IR35–207–2
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times, Exposure limit Note : 7 days (20 hours pre-baking is required at 125 °C afterwards).	VP15–207–2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature 120 °C or below (Package surface temperature), Exposure limit Note : 7 days (10 hours pre-baking is required at 125 °C afterwards).	WS60–107–1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Note Maximum allowable time from taking the soldering package out of dry pack to soldering.
Storage conditions: 25 °C and relative humidity of 65 % or less.

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Remark These conditions apply to the "version F" devices (whose 5th character position of the lot number is "F ").



Type of Through Hole Mount Device

μPD42280V-xx: 28-pin plastic ZIP (400 mil)

Soldering process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or less (per each lead)

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.