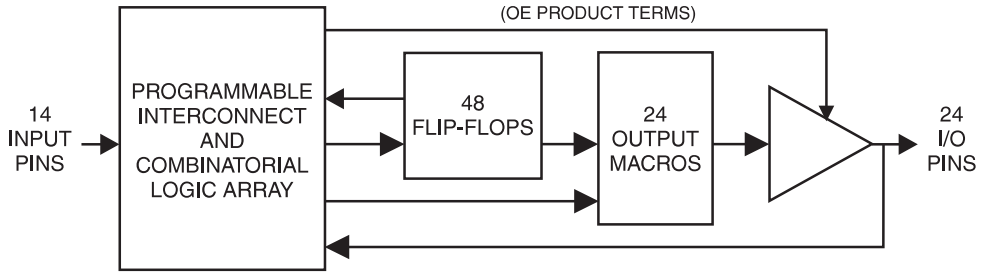
High-Density UV-Erasable Programmable Logic Device

ATV2500H
ATV2500L

Features

- **Third Generation Programmable Logic Structure**
  - **Easily Achieves Gate Utilization Factors of 80 Percent**
- **Increased Logic Flexibility**
  - **86 Inputs and 72 Sum Terms**
- **Flexible Output Macrocell**
  - **48 Flip-Flops - 2 per Macrocell**
  - **3 Sum Terms - Can Be OR'ed and Shared**
- **High-Speed**
- **Low-Power — Less than 0.5 mA Typical (ATV2500L)**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Asynchronous Clocks and Resets**
  - **Multiple Synchronous Presets - One per Four or Eight Flip-Flops**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **40-pin Dual-In-line and 44-Lead Surface Mount Packages**

Block Diagram



Description

The ATV2500H/L is the most powerful programmable logic device available in a 40-pin package. Increased product terms, sum terms, and flip-flops translate into many more usable gates. High gate utilization is easily obtainable.

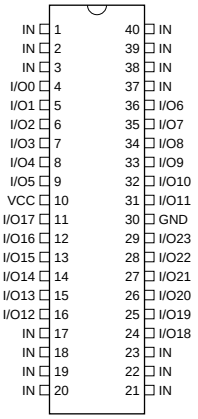
The ATV2500H/L is organized around a global bus. All pin and feedback terms are always available to every logic cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 flip-flops.

(continued)

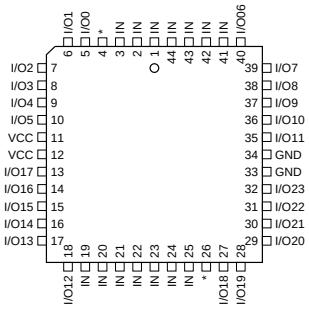
Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O, 0,2,4..	“Even” I/O Buffers
I/O, 1,3,5..	“Odd” I/O Buffers
*	No Internal Connection
VCC	+5V Supply

DIP



PLCC/LCC



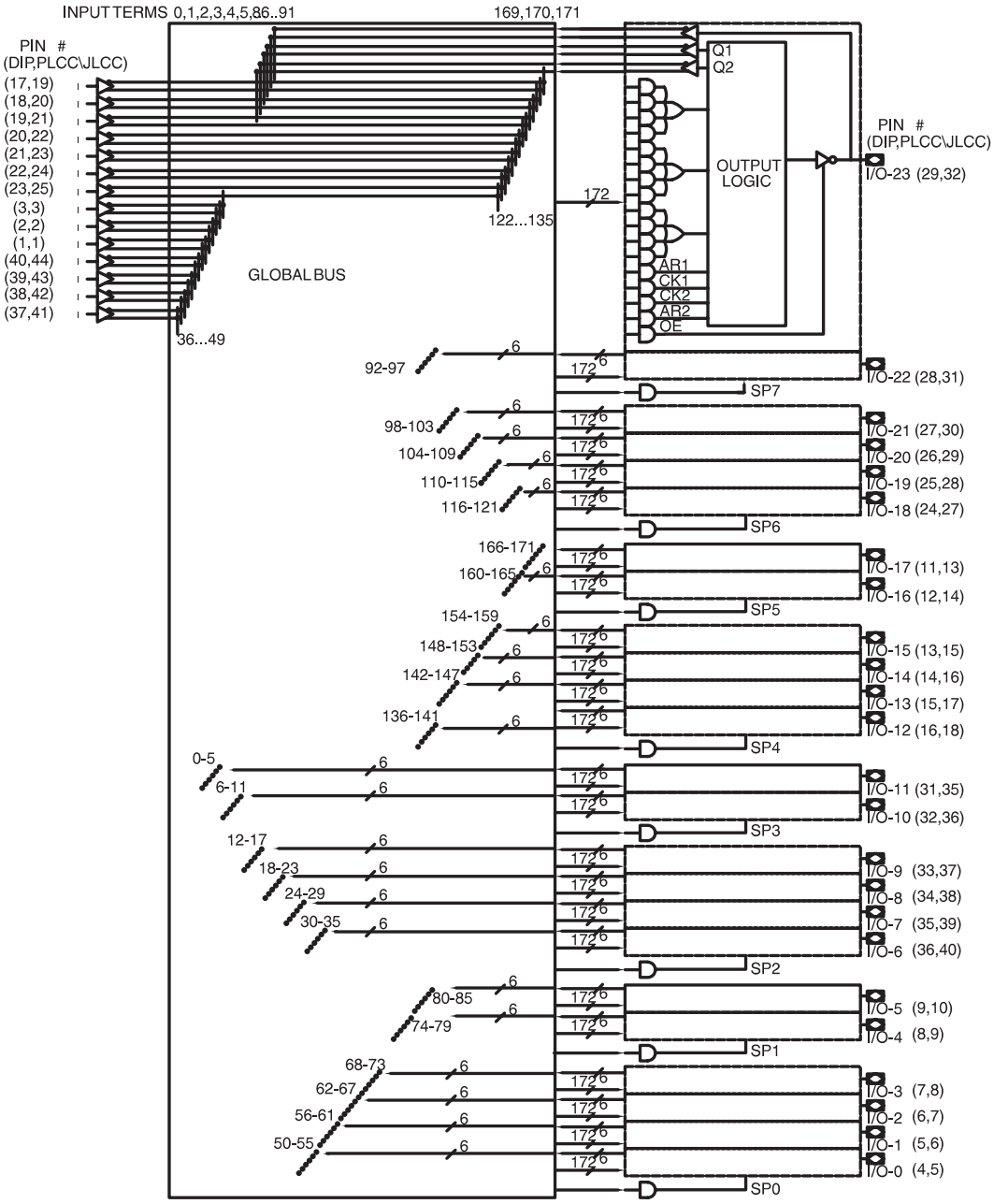
* = No Connect

Rev. 0025E–05/98

There are 416 product terms available. Four product terms are input to each sum term. The three sum terms per logic cell can be combined to provide up to twelve product terms, combinatorial and registered. Independent of output configuration, the two flip-flops are always usable, and always have at least four product term inputs.

Product terms are available providing asynchronous resets, flip-flop clocks, and output enables. One reset and one clock term are provided per flip-flop, with one enable term per output. Eight product terms provide local synchronous presets, divided up into banks of four and eight flip-flops. Register preload and buried register observability simplify testing. The device has an internal power up clear function.

Functional Logic Diagram ATV2500H/L



Functional Logic Diagram Description

The ATV2500H/L Functional Logic Diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the global bus.

The ATV2500H/L is a straightforward and uniform PLD. The twenty-four macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top twelve product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The fourteen dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) flip-flop Q2 true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

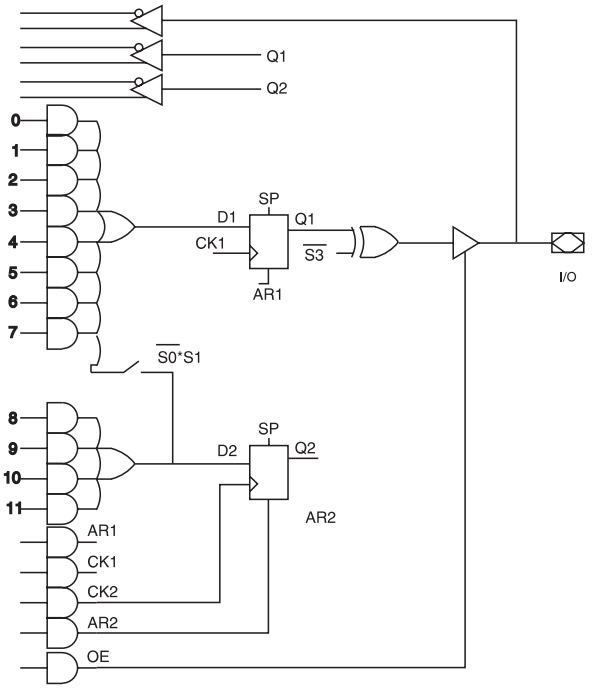
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to + 125°C
Storage Temperature	-65°C to + 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W.sec/cm^2

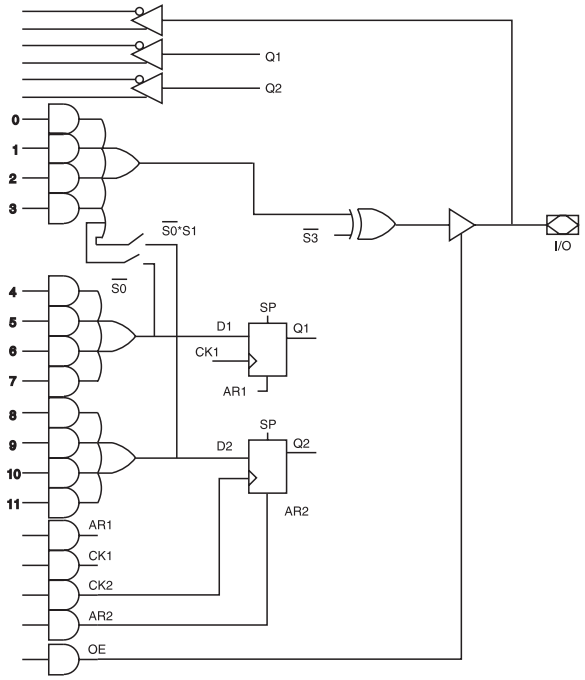
*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V dc, which may overshoot to 7.0V for pulses of less than 20 ns.

Output Logic, Registered



Output Logic, Combinatorial



These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

S2	S1	S0	Terms In D1	Terms In D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4(1)	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

S2	S1	S0	Terms In D1	Terms In D2	Output Configuration
1	0	0	4(1)	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4(1)	4(1)	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

DC and AC Operating

		ATV2500H-25	ATV2500H/L-30	ATV2500H/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	ATV2500L	Com.		0.5	5	mA
				Ind.,Mil.		0.5	10	mA
			ATV2500H	Com.		80	160	mA
				Ind.,Mil.		80	180	mA
I_{OS}(1)	Output Short Circuit Current	V_{OUT} = 0.5V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or $V_{IL,}$ I_{OL} = 8 mA Com,Ind; 6 mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC} - 0.3			V
		I_{OH} = -4.0 mA			2.4			V

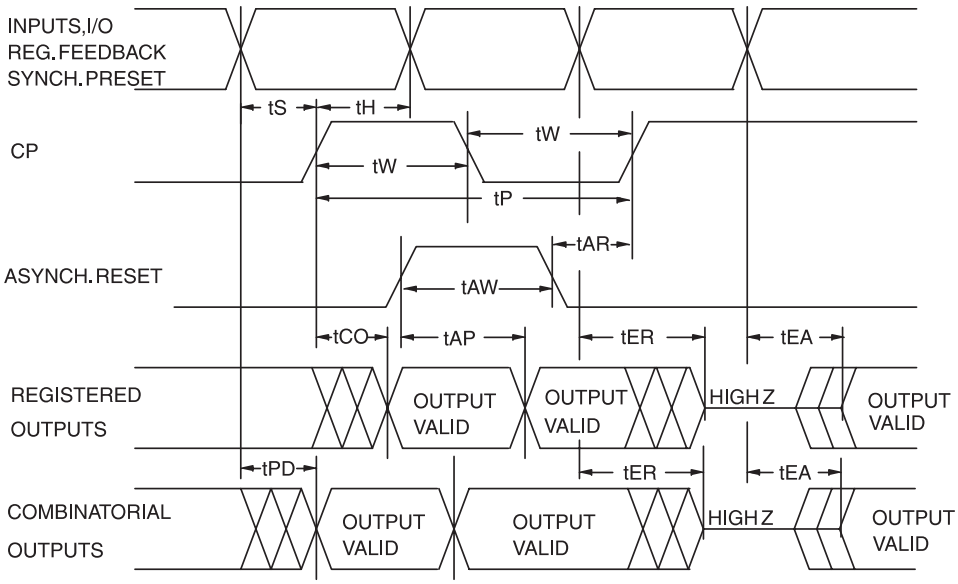
Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

Pin Capacitance (f = MHz, T = 25°C)(1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = OV
C_{OUT}	8	12	pF	V_{OUT} = OV

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

AC Waveforms[1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics for the ATV2500L

Symbol	Parameter	ATV2500L-30		ATV2500L-35		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		30		35	ns
t_{EA}	Input to Output Enable		30		35	ns
t_{ER}	Input to Output Disable		30		35	ns
t_{CO}	Clock to Output	5	30	5	35	ns
t_{CF}	Clock to Feedback	10	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	20		22		ns
t_{SI2}	Input Setup Time, Buried Register[1]	20		22		ns
t_{SF}	Feedback Setup Time	10		15		ns
t_{H1}	Hold Time, Output Register	10		15		ns
t_{H2}	Hold Time, Buried Register[1]	5		5		ns
t_W	Clock Width	15		17		ns
t_P	Clock Period	30		35		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		33		28	MHz
t_{AW}	Asynchronous Reset Width	18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35	ns

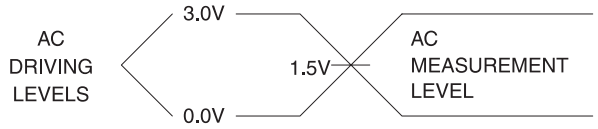
Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

AC Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25		ATV2500H-30		ATV2500H-35		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register(1)	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

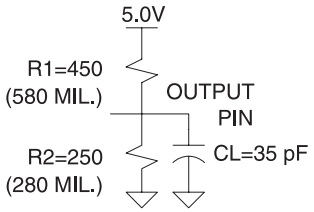
Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Loads

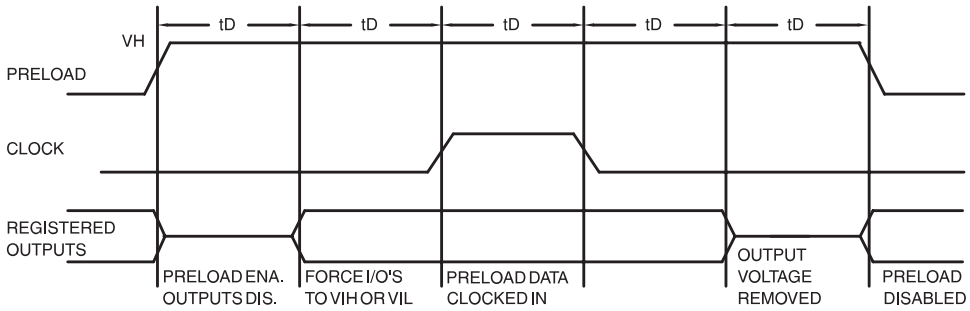


Preload and Observability of Registered Outputs

The ATV2500H/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The preload state is entered by placing an 11V to 14V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 11V to 14V signal on pin 2 (DIP or SMP). In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.



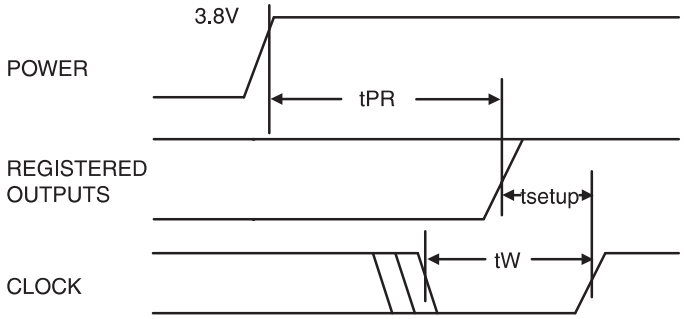
Level forced on Odd I/O pin during preload cycle.	Q Select pin state	Even/ Odd select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power-Up Reset

The registers in the ATV2500H/L are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high,
3. The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500H/L fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits preload and Q2 observability.

Atmel CMOS PLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

Using the ATV2500H/L's Many Advanced Features

The ATV2500H/L's flexibility puts more usable gates in 40 pins than other PLDs. Some of the ATV2500H/L's key features are:

- Asynchronous Clocks -

Each of the flip-flops in the ATV2500H/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500H/L clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500H/L provides two flip-flops for each output macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own sum term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's output enable, facilitates designs using bi-directional I/O buses.

- Three Sum Terms per Macrocell -

The ATV2500H/L macrocell can be configured with one SUM term feeding the output, and still have two SUM terms feeding the flip-flops. This is the simplest method for interfacing with an I/O bus, and no flip-flops need be sacrificed.

- Combinable Sum Terms -

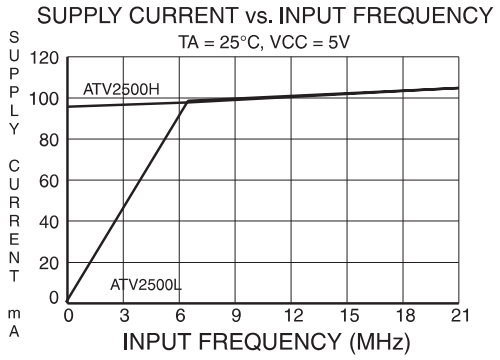
Each output macrocell's three SUM terms can be combined in an OR gate before the output or the register. This provides up to twelve product terms per output or flip-flop. When the registered output configuration is chosen, eight terms are automatically available to D1. The four terms feeding D2 can also be shared with D1, giving it a total of twelve. In the combinatorial mode, four, eight, or twelve terms can feed the output, with the middle four still driving D1 and the bottom four still driving D2.

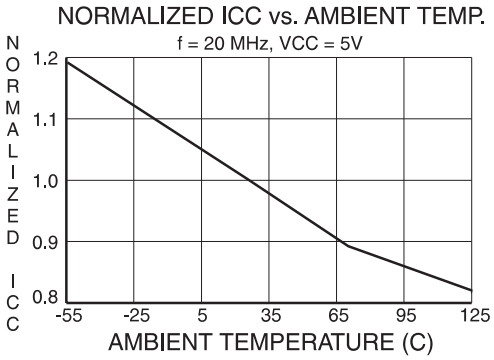
Programming Software Support

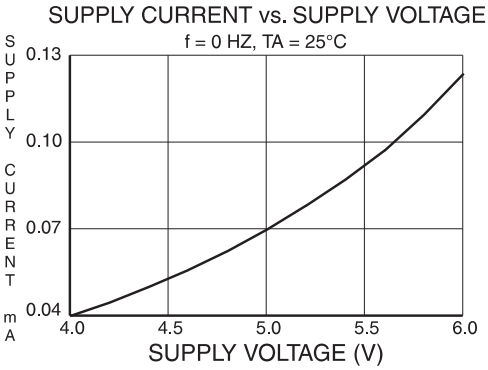
Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500H/L is currently available from several PLD software vendors. Please refer to the *Programmable Logic Development Tools* section for a complete listing of the PLD software support.

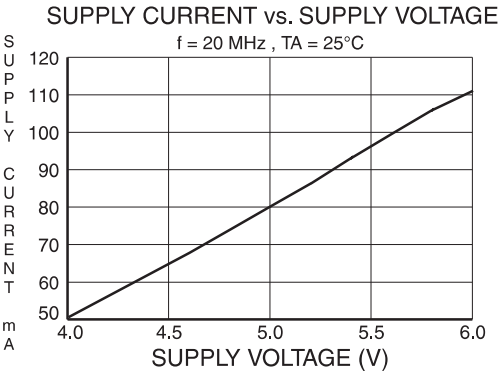
Erasure Characteristics

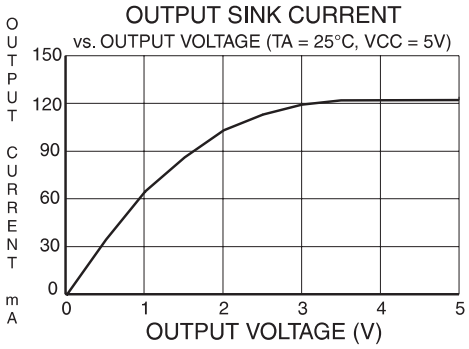
The entire memory array of an ATV2500H/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of twenty minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of fifteen $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

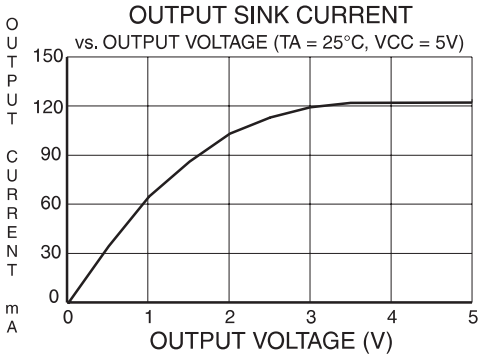


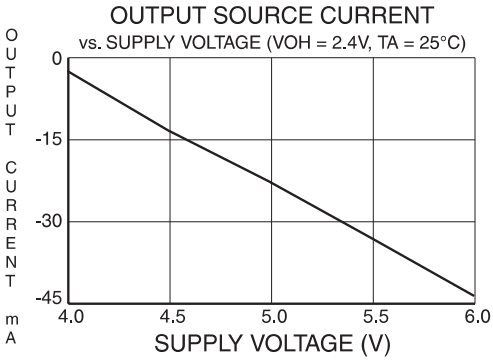


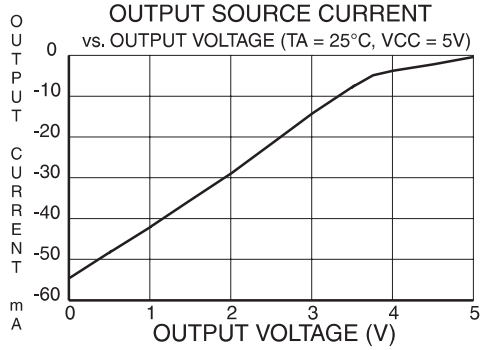




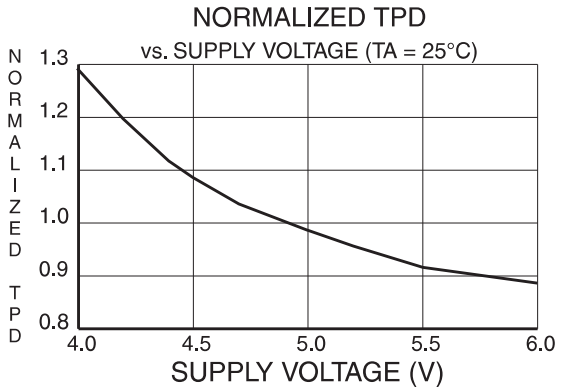


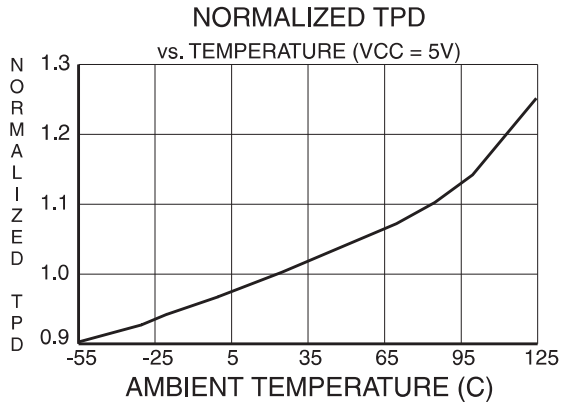


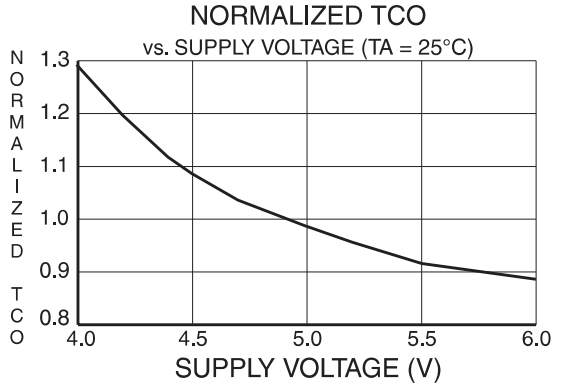


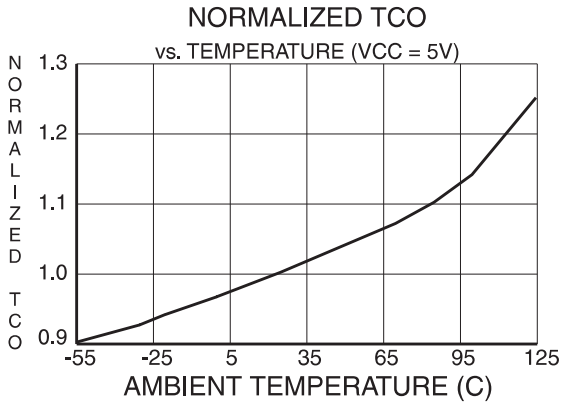


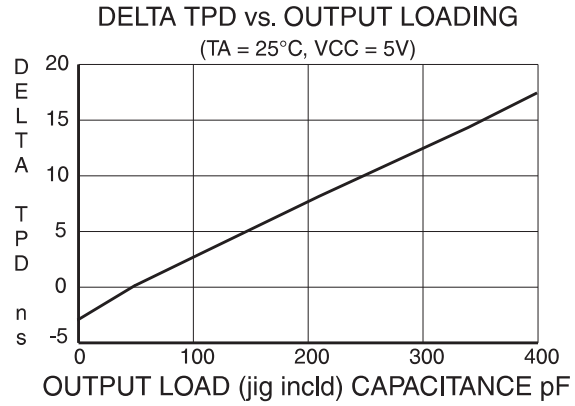
Note: All normalized values referenced to maximum specification in AC characteristics section of datasheet.

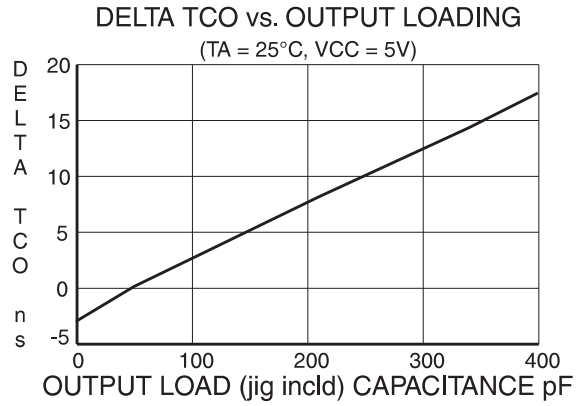












Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	**25**	**40**	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
25	25	40	5962-91545 02M QA 5962-91545 02M XX 5962-91545 02M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

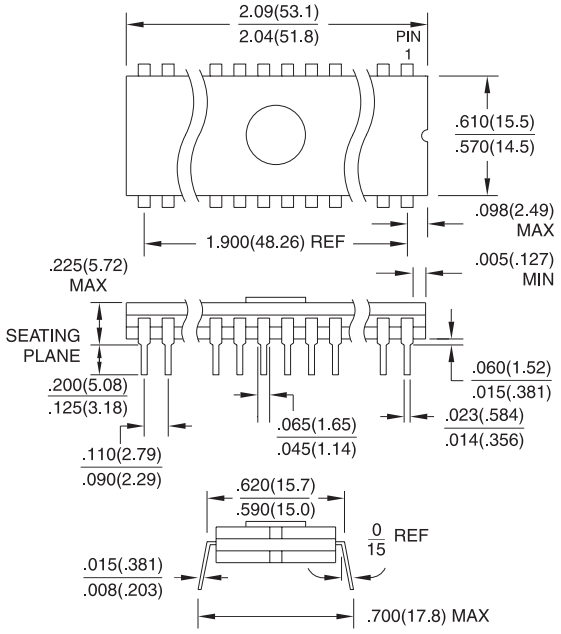
Ordering Information (Continued)

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500L-30DC ATV2500L-30JC ATV2500L-30KC ATV2500L-30LC ATV2500L-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-30DI ATV2500L-30JI ATV2500L-30KI ATV2500L-30LI ATV2500L-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-30DM ATV2500L-30KM ATV2500L-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-30DM/883 ATV2500L-30KM/883 ATV2500L-30LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500L-35DC ATV2500L-35JC ATV2500L-35KC ATV2500L-35LC ATV2500L-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-35DI ATV2500L-35JI ATV2500L-35KI ATV2500L-35LI ATV2500L-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
30	30	33	5962-91545 03M QA 5962-91545 03M XX 5962-91545 03M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

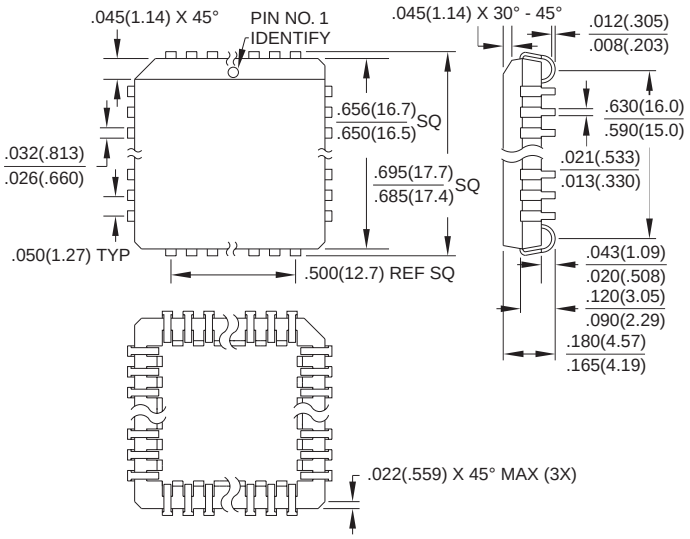
Package Type	
40DW6	40-Lead, 0.600" Wide Windowed, Ceramic Dual In-line Package (Cerdip)
44J	44-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40-Lead, 0.600" Wide Plastic Dual In-line Package OTP (PDIP)

Packaging Information

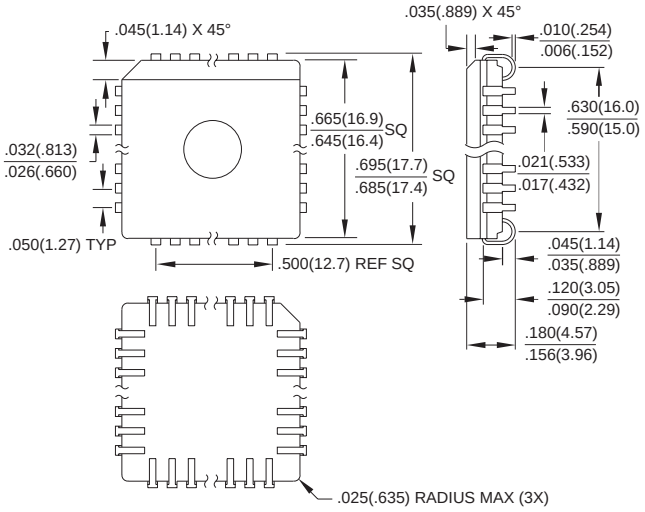
40DW6, 40-Lead, 0.600" Wide Windowed, Ceramic Dual In-line Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



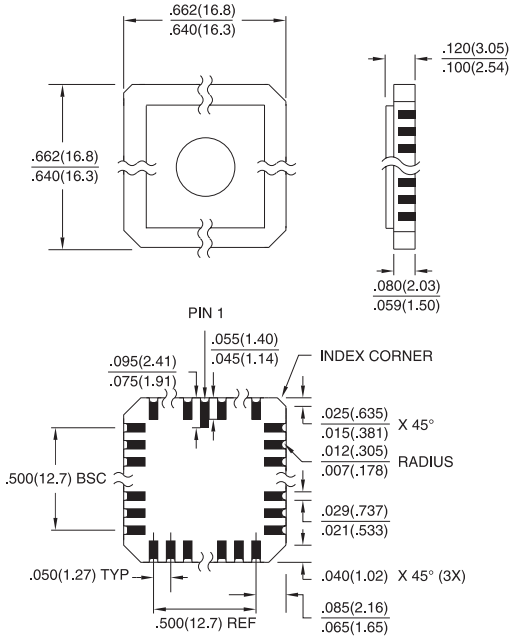
44J, 44-Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
Dimensions in Inches and (Millimeters)



44KW, 44-Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J1



44LW, 44-Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-5



Packaging Information

40P6, 40-Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AC