

131,072-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

The TC558128BJ/BFT is a 1,048,576-bit high-speed static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 5 V power supply. There are two control inputs. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly TTL compatible. The TC558128BJ/BFT is available in a plastic 32-pin SOJ (400 mil width) and TSOP packages for high density surface assembly.

FEATURES

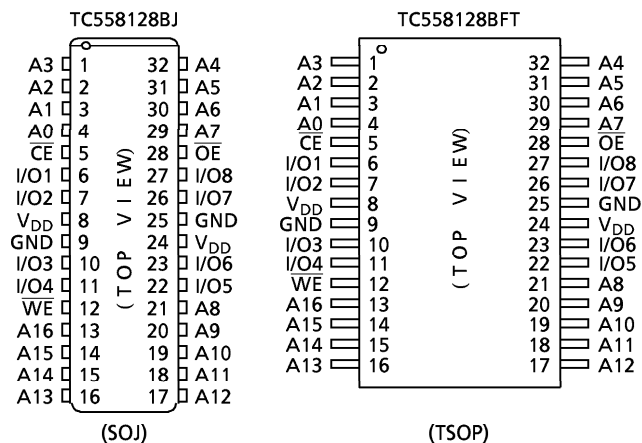
- Fast access time (the following are maximum values)
 - TC558128BJ/BFT-12: 12 ns
 - TC558128BJ/BFT-15: 15 ns
- Low-power dissipation (the following are maximum values)
- Single power supply voltage of 5 V \pm 10%
- Fully static operation
- All inputs and outputs are TTL compatible
- Output buffer control using \overline{OE}
- Package:

Cycle Time	12	15	20	25	30	ns
Operation (max)	190	170	140	130	120	mA

Standby: 1 mA (both devices)

SOJ32-P-400-1.27A (BJ) (Weight: 1.22 g typ)
 TSOP II 32-P-400-0.80C (BFT) (Weight: 0.34 g typ)

PIN ASSIGNMENT



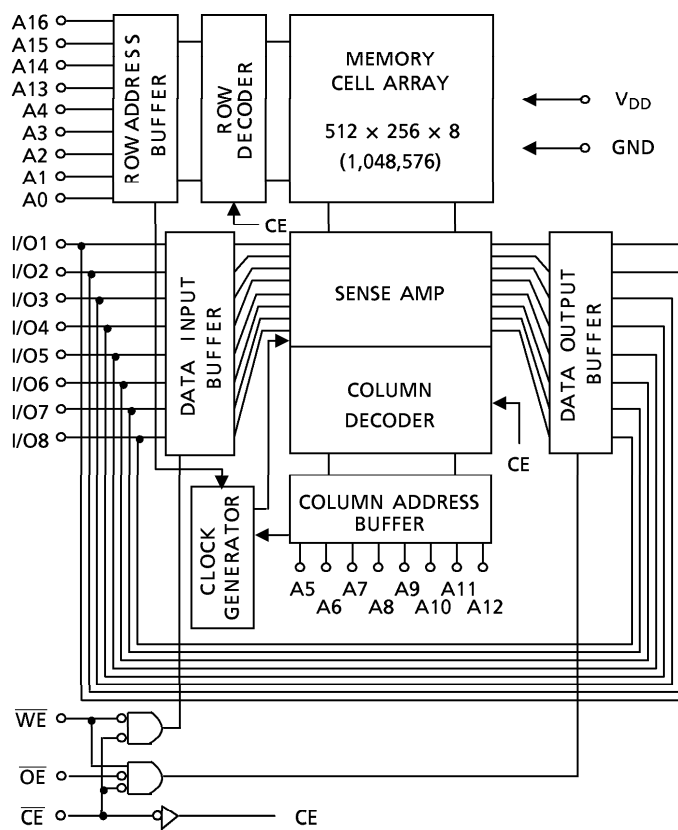
PIN NAMES

A0 to A16	Address Inputs
I/O1 to I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable
V_{DD}	Power (+ 5 V)
GND	Ground

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 7.0	V
V_{IN}	Input Terminal Voltage	- 2.0* to 7.0	V
$V_{I/O}$	Input/Output Terminal Voltage	- 0.5* to $V_{DD} + 0.5$	V
P_D	Power Dissipation	1.1	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 65 to 150	°C
T_{opr}	Operating Temperature	- 10 to 85	°C

*: - 3 V with a pulse width of 10 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage	- 0.5 *	-	0.8	V

*: - 3 V with a pulse width of 10 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 10	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}	-	-	± 10	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V	- 4	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V	8	-	-	mA	
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0 mA Other Inputs = V _{IH} or V _{IL}	tcycle = 12 ns	-	-	190	mA
			tcycle = 15 ns	-	-	170	
			tcycle = 20 ns	-	-	140	
			tcycle = 25 ns	-	-	130	
			tcycle = 30 ns	-	-	120	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} or V _{IL}	-	-	30	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2$ V Other Inputs = V _{DD} - 0.2 V or 0.2 V	-	-	1		

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O1 to I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	x	L	Input	I_{DDO}
Outputs Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	x	x	High Impedance	I_{DDs}

X: Don't care

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C (Note 1), $V_{DD} = 5\text{ V} \pm 10\%$)

READ CYCLE

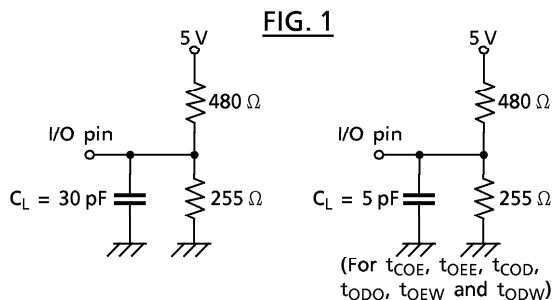
SYMBOL	PARAMETER	TC558128BJ/BFT-12		TC558128BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{ACC}	Address Access Time	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	12	–	15	
t_{OE}	Output Enable Access Time	–	6	–	8	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from Chip Enable	5	–	5	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	6	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	6	–	8	

WRITE CYCLE

SYMBOL	PARAMETER	TC558128BJ/BFT-12		TC558128BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{WP}	Write Pulse Width	8	–	9	–	
t_{CW}	Chip Enable to End of Write	10	–	12	–	
t_{AW}	Address Valid to End of Write	10	–	12	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	6	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from Write Enable	1	–	1	–	
t_{ODW}	Output Disable Time from Write Enable	–	6	–	8	

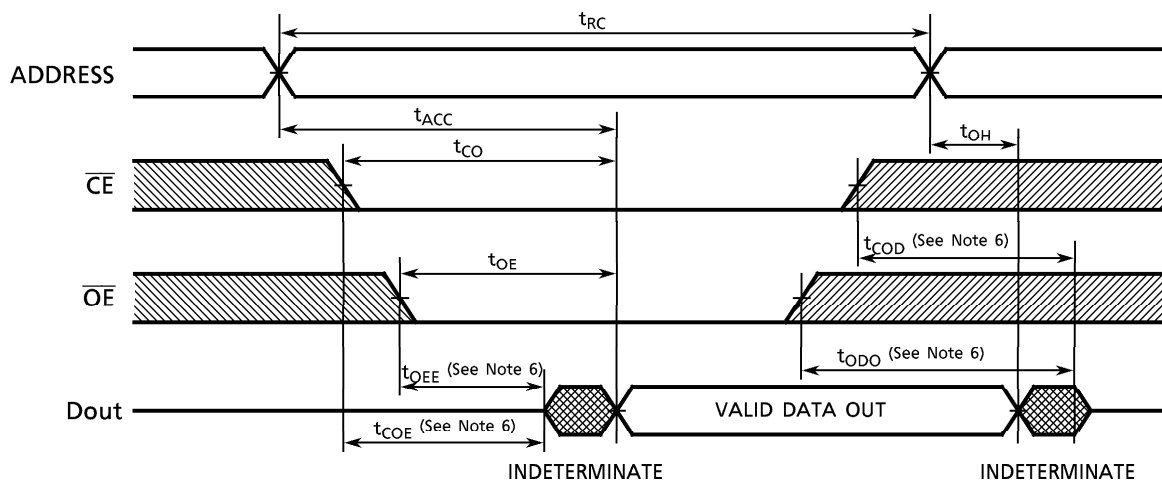
AC TEST CONDITIONS

Input Pulse Level	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig. 1

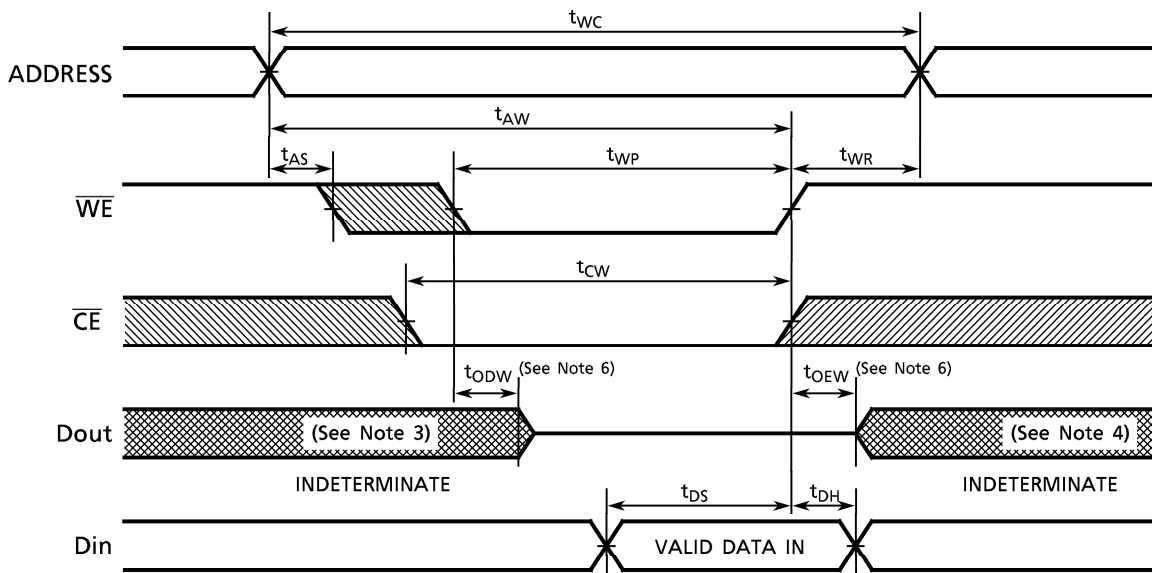


TIMING DIAGRAMS

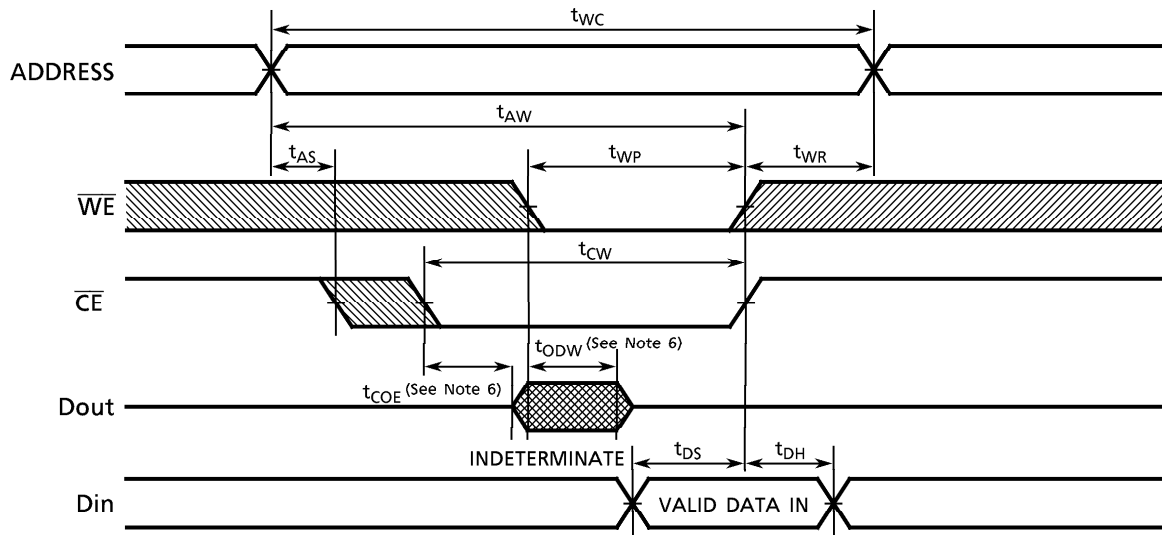
READ CYCLE (See Note 2)



WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 5)



Note: (1) Operating temperature (T_a) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) \overline{WE} remains HIGH for the Read Cycle.

(3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.

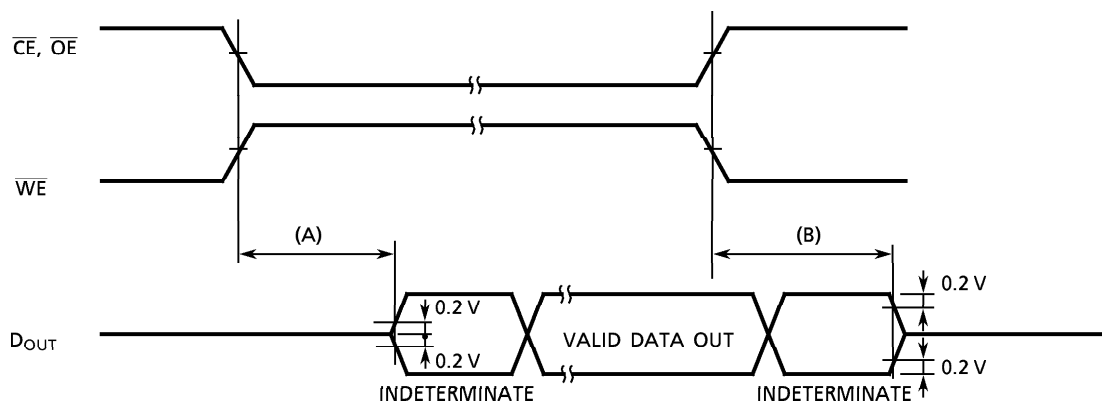
(4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

(5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{OEW}$ Output Enable Time

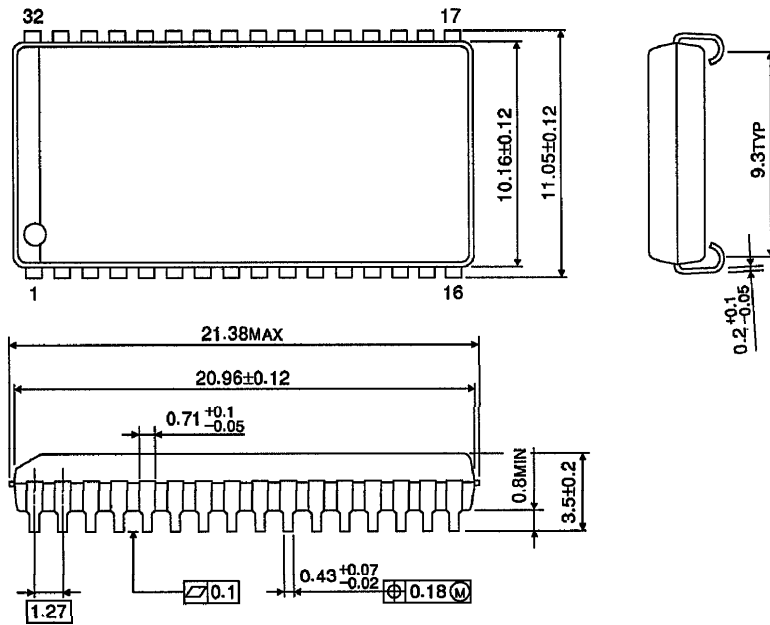
(B) $t_{COD}, t_{ODO}, t_{ODW}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ32-P-400-1.27A)

Units in mm

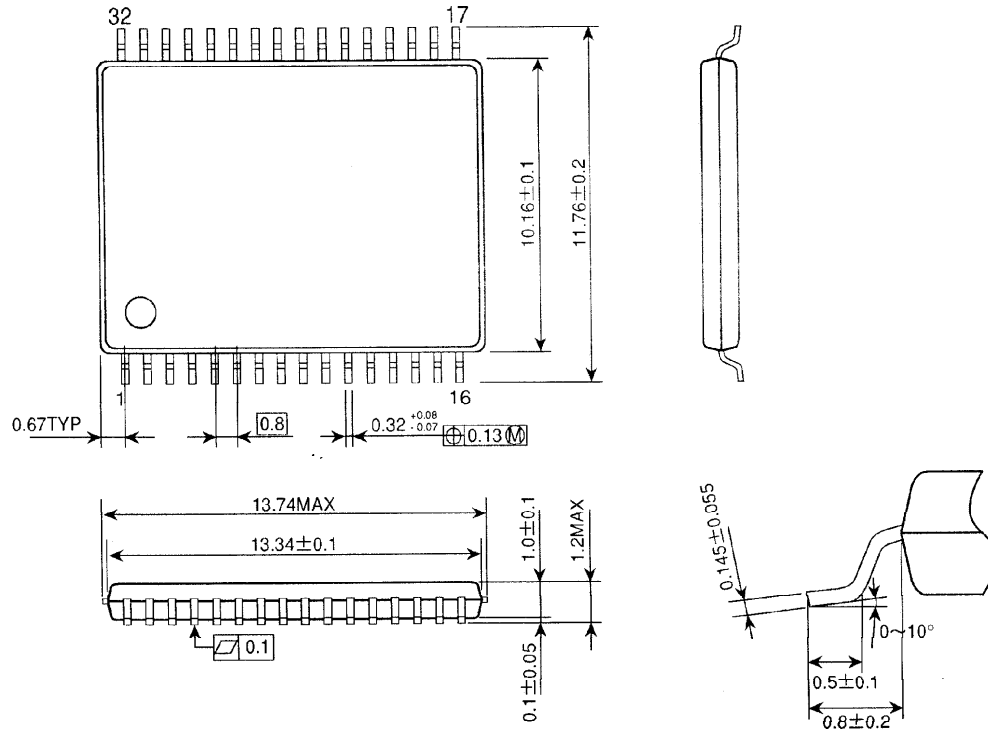


Weight: 1.22 g (typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 32-P-400-0.80C)

Units in mm



Weight: 0.34 g (typ)