TOSHIBA Digital Integrated Circuit Silicon Monolithic

TC7SP3125TU

Low Voltage/Low Power 1-Bit Dual Supply Bus Buffer

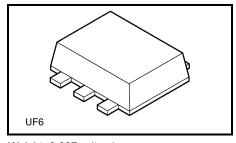
The TC7SP3125 is a dual supply, advanced high-speed CMOS 1-bit dual supply voltage interface bus buffer fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.6-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.6-V supply systems.

The A-input interfaces with the 1.2-V, 1.5-V, 1.8-V or 2.5-V bus, the B-output with the 1.8-V, 2.5-V, 3.3-V bus.

The enable input (\overline{OE}) can be used to disable the device so that the signal lines are effectively isolated.



Weight: 0.007 g (typ.)

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features (Note)

- Level converter for interfacing 1.2-V to 1.8-V, 1.2-V to 2.5-V, 1.2-V to 3.3-V, 1.5-V to 2.5-V, 1.5-V to 3.3-V, 1.8-V to 2.5-V, 1.8-V to 3.3-V or 2.5 V to 3.3-V system.
- High-speed operation: $t_{pd} = 6.8 \text{ ns (max)} (V_{CCA} = 2.5 \pm 0.2 \text{ V}, V_{CCB} = 3.3 \pm 0.3 \text{ V})$

 $t_{pd} = 7.8 \text{ ns (max) (VCCA} = 1.8 \pm 0.15 \text{ V, VCCB} = 3.3 \pm 0.3 \text{ V)}$

 t_{pd} = 8.6 ns (max) (V_{CCA} = 1.5 ± 0.1 V, V_{CCB} = 3.3 ± 0.3 V)

 $t_{pd} = 22 \text{ ns (max) (VCCA} = 1.2 \pm 0.1 \text{ V, VCCB} = 3.3 \pm 0.3 \text{ V)}$

 t_{pd} = 9.5 ns (max) (VCCA = 1.8 ± 0.15 V, VCCB = 2.5 ± 0.2 V)

 $t_{pd} = 10.5 \text{ ns (max)} (V_{CCA} = 1.5 \pm 0.15 \text{ V}, V_{CCB} = 2.5 \pm 0.2 \text{ V})$

 t_{pd} = 23 ns (max) (V_{CCA} = 1.2 ± 0.15 V, V_{CCB} = 2.5 ± 0.2 V)

 $t_{pd} = 30 \text{ ns (max) (V}_{CCA} = 1.2 \pm 0.1 \text{ V}, \text{ V}_{CCB} = 1.8 \pm 0.15 \text{ V})$

• Output current : I_{OH} / I_{OL} = ± 12 mA (min) (V_{CC} = 3.0 V)

 $I_{OH} / I_{OL} = \pm 9 \text{mA (min)} (V_{CC} = 2.3 \text{ V})$

 I_{OH} / I_{OL} = ±3 mA (min) (V_{CC} = 1.65 V)

- Latch-up performance: -300 mA
- ESD performance: Machine model $\geq \pm 200 \text{ V}$

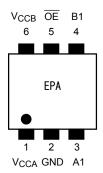
Human body model ≥ ±2000 V

- Ultra-small package: UF6
- Low current consumption: Using the new circuit significantly reduces current consumption when $\overline{OE} = \text{``H''}$. Suitable for battery-driven applications such as PDAs and cellular phones.
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

Pin Assignment (top view)





Truth Table

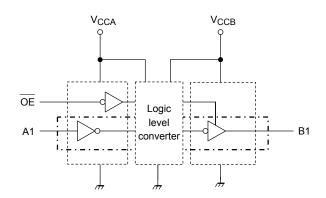
Inputs		Output
ŌĒ	A1	B1
L	L	L
L	Н	Н
Н	X	Z

X: Don't care

Z: High impedance

Block Diagram

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Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2	V _{CCA}	−0.5 to 4.6	V
Tower supply voltage (Note 2	V _{CCB}	−0.5 to 4.6	V
DC input voltage (A1, \overline{OE})	V _{IN}	−0.5 to 4.6	V
DC output voltage	V	-0.5 to 4.6 (Note 3)	V
(B1)	V _{OUTB}	-0.5 to V _{CCB} + 0.5 (Note 4)	V
Input diode current	I _{IK}	-25	mA
Output diode current	lok	±50 (Note 5)	mA
DC output current	loutb	±25	mA
DC V _{CC} /ground current per supply pir	ICCA	±25	mA
DC VCC/ground current per supply pil	ICCB	±50	IIIA
Power dissipation	PD	200	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.

Note 3: Output in OFF state

Note 4: High or Low stats. IOUT absolute maximum rating must be observed.

Note 5: $V_{OUT} < GND, V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V_{CCA}	1.1 to 2.7	V	
	V _{CCB}	1.65 to 3.6	V	
Input voltage (A1, \overline{OE})	V _{IN}	0 to 3.6	V	
Output voltage	Voutp	0 to 3.6 (Note 2)	V	
(B1)	V _{OUTB}	0 to V _{CCB} (Note 3)	V	
Output current		±12 (Note 4)		
(B1)	Гоитв	±9 (Note 5)	mA	
(61)		±3 (Note 6)		
Operating temperature	T _{opr}	−40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V	

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in OFF state

Note 3: High or low state

Note 4: V_{CCB} = 3.0 to 3.6 V

Note 5: $V_{CCB} = 2.3 \text{ to } 2.7 \text{ V}$

Note 6: $V_{CCB} = 1.65 \text{ to } 1.95 \text{ V}$

Note 7: $V_{IN} = 0.8$ to 2.0 V, $V_{CCA} = 2.5$ V, $V_{CCB} = 3.0$ V



Electrical Characteristics

DC Characteristics (1.1 V \leq V_{CCA} \leq 2.7 V , 1.65 V \leq V_{CCB} \leq 3.6 V)

Characteristics	Cumbal	Test Condition		Vac. (V)	Voor (V)	Ta = -40 to 85°C		Unit
Characteristics	Symbol	1	est Condition	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Offic
				1.1 ≤ V _{CCA} <1.4	1.65 to 3.6	0.65×		
				1.1 ≥ VCCA \1.4	1.00 to 0.0	V _{CCA}		
				1.4 ≤ V _{CCA} <1.65	1.65 to 3.6	0.65×		
H-level input voltage	VIHA	VIN		= VCCA		VCCA		V
				1.65 ≤ V _{CCA} <2.3	1.65 to 3.6	0.65×	_	
						V _{CCA}		
				2.3 ≤ V _{CCA} <2.7	1.65 to 3.6	1.6	_	
				1.1 ≤ V _{CCA} <1.4	1.65 to 3.6	_	0.30×	
							V _{CCA}	
				1.4 ≤ V _{CCA} <1.65	1.65 to 3.6	_	0.30×	
L-level input voltage	VILA	VIN					VCCA	V
				1.65 ≤ V _{CCA} <2.3	1.65 to 3.6	_	0.30×	
				23 < V/22 < 27	1.65 to 3.6		VCCA	
				2.3 ≤ V _{CCA} <2.7	1.05 10 3.0		0.7	
	$I_{OHB} = -100 \mu A$	1.1 to 2.7	1.65 to 3.6	V _{CCB} - 0.2	_			
H-level output voltage	Vонв	OHB A1 = V _{IH}	$I_{OHB} = -3 \text{ mA}$	1.1 to 2.7	1.65	1.25	_	V
H-level output voltage V _{OHI}			$I_{OHB} = -9 \text{ mA}$	1.1 to 2.7	2.3	1.7	_	
			$I_{OHB} = -12 \text{ mA}$	1.1 to 2.7	3.0	2.2	_	
			$I_{OLB} = 100 \; \mu A$	1.1 to 2.7	1.65 to 3.6	_	0.2	
L-level output voltage	V _{OLB}	A1 = V _{IL}	I _{OLB} = 3 mA	1.1 to 2.7	1.65	_	0.3	V
L-ievel output voltage	VOLB	AI - VIL	$I_{OLB} = 9 \text{ mA}$	1.1 to 2.7	2.3	_	0.6	V
			$I_{OLB} = 12 \text{ mA}$	1.1 to 2.7	3.0	_	0.55	
3-state output OFF	I _{OZB}	$A1 = V_{IHA}$	or V _{ILA}	1.1 to 2.7	1.65 to 3.6	_	±2.0	μА
state current	IOZB	B1 = 0 to 3	3.6 V	1.1 to 2.7	1.00 to 0.0		12.0	μΛ
Input leakage current	I _{IN}	$V_{IN}=0$ to	3.6 V	1.1 to 2.7	1.65 to 3.6	_	±1.0	μΑ
	I _{OFF1}	V_{IN} , $B1 = 0$	0 to 3.6 V	0	0	_	2.0	
Power-off leakage current	I _{OFF2}	OE = V _{CC}	A	1.1 to 2.7	0	_	2.0	μΑ
	I _{OFF3}	A1, B1 = 0	to 3.6 V	1.1 to 2.7	Open	_	2.0	
	I _{CCA}	$V_{IN} = V_{CC}$	A or GND	1.1 to 2.7	1.65 to 3.6	_	2.0	
Outpoont supply	I _{CCB}	$V_{IN} = V_{CC}$	A or GND	1.1 to 2.7	1.65 to 3.6	_	2.0	
Quiescent supply current	I _{CCA}	$V_{CCA} < V_{I}$	N ≤ 3.6 V	1.1 to 2.7	1.65 to 3.6	_	±2.0	μΑ
	I _{CCB}	$V_{IN} = V_{CC}$ $V_{CCB} \le B1$		1.1 to 2.7	1.65 to 3.6	_	±2.0	

AC Characteristics (Ta = -40 to 85°C, Input: $t_r = t_f = 2.0$ ns)

$\mbox{V}_{\mbox{CCA}} = 2.5 \pm 0.2 \mbox{ V, V}_{\mbox{CCB}} = 3.3 \pm 0.3 \mbox{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	6.8	
3-state output enable time $(\overline{OE} \rightarrow B1)$	t _{pZL}	Figure 1, Figure 3	1.0	8.7	ns
3-state output disable time $(\ \overline{OE} \ \to B1)$	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	3.9	

$V_{CCA} = 1.8 \pm 0.15$ V, $V_{CCB} = 3.3 \pm 0.3$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH}	Figure 1, Figure 2	1.0	7.8	
3-state output enable time $(\overline{OE} \to B1)$	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	10.7	ns
3-state output disable time (OE → B1)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	5.2	

$V_{\mbox{\footnotesize CCA}} = 1.5 \pm 0.1 \mbox{ V}, \, V_{\mbox{\footnotesize CCB}} = 3.3 \pm 0.3 \mbox{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time	t _{pLH}	Figure 1, Figure 2	8.6		
(A1 → B1)	t _{pHL}		1.0	0.0	
3-state output enable time	t _{pZL}	Figure 1 Figure 2	1.0	14.3	ns
$(\overline{OE} \to B1)$	t _p ZH	Figure 1, Figure 3		14.5	115
3-state output disable time	t _{pLZ}	Figure 1 Figure 2	1.0	6.6	
(OE → B1)	t _{pHZ}	Figure 1, Figure 3		6.6	

$\mbox{V}_{\mbox{CCA}} = 1.2 \pm 0.1 \mbox{ V}, \mbox{V}_{\mbox{CCB}} = 3.3 \pm 0.3 \mbox{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	22	
3-state output enable time $(\ \overline{OE} \ \to B1)$	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	52	ns
3-state output disable time (OE → B1)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	18	



$V_{CCA} = 1.8 \pm 0.15$ V, $V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (A1 → B1)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	9.5	
3-state output enable time (OE → B1)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	12.6	ns
3-state output disable time (OE → B1)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	5.1	

$V_{CCA} = 1.5 \pm 0.1 \text{ V}, V_{CCB} = 2.5 \pm 0.2 \text{ V}$

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.0	10.5	
3-state output enable time (OE → B1)	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	15.4	ns
3-state output disable time $(\ \overline{OE} \ \to B1)$	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	6.4	

$V_{CCA} = 1.2 \pm 0.1$ V, $V_{CCB} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH}	Figure 1, Figure 2	1.0	23	
3-state output enable time $(\overline{OE} \to B1)$	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.0	54	ns
3-state output disable time $(\ \overline{\rm OE} \ \to \rm B1)$	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	17	

$V_{CCA} = 1.2 \pm 0.1$ V, $V_{CCB} = 1.8 \pm 0.15$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time $(A1 \rightarrow B1)$	t _{pLH}	Figure 1, Figure 2	1.0	30	
3-state output enable time (OE → B1)	t _{pZL}	Figure 1, Figure 3	1.0	55	ns
3-state output disable time (OE → B1)	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.0	17	

Capacitive Characteristics (Ta=25°C)

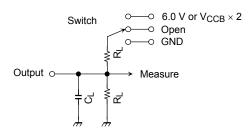
Characteristics	S.v	Symbol	Test Condition			Тур.	Unit
Griaracteristics		Syllibol	rest Gondinon	V _{CCA} (V)	V _{CCB} (V)		
Input capacitance		CIN	ŌE, A1	2.5	3.3	7	pF
Output capacitance		C _{OUT}	B1	2.5	3.3	8	pF
Power dissipation capacitance	(Note) C _{PDB}	C _{PDA}	OE ="L"	2.5	3.3	3	- - pF
			OE ="H"	2.5	3.3	0	
		C===	OE ="L"	2.5	3.3	13	
		OE ="H"	2.5	3.3	0		

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 (per bit)$

AC Test Circuit



Parameter	Switch		
t _{pLH} , t _{pHL}	Open		
	6.0 V @ V _{CCB} =3.3±0.3V		
t_{pLZ},t_{pZL}	V _{CCB} × 2 @ V _{CCB} =2.5±0.2V		
	@ V _{CCB} =1.8±0.15V		
t _{pHZ} , t _{pZH}	GND		

Symbol	V _{CC} (output)		
	3.3 ± 0.3 V 2.5 ± 0.2 V	1.8 ± 0.15 V	
R_{L}	500 Ω	1 kΩ	
CL	30 pF	30 pF	

Figure 1

AC Waveform

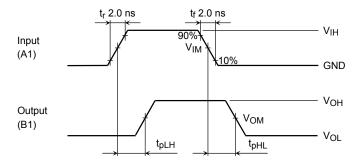


Figure 2 tpLH, tpHL

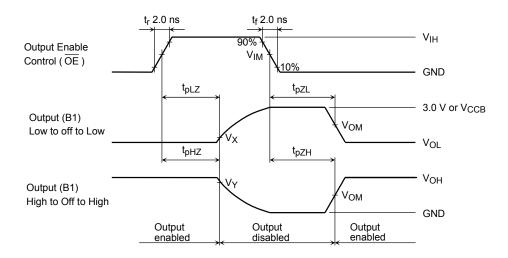
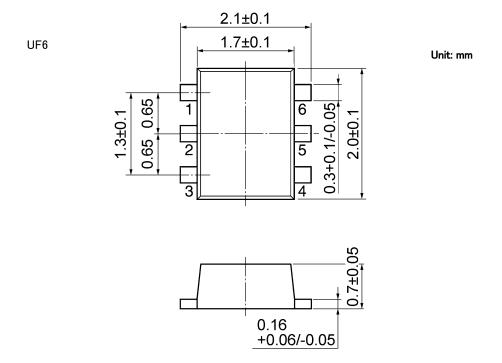


Figure 3 $t_{\text{pLZ}},\,t_{\text{pHZ}},\,t_{\text{pZL}},\,t_{\text{pZH}}$

		V _{CCA} , V _{CCB}				
Symbol		3.3 ± 0.3 V	$2.5\pm0.2~\textrm{V}$	1.5 ± 0.1 V		
		3.3 ± 0.3 V	$1.8\pm0.15~\textrm{V}$	$1.2\pm0.1~\textrm{V}$		
Input	VIH	-	Vcca	VCCA		
	V _{IM}	-	V _{CCA} / 2	V _{CCA} / 2		
Output	V _{OM}	V _{OH} / 2	V _{OH} / 2	-		
	VX	V _{OL} + 0.3 V	V _{OH} + 0.15 V	-		
	VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	=		

8 2008-04-09

Package Dimensions



weight: 0.007 g (typ.)

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20070701-EN GENERAL

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