4:1 ATM MULTIPLEXER/DEMULTIPLEXER

IDT77310
PRELIMINARY

FEATURES

- **TableFull-duplex 4:1 ATM cell mux/demux**
- **High speed, up to 800-Mb/s transfer rate**
- **18-Kbit FIFO buffering on chip**
- **Expandable up to 31-to-1 mux/demux**
- **Variable cell length for routing tag insertion**
- **Byte- and word-width UTOPIA data ports**
- **Generic microprocessor interface for configuration, testing, network management**
- **Loopback test modes for network/system verification**
- **JTAG port for boundary-scan testing**
- **Advanced low-power CMOS technology**
- **Space-saving 208-pin QFP package**
- **5V power supply**
- **–40°C to 85°C operating temperature**

FUNCTIONAL DESCRIPTION

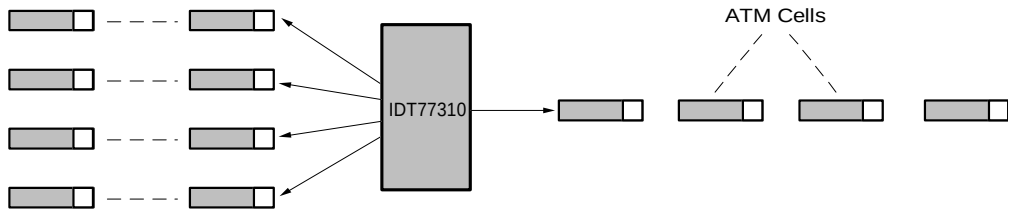
The IDT77310 is a full-duplex high-speed 4:1 ATM cell multiplexer/demultiplexer with built-in FIFO buffering. It provides five industry-standard UTOPIA ports to connect to a variety of physical-layer and adaptation-layer devices. Four full-duplex ATM data streams of up to 200Mb/s can be multiplexed/demultiplexed into one data stream of up to 800Mb/s. Up to eight IDT77310's can be connected in parallel to make wider multiplexer/demultiplexers, up to 31:1. (Note: Port address 11111b is used in the system for bus arbitration, and thus is unavailable as a port address.)

The IDT77310 (see Figure 1) can be used as an inexpensive concentrator or fanout expander to combine multiple low- to medium-speed ATM cell streams into higher-speed streams. This allows various ATM data rates to be efficiently mixed and matched within the same local switch fabric. The part can also be used as a building block for low-cost non-blocking crosspoint switches. (See **APPLICATION EXAMPLES**.)

Each IDT77310 has five ATM UTOPIA interface ports. Ports A, B, C, and D are byte-wide UTOPIA Level 1 ports while Port W is a programmable byte- or word-wide UTOPIA Level 2–compatible port. Data parity bit transfers are also supported, one parity bit for each byte if bit 6 of the configuration register is set to “0”, or one parity per word if bit 6 is set to “1”.

ATM cells are multiplexed from Ports A, B, C, D to Port W and demultiplexed from Port W to Ports A, B, C, D. Port W operates at bus cycle speeds up to 50MHz, while Ports A, B, C, D run at half the Port W cycle rate, 25MHz maximum. Transmit and receive clocks for Ports A, B, C, D are generated internally by dividing down the transmit and receive clocks of Port W (see Figure 2).

FIGURE 1. IDT77310 CONCENTRATOR, FOUR ATM CELL STREAMS INTO ONE



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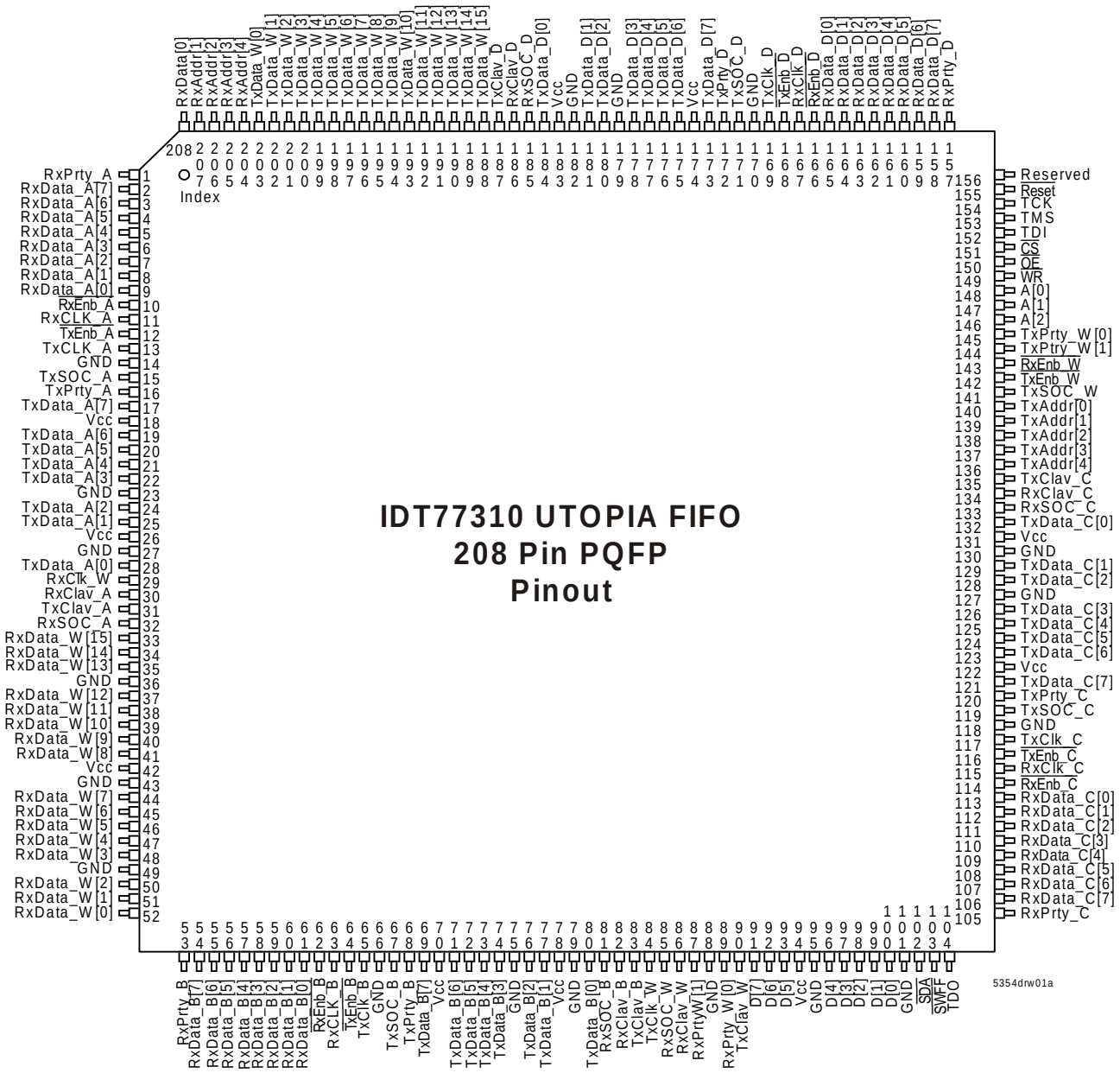
PIN CONFIGURATION



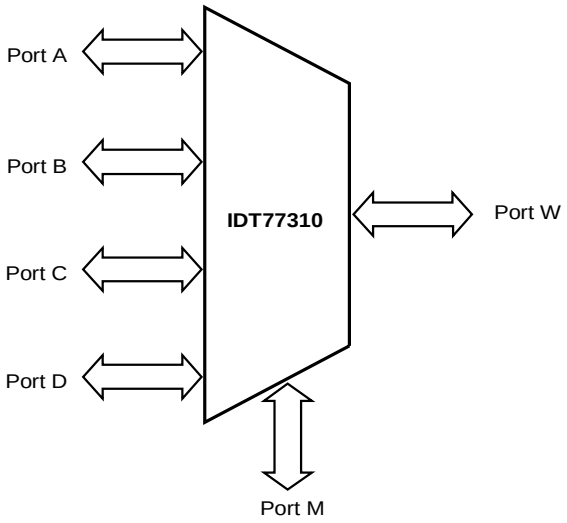
The IDT77310 provides individual byte/word conversion and transmit/receive FIFO buffering of up to four cells in each direction for each of the 8-bit ports to reconcile data-width and data-rate differences between the two sides of the device. Controls for 4-to-1 multiplexing of receive data and 1-to-4 demultiplexing of transmit data are accomplished by port address polling as described in the UTOPIA interface standard. The device supports cell-level flow control as specified in UTOPIA.

The IDT77310 supports standard ATM cell sizes of 53 bytes. In addition, the cell sizes can be programmed from 48 to 64 bytes to support insertion/deletion of routing tags (as shown is Table 5).

The IDT77310 has six internal registers for port addresses, device configuration, status, and loopback control. These registers are accessed through a processor interface port, using generic I/O or memory access signals. The processor interface port (Port M) has the capability of transmitting/receiving data in ATM cell format from Port W (see Figure 2). This feature provides a convenient way of relaying interprocessor messages or other system management information.

The IDT77310 supports loopback mode at all five UTOPIA interface ports; loopback among Ports A, B, C, D; and loopback between the processor interface port and any of the Ports A, B, C, D. The multitude of loopback modes enable various system checkout and creative applications. The IDT77310 also supports board-level device operational tests with its built-in JTAG boundary-scan test capability.

FIGURE 2. IDT77310 FUNCTION SYMBOL



APPLICATION EXAMPLES

The high data-transfer rate and on-chip FIFO buffering of the IDT77310 allow it to be used in a number of different applications within the ATM "fabric," a term used to describe the infrastructure of an ATM network with its switches and transmission lines. Most of the common applications of the part fall into three categories, which are covered in the sections that follow. The categories covered are, respectively: 1) fanout expansion for high-end ATM switching equipment; 2) workgroup switching hub switch element; and 3) transmission line concentrator.

FANOUT EXPANSION FOR ATM SWITCH

The switch core of a high-end ATM switch is typically built up from ASIC or standard-product IC switch elements, such as 4 x 4 crosspoint switch ICs. To maximize the throughput capacity of the switch, very high data transfer rates are sought for the switch core, and consequently the core is fairly expensive to implement. In addition, as the number of ports, N, becomes large, the switch core needed to handle the ports grows as N^2, as shown in the example of a 16 x 16 crosspoint switch made up from 4 x 4 crosspoint chips (16 chips) (see Figure 3). The use of multiplexing/demultiplexing to fan out from the switch core to the ports is an effective way of controlling IC costs while keeping throughput high.

The same type of switch, implemented with the fanout technique shown in Figure 4, requires only one 4 x 4 crosspoint chip and four IDT77310 mux/demux chips, providing the function of 16 of the pricey crosspoint chips for the cost of only four less expensive mux/demux chips. Besides the obvious cost savings of this technique, the mux/demux I/O ring around the periphery of the switch can be implemented on add-in port cards of various types, allowing different protocols and data rates to be mixed and matched in the switch.

LOW-COST ATM SWITCH BUILDING BLOCK

By feeding the output of the multiplexer portion of the IDT77310 back into the demultiplexer portion, and adding some external logic to control the UTOPIA bus and port addressing, the device becomes a switch capable of switching any input port to any output port (see Figure 5). In fact, since the device has FIFO buffers, and Port W of the device has an 800-Mb/s transfer rate, up to 200-Mb/s traffic from each switch port can be handled simultaneously without loss or blocking.

FIGURE 3. A 16 X 16 CROSSPOINT SWITCH MADE UP OF 4 X 4 CROSSPOINT CHIPS REQUIRES 16 CHIPS

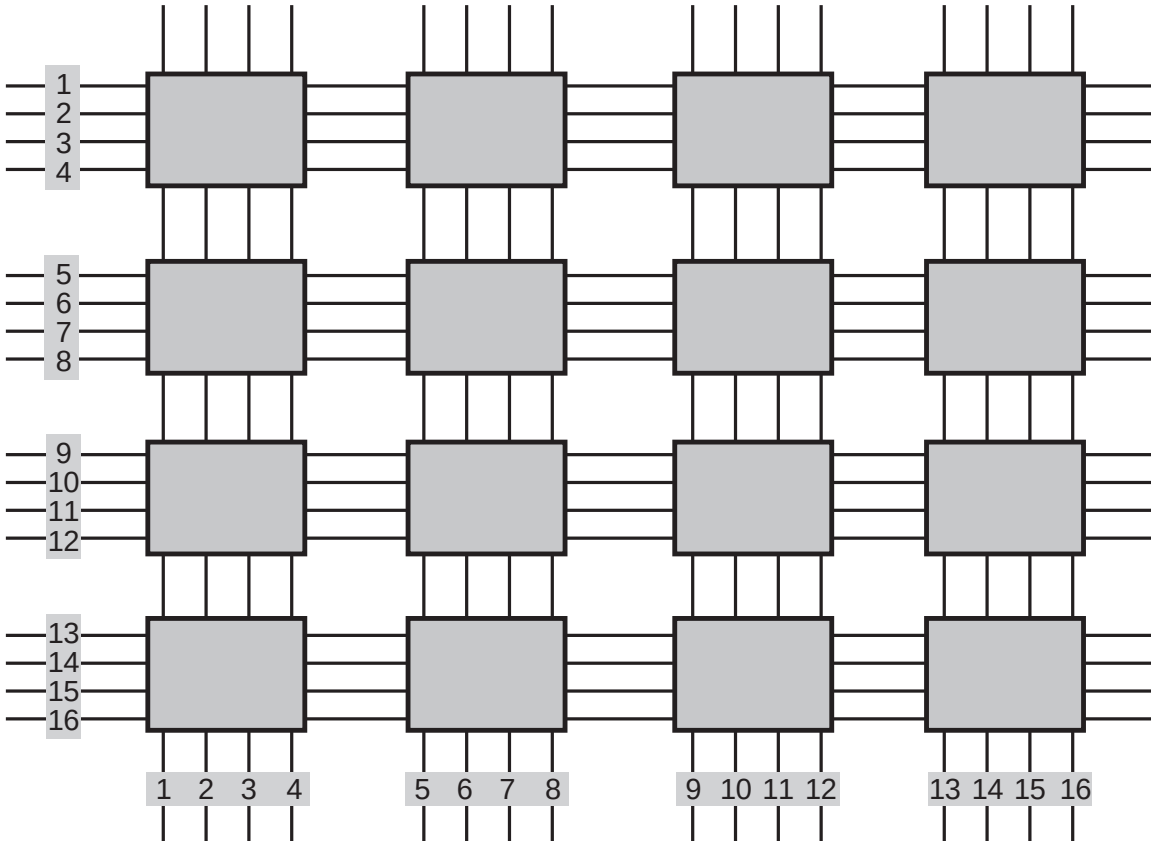


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FIGURE 4. A 16 X 16 CROSSPOINT SWITCH USING MUX/DEMUX FANOUT EXPANSION ON THE PORT CARDS, A FLEXIBLE, COST-SAVING ARCHITECTURE

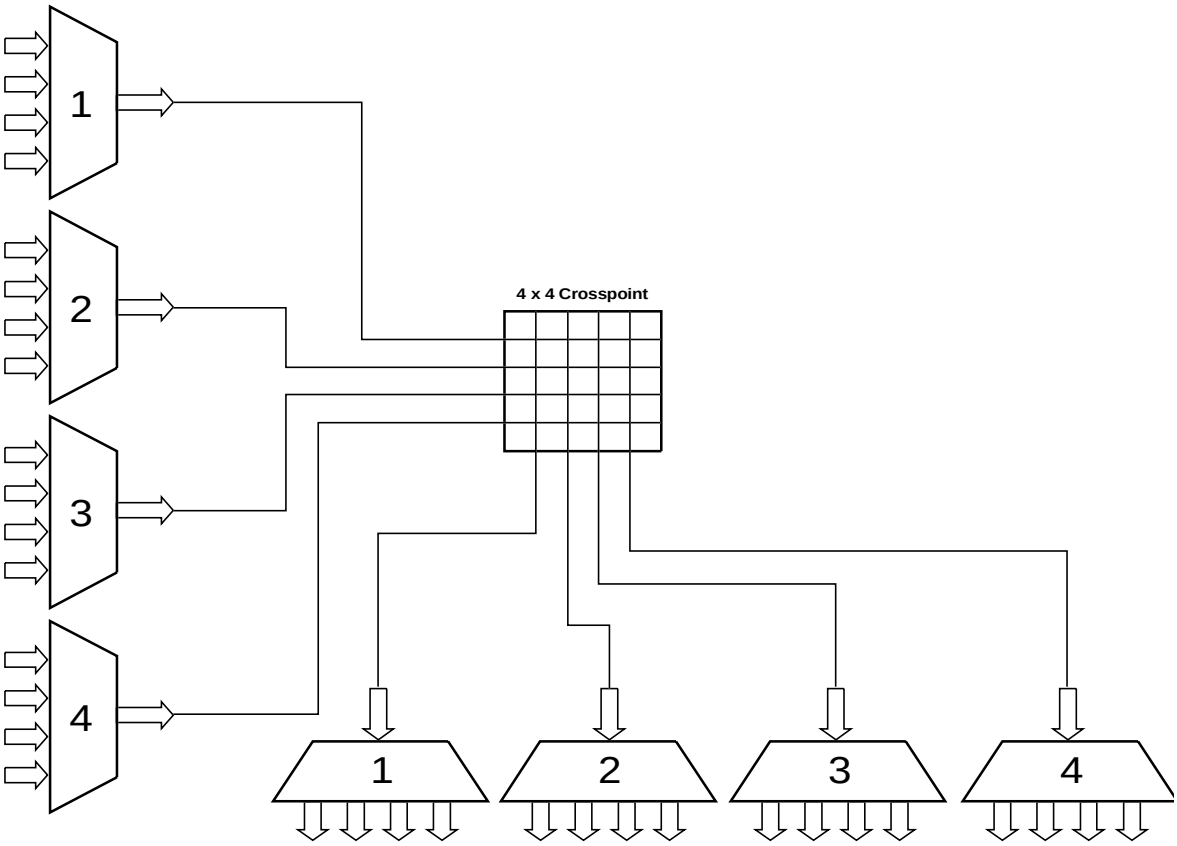

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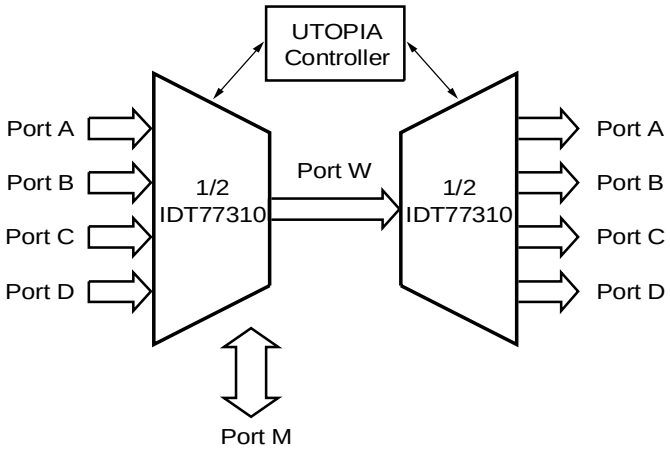
FIGURE 5. IDT77310 USED AS SWITCHING DEVICE WITH UTOPIA CONTROLLER



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Wider multiplexers/demultiplexers can be configured by tying the Port W data lines of several chips together, as shown in Figure 6. Up to eight devices can be paralleled in this way.

With a combination of mux/demux width expansion, a bit of UTOPIA bus controller logic, and (optional) external buffering, the IDT77310 can be used in access equipment, such as the workgroup switch shown in Figures 7 and 8.

FIGURE 6. MULTIPLEXER/DEMULTIPLEXER WIDTH EXPANDED BY PARALLEL CONNECTION OF UP TO EIGHT IDT77310S

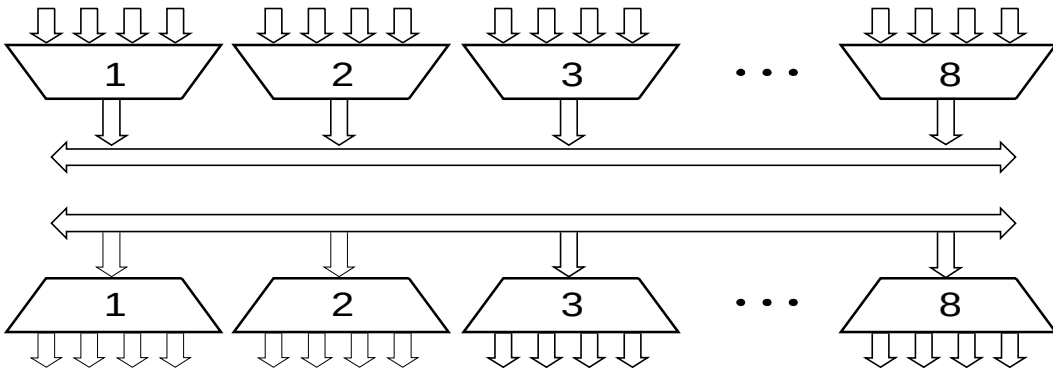

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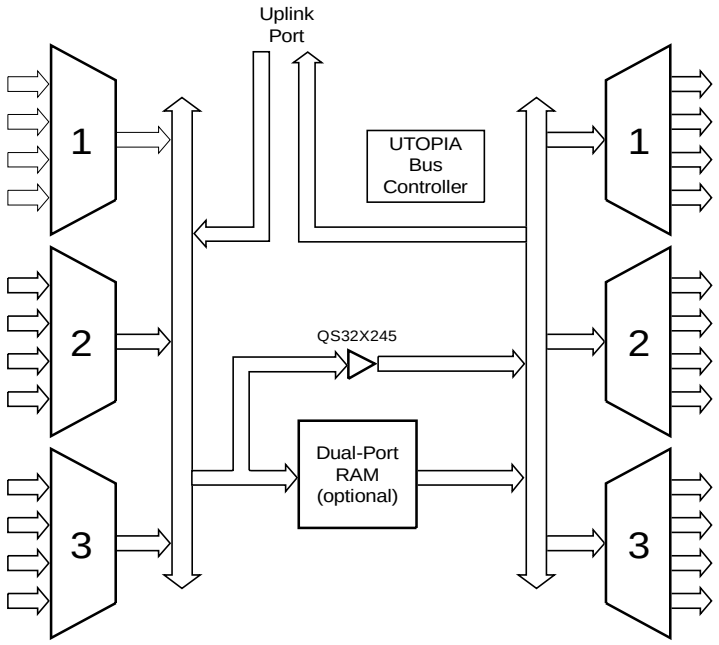
FIGURE 7. IDT77310S USED IN 12-PORT OC1 WORKGROUP SWITCH



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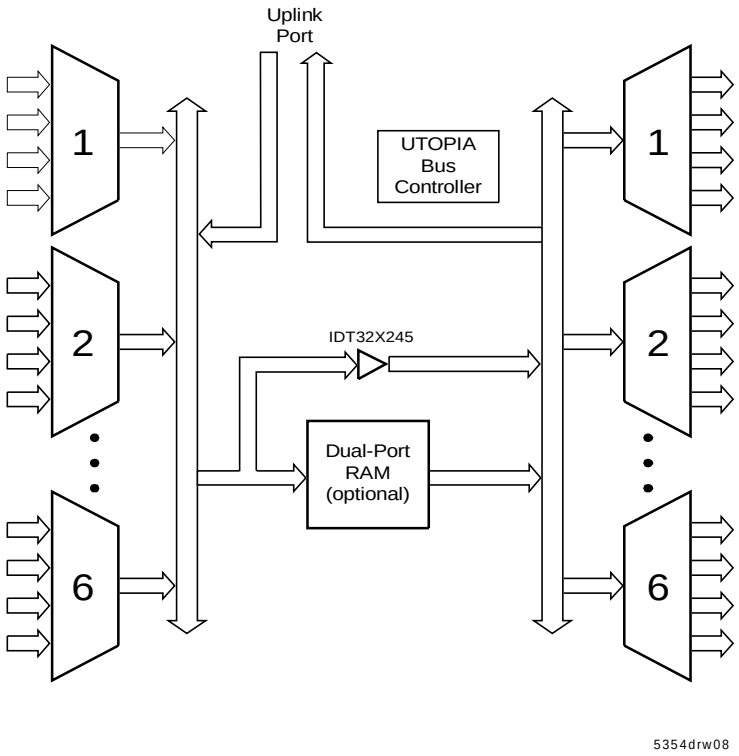
Notes:
1. Provides 12 ports with local switching with 51.84-Mb/s per port full duplex.
2. Connects workgroup of 12 to ATM switch fabric via 622-Mb/s OC12 line (Uplink Port).
3. 51.84-Mb/s bandwidth available for each of 12 ports (OC1-compatible).
4. Input and output FIFO buffering:
   – Inputs: four cells per port.
   – Outputs: four cells per port.
5. QS32X245 QuickSwitch™ isolates in and out high-speed buses (optional).

FIGURE 8. IDT77310S USED IN 24-PORT ATM 25 WORKGROUP SWITCH



Notes:
1. Provides 24 ports with local switching at 25-Mb/s per port full duplex.
2. 25-Mb/s bandwidth available for each of 24 ports (ATM 25-compatible).
3. Connects workgroup to ATM switch fabric via 622-Mb/s OC12 line (Uplink Port).
4. Input and output FIFO buffering.
   – Inputs: four cells per port.
   – Outputs: four cells per port.
5. QS32X245 QuickSwitch isolates in and out buses (optional).

OC3-TO-OC12 LINE CONCENTRATOR

With the addition of SONET Framer and physical layer interface (PHY), the IDT77310 can concentrate 51.84-Mb/s OC1 and 155-Mb/s OC3 lines into 622-Mb/s OC12 lines, as shown in Figures 9 and 10, respectively.

FIGURE 9. 12:1 CONCENTRATOR FOR OC1 LINES

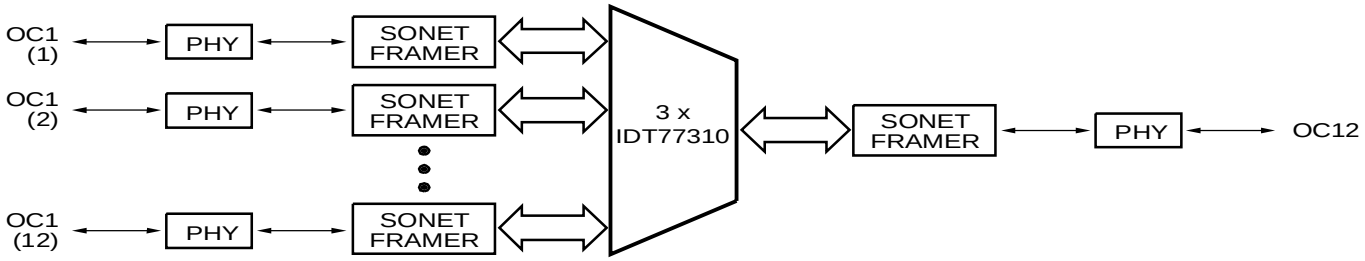


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FIGURE 10. 4:1 CONCENTRATOR FOR OC3 LINES

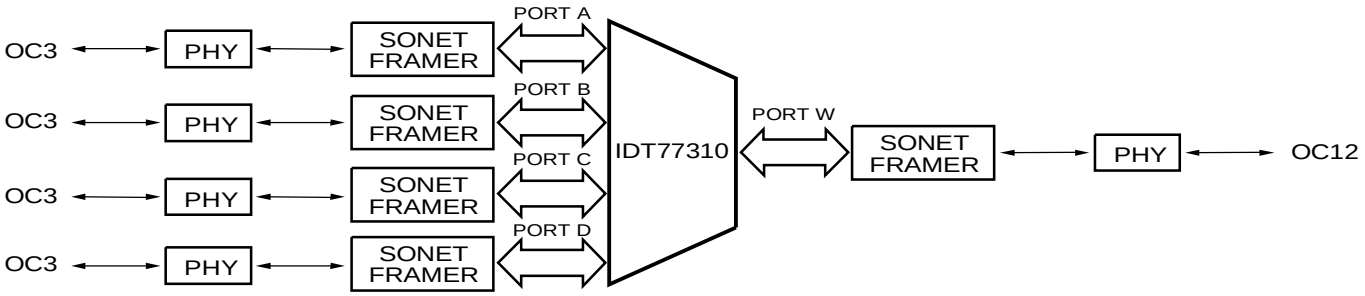

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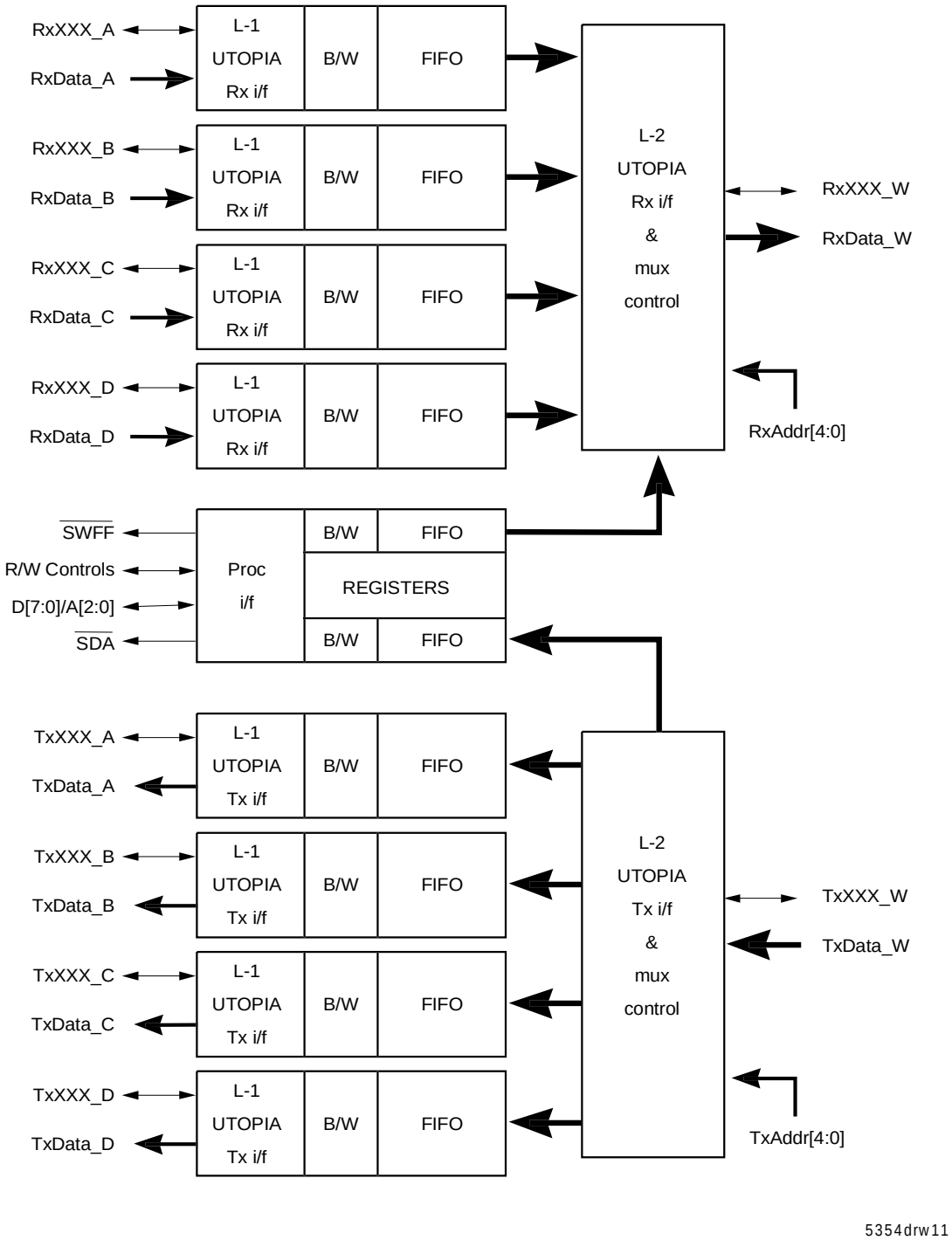
FIGURE 11. IDT77310 FUNCTION BLOCK DIAGRAM



Notes:
- RxXXX = RxClk, RxSOC, RxClav and $\overline{\text{RxEnb}}$; TxXXX = TxClk, TxSOC, TxClav and $\overline{\text{TxEnb}}$.
- RxData_X and TxData_X, X = A, B, C and D are 9 bits wide, including a parity bit. RxData_W and TxData_W are 18 bits wide, including two parity bits, or 9 bits wide including one parity bit.
- R/W controls = $\overline{\text{WR}}$, $\overline{\text{CS}}$ and $\overline{\text{OE}}$.
- B/W = byte-word and word-byte conversions.
- Loopback interrupt flags: $\overline{\text{SWFF}}$ = System Write FIFO Full (insufficient space available in outgoing FIFO for another whole cell); $\overline{\text{SDA}}$ = System Data Available (one or more full cell(s) available in incoming FIFO).

PIN ASSIGNMENTS AND DESCRIPTIONS

The IDT77310 I/O signals are listed in Table 1 in incremental pin number order. Definitions of these signals are presented in Tables 2, 3, and 4, grouped according to function. All signals are active-high signals except those denoted with an overbar. A signal that is tri-stateable is denoted by a dagger (†) in the I/O column.

Table 1. IDT77310 Pin Numbers and Signal Descriptions

Pin#	Signal	I/O	Pin#	Signal	I/O	Pin#	Signal	I/O	Pin#	Signal	I/O
1	RxPrty_A	I	53	RxPrty_B	I	105	RxPrty_C	I	157	RxPrty_D	I
2	RxData_A[7]	I	54	RxData_B[7]	I	106	RxData_C[7]	I	158	RxData_D[7]	I
3	RxData_A[6]	I	55	RxData_B[6]	I	107	RxData_C[6]	I	159	RxData_D[6]	I
4	RxData_A[5]	I	56	RxData_B[5]	I	108	RxData_C[5]	I	160	RxData_D[5]	I
5	RxData_A[4]	I	57	RxData_B[4]	I	109	RxData_C[4]	I	161	RxData_D[4]	I
6	RxData_A[3]	I	58	RxData_B[3]	I	110	RxData_C[3]	I	162	RxData_D[3]	I
7	RxData_A[2]	I	59	RxData_B[2]	I	111	RxData_C[2]	I	163	RxData_D[2]	I
8	RxData_A[1]	I	60	RxData_B[1]	I	112	RxData_C[1]	I	164	RxData_D[1]	I
9	RxData_A[0]	I	61	RxData_B[0]	I	113	RxData_C[0]	I	165	RxData_D[0]	I
10	$\overline{\text{RxEnb\_A}}$	O	62	$\overline{\text{RxEnb\_B}}$	O	114	$\overline{\text{RxEnb\_C}}$	O	166	$\overline{\text{RxEnb\_D}}$	O
11	RxClk_A	O	63	RxClk_B	O	115	RxClk_C	O	167	RxClk_D	O
12	$\overline{\text{TxEnb\_A}}$	O	64	$\overline{\text{TxEnb\_B}}$	O	116	$\overline{\text{TxEnb\_C}}$	O	168	$\overline{\text{TxEnb\_D}}$	O
13	TxClk_A	O	65	TxClk_B	O	117	TxClk_C	O	169	TxClk_D	O
14	GND	I	66	GND	I	118	GND	I	170	GND	I
15	TxSOC_A	O	67	TxSOC_B	O	119	TxSOC_C	O	171	TxSOC_D	O
16	TxPrty_A	O	68	TxPrty_B	O	120	TxPrty_C	O	172	TxPrty_D	O
17	TxData_A[7]	O	69	TxData_B[7]	O	121	TxData_C[7]	O	173	TxData_D[7]	O
18	V_{CC}	I	70	V_{CC}	I	122	V_{CC}	I	174	V_{CC}	I
19	TxData_A[6]	O	71	TxData_B[6]	O	123	TxData_C[6]	O	175	TxData_D[6]	O
20	TxData_A[5]	O	72	TxData_B[5]	O	124	TxData_C[5]	O	176	TxData_D[5]	O
21	TxData_A[4]	O	73	TxData_B[4]	O	125	TxData_C[4]	O	177	TxData_D[4]	O
22	TxData_A[3]	O	74	TxData_B[3]	O	126	TxData_C[3]	O	178	TxData_D[3]	O
23	GND	I	75	GND	I	127	GND	I	179	GND	I
24	TxData_A[2]	O	76	TxData_B[2]	O	128	TxData_C[2]	O	180	TxData_D[2]	O
25	TxData_A[1]	O	77	TxData_B[1]	O	129	TxData_C[1]	O	181	TxData_D[1]	O
26	V_{CC}	I	78	V_{CC}	I	130	GND	I	182	GND	I
27	GND	I	79	GND	I	131	V_{CC}	I	183	V_{CC}	I
28	TxData_A[0]	O	80	TxData_B[0]	O	132	TxData_C[0]	O	184	TxData_D[0]	O
29	RxClk_W	I	81	RxSOC_B	I	133	RxSOC_C	I	185	RxSOC_D	I
30	RxClav_A	I	82	RxClav_B	I	134	RxClav_C	I	186	RxClav_D	I
31	TxClav_A	I	83	TxClav_B	I	135	TxClav_C	I	187	TxClav_D	I
32	RxSOC_A	I	84	TxClk_W	I	136	TxAddr[4]	I	188	TxData_W[15]	I
33	RxData_W[15]	O†	85	RxSOC_W	O†	137	TxAddr[3]	I	189	TxData_W[14]	I
34	RxData_W[14]	O†	86	RxClav_W	O†	138	TxAddr[2]	I	190	TxData_W[13]	I
35	RxData_W[13]	O†	87	RxPrty_W[1]	O†	139	TxAddr[1]	I	191	TxData_W[12]	I
36	GND	I	88	GND	I	140	TxAddr[0]	I	192	TxData_W[11]	I
37	RxData_W[12]	O†	89	RxPrty_W[0]	O†	141	TxSOC_W	I	193	TxData_W[10]	I
38	RxData_W[11]	O†	90	TxClav_W	O†	142	TxEnb_W	I	194	TxData_W[9]	I
39	RxData_W[10]	O†	91	D[7]	I/O	143	RxEnb_W	I	195	TxData_W[8]	I
40	RxData_W[9]	O†	92	D[6]	I/O	144	TxPrty_W[1]	I	196	TxData_W[7]	I
41	RxData_W[8]	O†	93	D[5]	I/O	145	TxPrty_W[0]	I	197	TxData_W[6]	I

(continued)

TABLE 1. IDT77310 PIN NUMBERS AND SIGNAL DESCRIPTIONS (CONTINUED)

Pin #	Signal	I/O	Pin #	Signal	I/O	Pin #	Signal	I/O	Pin #	Signal	I/O
42	V_{CC}	I	94	V_{CC}	I	146	A[2]	I	198	TxData_W[5]	I
43	GND	I	95	GND	I	147	A[1]	I	199	TxData_W[4]	I
44	RxData_W[7]	O†	96	D[4]	I/O	148	A[0]	I	200	TxData_W[3]	I
45	RxData_W[6]	O†	97	D[3]	I/O	149	$\overline{WR}$	I	201	TxData_W[2]	I
46	RxData_W[5]	O†	98	D[2]	I/O	150	$\overline{OE}$	I	202	TxData_W[1]	I
47	RxData_W[4]	O†	99	D[1]	I/O	151	$\overline{CS}$	I	203	TxData_W[0]	I
48	RxData_W[3]	O†	100	D[0]	I/O	152	TDI	I	204	RxAddr[4]	I
49	GND	I	101	GND	I	153	TMS	I	205	RxAddr[3]	I
50	RxData_W[2]	O†	102	$\overline{SDA}$	O	154	TCK	I	206	RxAddr[2]	I
51	RxData_W[1]	O†	103	$\overline{SWFF}$	O	155	$\overline{Reset}$	I	207	RxAddr[1]	I
52	RxData_W[0]	O†	104	TDO	O	156	Reserved	N/C	208	RxAddr[0]	I

TABLE 2. PORTS A, B, C, D DATA TRANSFER INTERFACE

Note: X represents A, B, C, or D.

Name	Pin #	I/O	Description
RxData_X[7-0]	A: 2-9 B: 54-61 C: 106-113 D: 158-165	I	Byte-wide data received into Port X.
RxPrty_X	1, 53, 105, 157	I	Odd parity bit over RxData_X[7–0].
RxSOC_X	32, 81, 133, 185	I	Start of Cell. This signal shows that RxData_X contains first valid byte of a cell.
$\overline{RxEnb\_X}$	10, 62, 114, 166	O	Enable. This signal indicates that RxData_X and RxSOC_X will be sampled at the end of the next clock cycle.
RxClav_X	30, 82, 134, 186	I	Cell Available. Asserted by device connected to Port X to indicate it has a complete cell available for transfer to the IDT77310.
RxClk_X	11, 63, 115, 167	O	Data transfer clock provided by the IDT77310 for synchronizing transfers on RxData_X.
TxData_X[7-0]	A: 17, 19-22 24, 25, 28 B: 69, 71 -74 76, 77, 80 C: 121, 123-126 128, 129, 132 D: 173, 175-178 180, 181, 184	O	Byte-wide data transmitted out of Port X.
TxPrty_X	16, 68, 120, 172	O	Odd parity bit over TxData_X[7–0].
TxSOC_X	15, 67, 119, 171	O	Start Of Cell. Asserted by the IDT77310 when TxData_X contains first valid byte of a cell.
$\overline{TxEnb\_X}$	12, 64, 116, 168	O	Enable. Asserted by the IDT77310 during cycles when TxData_X contains valid cell data.
TxClav_X	31, 83, 135, 187	I	Cell Available. Asserted by device connected to Port X to indicate it can accept the transfer of a complete cell.
TxClk_X	13, 65, 117, 169	O	Data transfer clock provided by the IDT77310 for synchronizing transfers on TxData_X.

TABLE 3. PORT W DATA TRANSFER INTERFACE

Name	Pin #	I/O	Description
RxData_W[15-0]	33-35, 37-41 44-48, 50-52	O†	16-bit received data driven out of IDT77310 Port W. These bits are tri-stated when Port W is not active. When Port W operates in 8-bit mode, the data is transferred in RxData_W[7-0].
RxPrty_W[1-0]	87, 89	O†	RxPrty_W[1] is the odd parity bit for RxData_W[15-8], RxPrty_W[0] is the odd parity bit for RxData_W[7-0]. These two bits are tri-stated when the RxData_W[15-0] are tri-stated. Look for more information on the parity description (Table 18).
RxSOC_W	85	O†	Start Of Cell. Active-high signal asserted by the IDT77310 when RxData_W contains first valid word or byte of a cell. This bit is tri-stated when Port W is not active.
$\overline{\text{RxEnb\_W}}$	143	I	Enable. Active-low input signal indicating that RxData_W and RxSOC_W will be sampled at the end of the next clock cycle.
RxClav_W	86	O†	Cell Available. Asserted by IDT77310 to indicate it has a complete cell available for transfer. This bit is tri-stated whenever RxAddr[4-0] does not match with any port addresses assigned to the device.
RxClk_W	29	I	Data transfer clock input to the IDT77310 for synchronizing transfers on RxData_W and RxPrty_W.
RxAddr[4-0]	204-208	I	Receiving operation polling address set up by system.
TxDATA_W[15-0]	188-203	I	16-bit transmitted data driven into the IDT77310 Port W. When Port W operates in 8-bit mode, the data is transferred in TxData_W[7-0].
TxPrty_W[1-0]	144, 145	I	TxPrty_W[1] is the odd parity bit for TxData_W[15-8]; TxPrty_W[0] is the odd parity bit for TxData_W[7-0]. Look for more information on the parity description (Table 18).
TxSOC_W	141	I	Start Of Cell. Active-high signal indicating the TxData_W contains first valid word of a cell.
$\overline{\text{TxEnb\_W}}$	142	I	Enable. This signal is low during cycles when TxData_W contains valid cell data.
TxClav_W	90	O†	Cell Available. Asserted by the IDT77310 to indicate it can accept the transfer of a complete cell. This bit is tri-stated whenever TxAddr[4-0] does not match the port addresses assigned to the device.
TxClk_W	84	I	Data transfer clock input to the IDT77310 for synchronizing transfers on TxData_W.
TxAddr[4-0]	136-140	I	Transmitting operation polling address set up by system.

TABLE 4. PROCESSOR INTERFACE (PORT M) AND POWER SUPPLY

Name	Pin #	I/O	Description
D[7-0]	91-93, 96-100	I/O	Processor interface data bus.
A[2-0]	146-148	I	Processor interface address bus.
$\overline{WR}$	149	I	Processor interface write enable.
$\overline{OE}$	150	I	Processor interface output enable.
$\overline{CS}$	151	I	Processor interface IDT77310 chip select.
$\overline{SDA}$	102	O	System Data Available. This signal is asserted when a full cell of data is stored into Port M transmitting FIFO from Port W. It is negated when there is only one byte left in the FIFO and a host read operation is initiated. At power on or after system reset the signal is negated.
$\overline{SWFF}$	103	O	System Write FIFO Full. This signal is asserted when there is only one empty location left in the Port M receiving FIFO due to a system write operation and a falling edge of the $\overline{WR}$ signal initiating the last write operation. It is negated when a receiving transfer to Port W creates an empty cell location in the FIFO. At power on or after system reset the signal is negated.
$\overline{Reset}$	155	I	A low on this pin resets the IDT77310 and configures the device to its default setup.
TDI	152	I	JTAG Test Data Input.
TDO	104	O	JTAG Test Data Output.
TMS	153	I	JTAG Test Mode Select.
TCK	154	I	JTAG Test Clock.
Reserved	156		This pin is reserved for factory use only; do not make any connection to this pin.
V_{CC}	18, 26, 42, 70, 78, 94, 122, 131, 174, 183	I	5V power supplies.
GND	14, 23, 27, 36, 43, 49, 66, 75, 79, 88, 95, 101, 118, 127, 130, 170, 179, 182	I	Ground.

OPERATIONAL DESCRIPTION

ARCHITECTURE

There are five UTOPIA ports in the IDT77310: they are designated Port A, Port B, Port C, Port D, and Port W, respectively. Each of the Ports A, B, C, D has a 5-bit system address, which is assigned by the user after power-on reset and system reset. The system address assigned to these ports can be any four consecutive integers in the range from 0 to 30d. Ports A, B, C, D are 8-bit-wide data ports with an optional parity bit, while Port W is a 16-bit-wide data port with two optional parity bits. A 4-cell-deep receiving FIFO and a 4-cell-deep transmitting FIFO are provided to each of the Ports A, B, C, D for data buffering. These FIFOs are 36 bits wide and are connected to Ports A, B, C, D through converting logic.

Data transfers in or out of the IDT77310 are carried out in whole cell units, where one cell equals 48 to 64 data bytes or 24 to 32 data words (dual-byte), as determined by the cell-length register setting. Following the UTOPIA convention, data is said to be transmitted from Port W to Ports A, B, C, D and received from Ports A, B, C, D to Port W. In terms of multiplexing and demultiplexing, data is multiplexed from Ports A, B, C, D to Port W and demultiplexed from Port W to Ports A, B, C, D.

PROCESSOR INTERFACE

Access to IDT77310's internal registers and the two Port M FIFOs is made through the processor interface under the control of A[2-0], $\overline{CS}$, $\overline{WR}$, and $\overline{OE}$. Address assignments for these registers and FIFOs are listed in Figure 12.

FIGURE 12. PROCESSOR INTERFACE REGISTER MAP

A[2:0]	000	001	010	011	100	101	110	111
Access	Port M FIFOs	PAL	PAH	PMA	Configuration	Status	Loopback	Reserved

5354tbl06

Reading and writing of Port M FIFOs with the processor interface is done at byte-level: i.e., every read or write operation does not have to read/write a full cell of 53 bytes.

6.3 INTERNAL REGISTERS

The IDT77310 has six 8-bit wide registers: Port Address Low (PAL) register, Port Address High (PAH) register, Port M Address (PMA) register, Configuration register, Status register, and Loopback register. All these registers, except the Status register, are readable and writeable through the processor interface. The Status register is a read-only register. Timings for reading and writing these registers are shown in Figures 22 and 23.

PORT ADDRESS REGISTERS

Addresses for the IDT77310's 8-bit ports are in ascending order from Port A to Port D. The PAL register holds the lowest address assigned to the IDT77310 ports and is always the address of Port A. The PAH register holds the highest address assigned to the IDT77310 ports and it could be the address of Port A, Port B, Port C, or Port D. If the difference between PAL and PAH is less than 3, one or more of the IDT77310's ports are not accessible. This feature can be used to configure the IDT77310 as a 2:1, 3:1, or 4:1 multiplexer/demultiplexer. If PAH is lower than PAL, the IDT77310 will not function. If PAH is higher than PAL by more than 3, undefined states may exist and the IDT77310 will function unpredictably. Only bit 0 through bit 4 are used in these two registers as shown in Figure 13, the others being reserved. After power-on reset or system reset, the two registers are set to "0"; the user is required to program them with appropriate addresses before the IDT77310 will function properly.

FIGURE 13. PAH AND PAL REGISTERS

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Resvered	Resvered	Reserved	XA4	XA3	XA2	XA1	XA0

5354tbl07

Note:
Bits 5-7 are reserved for possible future use. Always write 0s to these bits.

Port M Address Register

The IDT77310 has an 8-bit-wide system microprocessor interface for reading/writing its internal registers. In addition, the processor interface is equipped with two 2-cell-deep FIFOs and data converting logic to give it the capability to send and receive data from Port W. This enables the system processor to do interprocessor or system information relay through Port W and ATM switches. The processor interface port is identified as Port M and, like Ports A, B, C, D, a system address must be assigned to Port M to allow it to transmit and receive data from Port W and other ports in the device. Bit 4 to bit 0 of Port M Address (PMA) register hold the address assigned to Port M.

Bit 7 to bit 5 of this register are used to select the cell length when bit 5 of the Configuration Register is set to 1. Refer to the Configuration Register section for more information on this usage.

The format of Port M Address register is shown in Figure 14. The register bits are set to "0" after reset and must be programmed for proper function.

FIGURE 14. PMA REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CL2	CL1	CL0	MA4	MA3	MA2	MA1	MA0

5354tbl08

CONFIGURATION REGISTER

The Configuration Register holds information that controls the device's configuration (see Figure 15). This information is defined and described in the notes to the figure. Bits 6-7 are reserved.

FIGURE 15. CONFIGURATION REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UC	WP/BP	VCL	PW8	SP	FS	RFM	WFM

5354tbl09

Notes:

WFM Write Flag Mask. Setting this bit to "1" prevents assertion of processor interface's $\overline{SWFF}$ output signal. Default is "0".

RFM Read Flag Mask. Setting this bit to "1" prevents assertion of processor interface's $\overline{SDA}$ output signal. Default is "0".

FS FIFO Size select. Setting this bit to "1" reduces the size of Ports A, B, C, D's transmitting and receiving FIFOs to 2 cells each. Default is "0", which makes each of these FIFOs 4 cells deep. This bit does not affect the size of Port M's FIFOs, which is fixed at 2 cells each for transmit and receive.

SP Signal Polarity. Setting this bit to "1" forces the RxSOC_W, RxClav_W, TxClav_W, and TxSOC_W to become active low signals. In default this bit is "0" and the four signals are active high signals.

PW8 8-bit Port W. Setting this bit to "1" changes the transferred data width at Port W from 16-bit to 8-bit. Default is "0" which specifies a 16-bit data width at Port W. In the 8-bit mode, Port W data is transferred in TxData_W[7-0] and RxData_W[7-0] as it is, without the addition of UDF2 byte in a receiving operation or removing of UDF2 byte in a transmitting operation. Maximum frequency of Tx/RxClk_W and Tx/RxClk_X remains to be 50MHz and 25MHz respectively in the 8-bit Port W mode.

VCL Variable Cell Length. Setting this bit to "1" changes the length of a cell used in the IDT77310 operation from the standard 53 bytes (in 8-bit mode) or 27 words (in 16-bit mode) to a length defined by bit 7 to bit 5 of the PMA register. Default of this bit is "0," which specifies a cell length of the standard 53 bytes or 27 words. In the default situation, the bit settings in bit 7 to bit 5 of the PMA register are ignored.

When the cell length is larger than 53 bytes, the additional bytes are to be placed at the front end of a standard ATM cell and before the ATM cell. When Port W is in word-wide mode, insertion and deletion of UDF2 bytes for odd-length cells will be carried out at the sixth byte of the standard ATM cell, the same as when a standard ATM cell is transferred. When the cell length is even, 48 or 64 bytes, no UDF2 byte insertion or deletion is performed.

BP/WP Bit Parity/Word Parity: When bit 6 is set to "0" (Default), the one parity bit per byte mode is selected. When it is set to "1", the one parity bit per word mode is selected. For a detailed description, see the parity description (Table 18).

UC Utopia Compliant: When bit 7 is set to "0" (Default), the IDT77310 is in the UTOPIA compliant mode:

1st clock → RxClav_X
2nd clock ← RxEnb_X
3rd clock → RxSoc_X

When bit 7 is set to "1", RxSoc_X can respond immediately on RxEnb_X going low:

1st clock → RxClav_X
2nd clock ← RxEnb_X
2nd clock → RxSoc_X

Definition of cell length is shown in Table 5 when the VCL bit is set to "1".

TABLE 5. CELL LENGTHS WHEN VCL BIT IS SET TO "1"

PMA			PW8 = "0"		PW8 = "1"	
Bit 7	Bit 6	Bit 5	Port X (8-bit)	Port W (16-bit)	Port X (8-bit)	Port W (8-bit)
0	0	0	53 bytes	27 words	53 bytes	53 bytes
0	0	1	55 bytes	28 words	55 bytes	55 bytes
0	1	0	57 bytes	29 words	57 bytes	57 bytes
0	1	1	59 bytes	30 words	59 bytes	59 bytes
1	0	0	61 bytes	31 words	61 bytes	61 bytes
1	0	1	63 bytes	32 words	63 bytes	63 bytes
1	1	0	64 bytes	32 words	64 bytes	64 bytes
1	1	1	48 bytes	24 words	48 bytes	48 bytes

STATUS REGISTER

The Status register holds status information on the two FIFOs in Port M; it is a read-only register. The register's bit definitions are shown in Figure 16. $\overline{SWFF}$ and $\overline{SDA}$ read the inverse binary value of pins 103 and 102, respectively (see pin descriptions). Bits 7-2 are reserved for possible future use.

FIGURE 16. STATUS REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	$\overline{SWFF}$	$\overline{SDA}$

5354tbl10

Notes:

$\overline{SWFF}$ System Write FIFO Full flag. This bit has the same definition as the output pin of the same name. This bit is set to "0" when the Port M receiving FIFO is full from a system write operation and it remains so until one full cell is transferred out of the FIFO. The bit is then set to "1". Default of this bit is "1".

$\overline{SDA}$ System Data Available flag. This bit has the same definition as the output pin of the same name. This bit is set to "0" after the first full cell is stored into the Port M transmitting FIFO and it remains so until the last byte in the FIFO is being retrieved by the system processor. The bit is then set to "1". Default of this bit is "1".

Res Reserved bits (2-7). Always write 0s to these bits.

LOOPBACK REGISTER

The Loopback Register is used to configure system loopback operations (see Figure 17). Bit definition of the loopback register is as shown in Table 6.

FIGURE 17. LOOPBACK REGISTER

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode		Input Port			Output Port		

5354tbl11

TABLE 6. LOOPBACK REGISTER DEFINITIONS

a. Bits 7-6: Mode		
B7	**B6**	**Mode**
0	0	Normal operation (default)
0	1	Port W loopback
1	0	Port X loopback
1	1	Undefined

b. Bits 5-3: Port X Loopback Input Port Select			
B5	**B4**	**B3**	**Input Port**
0	0	0	Port A (default)
0	0	1	Port B
0	1	0	Port C
0	1	1	Port D
1	0	0	Port M
1	0	1	Undefined
1	1	0	Undefined
1	1	1	Undefined

c. Bits 2-0: Port X Loopback Output Port Select			
B2	**B1**	**B0**	**Output Port**
0	0	0	Port A (default)
0	0	1	Port B
0	1	0	Port C
0	1	1	Port D
1	0	0	Port M
1	0	1	Undefined
1	1	0	Undefined
1	1	1	Undefined

The IDT77310 supports two types of loopback:

- Port W loopback — In this mode, data is written into IDT77310 via TxData_W and directly read back from RxData_W. The data is not routed through any port FIFO. The IDT77310 negates all $\overline{\text{TxEnb\_X}}$ and $\overline{\text{RxEnb\_X}}$ lines and the $\overline{\text{SDA}}$ line and asserts the $\overline{\text{SWFF}}$ line during the Port W loopback operation.

- Port X loopback — In this mode, cell-level data is written into a selected input port's (Ports A, B, C, D or Port M) receiving FIFO through the port's RxData bus or processor interface's data bus. Data is then routed through the selected output port's transmitting FIFO before being read back from the port's TxData bus or the processor interface's data bus. The input port and output port in this loopback configuration can be of the same or different port, however *a loopback configuration that has both input and output ports set for Port M is not supported. The IDT77310 negates TxClav_W and RxClav_W during the Port X loopback operation. It also negates $\overline{\text{TxEnb\_X}}$ and $\overline{\text{RxEnb\_X}}$ of those ports not involved in the loopback and, depending on whether or not Port M is involved in the loopback, negates the $\overline{\text{SDA}}$ and asserts $\overline{\text{SWFF}}$ as appropriate.*

The IDT77310 is set into a loopback test mode by writing the loopback register's mode bits 7-6 with a loopback-select code. Only one loopback operation is allowed at a time. All ports not configured for loopback will be kept idle. During Port X Loopback, although Port W is idle, TxClk_W and RxClk_W must be active for sourcing TxClk_X and RxClk_X, respectively. The loopback function will not affect the port address registers and the configuration register's settings. Internal registers remain accessible as long as Port M is not configured for a loopback operation. When a loopback test mode is started:

- All data originally stored in the device becomes invalid; all FIFOs inside the device will be flushed, resulting in the $\overline{\text{SDA}}$ and the $\overline{\text{SWFF}}$ status bits being set to their defaults.

- The TxAddr[4-0] and RxAddr[4-0] inputs will be ignored. Loopback input and output ports are selected through the loopback register's bits 5-3 and having bits 2-0 in the Port X Loopback mode.

- Actual loopback data transfer should not be started until five clock cycles, either Tx/RxClk_W or Tx/RxClk_X cycles, after entering a loopback mode, to allow time for setup of initial internal conditions.

To maintain data synchronization in a Port W loopback operation the TxClk_W must be at the same frequency as the RxClk_W. After the Port W loopback is set up:

1. The IDT77310 asserts both TxClav_W and RxClav_W and holds them asserted during the loopback test. The IDT77310 also negates all the $\overline{\text{TxEnb\_X}}$, $\overline{\text{RxEnb\_X}}$, and $\overline{\text{SDA}}$ lines and asserts $\overline{\text{SWFF}}$ to prevent Ports A, B, C, D and Port M from becoming active.

2. To start the loopback operation the ATM Layer device or other device connected to Port W should assert the $\overline{\text{RxEnb\_W}}$ signal before, or no later than, it asserts the $\overline{\text{TxEnb\_W}}$ and TxSOC_W. $\overline{\text{RxEnb\_W}}$ should stay asserted during the loopback, whereas $\overline{\text{TxEnb\_W}}$ can be negated and then asserted again to control data flow. TxSOC_W should be always used to indicate the first word of a cell transfer.

3. The IDT77310 will route the incoming data on the TxData_W lines to the RxData_W lines and will assert RxSOC_W when the first word of a cell appears at RxData_W lines.

A timing diagram of the loopback operation is shown in Figure 25.

POWER-ON INITIALIZATION AND RESET

After receiving a power-on reset or a system reset input, the IDT77310 sets all the configuration bits and status bits to their defaults, as defined above, and flushes all the FIFOs in the device. It also tri-states all the outputs of Port W, including RxData_W[15-0], RxPrty[1-0], RxSOC_W, RxClav_W, and TxClav_W, and enters into an idle state. After the reset, the user is required to program the device's port address registers with appropriate addresses before the IDT77310 can function properly.

TRANSMITTING OPERATION

When the external device connected to Port W of the IDT77310 starts a transmission, it sets up TxAddr[4-0] to indicate the port of the IDT77310 for which the data is destined. The IDT77310 compares this input with the contents of its PAL, PAH, and PMA registers to determine if the data is for one of its ports. If it is, the IDT77310 then checks the port's transmitting FIFO to see if it has space to store one full cell or not. If the FIFO does not have the space, the IDT77310 will respond with a negated TxClav_W and enter a continuously checking cycle until either the space is available or the TxAddr[4-0] is changed. When the space is available on the selected port, the IDT77310 asserts its TxClav_W signal and keeps it asserted as long as address on the TxAddr[4-0] is unchanged.

Incoming data from Port W, in a word- or byte-width cell format as defined in the UTOPIA standard, is clocked by TxClk_W and gated into the IDT77310, following the UTOPIA protocol, and stored in the designated port's transmitting FIFO. The IDT77310 uses the incoming TxSOC_W and $\overline{\text{TxEnb\_W}}$ signals to identify the beginning and end of a cell, as specified in the UTOPIA interface. Data transmission stops when all data for the designated port is transmitted, or until the designated port's FIFO cannot accept another cell of data.

As soon as one of the Ports A, B, C, D's transmitting FIFO contains a full cell of data, the IDT77310 checks the state of the port's TxClav_X signal. If the signal is asserted, the IDT77310 will assert the $\overline{\text{TxEnb\_X}}$ and start to transfer data out of the FIFO, along with an asserted TxSOC_X signal to identify the first byte of a cell. Data transmission follows the UTOPIA protocols until all cells stored in the FIFO are transmitted or until the external receiving device negates the TxClav_X signal to indicate it can no longer accept another cell of data. In the word-width Port W mode, all data is converted from 18-bit-wide format (including two parity bits) into 9-bit-wide format (including one parity bit) before being sent to the designated port. During this unpacking process, the UDF2 byte, if present (odd-length cells only), is removed from the cell and discarded.

If the transmitted data is destined for Port M's system FIFO, the IDT77310 sets the $\overline{\text{SDA}}$ flag low as soon as a full cell is stored into the FIFO, to indicate there is data in the IDT77310 for the host to retrieve. Data retrieving is under the control of $\overline{\text{CS}}$ and $\overline{\text{OE}}$ signals, as shown in Figure 22. Like the transmit operation with Ports A, B, C, D, data is converted from 18-bit-wide format (including two parity bits) to 9-bit-wide format (including one parity bit) for retrieval if Port W is operating in word-width mode. The UDF2 byte, if present (odd-length cells only), and all the

parity bits, if any, are removed from the cell and discarded. The $\overline{SDA}$ flag remains asserted until all data in the FIFO is retrieved; at that moment the IDT77310 negates the flag to stop further reading from the FIFO. Data retrieval through the processor interface is on a byte level; thus the user is not required to retrieve a complete cell in one reading operation. It is up to the system processor to maintain cell alignment if so desired.

RECEIVING OPERATION

During normal operation the IDT77310 continuously checks for an asserted RxClav_X (X is A, B, C, or D). When one is found and the Port X's receiving FIFO has space for a full cell, it asserts the associated $\overline{RxEnb\_X}$ signal to start a receiving operation. Incoming data, in byte-wide format and clocked by RxClk_X, is transferred into the receiving FIFO, following the UTOPIA protocol. During the process, if Port W is operating in the word-width mode and the cell length in bytes is odd, the fifth byte of a cell, the UDF1 byte, is copied and inserted after this byte to become the UDF2 byte of the cell. The $\overline{RxEnb\_X}$ signal will be negated in the middle of the 47th payload byte, as shown in Figure 20, for every cell received, even if the PHY device has more cells to be transferred and its associated IDT77310 FIFO has space to accept them. Since the IDT77310 operates in cell level only, the negation of $\overline{RxEnb\_X}$ in the middle of the 47th payload byte does not constitute the condition of a reduced read window, and the PHY device should continue to finish the transfer of a full cell.

Incoming data for Port M's receiving FIFO is written into the IDT77310 at byte level under the control of $\overline{WR}$ and $\overline{CS}$ signals. Before the data is written into the FIFO, an odd parity bit is generated by the IDT77310 for every data byte and attached to the data byte. Like other ports, if Port W is operating in a word-width mode and the cell length in bytes is odd, the fifth byte of the ATM cell, the UDF1 byte, is copied and inserted after this byte to become the UDF2 byte of the cell. When the FIFO is full, the $\overline{SWFF}$ flag is asserted to stop further writing from the host. Any data written following assertion of the $\overline{SWFF}$ flag will be lost. The flag remains asserted until one cell of data is completely transferred out of the IDT77310 through Port W.

While the receiving operations on Port X and Port M are in process, the IDT77310 compares RxAddr[4-0] inputs with contents of the PAL, PAH and PMA registers to determine if data is requested from one of its ports. If so, the IDT77310 checks the requested port's receiving FIFO to see if it has at least one full cell of data. If not, the IDT77310 negates its RxClav_W and enters a continuously checking cycle until either one cell is available or the RxAddr[4-0] is changed. When a cell is available, the IDT77310 asserts its RxClav_W signal to start a receiving operation at Port W. After Port W receives an asserted $\overline{RxEnb\_W}$ input, the first dual-byte of data will appear at the RxData_W output lines during the next clock cycle. The operation is carried out as specified in the UTOPIA standard until a full cell is transferred.

The RxClav_W output is active only when RxAddr[4-0] is pointing to one of the IDT77310's ports, including Port M. Otherwise it is tri-stated.

OPERATIONAL NOTES

The IDT77310 is designed so that receiving/transmitting operations at Port W are independent of the receiving/transmitting operations at Ports A, B, C, D. Receiving or transmitting operations can be carried out at both sides of the IDT77310 simultaneously and independently.

Furthermore, if transmitted data is longer than one cell, the IDT77310 is capable of starting transmission out of Ports A, B, C, D after one full cell is stored in the port's transmitting FIFO while continuously accepting transmitted data from Port W. Similarly, while receiving a data stream longer than one cell from Ports A, B, C, D or Port M, the IDT77310 is capable of starting a receive transfer at Port W after one full cell is stored in the source port's receiving FIFO.

The receiving/transmitting operations at the IDT77310's Ports A, B, C, D are independent of each other; as a result, receiving/transmitting interface at each of the 8-bit ports can take place at the same time without slowing other operations.

The design of IDT77310 allows multiple address polling during the time $\overline{Tx/RxEnb\_W}$ is asserted and during the time $\overline{Tx/RxEnb\_W}$ is negated, whether or not the IDT77310 answers the polling with an asserted or negated Tx/RxClav_W signal. The port that is actually selected for transmitting or receiving is the port whose address matches the TxAddr or the RxAddr at the falling edge of the Tx/RxEnb_W signal. This allows the system to conduct flexible polling schemes to meet its system requirements.

JTAG TEST PORT

The JTAG test port allows access to the TAP (Test Access Port) controller and the four TAP registers: instruction, bypass, device ID, and boundary scan. This permits the user to read device input logic levels, force device outputs, read the device's ID code and bypass scan path if desired. Refer to IEEE Standard Test Access Port (TAP) and Boundary-Scan Architecture manual for more detailed description of how JTAG works. In the discussion below, it is assumed that the reader is familiar with JTAG architecture and the TAP controller logic.

Table 7 defines the IDT77310 JTAG instruction codes, the instructions, and the register selected. Table 8 shows the boundary-scan register sequence. All "SystemInt1" signals are internal to the device and are provided for reference only. The length of the boundary-scan register is 185 bits. Serial input of data and instruction code is entered from TDI, starting with the LSB.

TABLE 7. INSTRUCTION REGISTER

Instruction Code	Instruction	Selected Register
X00	EXTEST	Boundary Scan
001	SP_PRL	Boundary Scan
010	IDCODE	Identification
X11	BYPASS	Bypass
101	INTEST	Boundary Scan
110	No Operation	N/A

TABLE 8. BOUNDARY-SCAN REGISTER SEQUENCE

1	RxPrty_A	51	RxData_B[1]	101	RxData_C[3]	151	TxClk_D
2	RxData_A[7]	52	RxData_B[0]	102	RxData_C[2]	152	TxSOC_D
3	RxData_A[6]	53	$\overline{\text{RxEnb\_B}}$	103	RxData_C[1]	153	TxPrty_D
4	RxData_A[5]	54	RxClk_B	104	RxData_C[0]	154	TxData_D[7]
5	RxData_A[4]	55	$\overline{\text{TxEnb\_B}}$	105	$\overline{\text{RxEnb\_C}}$	155	TxData_D[6]
6	RxData_A[3]	56	TxClk_B	106	RxClk_C	156	TxData_D[5]
7	RxData_A[2]	57	TxSOC_B	107	TxEnb_C	157	TxData_D[4]
8	RxData_A[1]	58	TxPrty_B	108	TxClk_C	158	TxData_D[3]
9	RxData_A[0]	59	TxData_B[7]	109	TxSOC_C	159	TxData_D[2]
10	$\overline{\text{RxEnb\_A}}$	60	TxData_B[6]	110	TxPrty_C	160	TxData_D[1]
11	RxClk_A	61	TxData_B[5]	111	TxData_C[7]	161	TxData_D[0]
12	$\overline{\text{TxEnb\_A}}$	62	TxData_B[4]	112	TxData_C[6]	162	RxSOC_D
13	TxClk_A	63	TxData_B[3]	113	TxData_C[5]	163	RxClav_D
14	TxSOC_A	64	TxData_B[2]	114	TxData_C[4]	164	TxClav_D
15	TxPrty_A	65	TxData_B[1]	115	TxData_C[3]	165	TxData_W[15]
16	TxData_A[7]	66	TxData_B[0]	116	TxData_C[2]	166	TxData_W[14]
17	TxData_A[6]	67	RxSOC_B	117	TxData_C[1]	167	TxData_W[13]
18	TxData_A[5]	68	RxClav_B	118	TxData_C[0]	168	TxData_W[12]
19	TxData_A[4]	69	TxClav_B	119	RxSOC_C	169	TxData_W[11]
20	TxData_A[3]	70	RxSOC_W	120	RxClav_C	170	TxData_W[10]
21	TxData_A[2]	71	SystemInt1.trirxw _out_clav	121	TxClav_C	171	TxData_W[9]
22	TxData_A[1]	72	RxClav_W	122	TxAddr[4]	172	TxData_W[8]
23	TxData_A[0]	73	RxPrty_W[1]	123	TxAddr[3]	173	TxData_W[7]
24	RxClav_A	74	RxPrty_W[0]	124	TxAddr[2]	174	TxData_W[6]
25	TxClav_A	75	SystemInt1.tritxw _out_clav	125	TxAddr[1]	175	TxData_W[5]
26	RxSOC_A	76	TxClav_W	126	TxAddr[0]	176	TxData_W[4]
27	SystemInt1.tri _state_data	77	SystemInt1.triC	127	TxSOC_Wz	177	TxData_W[3]
28	RxData_W[15]	78	SystemInt1.dw[7]	128	$\overline{\text{TxEnb\_W}}$	178	TxData_W[2]
29	RxData_W[14]	79	SystemInt1.dw[6]	129	$\overline{\text{RxEnb\_W}}$	179	TxData_W[1]
30	RxData_W[13]	80	SystemInt1.dw[5]	130	TxPrty_W[1]	180	TxData_W[0]
31	RxData_W[12]	81	SystemInt1.dw[4]	131	TxPrty_W[0]	181	RxAddr[4]
32	RxData_W[11]	82	SystemInt1.dw[3]	132	A[2]	182	RxAddr[3]
33	RxData_W[10]	83	SystemInt1.dw[2]	133	A[1]	183	RxAddr[2]
34	RxData_W[9]	84	SystemInt1.dw[1]	134	A[0]	184	RxAddr[1]
35	RxData_W[8]	85	SystemInt1.dw[0]	135	$\overline{\text{WR}}$	185	RxAddr[0]
36	RxData_W[7]	86	SystemInt1.dr[7]	136	$\overline{\text{OE}}$		
37	RxData_W[6]	87	SystemInt1.dr[6]	137	$\overline{\text{CS}}$		
38	RxData_W[5]	88	SystemInt1.dr[5]	138	$\overline{\text{RESET}}$		
39	RxData_W[4]	89	SystemInt1.dr[4]	139	RxPrty_D		
40	RxData_W[3]	90	SystemInt1.dr[3]	140	RxData_D[7]		
41	RxData_W[2]	91	SystemInt1.dr[2]	141	RxData_D[6]		
42	RxData_W[1]	92	SystemInt1.dr[1]	142	RxData_D[5]		
43	RxData_W[0]	93	SystemInt1.dr[0]	143	RxData_D[4]		
44	RxPrty_B	94	$\overline{\text{SDA}}$	144	RxData_D[3]		
45	RxData_B[7]	95	$\overline{\text{SWFF}}$	145	RxData_D[2]		
46	RxData_B[6]	96	RxPrty_C	146	RxData_D[1]		
47	RxDta_B[5]	97	RxData_C[7]	147	RxData_D[0]		
48	RxData_B[4]	98	RxData_C[6]	148	$\overline{\text{RxEnb\_D}}$		
49	RxData_B[3]	99	RxData_C[5]	149	RxClk_D		
50	RxData_B[2]	100	RxData_C[4]	150	$\overline{\text{TxEnb\_D}}$		

The following is a description of IDT77310's JTAG instructions. Each instruction selects a proper serial test data register between the TDI and the TDO.

SAMPLE/PRELOAD INSTRUCTION

This instruction places the Boundary-Scan register between TDI and TDO and is a combination of two individual instructions:

Preload—This instruction stores a desired test datum into the Boundary Scan Cells (BSC) prior to the loading of other instruction, such as the Extest instruction. To preload, first enter the SP_PRL instruction and then, when in the Shift_DR state, enter the serial data from the TDI pin. A total of 185 bits of data (with zeros after the valid data if necessary) must be entered to let the LSB of data shift toward the last boundary-scan cell. Once all the data have been shifted properly, each BSC's scan-out pin (SO) should contain the one-bit valid data ready to be transferred according to the proper instruction chosen later.

Sample—This instruction takes a snapshot of the data while the chip is going through a normal operation. With this instruction, data at PI are captured and passed on to the SO of each BSC at the Capture_DR state. The captured values can then be viewed by shifting the Boundary-Scan register using the Shift_DR state.

EXTEST INSTRUCTION

The external test instruction selects the Boundary-Scan register as the data path between TDI and TDO. It allows testing of interconnection between this device and other devices. With the Extest Instruction, a pattern shifted in through a device's TDI can be loaded into PO of the device's out-cell BSC using the Update_DR state. This pattern can then be sampled into the next device's in-cell BSC using the Capture_DR state. The sampled values can then be viewed by shifting the Boundary-Scan register using the Shift_DR state.

INTEST INSTRUCTION

This instruction is used to test the device's on-chip system logic. With this instruction the Boundary-Scan register is connected between TDI and TDO. The POS of in-cell and out-cell BSC are both set to 1 during the Intest instruction, with the result that the only scanning path open for each BSC is from SI to SO, and no data goes into or out of normal parallel in/out pins (PI and PO). During the test, preloaded data at each in-cell BSC's SI is applied to the on-chip system logic using the Update_DR state. After a sequence of clock events, the on-chip system logic's response is routed to the out-cell BSC's SO using the Capture_DR state. The response can then be viewed by shifting the Boundary-Scan register using the Shift_DR state.

When performing the Intest instruction, the input system clocks (RxClk_W and TxClk_W) must be stopped prior to applying the appropriate value to TMS.

BYPASS INSTRUCTION

The Bypass Instruction is used to provide a minimum-length serial path between the TDI and TDO of a device at times when no testing will be done on the device. The instruction places the Bypass register between the TDI and the TDO. Data entered into the TDI is shifted out to TDO with one TCK clock period delay in a Shift_DR state.

ID CODE INSTRUCTION

This instruction connects the Identification register between the TDI and the TDO. The ID register consists of a chain of 32 1-bit ID cells that are hard-wired with the device's ID code. To read the ID code, enter the Shift-DR state and insert "0" (or any dummy value) 32 times. The ID code will be shifted out of TDO for examination. The ID code for the IDT77310 is 168101D3h, or "0001-0110-1000-0001-0000-0001-1101-0011" in binary code.

TABLE 9. ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to 7.0V
DC Output Voltage V_{OUT}	–0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN}	–0.5V to V_{CC} + 0.5V
Maximum Package Power Dissipation	3.5 watts
T_{STG} Storage Temperature	–65° to 165°C
ESD Protection	>2001V

Note: Absolute Maximum Ratings are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

TABLE 10. DC ELECTRICAL CHARACTERISTICS

(Operating Range: T_A = –40°C to 85°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

TABLE 11. POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typical	Max	Unit
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	230	350	mA

TABLE 12. INPUT/OUTPUT CAPACITANCE

Description	Applies to	Max	Unit
Input Capacitance	All input pins	10	pF
Tri-stated Output	All tri-stateable outputs and I/O pins	15	pF

TABLE 13. TRANSMIT SWITCHING CHARACTERISTICS: PORT W

Description	Applies to	Min	Max	Unit
TxClk_W frequency	TxClk_W	—	50	MHz
TxClk_W duty cycle	TxClk_W	40	60	%
Output delay from TxClk_W going high to TxClav_W valid	TxClav_W	2	15	ns
Input setup from signal valid to TxClk_W going high	TxData_W, TxPrty_W, $\overline{\text{TxEnb\_W}}$, TxAddr[4-0], TxSOC_W	5	—	ns
Input hold from TxClk_W going high to signal invalid	TxData_W, TxPrty_W, $\overline{\text{TxEnb\_W}}$, TxAddr[4-0], TxSOC_W	1	—	ns
TxClk_W peak jitter (measured from one rising edge to the next rising edge)	TxClk_W	—	±0.25	ns

TABLE 14. TRANSMIT SWITCHING CHARACTERISTICS: PORTS A, B, C, AND D

Description	Applies to (X = A, B, C, D)	Min	Max	Unit
TxClk_X frequency	TxClk_X	—	25	MHz
TxClk_X duty cycle	TxClk_X	40	60	%
Output delay from TxClk_X going high to signal valid	TxData_X, TxPrty_X, $\overline{\text{TxEnb\_X}}$, TxSOC_X	1	20	ns
Input setup from signal valid to TxClk_W going high	TxClav_X	10	—	ns
Input hold from TxClk_X going high to signal invalid	TxClav_X	1	—	ns

TABLE 15. RECEIVE SWITCHING CHARACTERISTICS: PORT W

Description	Applies to	Min	Max	Unit
RxClk_W frequency	RxClk_W	—	50	MHz
RxClk_W duty cycle	RxClk_W	40	60	%
Output delay from RxClk_W going high to signal valid	RxData_W, RxPrty_W, RxSOC_W	2	14	ns
Output delay from RxClk_W going high to signal valid	RxClav_W	2	15	ns
Input setup from signal valid to RxClk_W going high	$\overline{\text{RxEnb\_W}}$, RxAddr[4-0]	5	—	ns
Input hold from RxClk_W going high to signal invalid	$\overline{\text{RxEnb\_W}}$, RxAddr[4-0]	1	—	ns
RxClk_W peak jitter (measured from one rising edge to the next rising edge)	RxClk_W	—	±0.25	ns

TABLE 16. RECEIVE SWITCHING CHARACTERISTICS: PORTS A, B, C AND D

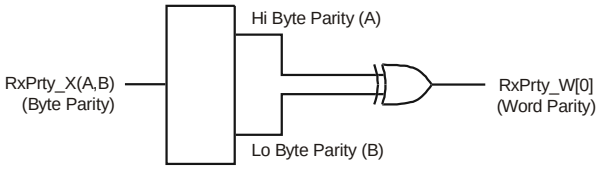
Description	Applies to (X = A, B, C, D)	Min	Max	Unit
RxClk_X frequency	RxClk_X	—	25	MHz
RxClk_X duty cycle	RxClk_X	40	60	%
Output delay from RxClk_X going high to signal valid	$\overline{\text{RxEnb\_X}}$	1	20	ns
Input setup from signal valid to RxClk_X going high	RxData_X, RxPrty_X, RxClav_X, RxSOC_X	10	—	ns
Input hold from RxClk_X going high to signal invalid	RxData_X, RxPrty_X, RxClav_X, RxSOC_X	1	—	ns

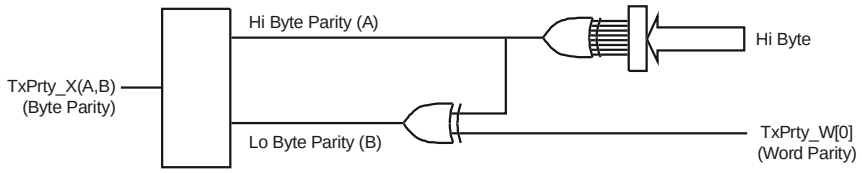
TABLE 17. MICROPROCESSOR PORT SWITCHING CHARACTERISTICS

Symbol	Description	Min	Max	Unit
READ Cycle				
t_{RC}	Read Cycle Time	40	—	ns
t_{AA}	Address Access Time	—	25	ns
t_{ACS}	Chip Select Access Time	—	25	ns
t_{OE}	Output Enable to Data Valid	—	10	ns
t_{OLZ}	Output Enable to Output in Low-Z	2	—	ns
t_{CLZ}	Chip Select to Output in Low-Z	2	—	ns
t_{OHZ}	Output Enable to Output in High-Z	—	10	ns
t_{CHZ}	Chip Select to Output in High-Z	—	10	ns
t_{OW}	Output Enable High and Low Width	15	—	ns
t_{OS}	Output Enable to $\overline{\text{SDA}}$ Negated	20	—	ns
WRITE Cycle				
t_{WC}	Write Cycle Time	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	ns
t_{AS}	Address Setup Time	8	—	ns
t_{CSS}	Chip Select Setup Time	8	—	ns
t_{WW}	Write Pulse High and Low Width	15	—	ns
t_{WR}	Write Recovery Time	5	—	ns
t_{DW}	Data Valid to End of Write	15	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{WS}	Write Enable to $\overline{\text{SWFF}}$ Asserted	20	—	ns
Miscellaneous				
t_{RS}	Reset Pulse Width, VCC and Tx/RxClk_W Stable	100	—	ns
t_{RTC}	Reset Recovery Time to TxClk_W Rising Edge	8	—	ns
t_{RRC}	Reset Recovery Time to RxClk_W Rising Edge	8	—	ns
t_{JCC}	JTAG Test Clock Cycle Time	100	—	ns

TABLE 18. PARITY DESCRIPTION

	PW8 = 0 (16 Bit)		PW8 = 1 (8 Bit)	
	WP/BP[1] = 0	WP/BP = 1	WP/BP = 0	WP/BP = 1
RxPrty_X(In)	A, B[2]	A, B	A, B	Illegal
RxPrty_W_1(Out)	A	A[3]	Don't Care	Illegal
RxPrty_W_0(Out)	B	A **xor** B	A, B	Illegal
TxPrty_X (Out)	A, B	A[4], B[5]	A, B	Illegal
TxPrty_W_1 (In)	A	Don't Care	Don't Care	Illegal
TxPrty_W_0 (In)	B	Word Parity	A, B	Illegal



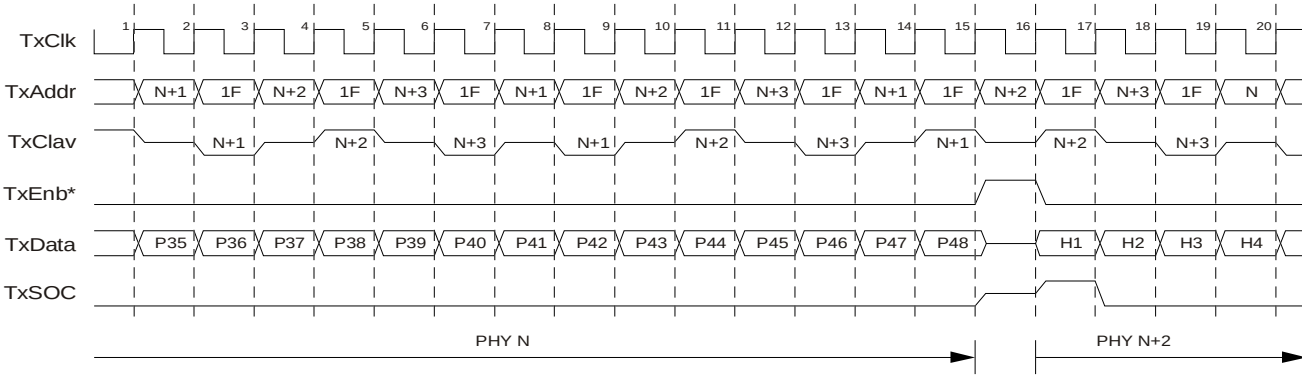


5354drw12

Notes:

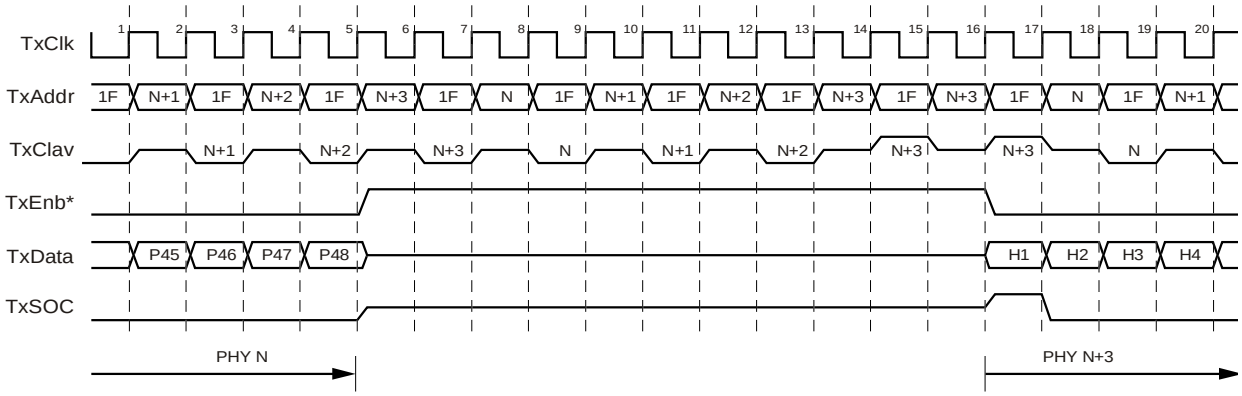
1. WP/BP = Word Parity/Bit Parity, and refers to bit #6 of the Configuration Register. When this bit is set to "0" (Default) the one parity bit per byte mode is selected. When it is set to "1", the one parity bit per word mode is selected
2. A, B indicates two consecutive cycles. A is the parity bit for the most significant byte, B is the parity bit for the second byte.
3. The high parity bit can be checked here if needed.
4. This high byte parity output is calculated internally using the upper 8-bit data.
5. This low byte parity output is the result of (word parity XOR high byte parity).

FIGURE 18A. POLLING PHASE AND SELECTION PHASE AT TRANSMIT INTERFACE TIMING DIAGRAM



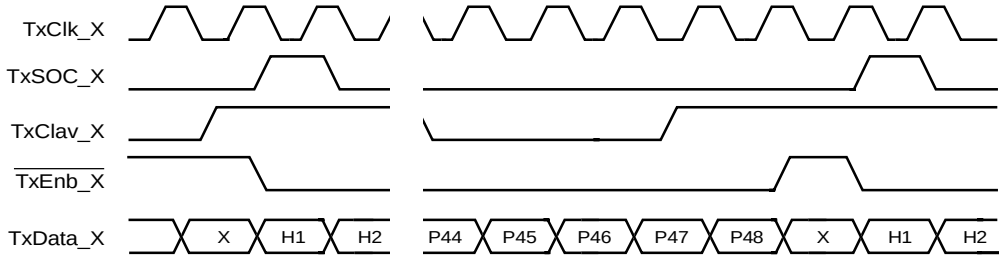
5354drw13

FIGURE 18B. END AND RESTART OF CELL TRANSMISSION AT TRANSMIT INTERFACE TIMING DIAGRAM



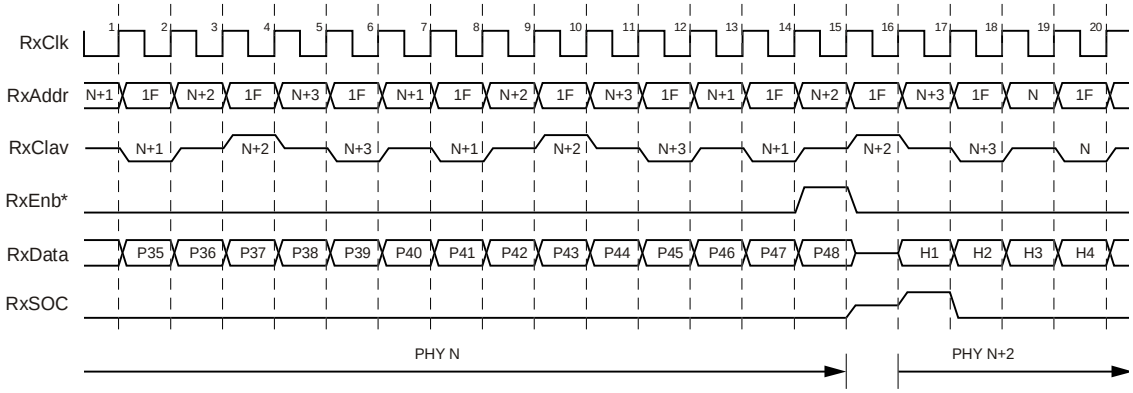
5354drw14

FIGURE 19. PORT A, B, C, OR D TRANSMIT TIMING DIAGRAM



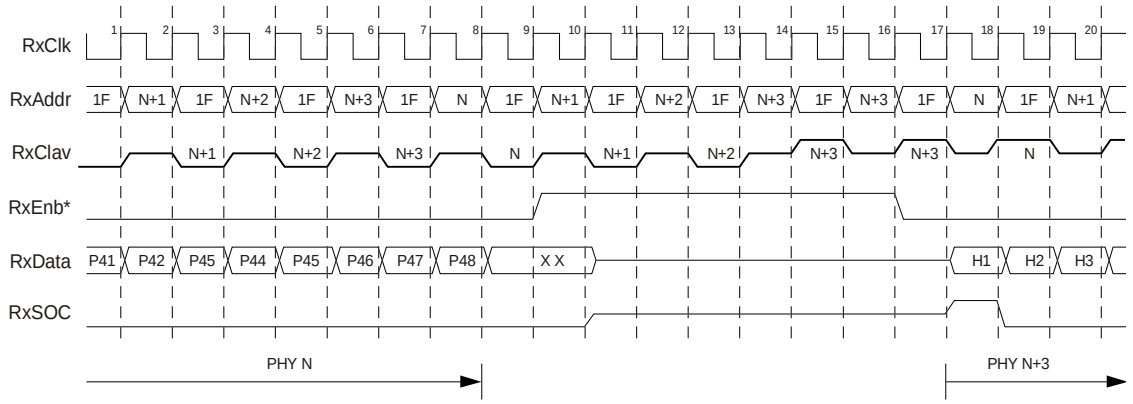
5354drw15

FIGURE 20A. POLLING PHASE AND SELECTION PHASE AT RECEIVE INTERFACE TIMING DIAGRAM



5354drw16

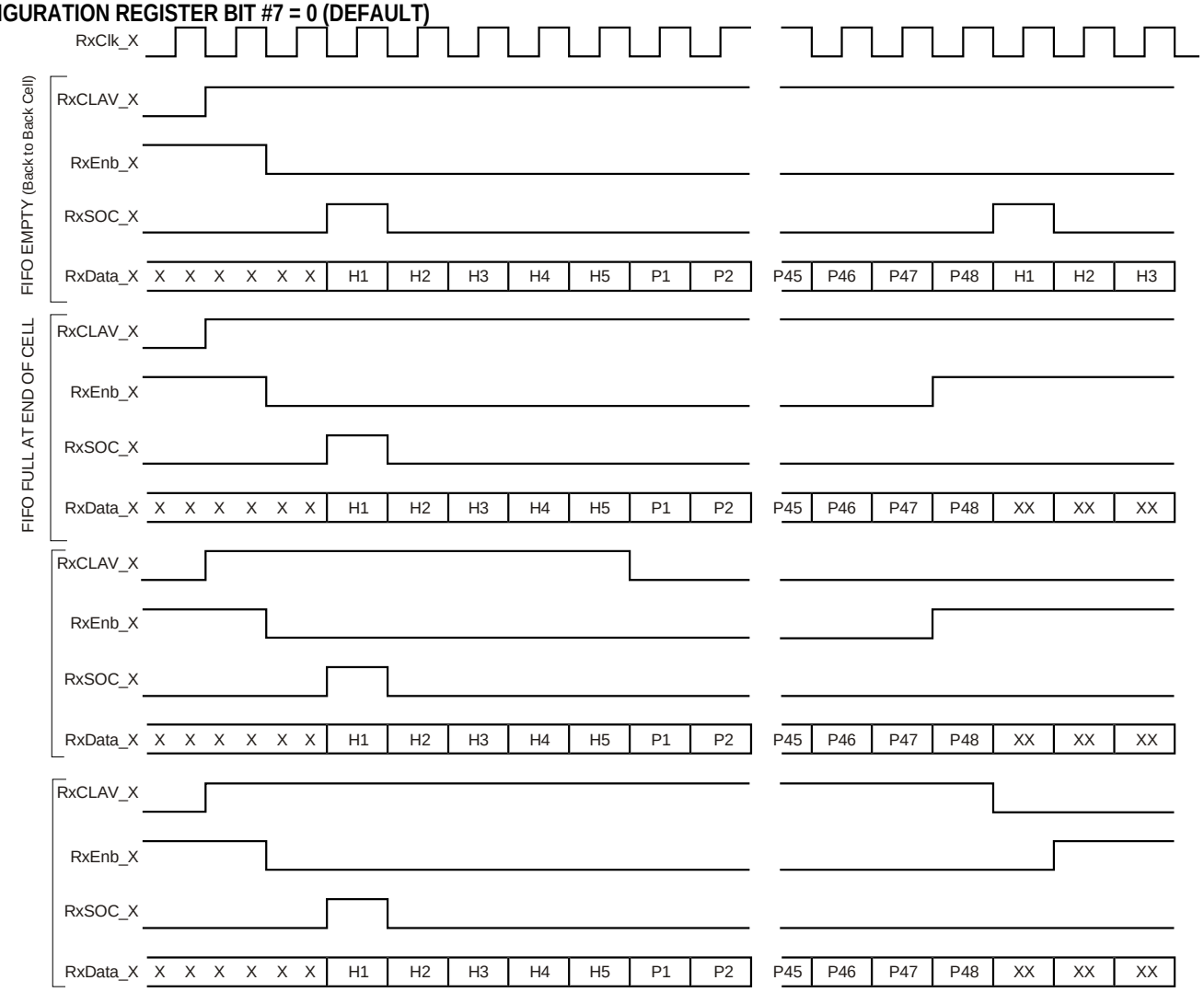
FIGURE 20B.END AND RESTART OF CELL TRANSMISSION AT RECEIVE INTERFACE TIMING DIAGRAM



5354drw17

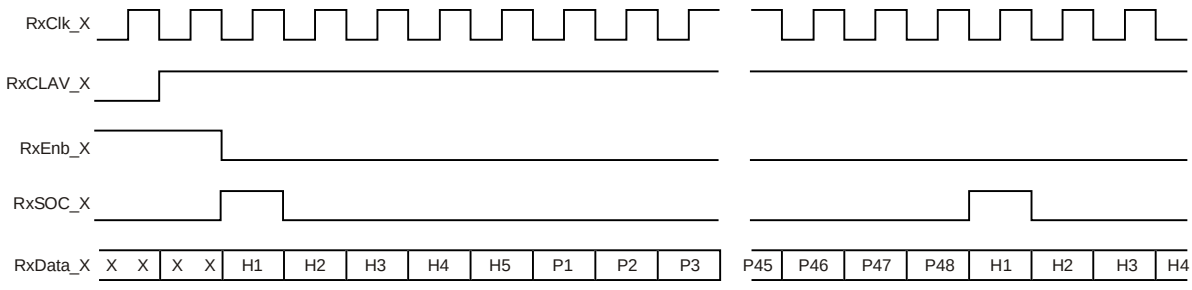
FIGURE 21. PORT A, B, C, OR D RECEIVE TIMING DIAGRAM

CONFIGURATION REGISTER BIT #7 = 0 (DEFAULT)



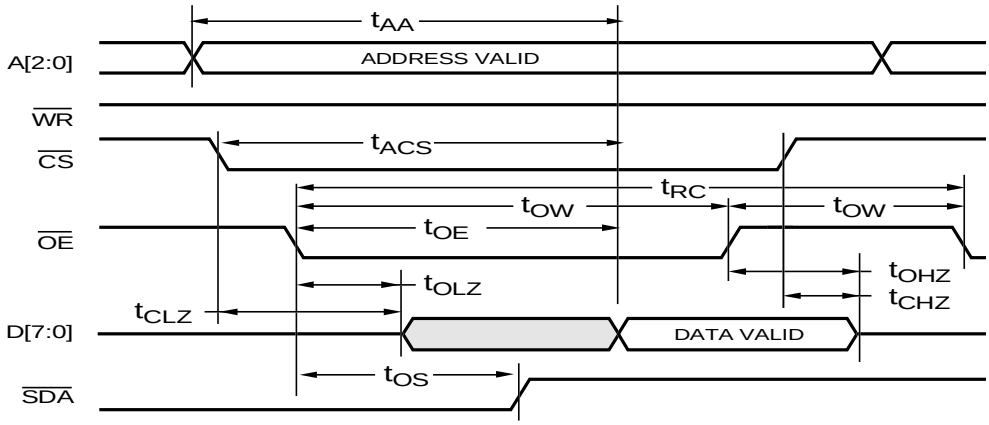
5354drw18

CONFIGURATION REGISTER BIT #7 = 1



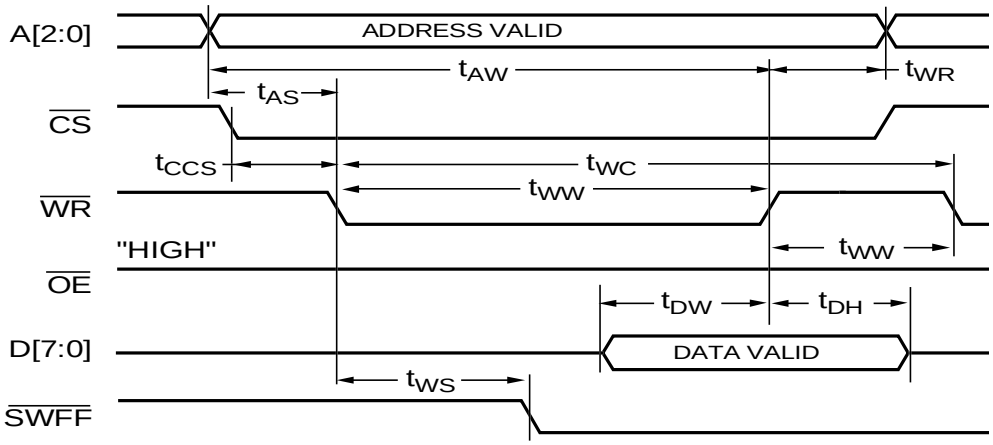
5354drw19

FIGURE 22. PROCESSOR INTERFACE READ CYCLE TIMING DIAGRAM



5354drw20

FIGURE 23. PROCESSOR INTERFACE WRITE CYCLE TIMING DIAGRAM



5354drw21

FIGURE 24. RESET TIMINGS TIMING DIAGRAM

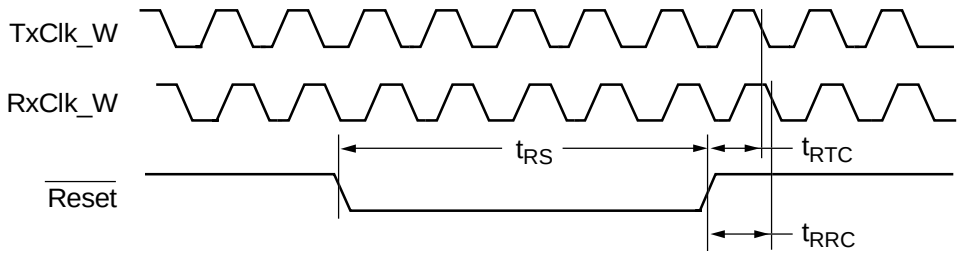
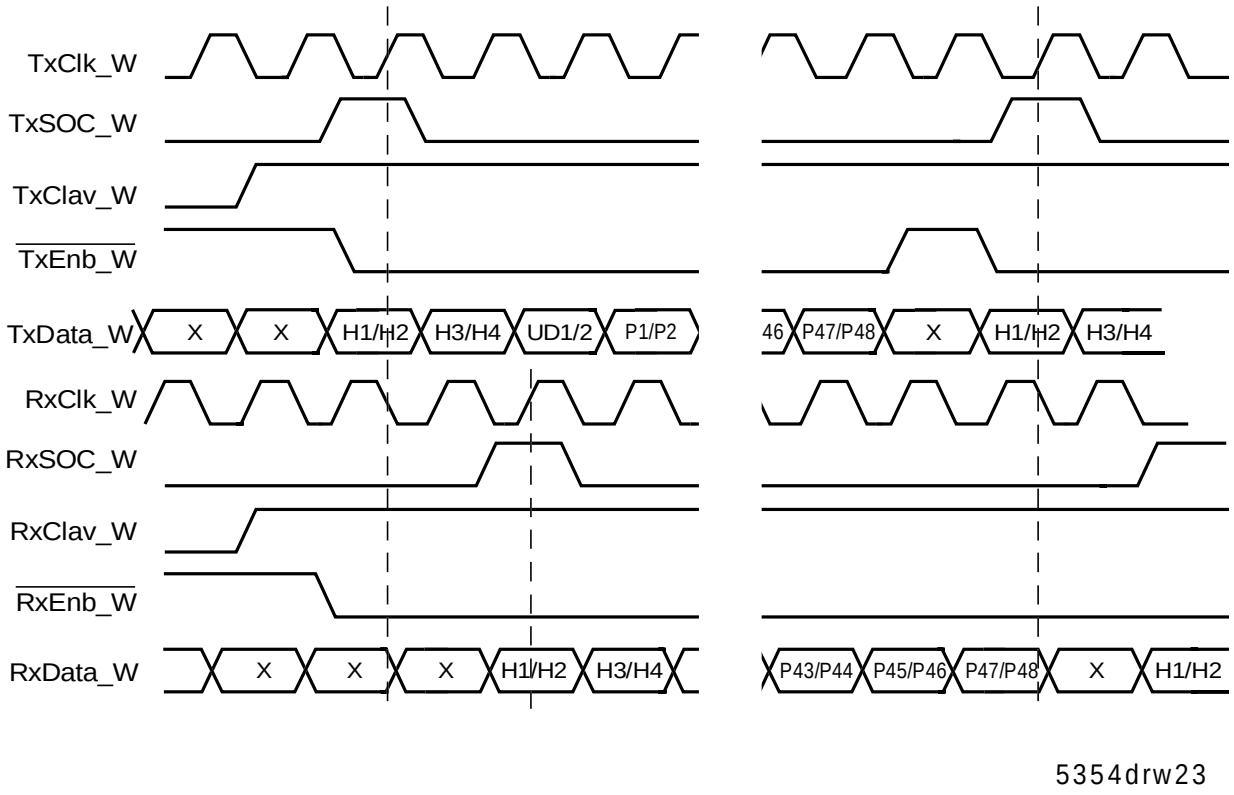


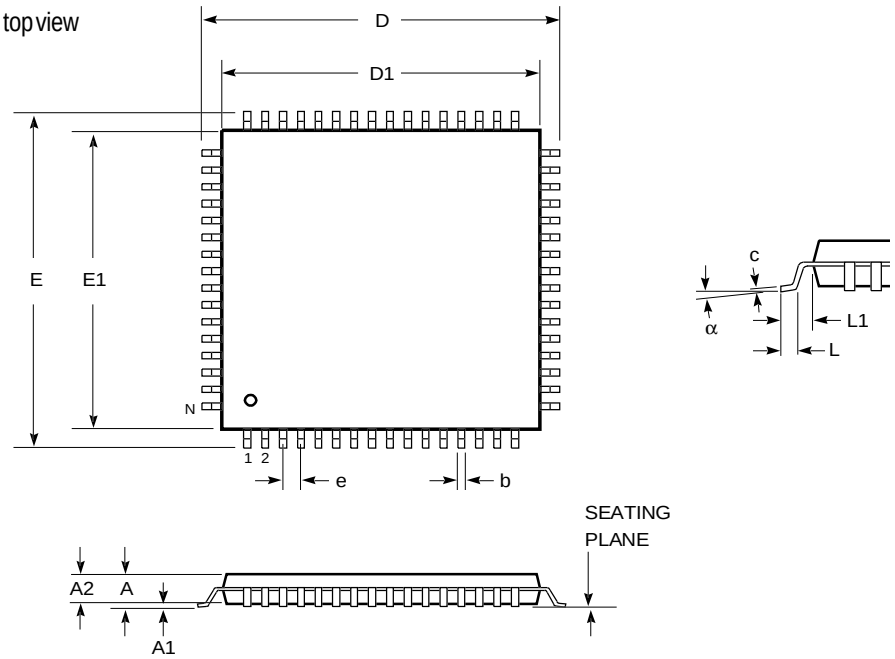
FIGURE 25. PORT W LOOPBACK TRANSMIT AND RECEIVE CYCLE TIMING DIAGRAM



QFP — PACKAGE CODE DS

PLASTIC QUAD FLATPACK PACKAGE

Counterclockwise orientation, top view



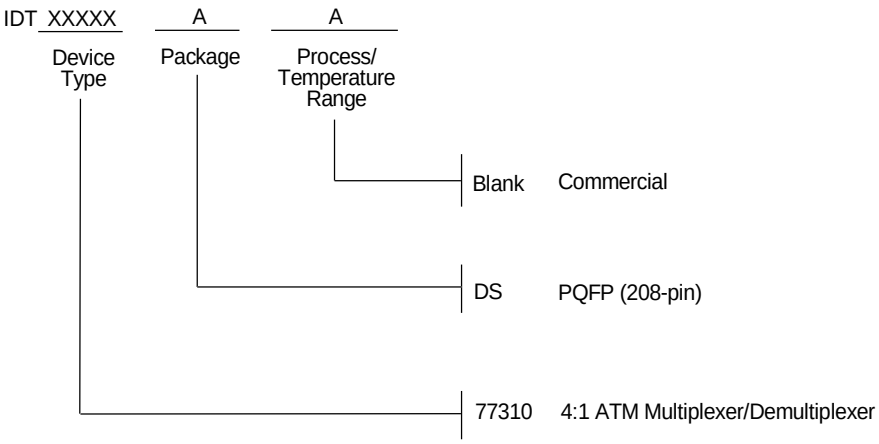
5354drw24

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in millimeters, unless otherwise specified.
3. Dimensions D and E do not include mold protrusions. Allowable mold protrustions are: D and E = 0.25mm Max.
4. ND and NE represent number of leads in D and E directions, respectively.
5. Lead coplanarity is 0.10mm maximum.

DWG #	DS208		
No. of Leads (N)	208		
Symbols	**Min**	**Nom**	**Max**
A	—	—	3.80
A1	0.25	0.35	0.45
A2	—	—	3.35
b	0.10	0.20	0.30
c	0.09	—	0.20
D	30.10	30.60	31.10
D1	27.70	28.0	28.30
e	0.50 BSC		
E	30.10	30.60	31.10
E1	27.70	28.0	28.30
L	0.40	0.50	0.60
α	0°	—	10°
ND/NE		52/52	

ORDERING INFORMATION



5354drw25

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