INTEGRATED CIRCUITS

DATA SHEET

SZA1000
QIC digital equalizer

Product specification
File under Integrated Circuits, IC01

1998 Feb 16

Philips Semiconductors

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FEATURES

- 3-wire serial interface for programming and status reading
- Suitable for MFM (Modified Frequency Modulation), RLL 1,7 (Run Length Limited) and similar codes
- Transfer rates with MFM code from 250 kbits/s to 4 Mbits/s
- Transfer rates with RLL(1,7) code from 500 kbits/s to 12 Mbits/s
- Programmable FIR (Finite Impulse-Response) filter makes it possible to equalize complex and asymmetric channel impulse responses
- Programmable fixed and tracking qualification thresholds provide reliable data recovery in read mode, and reliable bad sector detection in verify mode
- Read pulse output for floppy tape drives
- Digital data synchronizer based on digital PLL with maximum likelihood detector for a better error rate than can be achieved with conventional analog circuits
- Data verification can be used (with the maximum likelihood detector switched off) to find bad sectors on drives with conventional read electronics
- Servo stripe detection for TR4, QIC3080 and similar formats
- Gap detector
- 2 programmable current sources
- Peak-to-peak amplitude detector with lowpass filter for servo burst reading
- Fully digital PLL for clock and data recovery:
  - Fully programmable behaviour
  - No external components, no tolerance problems
  - Programmable window shift
  - Fast run-in capability
  - Ideal zero phase restart.
- Parallel 8-bit input and output for product development and production testing
- Programmable WEQ (write equalization) circuit with transfer rates of up to 2 Mbits/s for floppy tape drives and up to 8 Mbits/s for drives with internal controllers.

GENERAL DESCRIPTION

The SZA1000 is a single chip digital equalizer for single channel QIC (Quarter Inch Cartridge) systems with MR (Magneto Resistive) heads. It can be used with QIC 3010, QIC 3020, QIC 3080, QIC 3095, Travan 2, 3, 4 and 5, and similar formats.

It replaces a pulse detector, programmable filter and data synchronizer, and adds a FIR filter to the conventional analog solution. This makes it possible to equalize yoke-type MR heads as well as SIG (Sensor In Gap) MR heads.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}; V_{DDD2}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA1}; V_{DDA2}	analog supply voltage		4.5	5.0	5.5	V
I_{DDD1}; I_{DDD2}	digital supply current	f_s = 24 MHz	–	32	–	mA
I_{DDA1}; I_{DDA2}	analog supply current		–	50	–	mA
$f_{clk(CLKIN)}$	read circuit clock frequency		–	24	24	MHz
$f_{clk(WEQCLK)}$	WEQ circuit clock frequency		–	24	36	MHz
T_{amb}	ambient operating temperature		0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SZA1000H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm) body 10 × 10 × 1.75 mm	SOT307-2

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BLOCK DIAGRAM

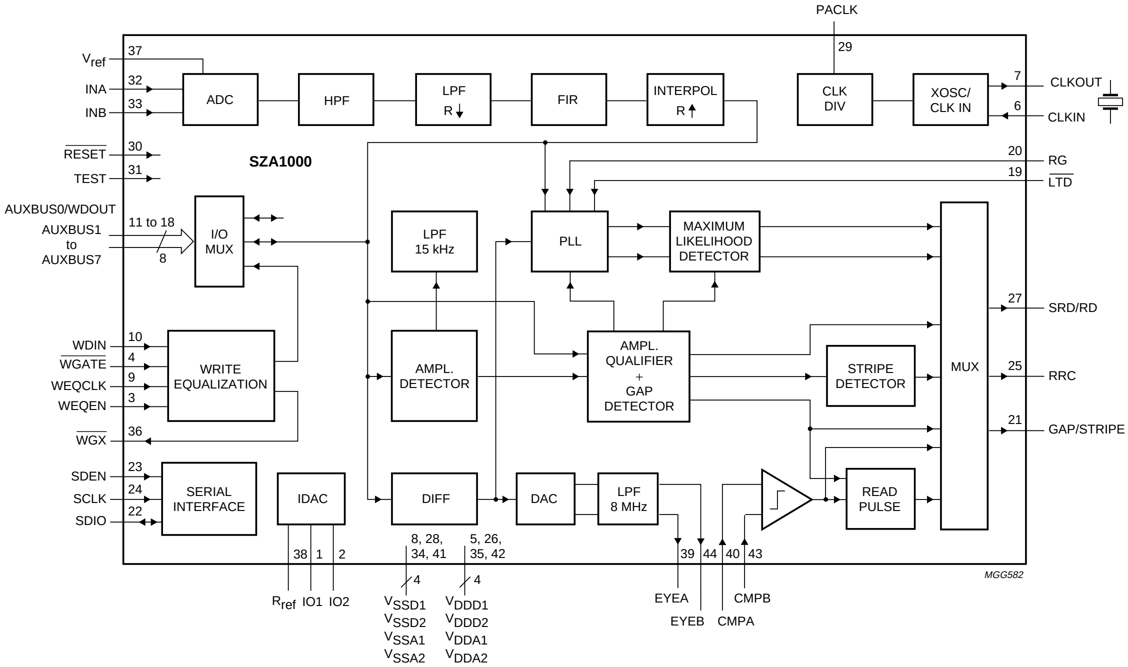

Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
IO1	1	programmable current source
IO2	2	programmable current source
WEQEN	3	write equalization circuit enable input
$\overline{WGATE}$	4	write gate input; active LOW
V_{DDD1}	5	digital supply voltage
CLKIN	6	external clock or crystal oscillator input
CLKOUT	7	crystal oscillator output
V_{SSD1}	8	digital ground
WEQCLK	9	write equalization circuit clock input
WDIN	10	write equalization circuit data input
AUXBUS0/WDOUT	11	bit 0 auxiliary I/O bus or write equalization output to write amplifier
AUXBUS1	12	bit 1 auxiliary I/O bus
AUXBUS2	13	bit 2 auxiliary I/O bus
AUXBUS3	14	bit 3 auxiliary I/O bus
AUXBUS4	15	bit 4 auxiliary I/O bus
AUXBUS5	16	bit 5 auxiliary I/O bus
AUXBUS6	17	bit 6 auxiliary I/O bus
AUXBUS7	18	bit 7 auxiliary I/O bus
$\overline{LTD}$	19	fast lock to data input; active LOW
RG	20	read gate input
GAP/STRIPE	21	gap or stripe detector output
SDIO	22	serial interface data input and output
SDEN	23	serial interface enable input
SCLK	24	serial interface clock input
RRC	25	read reference clock output
V_{DDD2}	26	digital supply voltage
SRD/RD	27	synchronized read data or read data output
V_{SSD2}	28	digital ground
PACLK	29	pre-amp clock output
$\overline{RESET}$	30	reset input; active LOW
TEST	31	test input; connect to ground
INA	32	analog signal from read amplifier; positive input
INB	33	analog signal from read amplifier; negative input
V_{SSA1}	34	analog ground
V_{DDA1}	35	analog supply voltage
$\overline{WGX}$	36	extended write gate output for floppy tape drives; active LOW
V_{ref}	37	positive A/D reference voltage input
R_{ref}	38	connect external resistor
EYEA	39	differentiated signal; positive output
CMPA	40	comparator for read pulse; positive input

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SYMBOL	PIN	DESCRIPTION
V_{SSA2}	41	analog ground
V_{DDA2}	42	analog supply voltage
CMPB	43	comparator for read pulse; negative input
EYEB	44	differentiated signal; negative output

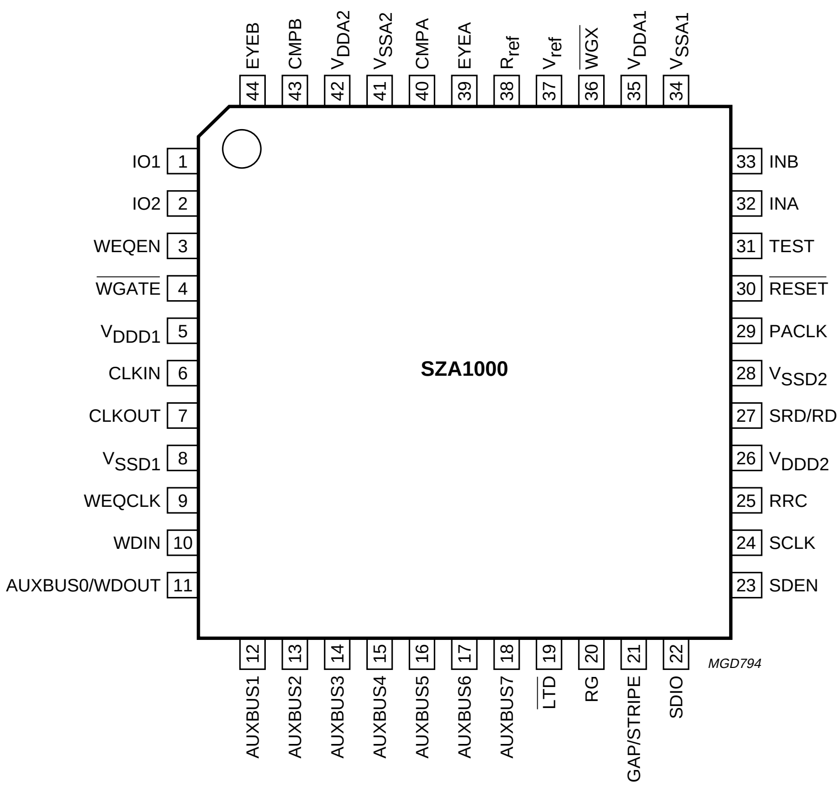

Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

Clock oscillator and divider

The clock source for the SZA1000 can be a crystal connected between pins 6 and 7, or an external clock signal connected to pin 6. This clock frequency is divided by a number programmable between 1 and 8 (see Tables 27 and 28). The resulting frequency, f_s, is used as clock input to all on-chip circuits except the write equalizer. The frequency of the PACLK output signal (pin 29) is equal to f_s.

ADC

The 8-bit ADC has a differential input. The total ADC conversion range is 1.6 V (p-p; differential). The ADC sample rate is equal to f_s.

High-pass filter after the ADC

This is a first order filter with a cut-off frequency of $\frac{f_s}{1608}$. It removes the DC component of the signal.

Low-pass filter

This low-pass filter is an even symmetrical FIR (Finite Impulse Response) filter. The number of taps depends on the sample rate reduction factor R (see Tables 30 and 31). The filter has 8 taps for R = 1 or 14 taps for R = 2 (see Table 7). The middle taps have a fixed coefficient value of +128, the coefficients of the other taps are programmable in the range –128 to +127 (see Table 6).

FIR

This transversal filter has 6 taps with the sample rate equal to f_s (R = 1), or 11 taps with the sample rate equal to $\frac{1}{2}f_s$ (R = 2). Tap 10 has a fixed coefficient value of +64, the coefficients of the other taps are programmable between –64 and +63 (see Table 2). The filter has 19 signal delay sections. The position of each tap can be selected from a subset of the 20 possible positions (see Tables 3 and 4).

Interpolator

If a sample rate of $\frac{1}{2}f_s$ has been selected for the FIR (R = 2), it is increased once again to f_s at the interpolator.

Amplitude detector

This circuit has a separate rectifier and a positive and negative peak detector.

Typical rise time (0 to 70%) for a normal MFM or RLL 1,7 code input signal is $\frac{1}{f_s}$, typical decay time (100 to 30%) is programmable between $\frac{500}{f_s}$ and $\frac{400}{f_s}$ (see Tables 10 and 11).

The output is an 8-bit number that can be polled via the serial interface. In addition, the peak-to-peak value is calculated and filtered by a first order low-pass filter with a cut-off frequency of $\frac{f_s}{3217}$

Both the filtered and unfiltered amplitudes can be read via the serial interface (see Table 44) or via the parallel output bus.

Amplitude qualifier

A peak is considered valid if its amplitude is above a qualification threshold. Separate qualification thresholds are used for the positive and negative peaks. Each threshold is the greater of:

- a programmable level (QUAL_FIX_ POS and QUAL_FIX_NEG; control register addresses 24 and 25)
- a programmable fraction ($\frac{1}{2}$, $\frac{3}{8}$, $\frac{1}{4}$, $\frac{1}{8}$ or 0; see Tables 9 and 12) of the peak amplitude of the incoming signal.

Gap detector

When the peak-to-peak amplitude of the measured signal is below a preset limit (GAP_THRESH; control register address 28), the gap detector output is HIGH, otherwise LOW (GAP output on pin 21 must be selected; see Table 22).

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Stripe detector

This circuit is used to signal the stripes in QIC 3080, QIC 3095 and TR4 servo formats (STRIPE output on pin 21 must be selected; see Table 22). A frequency detector counts the peaks above the qualification threshold (see Table 29). An input signal containing frequencies within ±25% of the programmable nominal frequency will be detected as a stripe. The microcontroller can then poll the amplitude of the following burst via the serial interface.

Differentiator

This function is realized by subtracting samples. The delay between samples is programmable between 1 and 6 periods of f_s, split into two parts to provide a balanced delay between the differentiated and non-differentiated signals (see Tables 24 to 26).

The PLL

This is a fully digital PLL (Phase Lock Loop) with a programmable nominal frequency (see Tables 35 and 36), zero phase restart, programmable window shift (WIN_SHIFT; control register address 42) and a loop filter with two separate programmable settings.

The PLL output reference clock is the RRC signal (pin 25; see Table 34). The frequency of this signal is rounded in time to f_s. The PLL is switched to the nominal frequency if RG (pin 20) is LOW, and makes a zero phase restart at the first detected peak after RG goes HIGH.

The LTD input (pin 19) is used to select between the two loop filter settings (see Tables 37 to 42). This allows for fast lock-in during preamble, before switching to a lower loop bandwidth for maximum data reliability (see Fig.3).

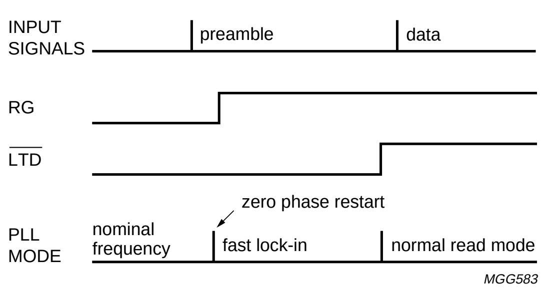

Fig.3 PLL timing diagram.

The maximum likelihood detector

This detector calculates the most likely position of the peaks in the signal. It checks for (d,k) code constraints, and for alternating peaks. If an error is detected, the ‘most likely’ correction is implemented.

Separate corrections can be enabled or disabled.
The SRD output of the maximum likelihood detector is valid during the rising edge of the RRC signal (see Fig.4).

The maximum likelihood detector is used only to generate the SRD signal, and not to generate the time continuous RD pulse.

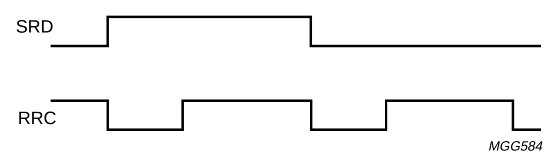

Fig.4 SRD/RRC timing.

The DAC

This is an internal differential 8-bit DAC operating at f_s.

The LPF after the DAC

This analog LPF filters the time quantized signal from the DAC to retain a time continuous signal. This provides more accurate timing of the detected zero crossings in the RD pulse output.

The LPF is a second order active filter with a cut-off frequency of 8 MHz.

The read pulse circuit

A peak in the equalized signal at the interpolator output generates a read pulse. The peak is detected if a zero crossing occurs in the filtered signal after the DAC while the non-differentiated signal is above the qualification threshold.

Uncommitted current sources

Two uncommitted 5-bit programmable current sink DACs (0 to 2 mA) are available as IO1 and IO2 (see Table 20 for programming). These could be used, for example, to drive the tape hole detector circuit.

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Parallel state bus

All internal digital signals can be monitored via an 8-bit parallel bus. An external DAC or an evaluation tool such as a phase error logger for TIA (Time Interval Analyzer), drop-out and symmetry measurements can be connected to this bus for evaluation purposes (see Table 34).

Write equalization

This circuit has an independent clock input WEQCLK at pin 9.

Write equalization can be programmed to conform to a number of formats including QIC 3010, QIC 3020, QIC 3080, QIC 3095, QIC 5010, Travan 2, Travan 3 and Travan 4.

This is achieved by programming the circuit to divide a channel bit-cell into 2, 3 or 6 time slots (see Tables 13 and 14). The external WEQ clock frequency should be selected such that an integer number of between 1 and 8 clock periods fits in a time slot (see Tables 18 and 19).

The width and position of the inserted write pulse can be programmed (see Tables 15 to 17).

The write equalization circuit input and output signals can be independently programmed to be in either WD or WDI format (see Table 15).

For QIC 3010 or 3020, the recording signal is typically generated by a circuit that uses a separate crystal.
An input buffer with variable delay is used to prevent errors occurring in the recorded signal. This buffer is set to its nominal position when writing begins.

Signals longer than a data block can be recorded during formatting. To avoid overloading the time buffer, the circuit can resynchronize automatically during gaps in the QIC 3010 or 3020 format.

Serial interface

The serial interface uses 8-bit addresses and 8-bit data. Its timing is shown in Fig.5. IC mode settings, filter coefficients, scale factors and thresholds can be loaded via the serial interface.

Measured signal amplitude, for example Burst level measurement at QIC 3095 or AGC control by the microcontroller, and the actual PLL frequency can be read via the serial interface. To read data from the status registers, hex address FF must be transmitted along with the required data code. The IC will then respond with the contents of the appropriate 8-bit status register (see Table 44).

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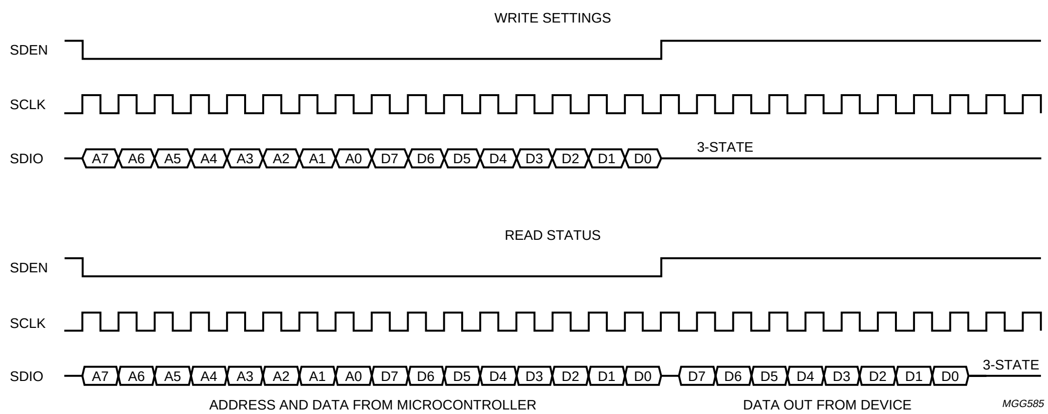

Fig.5 Serial I/O timing diagrams.

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CONTROL REGISTER

Control register settings

The control register is accessible through the serial interface and contains 46 8-bit entries as shown in Table 1.

Table 1 Control register

ADDRESS	NAME	DESCRIPTION
0	FIR_VAL0	FIR tap 0 coefficient value (see Table 2)
1	FIR_VAL1	FIR tap 1 coefficient value
2	FIR_VAL2	FIR tap 2 coefficient value
3	FIR_VAL3	FIR tap 3 coefficient value
4	FIR_VAL4	FIR tap 4 coefficient value
5	FIR_VAL5	FIR tap 5 coefficient value
6	FIR_VAL6	FIR tap 6 coefficient value
7	FIR_VAL7	FIR tap 7 coefficient value
8	FIR_VAL8	FIR tap 8 coefficient value
9	FIR_VAL9	FIR tap 9 coefficient value
10	FIR_SEL05	FIR tap positions (see Tables 3 and 4)
11	FIR_SEL16	FIR tap positions
12	FIR_SEL27	FIR tap positions
13	FIR_SEL38	FIR tap positions
14	FIR_SEL49	FIR tap positions
15	FIR_SEL10	FIR tap positions
16	FIR_SHIFT	FIR output scaling (see Table 5)
17	LPF_VAL1	LPF tap coefficient value (see Table 6)
18	LPF_VAL4	LPF tap coefficient value
19	LPF_VAL2	LPF tap coefficient value
20	LPF_VAL5	LPF tap coefficient value
21	LPF_VAL3	LPF tap coefficient value
22	LPF_VAL6	LPF tap coefficient value
23	LPF_SHIFT	LPF output scaling (see Table 8)
24	QUAL_FIX_POS	Amplitude qualifier positive fixed qualification threshold
25	QUAL_FIX_NEG	Amplitude qualifier negative fixed qualification threshold
26	QUAL_VAR_GAIN	Amplitude qualifier variable gain factors (see Tables 9 and 12)
27	QUAL_SLOPE_DEL	Amplitude detector slope qualification delay (see Table 10)
28	GAP_THRESH	Gap detector fixed threshold
29	WEQ_SET0	WEQ settings (see Tables 13 and 14)
30	WEQ_SET1	WEQ settings (see Tables 15, 16 and 17)
31	WEQ_CLK_DIV	WEQ clock divider (see Tables 18 and 19)
32	–	not used
33	IDAC1	IO1 DAC current (see Table 20)
34	IDAC2	IO2 DAC current (see Table 20)

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ADDRESS	NAME	DESCRIPTION
35	EQ MODE0	Mode setting for PACLK (pin 29) and GAP/STRIPE (pin 21) (see Tables 21, 22 and 23)
36	DIFF	differentiator settings (see Tables 24, 25 and 26)
37	CLK_DIV	main clock divider (see Tables 27 and 28)
38	STRIPE_F	stripe detector nominal frequency (see Table 29)
39	EQ_MODE1	equalizer mode settings
40	PLL_FREQL	PLL nominal frequency bits 0 to 7
41	PLL_FREQH	PLL nominal frequency bits 8 to 10
42	WIN_SHIFT	PLL window shift
43	PLL_NI	PLL loop filter integrating gain and range
44	PLL_NP	PLL loop filter proportional gain
45	MLD_SET	maximum likelihood detector settings

Control register functions

Control register functions are detailed in Tables 2 to 43.

FIR FUNCTION

Addresses 0 to 9: FIR tap coefficient values

Table 2 Coefficient values: FIR_VAL0 to FIR_VAL9; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	FIR_VALn.6	FIR_VALn.5	FIR_VALn.4	FIR_VALn.3	FIR_VALn.2	FIR_VALn.1	FIR_VALn.0

Note

1. These are 7-bit coefficient values in two's complement notation; taps 5 to 9 are only used when R = 2; tap 10 has a fixed coefficient value of +64.

Addresses 10 to 15: FIR tap position selection

Table 3 Tap position selection: FIR_SELnn; note 1

ADDR.	NAME	TAPS	D7	D6	D5	D4	D3	D2	D1	D0
10	FIR_SEL05	0 and 5	–	–	FS0.2	FS0.1	FS0.0	FS5.2	FS5.1	FS5.0
11	FIR_SEL16	1 and 6	–	–	FS1.2	FS1.1	FS1.0	FS6.2	FS6.1	FS6.0
12	FIR_SEL27	2 and 7	–	–	FS2.2	FS2.1	FS2.0	FS7.2	FS7.1	FS7.0
13	FIR_SEL38	3 and 8	–	–	FS3.2	FS3.1	FS3.0	FS8.2	FS8.1	FS8.0
14	FIR_SEL49	4 and 9	–	–	FS4.2	FS4.1	FS4.0	FS9.2	FS9.1	FS9.0
15	FIR_SEL10	10	–	–	–	–	FS10.3	FS10.2	FS10.1	FS10.0

Note

1. See Table 4 for the value of FSn.n.

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Table 4 Translation table: FS selection bits (FSn.n from Table 3) to tap position

FSn	TAP 0,5	TAP 1,6	TAP 2,7	TAP 3,8	TAP 4,9	TAP 10
0	12	9	6	3	0	2
1	13	10	7	4	1	3
2	14	11	8	5	2	4
3	15	12	9	6	3	5
4	16	13	10	7	4	6
5	17	14	11	8	5	7
6	18	15	12	9	6	8
7	19	16	13	10	7	9
8	–	–	–	–	–	10
9	–	–	–	–	–	11
10	–	–	–	–	–	12
11	–	–	–	–	–	13
12	–	–	–	–	–	14
13	–	–	–	–	–	15
14	–	–	–	–	–	16
15	–	–	–	–	–	17

Address 16: FIR output scaling

Table 5 Output scaling: FIR_SHIFT

FIR_SHIFT (BINARY)	FIR OUTPUT SCALING GAIN FACTOR
00000001	1
00000010	2
00000100	4
00001000	8
00010000	16
00100000	32
01000000	64
10000000	128

LOW-PASS FILTER FUNCTIONS

Addresses 17 to 22: LPF tap coefficient values

Table 6 Coefficient value: LPF_VAL1 to LPF_VAL6; notes 1 and 2

D7	D6	D5	D4	D3	D2	D1	D0
LPF_VALn.7	LPF_VALn.6	LPF_VALn.5	LPF_VALn.4	LPF_VALn.3	LPF_VALn.2	LPF_VALn.1	LPF_VALn.0

Notes

1. These are 8-bit coefficient values in two's complement notation; taps 4 to 6 are only used when R = 2.
2. See Table 7 for the values of LPF_VALn.n

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Table 7 LPF tap positions

TAP POSITION	COEFFICIENT VALUES R = 1	COEFFICIENT VALUES R = 2
0	LPF_VAL3	LPF_VAL6
1	LPF_VAL2	LPF_VAL5
2	LPF_VAL1	LPF_VAL4
3	+128	LPF_VAL3
4	+128	LPF_VAL2
5	LPF_VAL1	LPF_VAL1
6	LPF_VAL2	+128
7	LPF_VAL3	+128
8	0	LPF_VAL1
9	0	LPF_VAL2
10	0	LPF_VAL3
11	0	LPF_VAL4
12	0	LPF_VAL5
13	0	LPF_VAL6

Address 23: LPF output scaling

Table 8 Output scaling: LPF_SHIFT

LPF_SHIFT (BINARY)	LPF OUTPUT SCALING GAIN FACTOR
00000001	1
00000010	2
00000100	4
00001000	8
00010000	16
00100000	32
01000000	64
10000000	128

AMPLITUDE QUALIFIER/DETECTOR FUNCTIONS

Address 24: QUAL_FIX_POS and Address 25: QUAL_FIX_NEG

QUAL_FIX_POS and QUAL_FIX_NEG contain the positive and negative fixed threshold (8-bit signed) values.

Address 26: Variable gain factors

Table 9 Gain factors: QUAL_VAR_GAIN; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	GP.2	GP.1	GP.0	GN.2	GN.1	GN.0

Note

1. GP and GN set the factors of the measured amplitude that are to be used as variable qualifier thresholds: GP for the positive peaks and GN for the negative peaks.

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Address 27: Amplitude detector slope qualification delay

Table 10 Qualification delay: QUAL_SLOPE_DEL; notes 1 and 2

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	DEL.1	DEL.0	SL.1	SL.0

Notes

1. DEL is the programmable compensation delay, in cycles of f_s, between the qualifier and the analog zero crossing of the read pulse circuit; DEL is a 2-bit unsigned value
2. SL selects the decay time of the amplitude detectors.

Table 11 Amplitude detector decay time $\frac{500}{f_s}$

SL	DECAY TIME
0	$\frac{500}{f_s}$
1	$\frac{1000}{f_s}$
2	$\frac{2000}{f_s}$
3	$\frac{4000}{f_s}$

Table 12 Variable qualifier threshold

GP, GN	VARIABLE THRESHOLD
0	0
1	$\frac{1}{8}$
2	$\frac{1}{4}$
3	$\frac{3}{8}$
4, 5, 6, 7	$\frac{1}{2}$

GAP DETECTOR FUNCTIONS

Address 28: Fixed threshold: GAP_THRESH

Fixed threshold for the gap detector; 8-bit signed value.

WRITE EQUALIZATION (WEQ) FUNCTIONS

Address 29: WEQ settings

Table 13 Time slots: WEQ_SET0; see Table 14

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	N6	N3	N2

Table 14 Time slots in channel bit cell

NUMBER OF TIME SLOTS	N6	N3	N2
2	0	0	1
3	0	1	0
6	1	0	0

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Address 30: WEQ settings

Table 15 WEQ_SET1; notes 1 to 4, see also Tables 16 and 17.

D7	D6	D5	D4	D3	D2	D1	D0
WDI_O	WDI_I	RESYNC	TPS2	TPS1	TPS0	TWS1	TWS0

Notes

1. If bit WDI_O is HIGH, the circuit output is a WD signal, else a WDI signal.
2. If bit WDI_I is HIGH, the circuit expects a WD signal at the input, else a WDI signal.
3. If the RESYNC bit is HIGH, the WEQ circuit resynchronizes its time buffer during a gap in the QIC 3010 or QIC 3020 format; this setting is only permitted if 6 time slots in a bit-cell are selected (N6 = 1; see Table 14).
4. TPS sets the position of the inserted write equalization pulse, TWS sets its width.

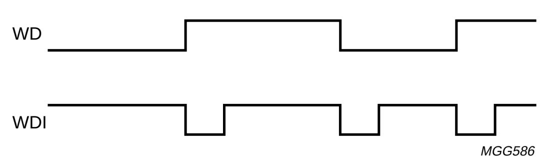

Fig.6 WD/WDI signal timing.

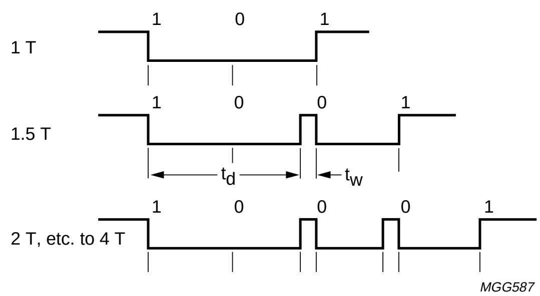

Fig.7 Position and width of write equalization pulse.

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Table 16 Write equalization pulse position

TPS	POSITION IN TIME SLOTS
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8

Table 17 Write equalization pulse width

TWS	WIDTH IN TIME SLOTS
0	WEQ off
1	1
2	2
3	3

Address 31: WEQ circuit clock divider

Table 18 Division factor: WEQ_CLK_DIV; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	WCD.2	WCD.1	WCD.0

Note

1. WCD sets the division factor between WEQCLK and the frequency of the time slot.

Table 19 WEQ clock division

WCD	WEQ CLOCK DIVISION FACTOR
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8

UNCOMMITTED CURRENT DAC FUNCTIONS

Addresses 33 and 34: Current DACs

Table 20 DAC current: IDAC1 and IDAC2; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	IDn.4	IDn.3	IDn.2	IDn.1	IDn.0

Note

1. These are 5-bit unsigned numbers; the DAC current is $\frac{IDn}{16}$ mA.

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O/P SIGNAL FUNCTION: PINS 21 AND 29

Address 35: O/P Select pins 21 and 29

Table 21 Output signal select: EQ MODE 0; see Tables 22 and 23

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	PA.1	PA.0	GAP.1	GAP.0

Table 22 Output signal: pin 21

GAP	OUTPUT SIGNAL ON PIN 21
0	GAP(1)
1	STRIPE
2	QUAL(2)
3	RD(3)

Notes

1. GAP, STRIPE or QUAL may be selected to detect gaps, stripes or valid signal peaks. All are active HIGH.
2. See also Table 34.
3. The RD output (read pulse): falling edge active.

Table 23 Output signal: pin 29

PA	OUTPUT SIGNAL ON PIN 29
0	f_s - PACLK on
1	1 - PACLK off
2	0 - PACLK off
3	0 - PACLK off

DIFFERENTIATOR FUNCTIONS

Address 36: Differentiator settings

Table 24 DIFF; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	DS	DL2.1	DL2.0	DL1.1	DL1.0

Note

1. DL1 and DL2 are programmable delays for the differentiator; DS is the gain factor of the differentiated signal.

Table 25 Differentiator delay; notes 1 and 2

DLn	DELAY IN f_s CYCLES
0	0
1	1
2	2
3	3

Notes

1. DL1 and DL2 are added to provide a maximum delay of $6 \times f_s$ cycles.
2. It is advisable to have DL1 and DL2 equal to avoid adding unwanted delay in the differentiator.

Table 26 Differentiator gain factor

DS	OUTPUT SCALING GAIN FACTOR
0	4
1	2

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CLOCK FUNCTIONS

Address 37: Main clock divider

Table 27 Clock divider: CLK_DIV; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	CD.2	CD.1	CD.0

Note

1. CD selects the main clock division factor. The CLKIN frequency (pin 6) divided by this factor gives the IC’s operating frequency f_s (apart from the WEQ circuit).

Table 28 Clock division factor

CD	CLOCK DIVISION
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8

STRIPE DETECTOR FUNCTIONS

Address 38: Stripe detector nominal frequency

Table 29 Qualification threshold: STRIPE_F; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	SF.4	SF.3	SF.2	SF.1	SF.0

Note

1. SF is an unsigned 5-bit value used to determine the detection threshold for the stripe detector. The nominal detection frequency is $\frac{f_s}{3 \times (SF + 1)}$

AUXBUS, PINS 25 AND 27, SAMPLE RATE REDUCTION AND STAND-BY FUNCTIONS

Address 39: Equalizer mode settings

Table 30 EQ_MODE 1; note 1, see also Tables 31 to 34

D7	D6	D5	D4	D3	D2	D1	D0
–	STBY2	ST.3	ST.2	ST.1	ST.0	STBY1	R1

Note

1. R1 selects the filter sample rate reduction factor; STBY1 and STBY2 are the DAC and ADC power on/off switches; ST selects output signal modes for pins 25 and 27.

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Table 31 FIR/LPF Sample Rate Reduction Factor: R

R1	R
0	2
1	1

Table 32 DAC power

STBY1	D/A POWER
0	on
1	off

Table 33 ADC power

STBY2	A/D POWER
0	on
1	off

Table 34 Mode settings: pins 25, 27 and AUXBUS

ST	IC MODE	PIN 27	PIN 25	AUXBUS
0	PLL off	RD	QUAL(1)	bit 0: WDOUT, bits 1 to 7 high-Z
1	PLL off	RD	COMP(2)	bit 0: WDOUT, bits 1 to 7 high-Z
2	PLL on	SRD	RRC	bit 0: WDOUT, bits 1 to 7 high-Z
3	ADC test	SRD	RRC	ADC output
4	DAC test	RD	COMP	DAC output
5	one shot test	–	–	–
6	PLL off, AD bypass	RD	QUAL	8-bit input to HPF
7	PLL off, AD bypass	RD	COMP	8-bit input to HPF
8	PLL on, AD bypass	SRD	RRC	8-bit input to HPF
9	PLL on, LPF output	SRD	RRC	LPF output after scaling
10	PLL on, FIR output	SRD	RRC	FIR output after scaling and interpolator
11	PLL on, PLL phase output	SRD	RRC	PLL phase error output
12	PLL on, PLL frequency output	SRD	RRC	PLL frequency output
13	PLL on, peak-to-peak level output	SRD	RRC	bits 7 to 1: LEVEL_ABS; bit 0:WDOUT
14	PLL on, filtered level output	SRD	RRC	bits 7 to 1: LEVEL_FIL; bit 0:WDOUT
15	PLL on, differentiator output	SRD	RRC	differentiator output after scaling

Notes

1. QUAL is a test signal (active HIGH) used to detect valid signal peaks (see also Table 22).
2. When COMP is selected, pin 25 is switched to the output of the read pulse circuit comparator for test purposes.

PLL FUNCTIONS

Addresses 40 and 41: PLL nominal frequency

Table 35 PLL_FREQL (address 40)

D7	D6	D5	D4	D3	D2	D1	D0
PF.7	PF.6	PF.5	PF.4	PF.3	PF.2	PF.1	PF.0

Table 36 PLL_FREQH (address 41); note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	PF.10	PF.9	PF.8

Note

1. The nominal PLL frequency is $f_s \times \frac{PF}{2048}$

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Address 42: Phase comparator window shift

WIN_SHIFT is an 8-bit number in two's complement format. The programmed phase shift is 180 × WIN_SHIFT degrees.

Address 43: PLL settings

Table 37 Address 43: PLL_NI; note 1

D7	D6	D5	D4	D3	D2	D1	D0
Q1	Q0	RNG.1	RNG.0	NI2.1	NI2.0	NI1.1	NI1.0

Note

1. If LTD (pin 19) is HIGH, NI2 is selected, else NI1.

Table 38 DL setting; note 1

DL SETTING	Q1	Q0
DL1 = DL2	1	1
DL1 < DL2	1	0
DL1 > DL2	0	1

Note

1. The Differentiator Delay (DL) settings (see Table 25) determine the values of Q1 and Q0 that should be entered.

Table 39 Integrating gain factor KI

NI	KI
0	$^1/_{64}$
1	$^1/_{128}$
2	$^1/_{256}$
3	$^1/_{512}$

Table 40 PLL range

RNG	PLL RANGE
0	±64
1	±128
2	±256
3	±512

Address 44: PLL loop filter proportional gain

Table 41 PLL_NP; note 1

D7	D6	D5	D4	D3	D2	D1	D0
–	–	NP2.2	NP2.1	NP2.0	NP1.2	NP1. 1	NP1. 0

Note

1. If LTD (pin 19) is HIGH, NP2 is selected, else NP1.

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Table 42 Proportional gain factor KP

NP	KP
0	1
1	$\frac{1}{2}$
2	$\frac{1}{4}$
3	$\frac{1}{8}$
4	$\frac{1}{16}$
5	$\frac{1}{32}$
6	–
7	–

MAXIMUM LIKELIHOOD DETECTOR FUNCTIONS

Address 45: Settings

Table 43 Address 45: MLD_SET

D7	D6	D5	D4	D3	D2	D1	D0
en_k(1)	en_d(2)	PR1(3)	PR0(4)	ks3(5)	ks2(5)	ks1(5)	ks0(5)

Notes

1. Check for k constraint: k is the maximum number of channel bit-cells allowed without a transition. For MFM code: k = 3 (ks = 4), for RLL(1,7) code: k = 7 (ks = 8).
2. Check for d = 1 constraint: d is the minimum number of channel bit-cells without transitions that must come between two bit cells with transitions. d = 1 for both MFM and RLL(1,7) codes
3. Check partial response constraints; delete incorrect peaks.
4. Check partial response constraints; add missing peaks.
5. ks = k + 1.

STATUS REGISTER

The status register contains 5 status bytes. The contents of the status bytes can be read via the serial interface.

Table 44 Status bytes; notes 1 to 4

ADDRESS	DATA	NAME	DESCRIPTION
255	0	FREQ	actual frequency of PLL
255	1	LEVEL_POS	positive peaks in measured level
255	2	LEVEL_NEG	negative peaks in measured level
255	3	LEVEL_ABS	measured peak-to-peak level
255	4	LEVEL_FIL	low-pass filtered LEVEL_ABS

Notes

1. The levels are measured behind the re-sampling block (interpolator) (see Fig.1).
2. Actual PLL frequency is an 8-bit unsigned number: $f_s \times \frac{FREQ}{256}$
3. LEVEL_FIL can be used for reading of the burst levels, or in an AGC loop (with the TZA1000 preamplifier).
4. LEVEL_POS, LEVEL_NEG, LEVEL_ABS and LEVEL_FIL are 8-bit numbers in two's complement format.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD1}	digital supply voltage		–0.3	+5.5	V
V_{DDD2}	digital supply voltage		–0.3	+5.5	V
V_{DDA1}	analog supply voltage		–0.3	+5.5	V
V_{DDA2}	analog supply voltage		–0.3	+5.5	V
V_i	input voltage		–0.3	V_{DD} + 0.3	V
I_I	input current on supply pins		–50	+50	mA
$I_{I(n)}$	input current on remaining pins		–10	+10	mA
P_{tot}	maximum total power dissipation		–	+1100	mW
T_{amb}	ambient temperature		–30	+85	°C
T_j	junction temperature		–30	+125	°C
T_{stg}	storage temperature		–50	+150	°C
$V_{ES(HB)}$	electrostatic handling: human body model	note 1	–3000	+3000	V
$V_{ES(MM)}$	electrostatic handling: machine model	note 2	–300	+300	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistance.
2. Equivalent to discharging a 200 pF capacitor through a 25 Ω series resistance and a 2.5 μH series inductance.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	70	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*.

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CHARACTERISTICS

V_{DDD1} = V_{DDD2} = V_{DDA1} = V_{DDA2} = 5 V ±5%; f_s = $f_{clk(CLKIN)}$ = 24 MHz; V_{ref} = 2 V ±5%; R_{ref} = 10 kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage		4.5	5.0	5.5	V
V_{DDD2}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA1}	analog supply voltage		4.5	5.0	5.5	V
V_{DDA2}	analog supply voltage		4.5	5.0	5.5	V
I_{DDD1}; I_{DDD2}	digital supply current	r = 2, no WEQ	–	32	80	mA
I_{DDA1}; I_{DDA2}	analog supply current	STBY1 = 0; STBY2 = 1; see Table 30	–	50	65	mA
		STBY 1= 1; STBY2 = 0	–	26	35	mA
$f_{clk(CLKIN)}$	read circuit clock frequency		–	24	24	MHz
$f_{clk(WEQCLK)}$	WEQ circuit clock frequency	N6 = 0; see Table 14; (3080; 3095)	–	–	36	MHz
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
V_{OL}	LOW-level output voltage	I_o = –4 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_o = +4 mA	V_{DD} – 0.5	–	–	V
C_i	input capacitance	I/O pins high-Z; note 1	–	–	5	pF
Analog section						
V_{ref}	reference voltage (pin 37)		1.8	2.0	2.2	V
I_{ref}	reference current (pin 37)		1.0	1.7	2.1	mA
$V_{cnv(A/D)}$	A/D conversion range		–	1.6	–	V
$V_{CM(A/D)}$	A/D common mode voltage		2	2.5	3	V
$R_{i(A/D)}$	A/D input resistance		2.3	3.3	4.4	kΩ
$C_{i(A/D)}$	A/D input capacitance		–	3	5	pF
$I_{I(32)}$	DC input current (INA)		–	0.42	0.6	mA
$I_{I(33)}$	DC input current (INB)		–	0.13	0.2	mA
V_{38}	voltage on pin 38 (R_{ref})		–	2.0	–	V
$I_{O(1)}$	output current on pin 1 (IO1)	IDAC1 = 0; see Table 20	–	0.0	0.05	mA
		IDAC1 = 31	1.40	1.95	2.60	mA
$I_{O(2)}$	output current on pin 2 (IO2)	IDAC2 = 0; see Table 20	–	0.0	0.05	mA
		IDAC2 = 31	1.40	1.95	2.60	mA
$V_{o(dif)}$	D/A differential output range (peak-to-peak)	note 2	1.5	1.72	1.8	V
$V_{CM(D/A)}$	D/A common mode voltage	note 2	1.0	1.16	1.4	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{-3dB(cutoff)(LPF)}$	–3dB cut-off frequency, analog LPF (DAC filter)	note 2	–	8	–	MHz
$V_{CM(COMP)}$	comparator common mode voltage	note 3	1.0	1.16	1.4	V
$R_{i(COMP)}$	comparator input resistance	note 4	17	26	35	kΩ
$V_{IO(COMP)}$	comparator offset voltage	note 4	–	–	45	mV
Serial interface						
$f_{clk(SIO)}$	serial i/f clock		–	–	$\frac{1}{4}f_s$	MHz
$t_{su(D-CLK)}$	set-up time: data-to-clock		10	–	–	ns
$t_{h(D-CLK)}$	hold time: data-to-clock	note 5	$t_s + 10$	–	–	ns
$t_{d(1)}$	delay clock: new data		–	–	$2t_s + 10$	ns
$t_{d(2)}$	delay clock: old data		t_s	–	–	ns
$t_{su(EN-CLK)}$	set-up time: enable-to-clock		$t_s + 10$	–	–	ns
$t_{h(EN-CLK)}$	hold time: enable-to-clock		$t_s + 10$	–	–	ns
Digital read section						
t_{CLKINH}	CLKIN HIGH time		15	–	–	ns
t_{CLKINL}	CLKIN LOW time		15	–	–	ns
t_{RDL}	RD LOW time		t_s	–	$2t_s + 10$	ns
$t_{su(SRD-RRC)}$	set-up time: SRD-to-RRC	note 6	$t_{CLKINL} - 5 - 0.2C_{o(L)(SRD)}$	–	$t_{CLKINL} + 2 - 0.2C_{o(L)(RRC)}$	ns
$t_{h(SRD-RRC)}$	hold time: SRD-to-RRC	note 6	$t_{CLKINH} - 2 - 0.2C_{o(L)(RRC)}$	–	–	ns
t_{RRCL}	RRC LOW time	note 6	$t_{CLKINL} - 5 - 0.2C_{o(L)(RRC)}$	–	t_{CLKINL}	ns
$t_{su(AUX-CLKIN)}$	input set-up time: AUXBUS-to-CLKIN (pin 6)		–	–	–	ns
$t_{h(AUX-CLKIN)}$	input hold time: AUXBUS-to-CLKIN (pin 6)		–	–	–	ns
t_{PACLKH}	PACLK HIGH time	note 7	$t_{CLKINH} - 2 - 0.2C_{o(L)(PACLK)}$	–	t_{CLKINH}	ns
t_{PACLKL}	PACLK LOW time	note 7	$t_{CLKINL} - 5 - 0.2C_{o(L)(PACLK)}$	–	t_{CLKINL}	ns
$t_{d(AUX-PACLK)}$	delay: AUXBUS-to-PACLK (pin 29)	note 8	–	–	$10 + 0.2C_{o(L)(AUX)}$	ns
$t_{d(PACLK-AUX)}$	delay: PACLK to AUXBUS	notes 7 and 8	–	–	$5 + 0.2C_{o(L)(PACLK)}$	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Write equalization section						
$f_{clk(WEQ)}$	WEQ clock frequency	N2 = 1 or N3 = 1; see Table 14	–	–	36	MHz
		N6 =1; see Table 14	–	24	24	MHz
t_{WEQL}	WEQ LOW time		10	–	–	ns
t_{WEQH}	WEQ HIGH time		10	–	–	ns
$t_{su(WD\text{-}WEQCLK)}$	setup time: WDIN-to-WEQCLK	N2 = 1 or N3 = 1; see Table 14	5	–	–	ns
$t_{h(WD\text{-}WEQCLK)}$	hold time: WD-to-WEQCLK	N2 = 1 or N3 = 1; see Table 14	10	–	–	ns
$t_{IL(WDIN)}$	WDIN input LOW time (WDI mode)	WDI_I = 0; see Table 15	10	–	–	ns
$t_{OL(WDOUT)}$	WDOUT output LOW time (WDI mode)	note 9	$t_{WEQH} - 2 - 0.2 \times C_{o(L)(WDOUT)}$	–	t_{WEQH}	ns
$\Delta f_{o(WDIN\text{-}WEQCLK)}$	frequency offset WDIN-WEQCLK	N6 = 1; see Table 14	0.5	–	–	%

Notes

1. Pins 3, 4, 6, 9 to 20, 22, 23, 24, 30 and 31.
2. Measured at pins 39 and 44 with a 10 MΩ/15 pF load.
3. Measured at pins 40 and 43.
4. Differential pins 40 and 43.
5. $t_s = \frac{1}{f_s}$
6. $C_{o(L)(SRD)}$ is the external load (pF), at SRD (pin 27) for $C_{o(L)(SRD)} < 50$ pF.
   $C_{o(L)(RRC)}$ is the external load (pF), at RRC (pin 25) for $C_{o(L)(RRC)} < 50$ pF.
7. $C_{o(L)(PACLK)}$ is the external load (pF), at PACLK (pin 29) for $C_{o(L)(PACLK)} < 50$ pF.
8. $C_{o(L)(AUX)}$ is the external load (pF), at AUX0 to AUX7 (pins 11 to 18) for $C_{o(L)(AUX)} < 50$ pF.
9. $C_{o(L)(WDOUT)}$ is the external load (pF), at WDOUT (pin 11) for $C_{o(L)(WDOUT)} < 50$ pF.

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TIMING DIAGRAMS

Serial interface

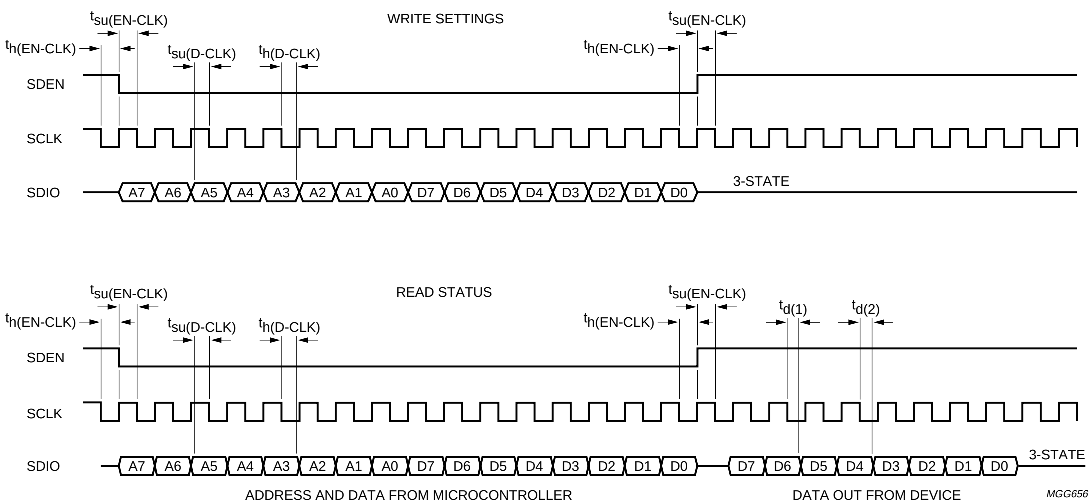

Fig.8 Serial I/O showing set-up, hold and delay timing.

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Digital read section

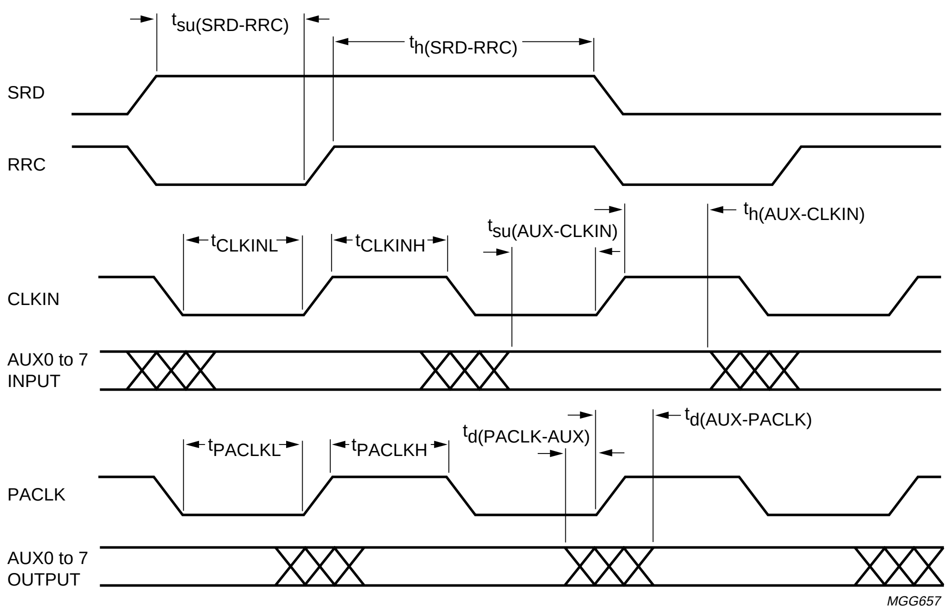

Fig.9 Digital read section showing set-up, hold and delay timing.

Write equalization section

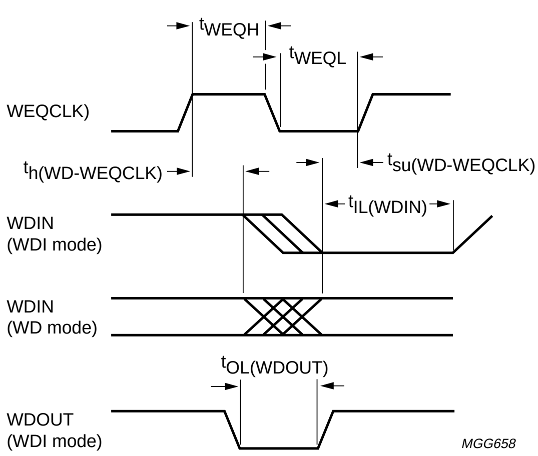

Fig.10 WEQ section showing set-up and hold timing.

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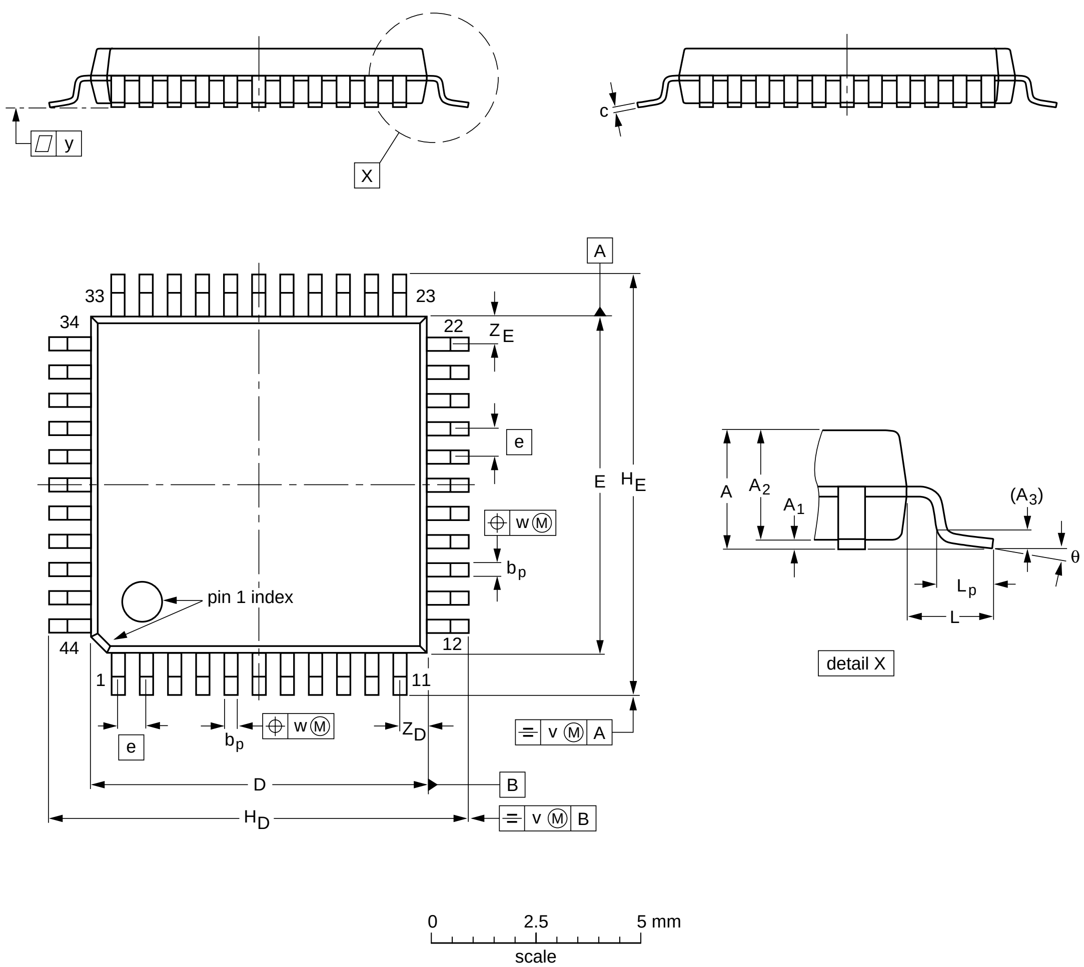
PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**

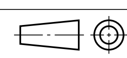


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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