DATA SHEET

SAA7126H; SAA7127H
Digital video encoder

Product specification
File under Integrated Circuits, IC22

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Philips
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Digital video encoder SAA7126H; SAA7127H

FEATURES

- Monolithic CMOS 3.3 V device, 5 V I²C-bus optionally
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- 54 MHz double-speed multiplexed D1 interface capable of splitting data into two separate channels (encoded and baseband)
- Four Digital-to-Analog Converters (DACs) for CVBS (CSYNC, VBS), RED (Cr, C), GREEN (Y, VBS) and BLUE (Cb, CVBS) two times oversampled (signals in parenthesis are optionally). RED (Cr), GREEN (Y) and BLUE (Cb) signal outputs with 9-bit resolution, whereas all other signal outputs have 10-bit resolution; CSYNC is an advanced composite sync on the CVBS output for RGB display centring.
- Real-time control of subcarrier
- Cross-colour reduction filter
- Closed captioning encoding and World Standard Teletext (WST) and North-American Broadcast Text System (NABTS) teletext encoding including sequencer and filter
- Copy Generation Management System (CGMS) encoding (CGMS described by standard CPR-1204 of EIAJ); 20 bits in lines 20/283 (NTSC) can be loaded via the I²C-bus
- Fast I²C-bus control port (400 kHz)
- Line 23 Wide Screen Signalling (WSS) encoding
- Video Programming System (VPS) data encoding in line 16 (CCIR line count)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Macrovision Pay-per-View copy protection system rev. 7.01 and rev. 6.1 as option; 'handsfree' Macrovision pulse support through on-chip timer for pulse amplitude modulation; this applies to SAA7126H only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- Controlled rise/fall times of output syncs and blanking
- On-chip crystal oscillator (3rd-harmonic or fundamental crystal)
- Down mode (low output voltage) or power-save mode of DACs
- QFP44 package.

GENERAL DESCRIPTION

The SAA7126H; SAA7127H encodes digital Cb-Y-Cr video data to an NTSC or PAL CVBS or S-video signal. Simultaneously, RGB or bypassed but interpolated Cb-Y-Cr signals are available via three additional Digital-to-Analog Converters (DACs). The circuit at a 54 MHz multiplexed digital D1 input port accepts two CCIR compatible Cb-Y-Cr data streams with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data with overlay and MPEG decoded data without overlay, whereas one data stream is latched at the rising, the other one at the falling clock edge.

It includes a sync/clock generator and on-chip DACs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7126H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
SAA7127H			

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.15	3.3	3.45	V
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
I_{DDA}	analog supply current	–	77	100	mA
I_{DDD}	digital supply current	–	37	46	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	1.30	1.45	1.55	V
R_L	load resistance	75	–	300	Ω
$LE_{lf(i)}$	low frequency integral linearity error	–	–	±3	LSB
$LE_{lf(d)}$	low frequency differential linearity error	–	–	±1	LSB
T_{amb}	ambient temperature	0	–	70	°C

BLOCK DIAGRAM

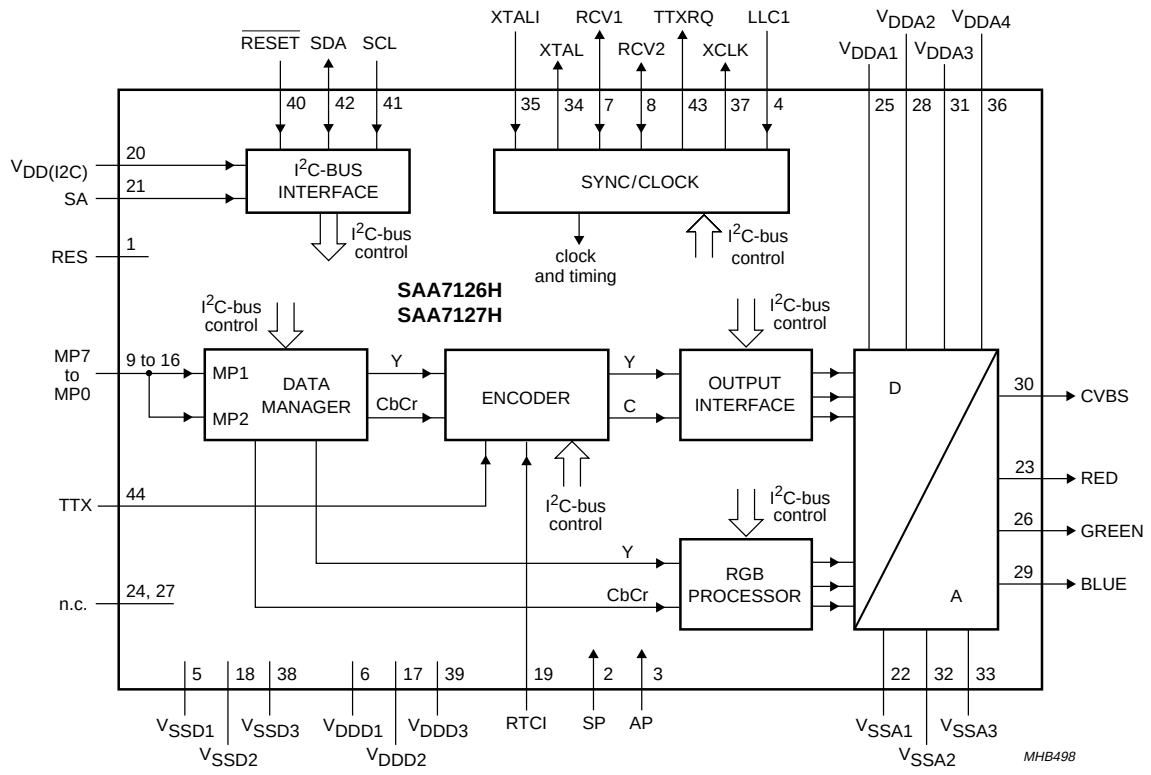


Fig.1 Block diagram.

PINNING

SYMBOL	TYPE	PIN	DESCRIPTION
RES	–	1	reserved pin; do not connect
SP	I	2	test pin; connected to digital ground for normal operation
AP	I	3	test pin; connected to digital ground for normal operation
LLC1	I	4	line-locked clock input; this is the 27 MHz master clock
V_{SSD1}	–	5	digital ground 1
V_{DDD1}	–	6	digital supply voltage 1
RCV1	I/O	7	raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal
RCV2	I/O	8	raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse
MP7	I	9	double-speed 54 MHz MPEG port; it is an input for *"CCIR 656"* style multiplexed Cb-Y-Cr data; data is sampled on the rising and falling clock edge; data sampled on the rising edge is then sent to the encoding part of the device; data sampled on the falling edge is sent to the RGB part of the device (or vice versa, depending on programming)
MP6	I	10	
MP5	I	11	
MP4	I	12	
MP3	I	13	
MP2	I	14	
MP1	I	15	
MP0	I	16	
V_{DDD2}	–	17	digital supply voltage 2
V_{SSD2}	–	18	digital ground 2
RTCI	I	19	real-time control input (I^2C-bus register SRES = 0): if the LLC1 clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality. Sync reset input (I^2C-bus register SRES = 1): a HIGH impulse resets synchronization of the encoder (first field, first line).
$V_{DD(I2C)}$	–	20	sense input for I^2C-bus voltage; connect to I^2C-bus supply
SA	I	21	select I^2C-bus address; LOW selects slave address 88H, HIGH selects slave address 8CH
V_{SSA1}	–	22	analog ground 1 for RED (Cr) (C) and GREEN (Y) (VBS) outputs
RED	O	23	analog output of RED (Cr) or (C) signal
n.c.	–	24	not connected
V_{DDA1}	–	25	analog supply voltage 1 for RED (Cr) (C) output
GREEN	O	26	analog output of GREEN (Y) or (VBS) signal
n.c.	–	27	not connected
V_{DDA2}	–	28	analog supply voltage 2 for GREEN (Y) (VBS) output
BLUE	O	29	analog output of BLUE (Cb) or (CVBS) signal
CVBS	O	30	analog output of CVBS (CSYNC) or (VBS) signal
V_{DDA3}	–	31	analog supply voltage 3 for BLUE (Cb) (CVBS) and CVBS (CSYNC) (VBS) outputs
V_{SSA2}	–	32	analog ground 2 for BLUE (Cb) (CVBS) and CVBS (CSYNC) (VBS) outputs
V_{SSA3}	–	33	analog ground 3 for the DAC reference ladder and the oscillator
XTAL	O	34	crystal oscillator output
XTALI	I	35	crystal oscillator input; if the oscillator is not used, this pin should be connected to ground
V_{DDA4}	–	36	analog supply voltage 4 for the DAC reference ladder and the oscillator

SYMBOL	TYPE	PIN	DESCRIPTION
XCLK	O	37	clock output of the crystal oscillator
V_{SSD3}	–	38	digital ground 3
V_{DDD3}	–	39	digital supply voltage 3
$\overline{RESET}$	I	40	reset input, active LOW. After reset is applied, all digital I/Os are in input mode; PAL black burst on CVBS, VBS and C; RGB outputs set to lowest voltage. The I^2C-bus receiver waits for the START condition.
SCL	I	41	I^2C-bus serial clock input
SDA	I/O	42	I^2C-bus serial data input/output
TTXRQ	O	43	teletext request output, indicating when text bits are requested
TTX	I	44	teletext bit stream input

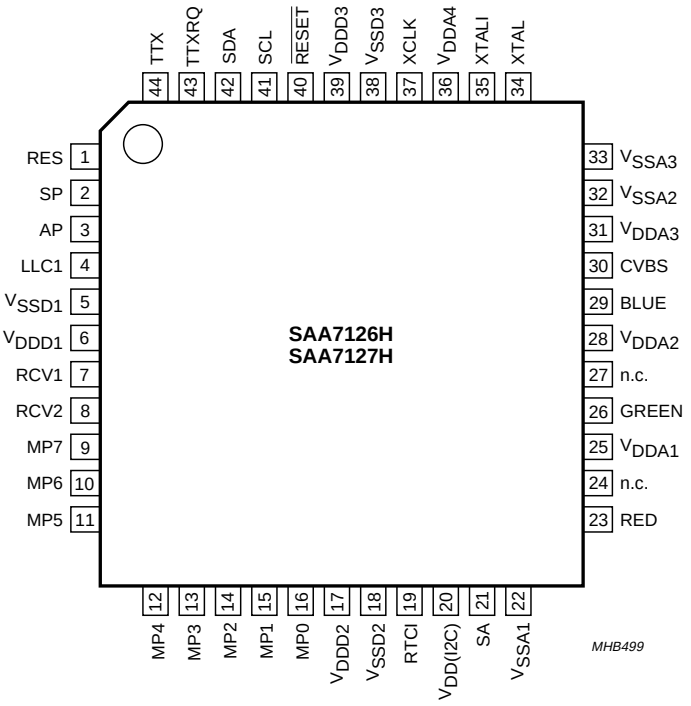


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital video encoder encodes digital luminance and colour difference signals into analog CVBS, S-video and simultaneously RGB or Cr-Y-Cb signals. NTSC-M, PAL B/G and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"ITU-R BT.470-3"*.

For ease of analog post filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

The total filter transfer characteristics are illustrated in Figs 3 to 8. The DACs for Y, C and CVBS are realized with full 10-bit resolution; 9-bit resolution for RGB output. The Cr-Y-Cb to RGB dematrix can be bypassed optionally in order to provide the upsampled Cr-Y-Cb input signals.

The 8-bit multiplexed Cb-Y-Cr formats are *"CCIR 656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally; when the device is operated in slave mode. Two independent data streams can be processed, one latched by the rising edge of LLC1, the other latched by the falling edge of LLC1. The purpose of that is e.g. to forward one of the data streams containing both video and On Screen Display (OSD) information to the RGB outputs, and the other stream containing video only to the encoded outputs CVBS and S-video.

For optimum display of RGB signals through a euro-connector TV set, an early composite sync pulse (up to 31LLC1 clock periods) can be provided optionally on the CVBS output.

It is also possible to connect a Philips digital video decoder (SAA7111, SAA7711A, SAA7112 or SAA7151B) to the SAA7126H; SAA7127H. Information concerning the actual subcarrier, PAL-ID and (with SAA7111 and newer types) definite subcarrier phase can be inserted via the RTCI pin, connected to the RTCO pin of a decoder.

The SAA7126H; SAA7127H synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCR's is loadable via the I^2C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision. It is also possible to load data for copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to the input mode and the encoder is set to PAL mode and outputs a 'black burst' signal on CVBS and S-video outputs, while RGB outputs are set to their lowest output voltages. A reset forces the I^2C-bus interface to abort any running bus transfer.

Data manager

In the data manager, alternatively to the external video data, a pre-defined colour look-up table located in this block can be read out in a pre-defined sequence (8 steps per active video line), achieving a colour bar test pattern generator without need for an external data source.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes, a blanking level can be set. Other manipulations used for the Macrovision anti-taping process such as additional insertion of AGC super-white pulses (programmable in height) are supported by SAA7126H only.

In order to enable easy analog post filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. The transfer characteristic of the luminance interpolation filter are illustrated in Figs 5 and 6. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 3 and 4.

The amplitude, beginning and ending of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on the subcarrier.

The numeric ratio between the Y and C outputs is in accordance with set standards.

TELETEXT INSERTION AND ENCODING

Pin TTX receives a WST or NABTS teletext bitstream sampled at the LLC clock. Two protocols are provided: at each rising edge of output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX. Or: the signal TTXRQ performs only a single LOW-to-HIGH transition and remains at HIGH level for 360, 296 or 288 teletext bits, depending on the chosen standard.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which are selectable independently for both fields. The internal insertion window for text is set to 360 (PAL-WST), 296 (NTSC-WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.14.

VIDEO PROGRAMMING SYSTEM (VPS) ENCODING

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21).
Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

ANTI-TAPING (SAA7126H ONLY)

For more information contact your nearest Philips Semiconductors sales office.

RGB processor

This block contains a dematrix in order to produce red, green and blue signals to be fed to a SCART plug.

Before Y, Cb and Cr signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 7 and 8.

Output interface/DACs

In the output interface, encoded Y and C signals are converted from digital-to-analog in a 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay (equal to 51 LLC clock periods, measured from MP input to the analog outputs) as the Y, C and RGB outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Red, green and blue signals are also converted from digital-to-analog, each providing a 9-bit resolution.

Outputs of the DACs can be set together via software control to minimum output voltage (approximately 0.2 V DC) for either purpose. Alternatively, the buffers can be switched into 3-state output condition; this allows for ‘wired AND’ing with other 3-state outputs and can also be used as a power-save mode.

Synchronization

The synchronization of the SAA7126H; SAA7127H is able to operate in two modes; slave mode and master mode.

In master mode (see Fig.10), the circuit generates all necessary timings in the video signal itself, and it can provide timing signals at the RCV1 and RCV2 ports. In slave mode, it accepts timing information either from the RCV pins or from the embedded timing data of the CCIR 656 data stream.

For the SAA7126H; SAA7127H, the only difference between master and slave mode is that it ignores the timing information at its inputs in master mode. Thus, if in slave mode, any timing information is missing, the IC will continue running free without a visible effect. But there must not be any additional pulses (with wrong phase) because the circuit will not ignore them.

In slave mode (see Fig.9), an interface circuit decides, which signal is expected at the RCV1 port and which information is taken from its active slope. The polarity can be chosen, if PRCV1 is logic 0 the rising slope will be active.

The signal can be:

- A Vertical Sync (VS) pulse; the active slope sets the vertical phase
- An odd/even signal; the active slope sets the vertical phase, the internal field flag to odd and optionally sets the horizontal phase
- A Field Sequence (FSEQ) signal; it marks the first field of the 4 (NTSC) or 8 (PAL) field sequence. In addition to the odd/even signal, it also sets the PAL phase and optionally defines the subcarrier phase.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The horizontal phase can be set via a separate input RCV2. In the event of VS pulses at RCV1, this is mandatory. It is also possible to set the signal path to blank via this input.

From the CCIR 656 data stream, the SAA7126H; SAA7127H decodes only the start of the first line in the odd field. All other information is ignored and may miss. If this kind of slave mode is active, the RCV pins may be switched to output mode.

In slave mode, the horizontal trigger phase can be programmed to any point in the line, the vertical phase from line 0 to line 15 counted from the first serration pulse in half line steps.

Whenever a synchronization information cannot be derived directly from the inputs, the SAA7126H; SAA7127H will calculate it from the internal horizontal, vertical and PAL phase. This gives good flexibility with respect to external synchronization but the circuit does not suppress illegal settings. In such an event, e.g the odd/even information may vanish as it does in the non-interlaced modes.

In master mode, the line lengths are fixed to 1728 clocks at 50 Hz and 1716 clocks at 60 Hz. To allow non-interlaced frames, the field lengths can be varied by ±0.5 lines. In the event of non-interlace, the SAA7126H; SAA7127H does not provide odd/even information and the output signal does not contain the PAL ‘Bruch sequence’.

At the RCV1 pin the IC can provide:

- A Vertical Sync (VS) signal with 2.5 (50 Hz) or 3 (60 Hz) lines duration
- An odd/even signal which is LOW in odd fields
- A Field Sequence (FSEQ) signal which is HIGH in the first field of the 4 or 8 field sequence.

At the RCV2 pin, there is a horizontal pulse of programmable phase and duration available. This pulse can be suppressed in the programmable inactive part of a field giving a composite blank signal.

The directions and polarities of the RCV ports can be chosen independently. Timing references can be found in Tables 29 and 37.

Clock

The input at LLC1 can either be an external clock source or the buffered on-chip clock XCLK. The internal crystal oscillator can be run with either a 3rd-harmonic or a fundamental crystal.

I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and readable, except one read only status byte.

The I²C-bus slave address is defined as 88H with pin 21 (SA) tied LOW and as 8CH with pin 21 (SA) tied HIGH.

Input levels and formats

The SAA7126H; SAA7127H expects digital Y, Cb, Cr data with levels (digital codes) in accordance with *"CCIR 601"*.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively Cr-Y-Cb path features a gain setting individually for luminance (GY) and colour difference signals (GCD).

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 *"CCIR 601"* signal component levels

COLOUR	SIGNALS(1)					
	Y	Cb	Cr	R(2)	G(2)	B(2)
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

Notes

1. Transformation:
   a) $R = Y + 1.3707 \times (Cr - 128)$
   b) $G = Y - 0.3365 \times (Cb - 128) - 0.6982 \times (Cr - 128)$
   c) $B = Y + 1.7324 \times (Cb - 128)$.
2. Representation of R, G and B (or Cr, Y and Cb) at the output is 9 bits at 27 MHz.

Table 2 8-bit multiplexed format (similar to *"CCIR 601"*)

TIME	BITS							
	0	1	2	3	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 3 Slave receiver (slave address 88H)

REGISTER FUNCTION	SUB ADDR (HEX)	DATA BYTE[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte (read only)	00H	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Null	01H to 25H	0	0	0	0	0	0	0	0
Wide screen signal	26H	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27H	WSSON	0	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28H	DECCOL	DECFIS	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29H	SRES	0	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2AH	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2BH	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2CH	CGEN	0	0	0	CG19	CG18	CG17	CG16
Output port control	2DH	VBSEN1	VBSEN0	CVBSEN	CEN	CVBSTRI	RTRI	GTRI	BTRI
Null	2EH to 37H	0	0	0	0	0	0	0	0
Gain luminance for RGB	38H	0	0	0	GY4	GY3	GY2	GY1	GY0
Gain colour difference for RGB	39H	0	0	0	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3AH	CBENB	0	0	SYMP	DEMOFF	CSYNC	MP2C2	MP2C1
VPS enable, input control 2	54H	VPSEN	CCIRS	0	0	0	0	EDGE2	EDGE1
VPS byte 5	55H	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56H	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57H	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58H	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59H	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5AH	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5BH	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5CH	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, real-time control, black level	5DH	GAINU8	DECOE	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, real-time control, blanking level	5EH	GAINV8	DECPH	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5FH	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60H	0	0	0	0	0	0	0	0
Standard control	61H	DOWNB	DOWNA	INPI	YGS	0	SCBW	PAL	FISE

REGISTER FUNCTION	SUB ADDR (HEX)	DATA BYTE[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
RTC enable, burst amplitude	62H	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63H	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64H	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65H	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66H	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67H	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68H	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69H	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6AH	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6BH	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6CH	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6DH	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6EH	SBLBN	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLCO
Closed caption, teletext enable	6FH	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70H	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71H	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72H	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73H	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H delay, length	74H	TTXHL3	TTXHL2	TTXHL1	TTXHL0	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance, Vsync shift	75H	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	VS_S2	VS_S1	VS_S0
TTX odd request vertical start	76H	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77H	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78H	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request vertical end	79H	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7AH	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7BH	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7CH	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7DH	0	0	0	0	0	0	0	0
Disable TTX line	7EH	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7FH	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13

Note

1. All bits labelled '0' are reserved. They **must** be programmed with logic 0.

I²C-bus format

Table 4 I²C-bus address; see Table 5

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 5 Explanation of Table 4

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X; note 1
ACK	acknowledge, generated by the slave
Subaddress; note 2	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.
2. If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Slave receiver

Table 6 Subaddresses 26H and 27H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
WSS	–	wide screen signalling bits 3 to 0 = aspect ratio 7 to 4 = enhanced services 10 to 8 = subtitles 13 to 11 = reserved
WSSON	0	wide screen signalling output is disabled; default after reset
	1	wide screen signalling output is enabled

Table 7 Subaddress 28H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
BS	–	starting point of burst in clock cycles	PAL: BS = 33 (21H); default after reset
			NTSC: BS = 25 (19H)
DECCOL	0	disable colour detection bit of RTCI input	
	1	enable colour detection bit of RTCI input	bit RTCE must be set to logic 1 (see Fig.13)
DECFIS	0	field sequence as FISE in subaddress 61	
	1	field sequence as FISE bit in RTCI input	bit RTCE must be set to logic 1 (see Fig.13)

Table 8 Subaddress 29H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
BE	–	ending point of burst in clock cycles	PAL: BE = 29 (1DH); default after reset
			NTSC: BE = 29 (1DH)
SRES	0	pin 19 is Real-Time Control Input (RTCI)	
	1	pin 19 is Sync Reset input (SRES)	a HIGH impulse resets synchronization of the encoder (first field, first line)

Table 9 Subaddresses 2AH to 2CH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CG	–	LSB of the respective bytes are encoded immediately after run-in, the MSBs of the respective bytes have to carry the CRCC bits, in accordance with the definition of copy generation management system encoding format.
CGEN	0	copy generation data output is disabled; default after reset
	1	copy generation data output is enabled

Table 10 Subaddress 2DH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
BTRI	0	DAC for BLUE output in 3-state mode (high-impedance)
	1	DAC for BLUE output in normal operation mode; default after reset
GTRI	0	DAC for GREEN output in 3-state mode (high-impedance)
	1	DAC for GREEN output in normal operation mode; default after reset
RTRI	0	DAC for RED output in 3-state mode (high-impedance)
	1	DAC for RED output in normal operation mode; default after reset
CVBSTRI	0	DAC for CVBS output in 3-state mode (high-impedance)
	1	DAC for CVBS output in normal operation mode; default after reset
CEN	0	RED output signal is switched to R DAC; default after reset
	1	chrominance output signal is switched to R DAC
CVBSEN	0	BLUE output signal is switched to B DAC; default after reset
	1	CVBS output signal is switched to B DAC
VBSEN0	0	if CSYNC = 0, CVBS output signal is switched to CVBS DAC; default after reset
	1	if CSYNC = 0, luminance (VBS) output signal is switched to CVBS DAC
VBSEN1	0	GREEN output signal is switched to G DAC; default after reset
	1	luminance (VBS) output signal is switched to G DAC

Table 11 Subaddresses 38H and 39H

DATA BYTE	DESCRIPTION
GY0 to GY4	gain luminance of RGB (Cr, Y and Cb) output, ranging from (1 – $^{16}/_{32}$) to (1 + $^{15}/_{32}$). Suggested nominal value = –6 (11010b), depending on external application.
GCD0 to GCD4	gain colour difference of RGB (Cr, Y and Cb) output, ranging from (1 – $^{16}/_{32}$) to (1 + $^{15}/_{32}$). Suggested nominal value = –6 (11010b), depending on external application.

Table 12 Subaddress 3AH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
MP2C1	0	input data is twos complement from MP1 input port (encoder path)
	1	input data is straight binary from MP1 input port; default after reset
MP2C2	0	input data is twos complement from MP2 input port (RGB path)
	1	input data is straight binary from MP2 input port; default after reset
CSYNC	0	If VBSEN0 = 0, CVBS output signal is switched to CVBS DAC. If VBSEN0 = 1, luminance output signal is switched to CVBS DAC; default after reset.
	1	advanced composite sync is switched to CVBS DAC
DEMOFF	0	Y, Cb and Cr for RGB dematrix is active; default after reset
	1	Y, Cb and Cr for RGB dematrix is bypassed
SYMP	0	horizontal and vertical trigger is taken from RCV2 and RCV1 respectively; default after reset
	1	horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP port
CBENB	0	data from input ports is encoded; default after reset
	1	colour bar with fixed colours is encoded

Table 13 Subaddress 54H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
EDGE1	0	MP1 data is sampled on the rising clock edge; default after reset
	1	MP1 data is sampled on the falling clock edge
EDGE2	0	MP2 data is sampled on the rising clock edge; default after reset
	1	MP2 data is sampled on the falling clock edge
CCIRS	0	If SYMP = 1, horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP2 port; default after reset.
	1	If SYMP = 1, horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP1 port.
VPSEN	0	video programming system data insertion is disabled; default after reset
	1	video programming system data insertion in line 16 is enabled

Table 14 Subaddresses 55H to 59H

DATA BYTE	DESCRIPTION	REMARKS
VPS5	fifth byte of video programming system data	LSBs of the respective bytes are encoded immediately after run-in and framing code in line 16; all other bytes are not relevant for VPS
VPS11	eleventh byte of video programming system data	
VPS12	twelfth byte of video programming system data	
VPS13	thirteenth byte of video programming system data	
VPS14	fourteenth byte of video programming system data	

Table 15 Subaddress 5AH

DATA BYTE	DESCRIPTION	VALUE	RESULT
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees	6BH	PAL-B/G and data from input ports
		95H	PAL-B/G and data from look-up table
		A3H	NTSC-M and data from input ports
		46H	NTSC-M and data from look-up table

Table 16 Subaddresses 5BH and 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINU = –2.17 × nominal to +2.16 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE	GAINU = –2.05 × nominal to +2.04 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Table 17 Subaddresses 5CH and 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINV = –1.55 × nominal to +1.55 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE	GAINV = –1.46 × nominal to +1.46 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Table 18 Subaddress 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation in accordance with *"CCIR 601"*	white-to-sync = 140 IRE; note 1	recommended value: BLCKL = 58 (3AH)
		BLCKL = 0; note 1	output black level = 29 IRE
		BLCKL = 63 (3FH); note 1	output black level = 49 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLCKL = 51 (33H)
		BLCKL = 0; note 2	output black level = 27 IRE
		BLCKL = 63 (3FH); note 2	output black level = 47 IRE
DECOE	real-time control	logic 0	disable odd/even field control bit from RTCI
		logic 1	enable odd/even field control bit from RTCI (see Fig.13)

Notes

1. Output black level/IRE = BLCKL × 2/6.29 + 28.9.
2. Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 19 Subaddress 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE; note 1	recommended value: BLNNL = 46 (2EH)
		BLNNL = 0; note 1	output blanking level = 25 IRE
		BLNNL = 63 (3FH); note 1	output blanking level = 45 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLNNL = 53 (35H)
		BLNNL = 0; note 2	output blanking level = 26 IRE
		BLNNL = 63 (3FH); note 2	output blanking level = 46 IRE
DECPH	real-time control	logic 0	disable subcarrier phase reset bit from RTCI
		logic 1	enable subcarrier phase reset bit from RTCI (see Fig.13)

Notes

1. Output black level/IRE = BLNNL × 2/6.29 + 25.4.
2. Output black level/IRE = BLNNL × 2/6.18 + 25.9; default after reset: 35H.

Table 20 Subaddress 5FH

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL
CCRS	select cross-colour reduction filter in luminance; see Table 21

Table 21 Logic levels and function of CCRS

CCRS1	CCRS0	DESCRIPTION
0	0	no cross-colour reduction; for overall transfer characteristic of luminance see Fig.5
0	1	cross-colour reduction #1 active; for overall transfer characteristic see Fig.5
1	0	cross-colour reduction #2 active; for overall transfer characteristic see Fig.5
1	1	cross-colour reduction #3 active; for overall transfer characteristic see Fig.5

Table 22 Subaddress 61H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); default after reset
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal if RTC is enabled (see Table 23)
DOWNA	0	DAC for CVBS in normal operational mode; default after reset
	1	DAC for CVBS forced to lowest output voltage
DOWNB	0	DACs for R, G and B in normal operational mode
	1	DACs for R, G and B forced to lowest output voltage; default after reset

Table 23 Subaddress 62AH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real-time control of generated subcarrier frequency; default after reset
	1	real-time control of generated subcarrier frequency through SAA7151B or SAA7111; for timing see Fig.13

Table 24 Subaddress 62BH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 2.02 × nominal	recommended value: BSTA = 63 (3FH)
		white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 2.82 × nominal	recommended value: BSTA = 45 (2DH)
		white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.90 × nominal	recommended value: BSTA = 67 (43H)
		white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 3.02 × nominal	recommended value: BSTA = 47 (2FH); default after reset

Table 25 Subaddresses 63H to 66H (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$; note 1	FSC3 = most significant byte; FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 26 Subaddresses 67H to 6AH

DATA BYTE	DESCRIPTION	REMARKS
L21O0	first byte of captioning data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.
L21O1	second byte of captioning data, odd field	
L21E0	first byte of extended data, even field	
L21E1	second byte of extended data, even field	

Table 27 Subaddress 6BH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	If ORCV2 = HIGH, pin RCV2 provides an HREF signal (horizontal reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking interval); default after reset. If ORCV2 = LOW and bit SYMP = LOW, the signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset.
	1	If ORCV2 = HIGH, pin RCV2 provides a 'composite-blanking-not' signal, for example a reference pulse that is defined by RCV2S and RCV2E, excluding vertical blanking interval, which is defined by FAL and LAL. If ORCV2 = LOW and bit SYMP = LOW, the signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal.
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of *"CCIR 656"* input (at bit SYMP = HIGH); default after reset
	1	horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)
SRCV1	–	defines signal type on pin RCV1; see Table 28

Table 28 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	not applicable	not applicable	–

Table 29 Subaddresses 6CH and 6DH

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals; reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 39H

Table 30 Subaddress 6DH

DATA BYTE	DESCRIPTION
VTRIG	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1FH)

Table 31 Subaddress 6EH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or RS170A (60 Hz)
BLCKON	0	encoder in normal operation mode
	1	output signal is forced to blanking level; default after reset
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 32
LDEL	–	selects the delay on luminance path with reference to chrominance path; see Table 33
FLC	–	field length control; see Table 34

Table 32 Logic levels and function of PHRES

DATA BYTE		DESCRIPTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 33 Logic levels and function of LDEL

DATA BYTE		DESCRIPTION
LDEL1	LDEL0	
0	0	no luminance delay; default after reset
0	1	1 LLC luminance delay
1	0	2 LLC luminance delay
1	1	3 LLC luminance delay

Table 34 Logic levels and function of FLC

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 35 Subaddress 6FH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual line 21 encoding; see Table 36
TTXEN	0	disables teletext insertion; default after reset
	1	enables teletext insertion
SCCLN	–	selects the actual line, where closed caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 36 Logic levels and function of CCEN

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	line 21 encoding off; default after reset
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 37 Subaddresses 70H to 72H

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on RCV2 pin values above 1715 (FISE = 1) or [1727 (FISE = 0)] are not allowed; first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = 11AH [0FDH]
RCV2E	end of output signal on RCV2 pin values above 1715 (FISE = 1) or [1727 (FISE = 0)] are not allowed; last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = 694H (687H)

Table 38 Subaddress 73H

DATA BYTE	DESCRIPTION	REMARKS
TTXHS	start of signal on pin TTXRQ; see Fig.14	PAL: TTXHS = 42H
		NTSC: TTXHS = 54H

Table 39 Subaddress 74H

DATA BYTE	DESCRIPTION	REMARKS
TTXHL	length of TTXRQ window; only active at old TTX protocol: bit TTXO = 1	TTXHL = 0: TTXRQ = 1398LLC; TTXHL = 15: TTXRQ = 1413LLC
TTXHD	indicates the delay in clock cycles between rising edge of TTXRQ output and valid data at pin TTX	minimum value: TTXHD = 2

Table 40 Subaddress 75H

DATA BYTE	DESCRIPTION
VS_S	vertical sync shift between RCV1 and RCV2 (switched to output); in master mode it is possible to shift H-sync (RCV2; CBLF = 0) against V-sync (RCV1; SRCV1 = 00) standard value: VS_S = 3
CSYNCA	advanced composite sync against RGB output from 0LLC to 31LLC

Table 41 Subaddresses 76H, 77H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXOVS	first line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVS + 1) for other systems	PAL: TTXOVS = 05H; NTSC: TTXOVS = 06H
TTXOVE	last line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVE + 3) for M-systems line = TTXOVE for other systems	PAL: TTXOVE = 16H; NTSC: TTXOVE = 10H

Table 42 Subaddresses 78H, 79H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXEVS	first line of occurrence of signal on pin TTXRQ in even field line = (TTXEVS + 4) for M-systems line = (TTXEVS + 1) for other systems	PAL: TTXEVS = 04H; NTSC: TTXEVS = 05H
TTXEVE	last line of occurrence of signal on pin TTXRQ in even field line = (TTXEVE + 3) for M-systems line = TTXEVE for other systems	PAL: TTXEVS = 16H; NTSC: TTXEVS = 10H

Table 43 Subaddress 7CH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
TTXO	0	new TTX protocol selected: at each rising edge of TTXRQ a single TTX bit is requested see Fig.14; default after reset
	1	old TTX protocol selected: the encoder provides a window of TTXRQ going HIGH; the length of the window depends on the chosen TTX standard see Fig.14
TTX60	0	enables NABTS (FISE = 1) or European TTX (FISE = 0); default after reset
	1	enables world standard teletext 60 Hz (FISE = 1)

Table 44 Subaddresses 7AH to 7CH

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems, = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems, = LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

Table 45 Subaddresses 7EH and 7FH

DATA BYTE	DESCRIPTION
LINE	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate) this bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE

In subaddresses 5BH, 5CH, 5DH, 5EH and 62H all IRE values are rounded up.

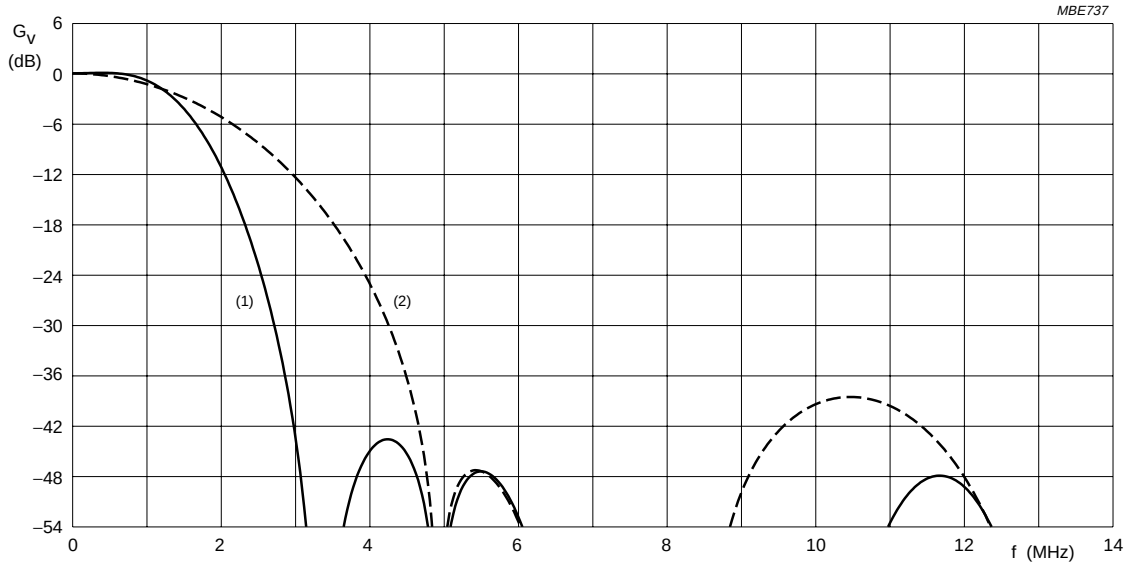
Slave transmitter

Table 46 Slave transmitter (slave address 89H)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	00H	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E

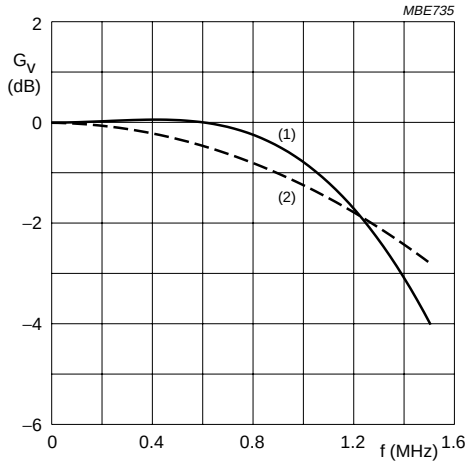
Table 47 Subaddress 00H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 000 binary
CCRDO	1	closed caption bytes of the odd field have been encoded
	0	the bit is reset after information has been written to the subaddresses 67H and 68H; it is set immediately after the data has been encoded
CCRDE	1	closed caption bytes of the even field have been encoded
	0	the bit is reset after information has been written to the subaddresses 69H and 6AH; it is set immediately after the data has been encoded
FSEQ	1	during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields)
	0	not first field of a sequence
O_E	1	during even field
	0	during odd field



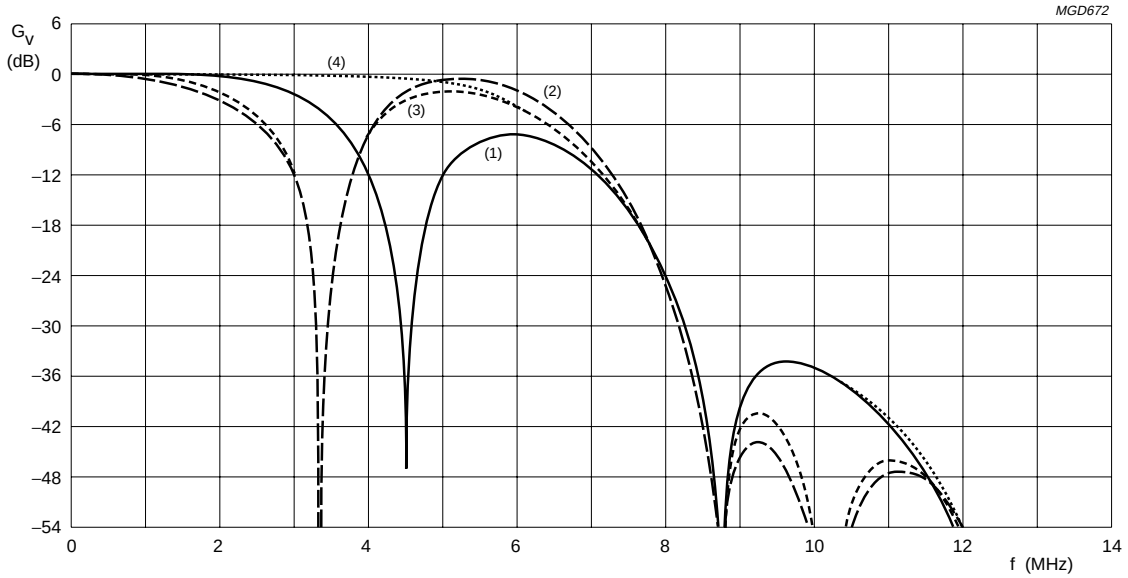
(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



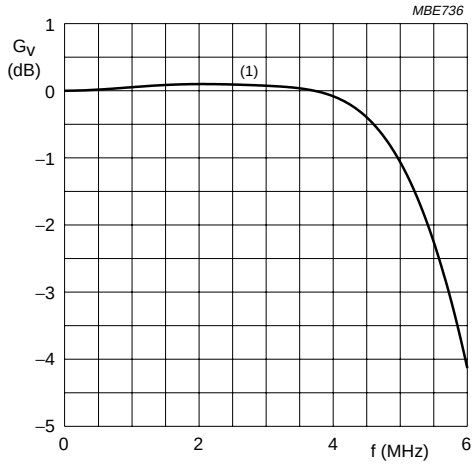
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.5 Luminance transfer characteristic 1.



(1) CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2.

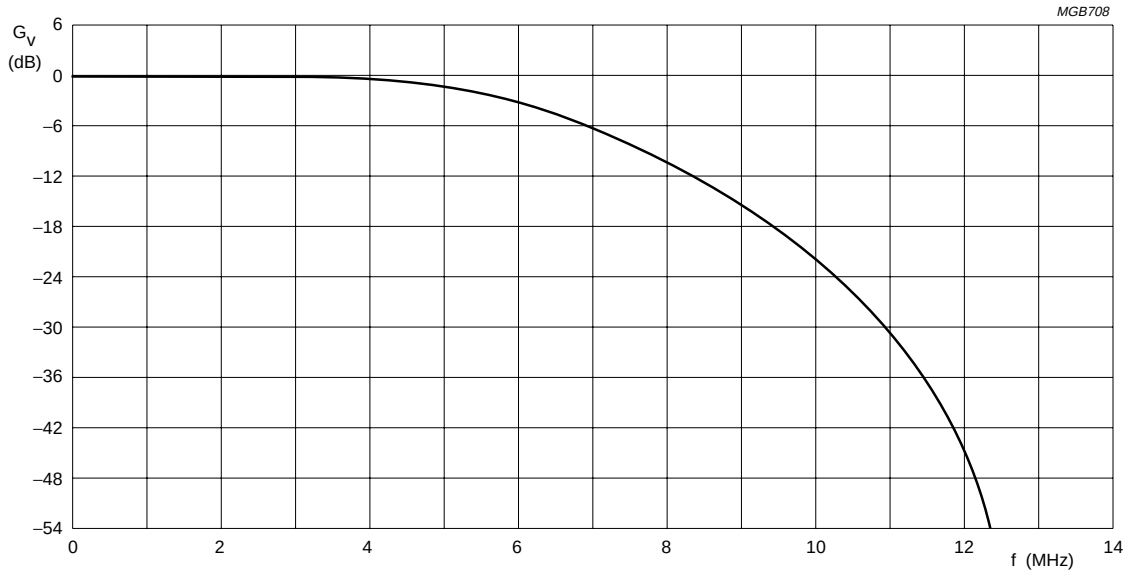


Fig.7 Luminance transfer characteristic in RGB.

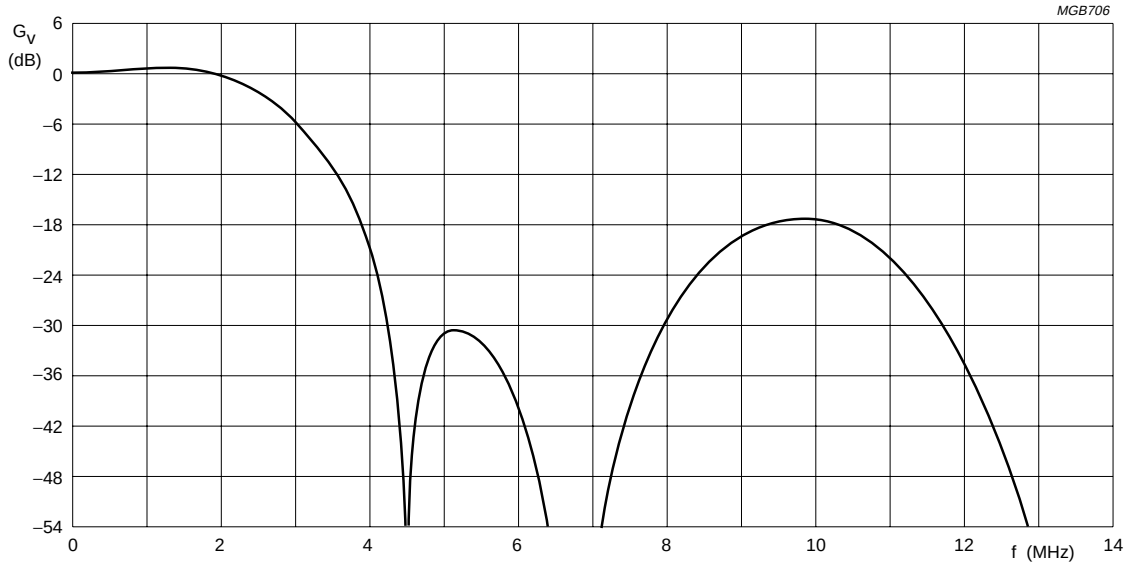
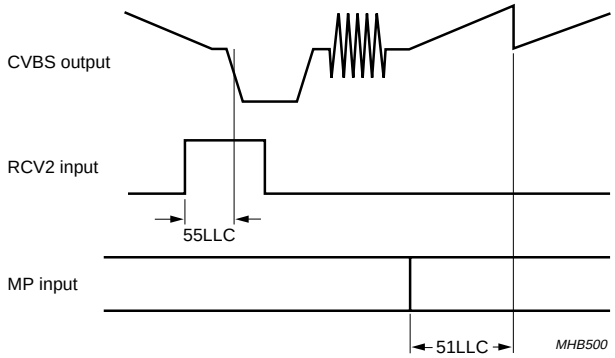
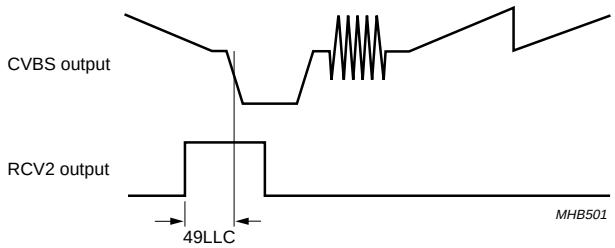


Fig.8 Colour difference transfer characteristic in RGB.



HTRIG = 0
PRCV2 = 0.
TRCV2 = 1.
ORCV2 = 0.

Fig.9 Sync and video input timing.



RCV2S = 0.
PRCV2 = 0.
ORCV2 = 1.

Fig.10 Sync and video output timing.

CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DDA}	analog supply voltage		3.15	3.45	V
V_{DDD}	digital supply voltage		3.0	3.6	V
I_{DDA}	analog supply current	note 1	–	100	mA
I_{DDD}	digital supply current	V_{DDD} = 3.3 V; note 1	–	46	mA
Inputs					
V_{IL}	LOW-level input voltage (pins LLC1, RCV1, RCV2, MP7 to MP0, RTCI, SA, $\overline{\text{RESET}}$ and TTX)		–0.5	+0.8	V
V_{IH}	HIGH-level input voltage (pins LLC1, RCV1, RCV2, MP7 to MP0, RTCI, SA, $\overline{\text{RESET}}$ and TTX)		2.0	V_{DDD} + 0.3	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high-impedance	–	8	pF
Outputs; pins RCV1, RCV2 and TTXRQ					
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA	2.4	–	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW-level input voltage		–0.5	$0.3V_{DD(I2C)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(I2C)}$	$V_{DD(I2C)}$ + 0.3	V
I_i	input current	V_i = LOW or HIGH	–10	+10	µA
V_{OL}	LOW-level output voltage (pin SDA)	I_{OL} = 3 mA	–	0.4	V
I_o	output current	during acknowledge	3	–	mA
Clock timing (pins LLC1 and XCLK)					
T_{LLC1}	cycle time	note 2	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC1}	LLC1 input	40	60	%
	duty factor t_{HIGH}/T_{XCLK}	XCLK output typical 50%	40	60	%
t_r	rise time	note 2	–	5	ns
t_f	fall time	note 2	–	6	ns
Input timing; pins LLC1, RCV1, RCV2, MP7 to MP0, RTCI, SA and TTX					
$t_{SU;DAT}$	input data set-up time		6	–	ns
$t_{HD;DAT}$	input data hold time		3	–	ns
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd-harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 3	–50	+50	10^{-6}

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CRYSTAL SPECIFICATION					
T_{amb}	ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 – 20%	1.5 + 20%	fF
C_0	parallel capacitance (typical)		3.5 – 20%	3.5 + 20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_h	output hold time		4	–	ns
t_d	output delay time		–	25	ns
CVBS and RGB outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 4	1.30	1.55	V
ΔV_o	inequality of output signal voltages		–	2	%
$R_{s(int)}$	internal serial resistance		1	3	Ω
R_L	output load resistance		75	300	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
$LE_{lf(i)}$	low frequency integral linearity error of DACs		–	±3	LSB
$LE_{lf(d)}$	low frequency differential linearity error of DACs		–	±1	LSB
$t_{d(pipe)(MP)}$	total pipeline delay from MP port	27 MHz	–	51	LLC

Notes

1. At maximum supply voltage with highly active input signals.
2. The data is for both input and output direction.
3. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
4. For full digital range, without load, V_{DDA} = 3.3 V. The typical voltage swing is 1.45 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

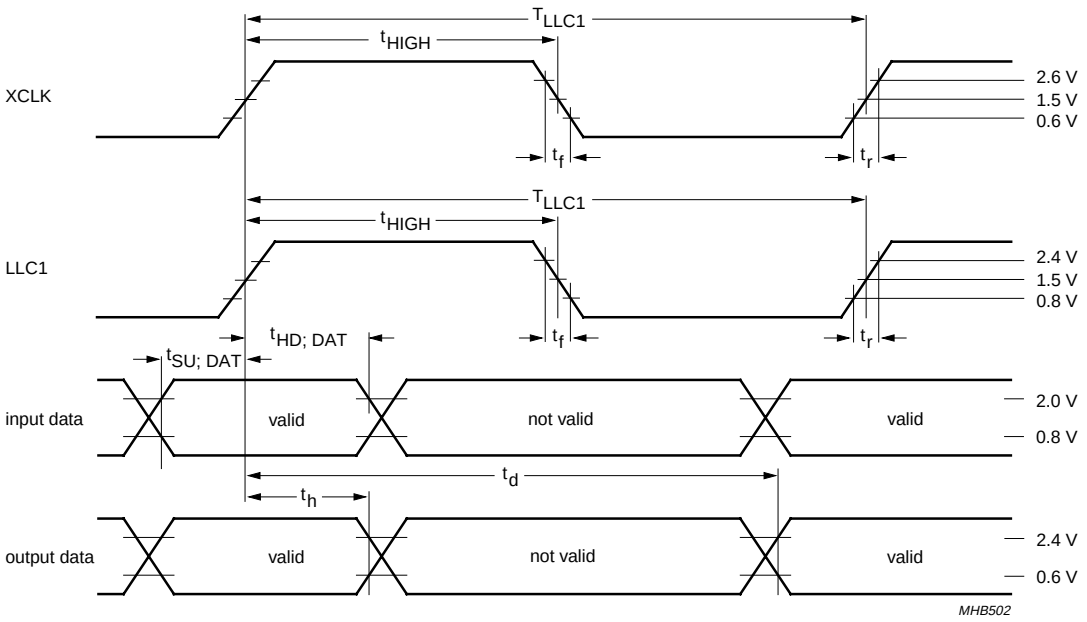
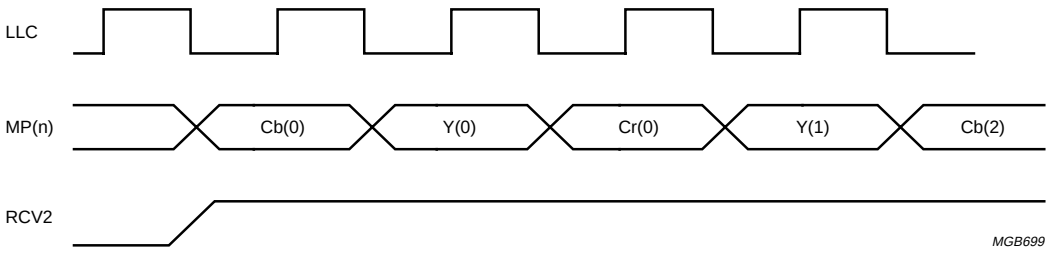


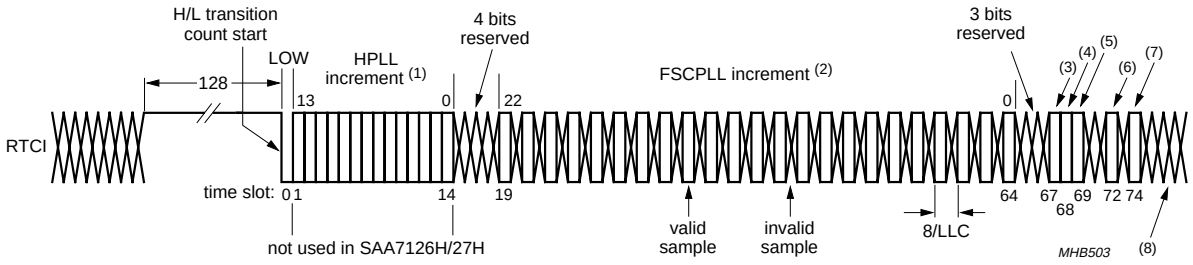
Fig.11 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (RCV2S).

Fig.12 Functional timing.

Explanation of RTCI data bits



(1) SAA7111/12 provides 14 to 0 bits, resulting in 2 reserved bits before FSCPLL increment.
(2) SAA7151 provides 21 to 0 bits only, resulting in 5 reserved bits before sequence bit.
(3) Sequence bit: PAL: 0 = (R – Y) line normal, 1 = (R – Y) line inverted; NTSC: 0 = no change.
(4) Reset bit: only from SAA7111 and SAA7112 decoder.
(5) FISE bit: 0 = 50 Hz, 1 = 60 Hz.
(6) Odd/even bit: odd_even from external.
(7) Colour detection: 0 = no colour detected, 1 = colour detected.
(8) Reserved bits: 229 with 50 Hz systems, 226 with 60 Hz systems.

Fig.13 RTCI timing.

1. The HPLL increment is not evaluated by SAA7126H; SAA7127H.
2. The SAA7126H; SAA7127H generates the subcarrier frequency from the FSCPLL increment if enabled (see item 7.).
3. The PAL bit indicates the line with inverted (R – Y) component of colour difference signal.
4. If the reset bit is enabled (RTCE = 1; DECPH = 1; PHRES = 00), the phase of the subcarrier is reset in each line whenever the reset bit of RTCI input is set to logic 1.
5. If the FISE bit is enabled (RTCE = 1; DECFIS = 1), the SAA7126H; SAA7127H takes this bit instead of the FISE bit in subaddress 61H.
6. If the odd/even bit is enabled (RTCE = 1; DECOE = 1), the SAA7126H; SAA7127H ignores it's internally generated odd/even flag and takes the odd/even bit from RTCI input.
7. If the colour detection bit is enabled (RTCE = 1; DECCOL = 1) and no colour was detected (colour detection bit = 0), the subcarrier frequency is generated by the SAA7126H; SAA7127H. In the other case (colour detection bit = 1) the subcarrier frequency is evaluated out of FSCPLL increment.

   If the colour detection bit is disabled (RTCE = 1; DECCOL = 0), the subcarrier frequency is evaluated out of FSCPLL increment, independent of the colour detection bit of RTCI input.

Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time $t_{d(pipe)(MP)}$ is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ, a new teletext bit must be provided by the source (new protocol) or a window of TTXRQ going HIGH is provided and the number of teletext bits, depending on the chosen TTX standard, is requested at input pin TTX (old protocol).

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of outgoing horizontal synchronization pulse.

Time $t_{i(TTXW)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbits/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

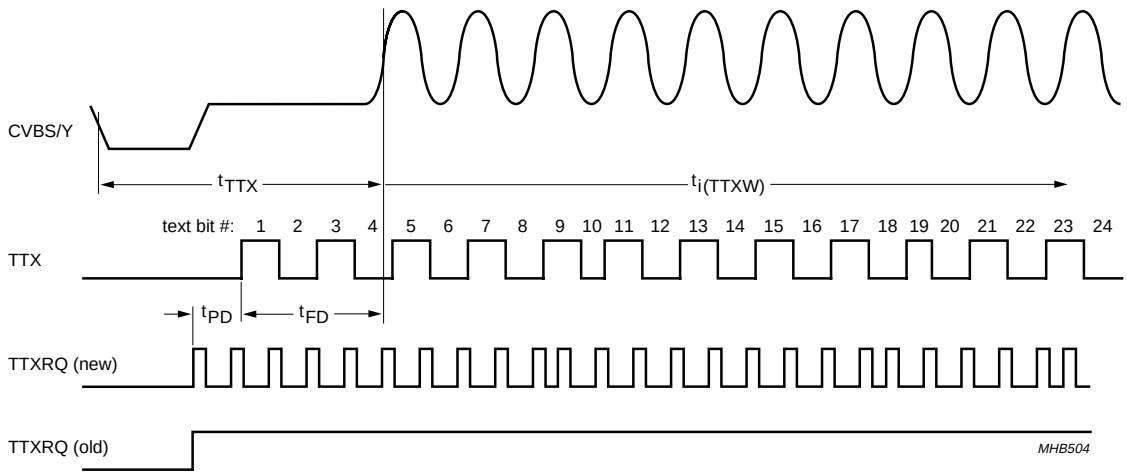
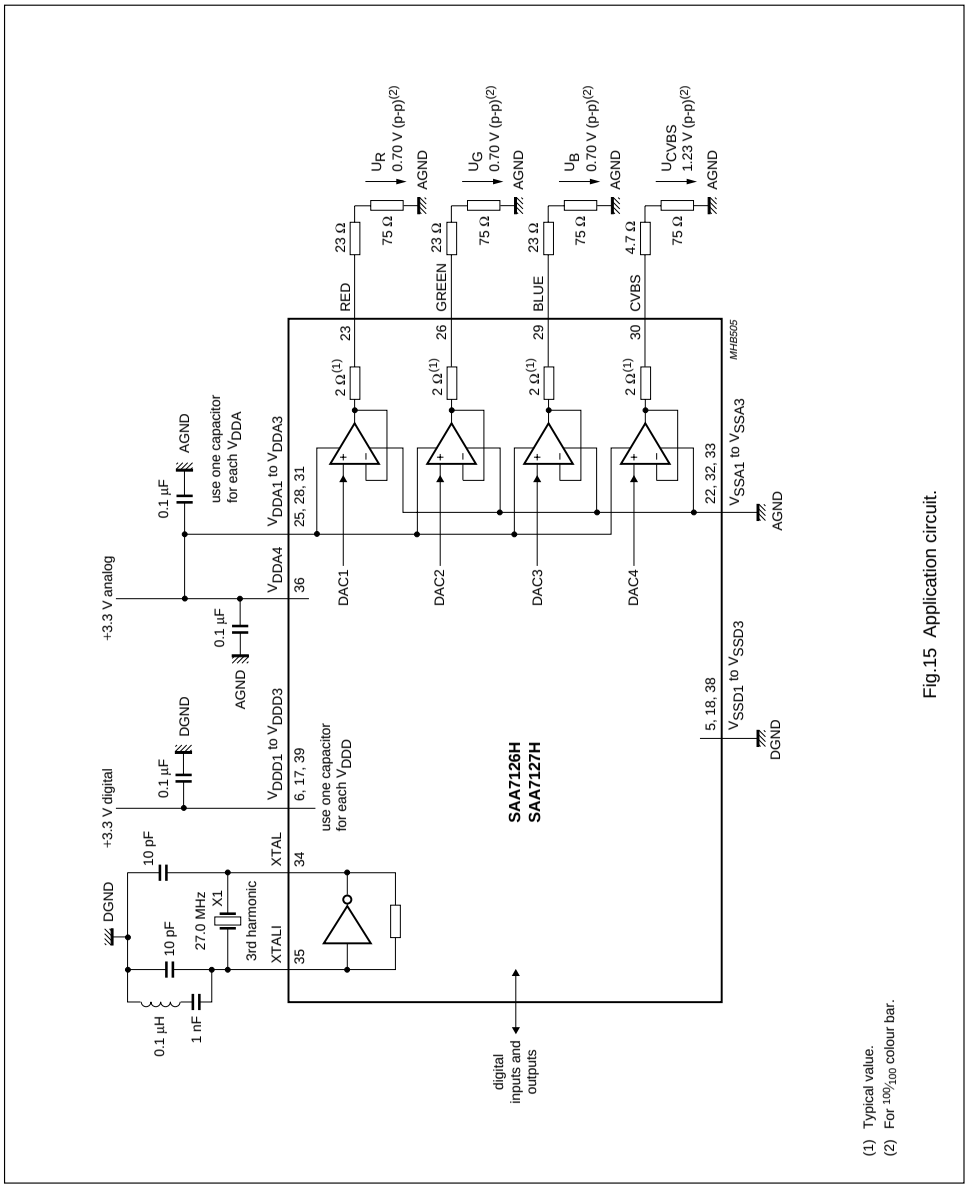


Fig.14 Teletext timing.

APPLICATION INFORMATION



(1) Typical value.
(2) For $^{100}/_{100}$ colour bar.

Fig.15 Application circuit.

Analog output voltages

The analog output voltages are dependent on the open-loop voltage of the operational amplifiers for full-scale conversion (typical value 1.375 V), the internal series resistor (typical value 2 Ω), the external series resistor and the external load impedance.

The digital output signals in front of the DACs under nominal conditions occupy different conversion ranges, as indicated in Table 48 for a $^{100}/_{100}$ colour bar signal.

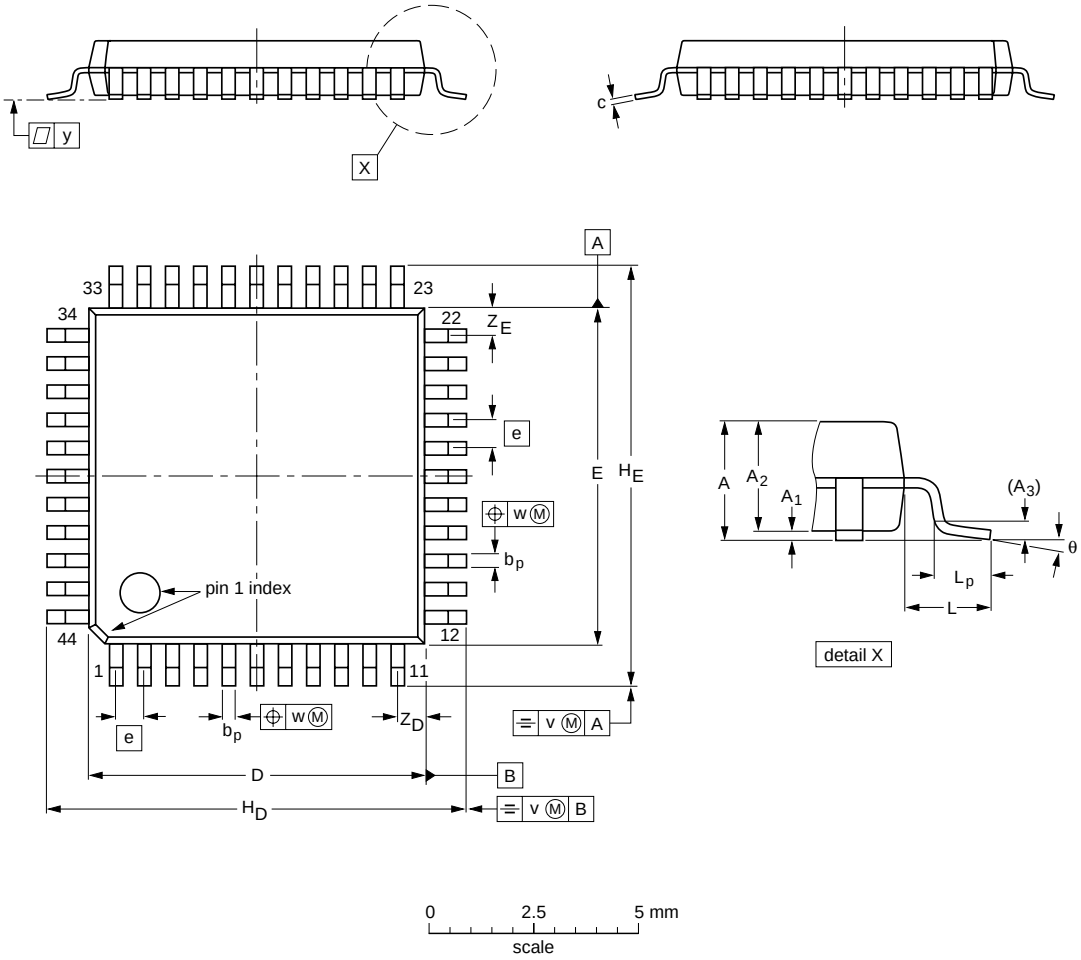
Values for the external series resistors result in a 75 Ω load.

Table 48 Digital output signals conversion range

CONVERSION RANGE (peak-to-peak)		
CVBS, SYNC TIP-TO-PEAK CARRIER (digits)	**Y (VBS) SYNC TIP-TO-WHITE (digits)**	**RGB (Y) BLACK-TO-WHITE AT GDY = GDC = −6 (digits)**
1016	881	712

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
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