

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4017B **MSI** 5-stage Johnson counter

Product specification
File under Integrated Circuits, IC04

January 1995

5-stage Johnson counter

HEF4017B MSI

DESCRIPTION

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop (\overline{O}_{5-9}), active HIGH and active LOW clock inputs (CP_0 , \overline{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while \overline{CP}_1 is LOW or a HIGH to LOW transition at \overline{CP}_1 while CP_0 is HIGH (see also function table).

When cascading counters, the \overline{O}_{5-9} output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{5-9} = \text{HIGH}$; O_1 to $O_9 = \text{LOW}$) independent of the clock inputs (CP_0 , \overline{CP}_1).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

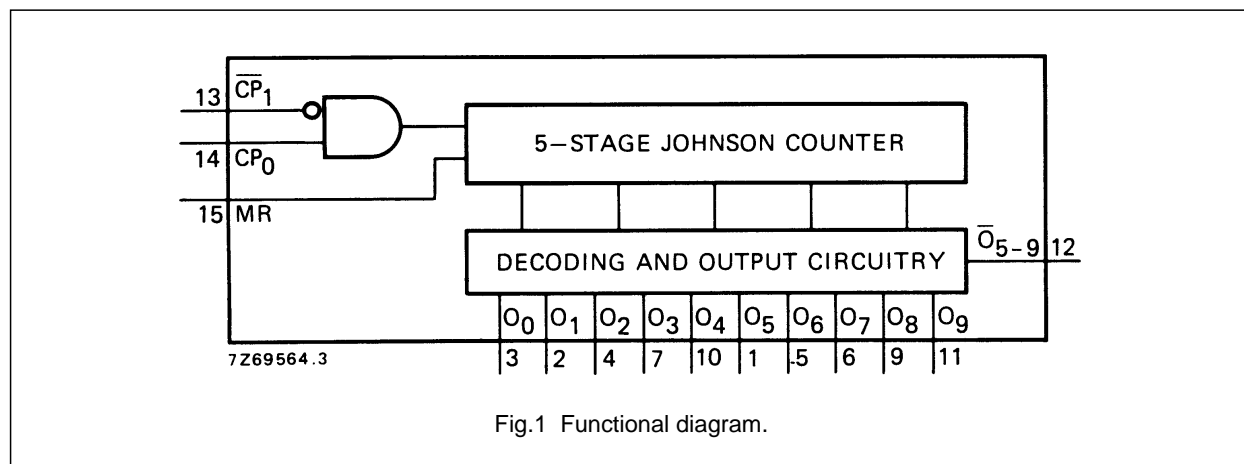


Fig.1 Functional diagram.

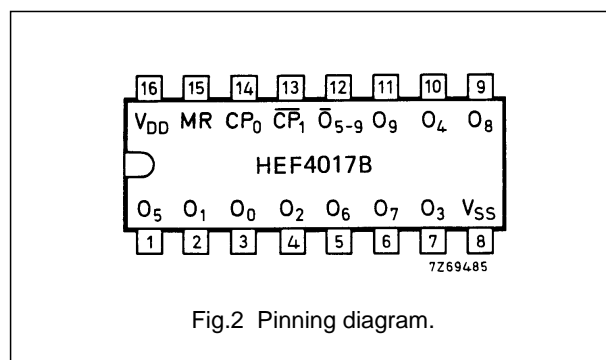


Fig.2 Pinning diagram.

PINNING

- CP_0 clock input (LOW to HIGH triggered)
- \overline{CP}_1 clock input (HIGH to LOW triggered)
- MR master reset input
- O_0 to O_9 decoded outputs
- \overline{O}_{5-9} carry output (active LOW)

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4017BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4017BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4017BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

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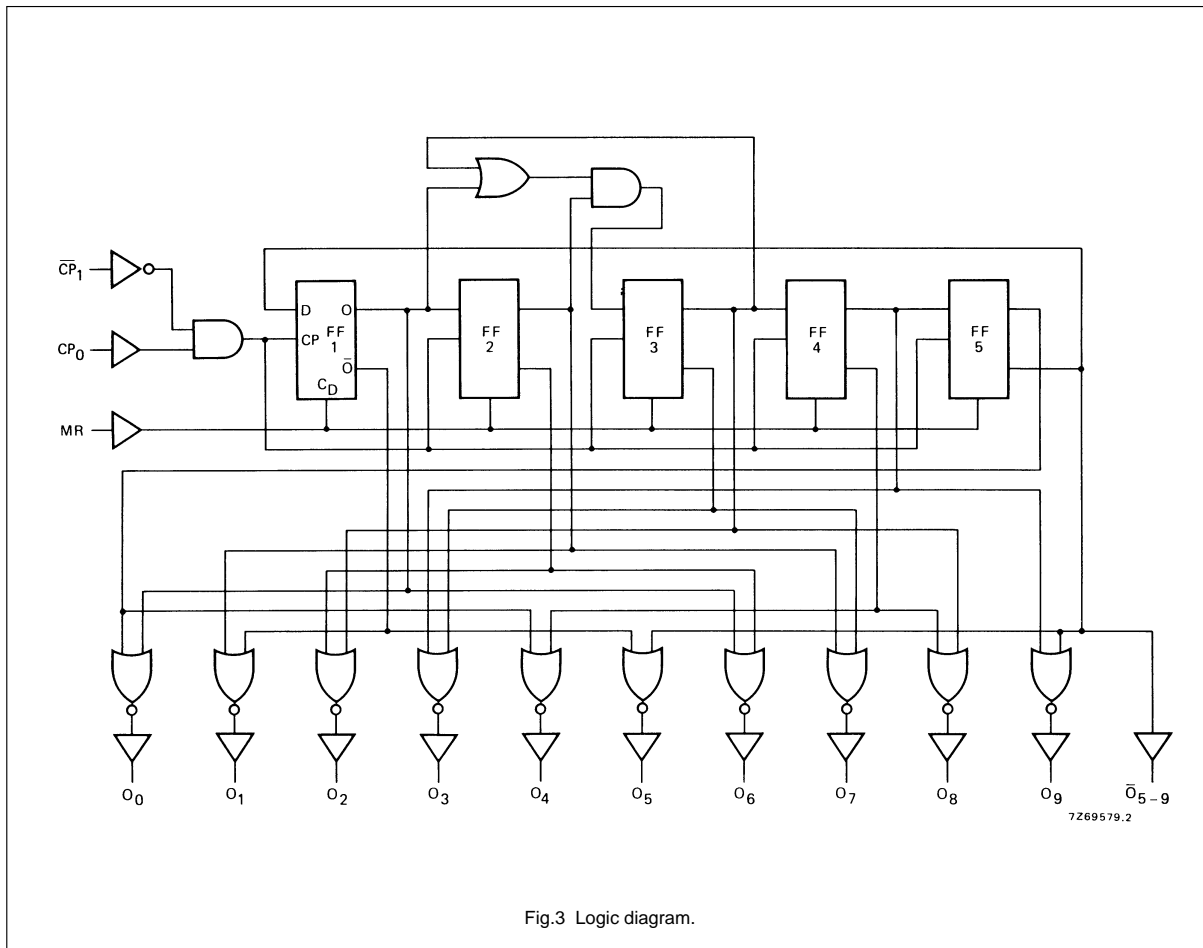






Fig.3 Logic diagram.



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FUNCTION TABLE

MR	CP ₀	$\overline{\text{CP}}_1$	OPERATION
H	X	X	O ₀ = $\overline{\text{O}}_{5-9}$ = H; O ₁ to O ₉ = L
L	H		Counter advances
L		L	Counter advances
L	L	X	No change
L	X	H	No change
L	H		No change
L		L	No change

Notes

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
-  = positive-going transition
-  = negative-going transition

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays CP ₀ , $\overline{\text{CP}}_1$ → O ₀ to O ₉ HIGH to LOW	5	t _{PHL}		140	280	ns	113 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		125	250	ns	98 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
CP ₀ , $\overline{\text{CP}}_1$ → $\overline{\text{O}}_{5-9}$ HIGH to LOW	5	t _{PHL}		145	290	ns	118 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		125	250	ns	98 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
MR → O ₁ to O ₉ HIGH to LOW	5	t _{PHL}		115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L	
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L	
MR → $\overline{\text{O}}_{5-9}$ LOW to HIGH	5	t _{PLH}		110	220	ns	83 ns + (0,55 ns/pF) C _L
	10		45	90	ns	34 ns + (0,23 ns/pF) C _L	
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L	
MR → O ₀ LOW to HIGH	5	t _{PLH}		130	260	ns	103 ns + (0,55 ns/pF) C _L
	10		55	105	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	75	ns	32 ns + (0,16 ns/pF) C _L	

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	

AC CHARACTERISTICS

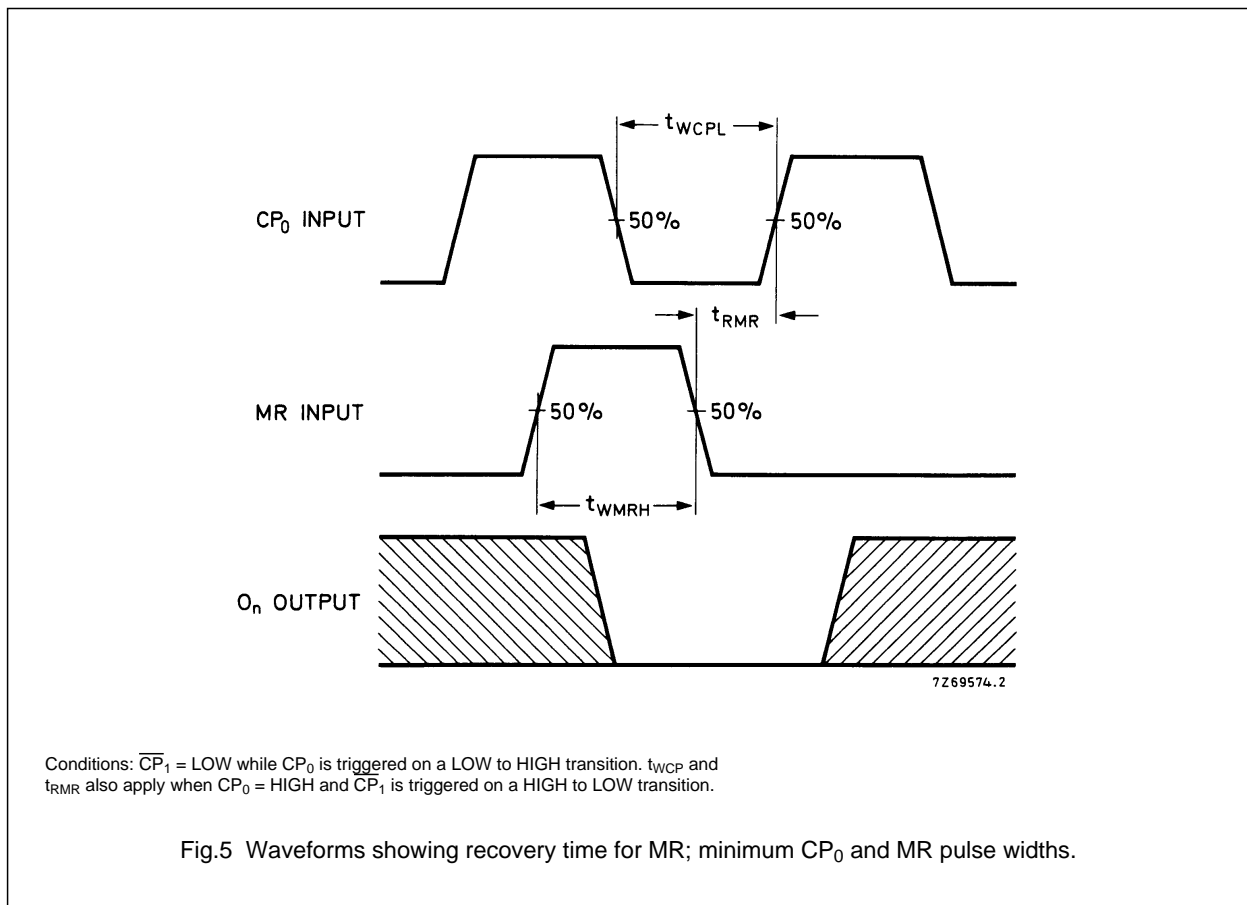
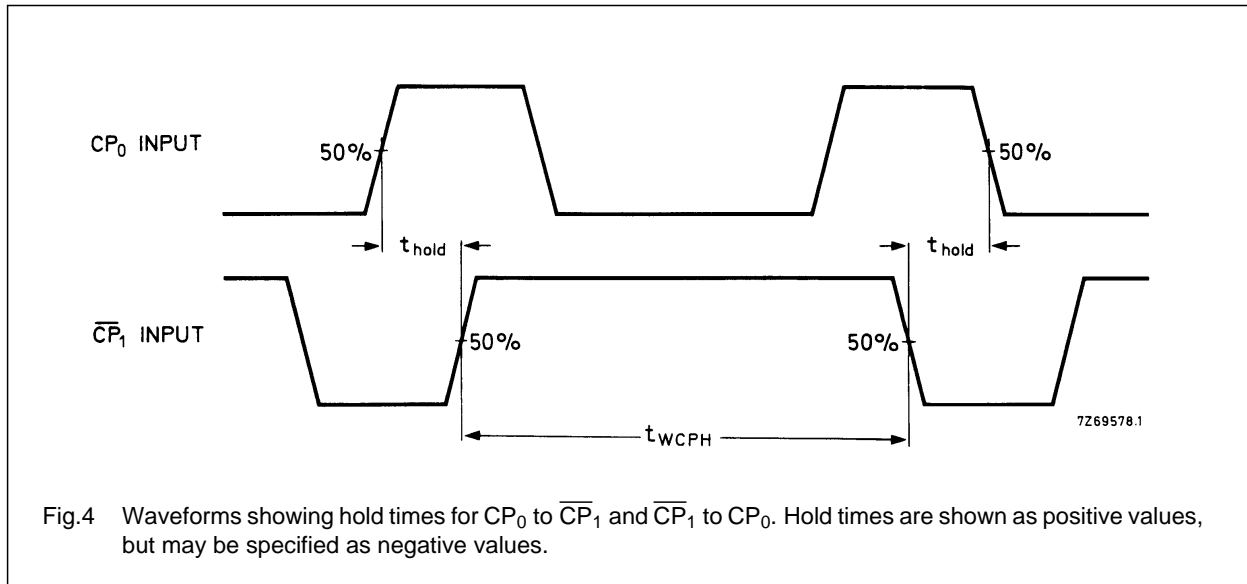
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Hold times CP ₀ → \overline{CP}_1	5	t _{hold}	90	45	ns	see also waveforms Figs 4 and 5
	10		40	20	ns	
	15		20	10	ns	
\overline{CP}_1 → CP ₀	5	t _{hold}	80	40	ns	
	10		40	20	ns	
	15		30	10	ns	
Minimum clock pulse width: CP ₀ = LOW; \overline{CP}_1 = HIGH	5	t _{WCPL} = t _{WCPH}	80	40	ns	
	10		40	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t _{RMR}	60	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f _{max}	6	12	MHz	
	10		12	24	MHz	
	15		15	30	MHz	

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	500 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load cap. (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	2200 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	6000 f _i + ∑ (f _o C _L) × V _{DD} ²	

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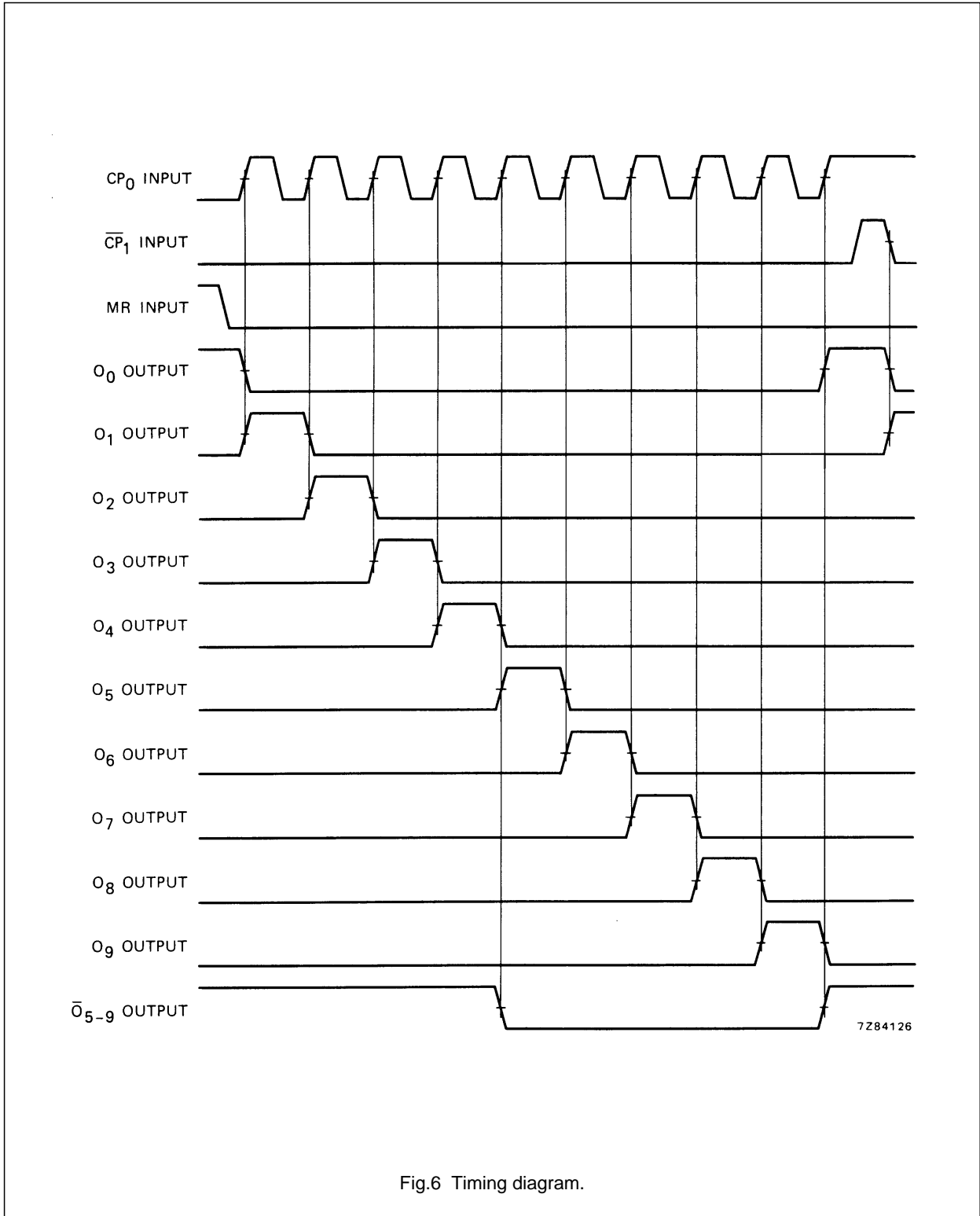


Fig.6 Timing diagram.

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APPLICATION INFORMATION

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer.

Figure 7 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

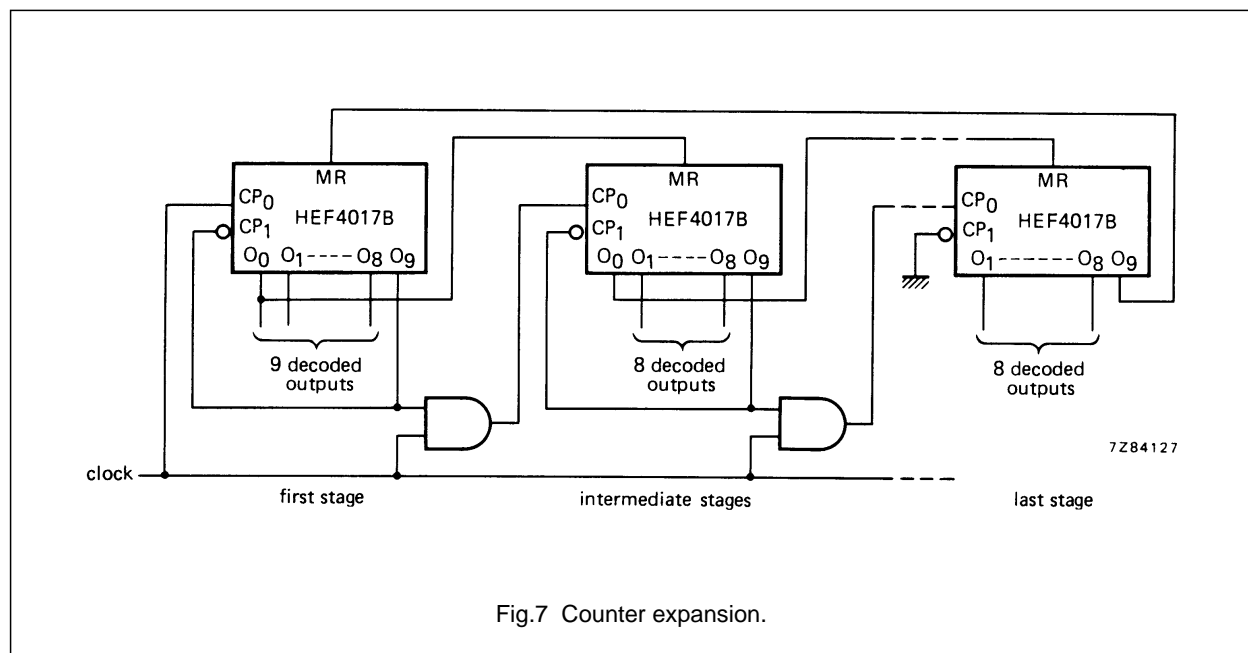


Fig.7 Counter expansion.

Note

It is essential not to enable the counter on $\overline{CP_1}$ when CP_0 is HIGH, or on CP_0 when $\overline{CP_1}$ is LOW, as this would cause an extra count.