PRELIMINARY

January 1999 File Number 4328.1

400MHz AGC Quadrature IF Modulator/Demodulator

The HFA3766 is a highly integrated baseband converter for quadrature modulation applications. It features all the necessary blocks for baseband modulation and demodulation of I and Q signals. It has a two stage integrated AGC IF amplifier with 82dB of voltage gain and 76dB of gain control range. Baseband antialiasing is integrated into the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. For baseband modulation digital I and Q data are delivered to the transmit section. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation and demodulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user. The device is housed in a thin 80 lead TQFP package well suited for PCMCIA board applications.

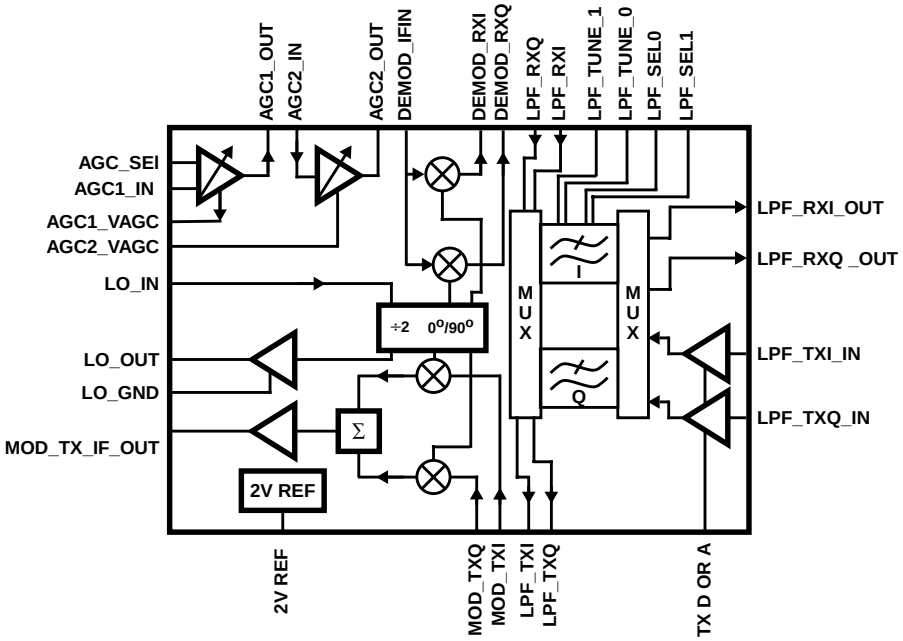
Features

- Integrates all IF Transmit and AGC Receive Functions
- Broad Frequency Range . . . . . 10MHz to 400MHz
- I/Q Amplitude and Phase Balance . . . . 0.2dB, 2 Degrees
- 5th Order Programmable Low Pass Filter . . . . . 2.2MHz to 17.6MHz
- 400MHz AGC Gain Strip 82dB
- AGC Range 75dB
- Low LO Drive Level . . . . . -15dBm
- Fast AGC Switching 1µs
- Fast Transmit-Receive Switching 1µs
- Power Management/Standby Mode
- Single Supply 3.0V Operation
- Wireless Local Loop
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- CDMA Radios
- PCS/Wireless PBX

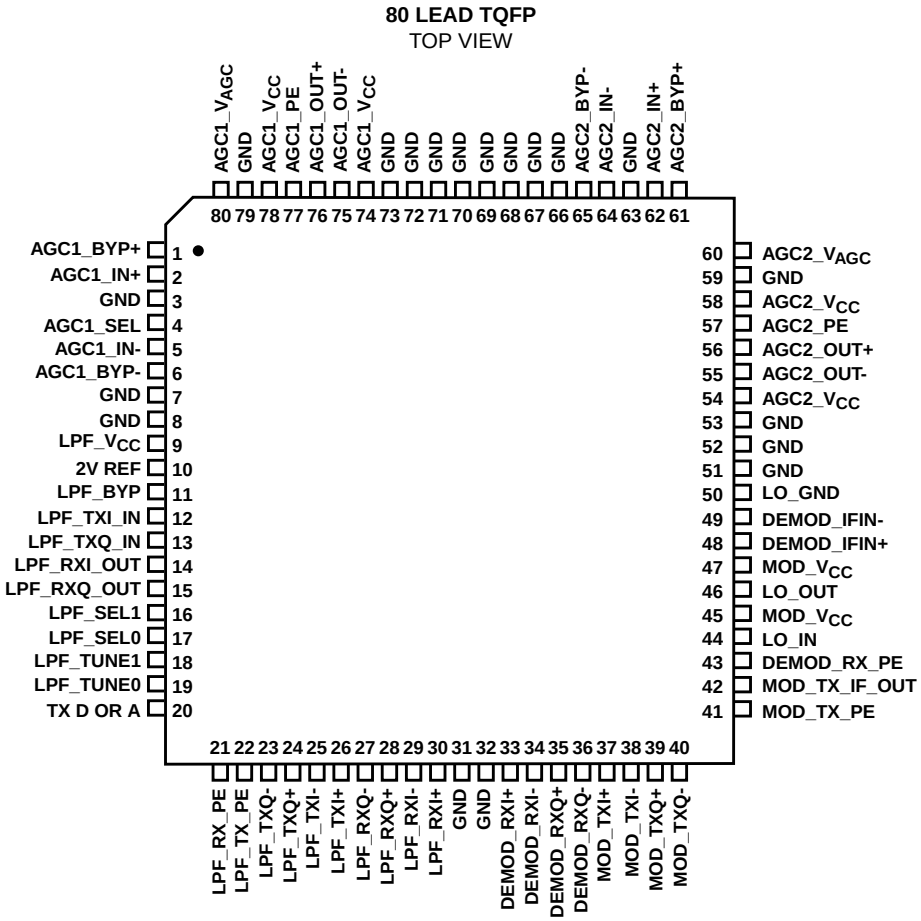
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3766IN	-40 to 85	80 Ld TQFP	Q80.14x14
HFA3766IN96	-40 to 85	Tape and Reel	

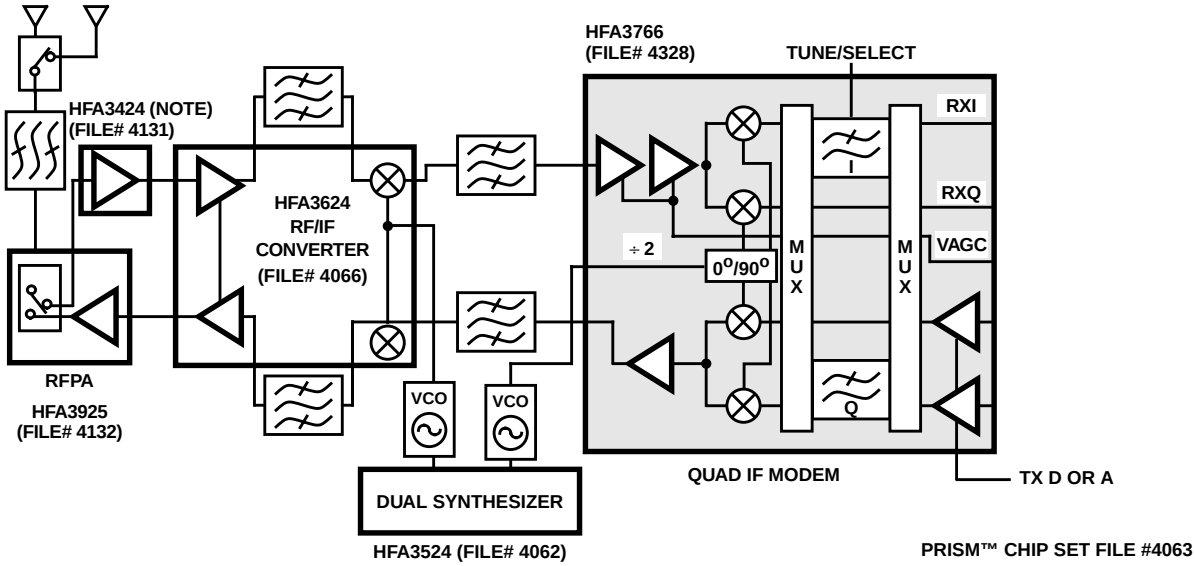
Simplified



Pinout



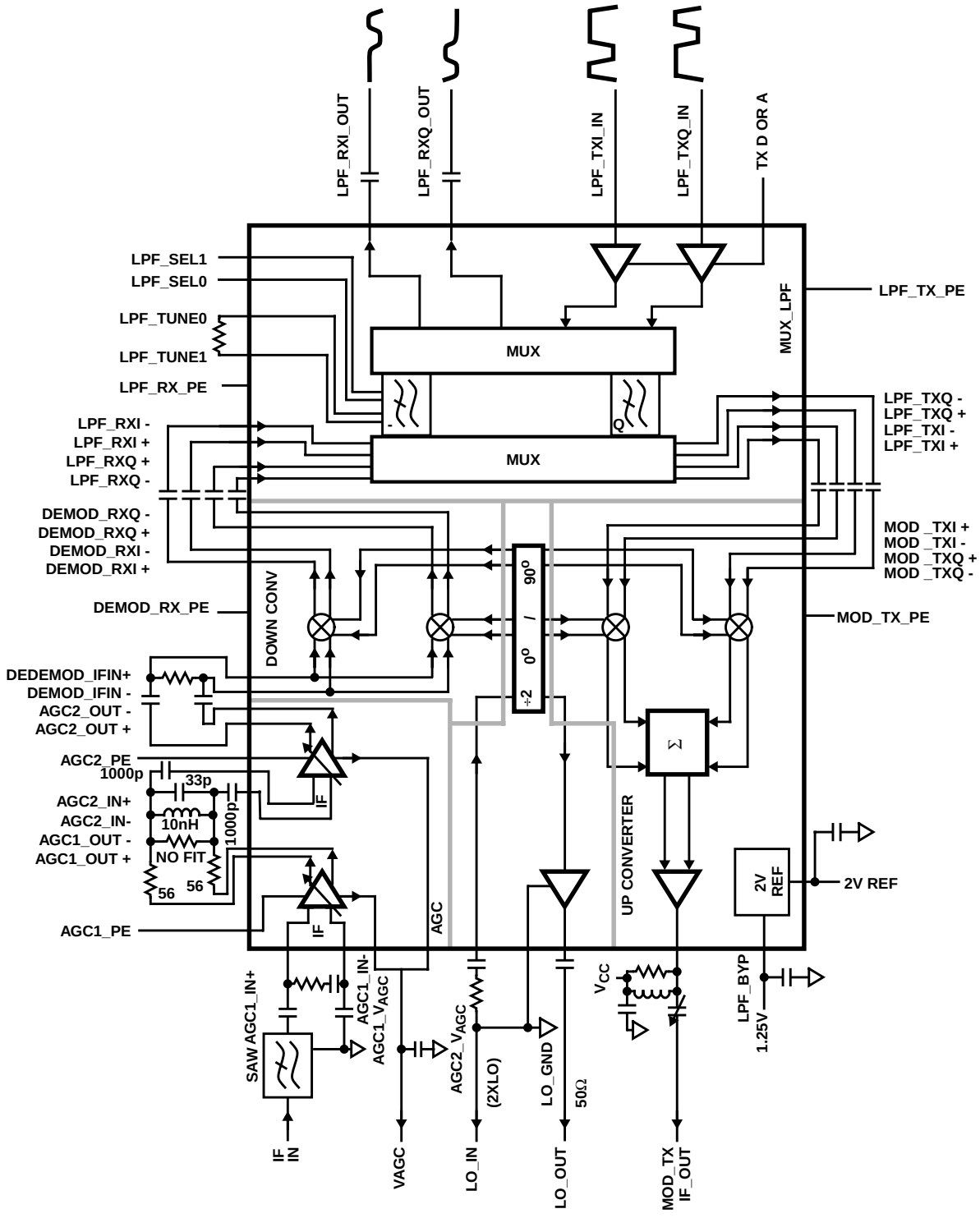
Typical Application Diagram



For additional information on the PRISM™ Full Duplex Radio Chip Set, call (407) 724-7800 to access Intersil's AnswerFAX system. When prompted, key in the four-digit document number (File #) of the data sheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Block Diagram



NOTE: V_{CC}, GND and Bypass capacitors not shown.

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	AGC1_BYP+	DC feedback pin for AGC amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
2	AGC1_IN+	Non-inverting analog input of AGC amplifier 1.
3	GND	Ground. Connect to a solid ground plane.
4	AGC_SEL	This pin selects either differential or single ended input configuration for the first stage AGC. Ground this pin for differential input configuration. Leave it floating for single ended input configuration.
5	AGC1_IN-	Inverting analog input of AGC amplifier 1.
6	AGC1_BYP-	DC feedback pin for AGC amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
7, 8	GND	Ground. Connect to a solid ground plane.
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_IN	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs.
13	LPF_TXQ_IN	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs
14	LPF_RX_I	Low pass filter in phase (I) channel receive output. Requires AC coupling.
15	LPF_RX_Q	Low pass filter quadrature (Q) channel receive output. Requires AC coupling.
16	LPF_SEL1	Digital control input pins. Selects four programmed cut off frequencies for the receive channel. Tuning speed from one cutoff to another is less than 1µs.
17	LPF_SEL0	**SEL1 SEL0 CUTOFF FREQUENCY** — LO LO 2.2MHz; LO HI 4.4MHz **SEI1 SEI0 CUTOFF FREQUENCY** — HI LO 8.8MHz; HI HI 17.6MHz
18	LPF_TUNE1	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune both transmit and receive filters. Refer to the tuning equation in the LPF AC specifications.
19	LPF_TUNE0	
20	TXD or TXA	Selects between digital or analog signals. Tie to GND for digital. Tie to V_{CC} for analog.
21	LPF_RX_PE	Digital input control pin to enable the LPF receive mode of operation. Enable logic level is High.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	LPF_RXQ-	Low pass filter inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the negative output of the quadrature demodulator (Mod_RXQ-), pin 36.

Pin Descriptions (Continued)

PIN	SYMBOL	DESCRIPTION
28	LPF_RXQ+	Low pass filter non inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the positive output of the quadrature demodulator (Mod_RXQ+), pin 35.
29	LPF_RXI-	Low pass filter inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the negative output of the in phase demodulator (Mod_RXI-), pin 34.
30	LPF_RXI+	Low pass filter non inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the positive output of the in phase demodulator (DEMOD_RXI-), pin 33.
31, 32	GND	Ground. Connect to a solid ground plane.
33	DEMOD_RXI+	In phase demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXI+), pin 30.
34	DEMOD_RXI-	In phase demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXI-), pin 29.
35	DEMOD_RXQ+	Quadrature demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXQ+), pin 28.
36	DEMOD_RXQ-	Quadrature demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXQ+), pin 27.
37	MOD_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	MOD_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	MOD_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	MOD_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.
41	MOD_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	MOD_TX_IF_OUT	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 316Ω.
43	DEMOD_RX_PE	Digital input control to enable the demodulator section. Enable logic level is High.
44	LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required demodulator LO frequency. Input current is optimum at 200μA_{RMS}. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω. This pin requires AC coupling. NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	MOD_V_{CC}	Supply pin for the Demodulator. Use high quality decoupling capacitors right at the pin.
46	LO_Out	Divide by 2 buffered output reference from “DEMOD_LO_in” input. Used for external applications where the demodulating carrier reference frequency is required. 50Ω single end driving capability. This output can be disabled by use of pin 50. AC coupling is required.
47	MOD_V_{CC}	Supply pin for the Demodulator. Use high quality decoupling capacitors right at the pin.
48	DEMOD_IFIN+	Demodulator, non-inverting input. Requires AC coupling.
49	DEMOD_IFIN-	Demodulator, inverting input. Requires AC coupling.
50	LO_GND	When grounded, this pin enables the LO buffer (DEMOD_LO_Out). When open (NC) it disables the LO buffer.
51, 52, 53	GND	Ground. Connect to a solid ground plane.
54	AGC2_V_{CC}	Supply pin for the AGC amplifier 2. Use high quality decoupling capacitors right at the pin.

Pin Descriptions (Continued)

PIN	SYMBOL	DESCRIPTION
55	AGC2_OUT-	Positive output of AGC amplifier 2. Requires AC coupling.
56	AGC2_OUT+	Negative output of AGC amplifier 2. Requires AC coupling.
57	AGC2_PE	Digital input control to enable the AGC amplifier 2. Enable logic level is High.
58	AGC2_V_{CC}	Supply pin for the AGC amplifier 2. Use high quality decoupling capacitors right at the pin.
59	GND	Ground. Connect to a solid ground plane.
60	AGC2_V_{AGC}	AGC amplifier 2, AGC control input.
61	AGC2_BYP+	DC feedback pin for AGC amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
62	AGC2_IN+	Non-inverting analog input of AGC amplifier 2.
63	GND	Ground. Connect to a solid ground plane.
64	AGC2_IN-	Inverting input of AGC amplifier 2.
65	AGC2_BYP-	DC feedback pin for AGC amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
66 - 73	GND	Ground. Connect to a solid ground plane.
74	AGC1_V_{CC}	AGC amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
75	AGC1_OUT-	Negative output of AGC amplifier 1. Requires AC coupling.
76	AGC1_OUT+	Positive output of AGC amplifier 1. Requires AC coupling.
77	AGC1_PE	Digital input control to enable the AGC amplifier 1. Enable logic level is High.
78	AGC1_V_{CC}	AGC amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
79	GND	Ground. Connect to a solid ground plane.
80	AGC1_V_{AGC}	AGC amplifier 1, AGC control input.

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +6.0V
Voltage on Any Other Pin. . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage 5.5V
Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
TQFP Package	75

Package Power Dissipation at 70^oC
TQFP Package 1.1W
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Cascaded DC Electrical Specifications V_{CC} = 4.5V to 5.5V, Unless Otherwise Specified

PARAMETER	(NOTE 2) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
Total Supply Current, at 5.5V	A	Full	-	80	112	mA
Shutdown (Standby) Current at 5.5V	A	Full	-	0.8	1.5	mA
All Digital Inputs V_{IH} (TTL Threshold for All V_{CC})	A	Full	2.0	-	V_{CC}	V
All Digital Inputs V_{IL} (TTL Threshold for All V_{CC})	A	Full	-0.2	-	0.8	V
High Level Input Current at 5.5V V_{CC} for pins 16 and 21 with V_{IN} = 2.4V	A	Full	-200	-65	0	µA
High Level Input Current at 5.5V V_{CC} for pins 16 and 21 with V_{IN} = 4.0V	A	Full	-150	-30	0	µA
Low Level Input Current at 5.5V V_{CC} for pins 16 and 21 with V_{IN} = 0.8V	A	Full	-300	-95	0	µA
High Level Input Current at 5.5V V_{CC} for pin 17, with V_{IN} = 2.4V	A	Full	0	50	200	µA
High Level Input Current at 5.5V V_{CC} for pin 17, with V_{IN} = 4.0V	A	Full	0	80	300	µA
Low Level Input Current at 5.5V V_{CC} for pin 17, with V_{IN} = 0.8V	A	Full	0	15	150	µA
High Level Input Current at 5.5V V_{CC} for pin 43 with V_{IN} = 2.4V	A	Full	-20	1	20	µA
High Level Input Current at 5.5V V_{CC} for pin 43 with V_{IN} = 4.0V	A	Full	0	110	300	µA
Low Level Input Current at 5.5V V_{CC} for pin 43 with V_{IN} = 0.8V	A	Full	-20	0.1	20	µA
V_{AGC} Input for Max Gain (Note 5)	A	25	0.8	1.1	-	V
V_{AGC} Input for Min Gain (Note 5)	A	25	-	2.1	2.2	V
V_{AGC} Control Input Impedance (Per Stage) (Note 3)	C	25	-	410	-	Ω
V_{AGC} Control Input Current (Per Stage) at Max Control Voltage	A	25	-	0.5	2.0	mA
Full Range AGC Switching Large Signal Recovery (Note 4)	B	25	-	400	-	ns
Full Range AGC Switching 1dB Settling Time (Note 4)	B	25	-	1.5	-	µs
Power Down/Up Switching Speed (Note 4)	B	25	-	2	-	µs
Reference Voltage	A	Full	1.85	2.0	2.15	V
Reference Voltage Variation Over Temperature	B	25	-	800	-	µV/^oC
Reference Voltage Variation Over Supply Voltage	B	25	-	1.6	-	mV/V
Reference Voltage Minimum Load Resistance	C	25	10	-	-	kΩ

NOTES:

2. A = Production Tested, B = Based on Characterization, C = By Design.
3. 1.2V reference source in series with 410Ω.
4. Determined by external components.
5. Measured at probe.

Cascaded AC Electrical Specifications, Demodulator Chain Performance V_{CC} = 3.0V, LO = 560 MHz, and IF = 280 MHz, Unless Otherwise Specified

PARAMETER	(NOTE 6) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
CASCADED CHARACTERISTICS						
Cascaded Power Gain	TBD	TBD	TBD	TBD	TBD	TBD
Cascaded OIP3	TBD	TBD	TBD	TBD	TBD	TBD
Cascaded Noise Figure		TBD	TBD	TBD	TBD	TBD
Cascaded Output 1dB Compression	TBD	TBD	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD	TBD	TBD
IF Demodulator I and Q Outputs Voltage Swing (IF input Range of -70dBm to -30dBm)	A	Full	-	250	-	mV_{P-P}
IF Demodulator I and Q Channels Output Drive Capability (Z_{OUT} = 50Ω) C_{MAX} = 10pF, V_{OUT} = 500mV_{P-P}	C	25	1.2	2	-	kΩ
IF Demodulator I/Q Amplitude Balance, IFin = -50dBm at 50Ω	A	Full	-1.0	0	+1.0	dB
IF Demodulator I/Q Phase Balance, IFin = -50dBm at 50Ω	A	Full	-4.0	0	+4.0	Degrees
IF Demodulator Output, P1dB	TBD	TBD	TBD	TBD	TBD	mV

NOTES:

6. A = Production Tested, B = Based on Characterization, C = By Design.
7. Determined by external components.

AC Electrical Specifications, Modulator Performance V_{CC} = 3.0V, Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 8) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
IF Modulator I/Q Amplitude Balance (Note 9)	Mabal	B	25	-1.0	0	+1.0	dB
IF Modulator I/Q Phase Balance (Note 9)	Mphbal	B	25	-4.0	0	+4.0	Degrees
IF Modulator SSB Output Power (Note 10)	Mssbpw	A	Full	-12	-7	-4	dBm
IF Modulator Side Band Suppression (Note 10)	Mssbss	A	Full	26	33	-	dBc
IF Mod Carrier Suppression (LO Buffer Enabled) (Note 10)	Mssbcs	A	Full	28	30	-	dBc
IF Mod Carrier Suppression (LO Buffer Disabled) (Note 10)	Mssbcs1	B	25	28	36	-	dBc
IF Modulator Output Noise Floor (Out of Band)	Moutn0	B	25	-	-132	-	dBm/Hz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 2.2MHz (Note 11)	Msel1f	A	Full	1.8	2.2	2.5	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 4.4MHz (Note 11)	Msel2f	A	Full	3.6	4.4	5.0	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 8.8MHz (Note 11)	Msel3f	A	Full	7.3	8.8	9.8	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 17.6MHz (Note 11)	Msel4f	A	Full	14.6	17.6	19.6	MHz
IF Modulator Spread Spectrum Output Power (Note 12)	Mdsspw	B	25	-12	-7	-4	dBm
IF Modulator Side Lobe to Main Lobe Ratio, LPF = 8.8MHz (Note 12)	Mdsssl	A	Full	32	35	-	dB

NOTES:

8. A = Production Tested, B = Based on Characterization, C = By Design.
9. Data is characterized by DC levels applied to MOD TXI and Q pins for 4 quadrants with LO output as reference or indirectly by the SSB characteristics.
10. Power at the fundamental SSB frequency of two 6MHz, 90 degrees apart square waves applied at TXI and TXQ inputs. V_{IH} = 3.0V, V_{IL} = 0.5V. LPF selected to 8.8MHz cutoff.
11. Cutoff frequencies are specified for both modulator and demodulator as the filter bank is shared and multiplexed for Transmit and Receive. Data is characterized by observing the attenuation of the fundamental of a square wave digital input swept at each channel separately. The IF output is down converted by an external wideband mixer with a coherent LO input for each of quadrature signals separately.
12. Typical ratio characterization with R_{TUNE} set to 7.7MHz, LPF selected for 8.8MHz. TXI and TXQ Digital Inputs at two independent and aligned 11M chip/s, 2^{23}-1 sequence code signals.

AC Electrical Specifications, Cascaded AGC Stages Performance V_{CC} = 3.0V

PARAMETER	(NOTE 13) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Frequency Range (Note 14)	B	25	10	-	400	MHz
Voltage Gain at Max Gain (Note 15) (V_{AGC} = 0.8V, R_S = 50Ω, R_L = 500Ω)	B	25	78	82	-	dB
Voltage Gain at Min Gain (V_{AGC} = 2.1V, R_S = 50Ω, R_L = 500Ω)	B	25	-	7	-	dB
Noise Figure at Max Gain, R_S = 50Ω	B	25	-	10	11	dB
Output P 1dB at Min Gain, R_S = 50Ω, dBm into R_L = 500Ω	B	25	-16	-13	-	dBm
Input P 1dB at Min Gain, R_S = 50Ω	B	25	-13	-10	-	dBm
Output IP3 at Min Gain, dBm into R_L = 500Ω	B	25	-5	-2	-	dBm
Input IP3 at Min Gain, R_S = 50Ω	B	25	-2	1	-	dBm
Group Delay, 20MHz Bandwidth	B	25	-	2.0	-	ns_{P-P}
Single Ended Input Impedance, AGC_SEL = floating	B	25	-	50	-	Ω
Differential Input Impedance, AGC_SEL = ground	B	25	-	100	-	Ω
Differential Output Impedance	B	25	-	80	-	Ω

NOTES:

13. A = Production Tested, B = Based on Characterization, C = By Design.
14. Determined by external components.
15. Measured at probe.

AC Electrical Specifications, I/Q Down Converter Individual Performance V_{CC} = 3.0V

PARAMETER	(NOTE 16) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Quadrature Demodulator Input Frequency Range	B	25	10	-	400	MHz
Demodulator Baseband I/Q Frequency Range	C	25	-	-	30	MHz
Demodulator Voltage Gain at Frequency Range	B	25	6	8	9	dB
Demodulator Differential Input Resistance	C	25	-	1	-	kΩ
Demodulator Differential Input Capacitance	C	25	-	0.5	-	pF
Demodulator Differential Output Level at 4K Load, (Output Controlled By AGC Action)	B	25	400	500	560	mV_{P-P}
Demodulator Amplitude Balance	B	25	-1.0	-	1.0	dB
Demodulator Phase Balance at 286MHz	B	25	-4	-	4	Degrees
Demodulator Phase Balance at 400MHz	B	25	-4	-	4	Degrees
Demodulator Output 1dB Compression Voltage at 4K Load	B	25	-	1.25	-	V_{P-P}

NOTE:

16. A = Production Tested, B = Based on Characterization, C = By Design.

AC Electrical Specifications, LO Individual Performance V_{CC} = 3.0V

PARAMETER	(NOTE 17) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
2XLO Input Frequency Range (2 X Input Range)	B	25	20	-	800	MHz
2XLO Input Current Range	C	25	50	200	300	$μA_{RMS}$
2XLO Input Impedance	C	25	-	130	-	Ω
Buffered LO Output Voltage, Single Ended	C	25	50	100	-	mV_{P-P}

AC Electrical Specifications, LO Individual Performance V_{CC} = 3.0V (Continued)

PARAMETER	(NOTE 17) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Buffered LO Output Impedance	C	25	-	50	-	Ω
Quadrature IF Modulator Output Frequency Range	B	25	10	-	400	MHz
IF Modulator I/Q Input Frequency Range	C	25	-	-	30	MHz
IF Modulator Differential I/Q Max Input Voltage	C	25	-	2.25	-	V_{P-P}
IF Modulator Differential I/Q Input Impedance	C	25	-	4	-	kΩ
IF Modulator Differential Input Capacitance	C	25	-	0.5	-	pF
IF Modulator I/Q Amplitude Balance	A	25	-0.5	-	0.5	dB
IF Modulator I/Q Phase Balance at 200MHz	A	25	-2	-	2	Degrees
IF Modulator I/Q Phase Balance at 400MHz	B	25	-4	-	4	Degrees
IF Modulator Output at SSB Into 50Ω, I and Q, 500mV_{P-P}	A	25	-22	-	-10.0	dBm
IF Modulator Carrier Suppression (LO Buffer Enabled)	A	25	28	30	-	dBc
IF Modulator Carrier Suppression (LO Buffer Disabled)	A	25	28	36	-	dBc
IF Modulator SSB Sideband Suppression at 200MHz	A	25	28	-	-	dBc
IF Modulator SSB Sideband Suppression at 400MHz	B	25	26	-	-	dBc
IF Output Level Compression Point	C	25	-	1.0	-	V_{P-P}
IF Modulator Intermodulation Suppression	B	25	26	-	-	dBc

NOTE:

17. A = Production Tested, B = Based on Characterization, C = By Design.

AC Electrical Specifications, RX 5TH Order LPF Cascaded Performance V_{CC} = 3.0V

PARAMETER	(NOTE 18) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 0	D	25	1.8	2.20	2.4	MHz
RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 0	D	25	3.6	4.40	4.8	MHz
RX LPF 3dB Bandwidth, Sel0 = 0, Sel1 = 1	D	25	7.4	8.80	9.6	MHz
RX LPF 3dB Bandwidth, Sel0 = 1, Sel1 = 1	D	25	14.8	17.60	19.2	MHz
RX LPF Sel0, Sel1 Tuning Speed	B	25	-	-	1	µs
RX LPF 3dB Bandwidth Tuning	D	25	-20	-	+20	%
LPF Tune Nominal Resistance	B	25	-	787	-	Ω
RX LPF Voltage Gain	D	25	-1.0	0	1.0	dB
RX LPF DC Output Voltage	A	25	-	1.3	-	V
TX/RX Offset Voltage	A	25	TBD	0	TBD	V
RX LPF Single Ended Output Voltage Swing at 2kΩ Load (Controlled By AGC Action)	B	25	-	-	550	mV_{P-P}
RX LPF Differential Input Impedance	C	25	4	5	-	kΩ
RX I/Q Channel Amplitude Match	C	Full	-1	-	1	dB
RX I/Q Channel Phase Match	C	Full	-4	-	4	Degrees
RX LPF Total Harmonic Distortion	A	25	-	3	6	%
LPF Output Impedance, Single-Ended	C	25	-	50	-	Ω

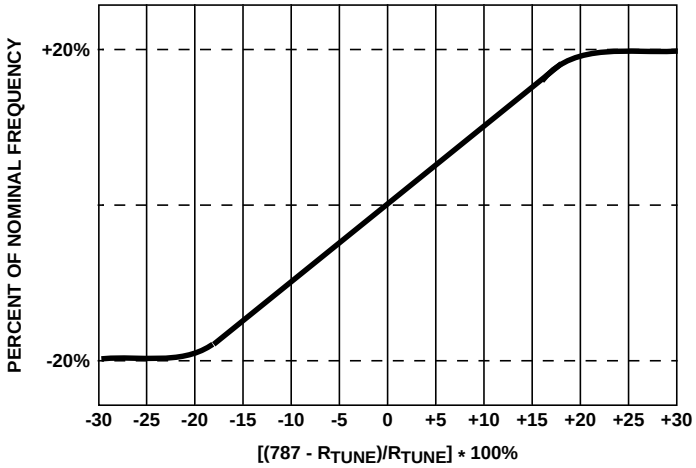
NOTE:

18. A = Production Tested, B = Based on Characterization, C = By Design D = Measured at Probe.

TABLE 1. LOW PASS FILTER PROGRAMING AND TUNING INFORMATION

MODE	LPF SEL1	LPF SEL0	f_{3dB} (NOMINAL R_{TUNE})
BW0	0	0	2.2MHz
BW1	0	1	4.4MHz
BW2	1	0	8.8MHz
BW3	1	1	17.6MHz

$$f_{TUNED\,3dB} = \frac{f_{3dBNOMINAL} * 787}{R_{TUNE}}$$



FREQUENCY	R_{TUNE}
20% Low	984Ω
Nominal	787Ω
20% High	656Ω

FIGURE 1. TYPICAL f_{3dB} vs R_{TUNE}

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029