19-1258; Rev 4; 4/05

EVALUATION KIT MANUAL AVAILABLE

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

General Description

The MAX3675 is a complete clock-recovery and data-retiming IC incorporating a limiting amplifier. It is intended for 622Mbps SDH/SONET applications and operates from a single +3.3V supply.

The MAX3675 has two differential input amplifiers: one accepts PECL levels, while the other accepts small-signal analog levels. The analog inputs access the limiting amplifier stage, which provides both a received-signal-strength indicator (RSSI) and a programmable-threshold loss-of-power (LOP) monitor. Selecting the PECL amplifier disables the limiting amplifier, conserving power. A loss-of-lock (LOL) monitor is also incorporated as part of the fully integrated PLL.

Applications

SDH/SONET Transmission Systems

SDH/SONET Access Nodes

Add/Drop Multiplexers

ATM Switches

Digital Cross-Connects

Pin Configuration appears at end of data sheet.

Features

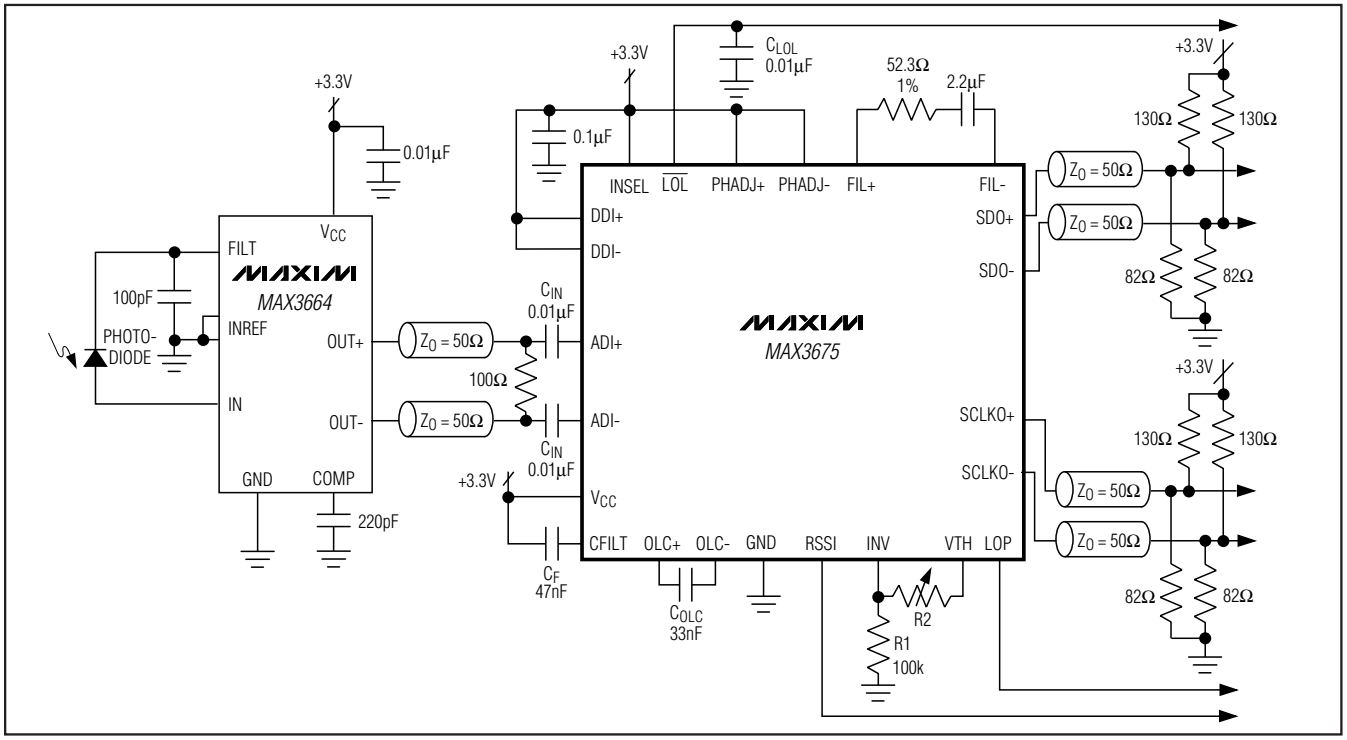
- ♦ **Single +3.3V or +5.0V Power Supply**
- ♦ **Complies with ANSI, ITU, and Bellcore SDH/SONET Specifications**
- ♦ **Low Power: 215mW at +3.3V**
- ♦ **Selectable Data Inputs, Differential PECL or Analog**
- ♦ **Received-Signal-Strength Indicator (RSSI)**
- ♦ **Loss-of-Power and Loss-of-Lock Monitors**
- ♦ **Differential PECL Clock and Data Outputs**
- ♦ **No External Reference Clock Required**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3675ECJ	-40°C to +85°C	32 TQFP	C32-1
MAX3675EHJ	-40°C to +85°C	5mm 32 TQFP	H32-1
MAX3675E/D	-40°C to +85°C	Dice*	DICE

**Contact factory for availability. Dice are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_J = +45°C.*

Typical Operating Circuit



For price, delivery, and to place orders, please contact Maxim Distribution at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .....-0.5V to +6.5V
Input Voltage Levels,
DDI+, DDI-, ADI+, ADI- .....-0.5V to (V_{CC} + 0.5V)
Input Differential Voltage (ADI+) - (ADI-) .....±3V
PECL Output Currents, SDO+, SDO-, SCLKO+, SCLKO-...100mA
$\overline{LOL}$, LOP, INSEL, PHADJ+, PHADJ-.....-0.5V to (V_{CC} + 0.5V)
FIL+, FIL-, OLC+, OLC-, RSSI, VTH .....-0.5V to (V_{CC} + 0.5V)
(OLC+) - (OLC-).....±3V
(FIL+) - (FIL-).....±700mV
CFILT.....(V_{CC} - 2.5V) to (V_{CC} + 0.5V)
INV .....-0.5V to +2.0V
Continuous Power Dissipation (T_A = +85°C)
7mm x 7mm TQFP (derate 20.7mW/°C above +85°C) ..1342mW
5mm x 5mm TQFP (derate 13.1mW/°C above +85°C) .845.6mW
Operating Junction Temperature Range.....-40°C to +150°C
Storage Temperature Range .....-65°C to +160°C
Processing Temperature (die).....+400°C
Lead Temperature (soldering,10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	MAX3675ECJ, PECL outputs unterminated	INSEL = V_{CC}		65	90	mA
			INSEL = GND		47	65	
PECL Input High Voltage	V_{IH}			V_{CC} - 1.16		V_{CC} - 0.88	V
PECL Input Low Voltage	V_{IL}			V_{CC} - 1.81		V_{CC} - 1.48	V
PECL Input High Current	I_{IH}			-10		10	µA
PECL Input Low Current	I_{IL}			-10		10	µA
PECL Output High Voltage	V_{OH}			V_{CC} - 1.03		V_{CC} - 0.88	V
PECL Output Low Voltage	V_{OL}			V_{CC} - 1.81		V_{CC} - 1.620	V
LOP, $\overline{LOL}$ High Voltage	V_{OH}			2.4			V
LOP Low Voltage	V_{OL}			0.1		0.4	V
$\overline{LOL}$ Low Voltage	V_{OL}	C_{LOL} = 0.01µF			0.44		V
ADI+, ADI- Input Bias Voltage				V_{CC} - 0.7	V_{CC} - 0.6	V_{CC} - 0.5	V
RSSI Output Voltage		ADI+, ADI- open			1.22		V
		(ADI+) - (ADI-) = 20mVp-p		2.00	2.12	2.30	
		(ADI+) - (ADI-) = 80mVp-p		2.38	2.51	2.70	
Op Amp Input Bias Current		1MΩ between INV and VTH		-100		+100	nA
INV Input Bias Voltage		1MΩ between INV and VTH		1.10	1.18	1.30	V

Note 1: Dice are tested at T_j = +45°C, V_{CC} = +4.25V.
Note 2: At T_A = -40°C, DC characteristics are guaranteed by design and characterization.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input Voltage Range	V_{ID}	BER < 10^{-10}, ADI inputs (Note 5)		0.003		1.2000	Vp-p
Input Referred Noise	V_N	ADI inputs			100		µV
Power-Detect Hysteresis		$V_{RELEASE}$ = 3.6mVp-p (Note 6)		2	3	5	dB
Limiting Amplifier Small-Signal Bandwidth	BW	(Note 7)			800		MHz
RSSI Output Voltage		(ADI+) - (ADI-) = 2mVp-p			1.36		V
		(ADI+) - (ADI-) = 20mVp-p			1.93		
Threshold Voltage	V_{TH}	$V_{RELEASE}$ = 3.6mVp-p			1.40		V
RSSI Linearity		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p			±0.7		%
RSSI Slope		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p (Note 8)			29		mV/dB
Loop Bandwidth		C_F = 2.2µF, R_F = 52.3Ω			350		kHz
		C_F = 0.022µF, R_F = 523Ω			3.5		MHz
Jitter Generation (Note 9)		C_F = 2.2µF, R_F = 52.3Ω			13		mUI
		C_F = 0.022µF, R_F = 523Ω			6		
Jitter-Transfer Peaking		R_F = 52.3Ω, C_F = 2.2µF				0.08	dB
Jitter Tolerance (Note 9)		R_F = 52.3Ω, C_F = 2.2µF	f = 10kHz		8		UI
			f = 25kHz	1.50	3.35		
			f = 250kHz	0.25	0.60		
			f = 1MHz	0.20	0.50		
Maximum Consecutive Input Run Length (1 or 0)					1000		Bits
Serial Clock-to-Q Delay	t_{CLK-Q}			195	275	370	ps
Serial Clock Frequency	f_{SCLK}				622.08		MHz

Note 3: AC parameters are guaranteed by design and characterization.
Note 4: The MAX3675 is characterized with a PRBS of 2^{23} - 1 maintaining a BER of ≤ 10^{-10} having a confidence level of 99.9%.
Note 5: A lower minimum input voltage of 2mVp-p is achievable; however, the LOP hysteresis is not guaranteed below 3.6mVp-p.
Note 6: Hysteresis = 20log($V_{RELEASE}$ / V_{ASSERT}).
Note 7: Small-signal bandwidth cannot be measured directly.
Note 8: RSSI slope = [V_{RSSI2} - V_{RSSI1}] / [20log (V_{ID2} / V_{ID1})].
Note 9: 1UI = 1 unit interval = (622.08MHz)$^{-1}$ = 1.608ns.

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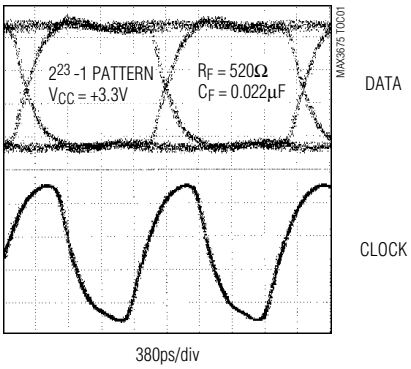
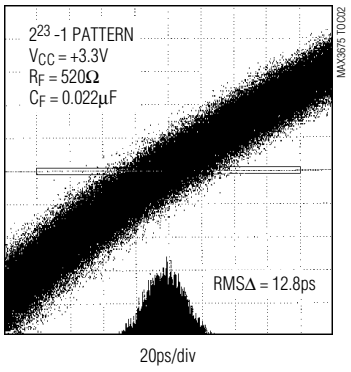
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

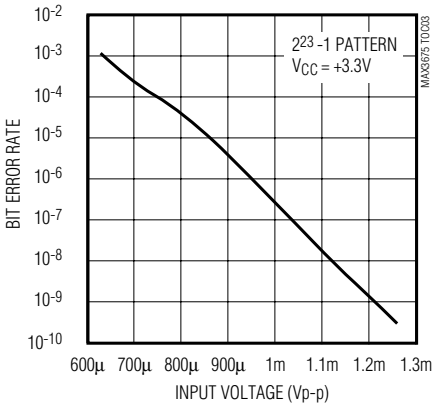
RECOVERED DATA AND CLOCK (SINGLE ENDED)



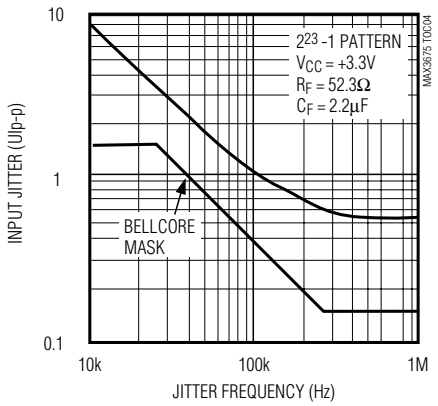
RECOVERED CLOCK JITTER



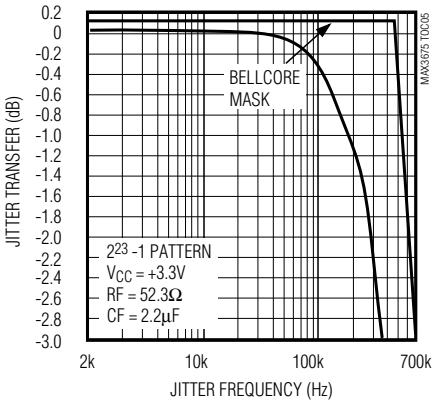
BIT ERROR RATE vs. INPUT VOLTAGE



JITTER TOLERANCE



JITTER TRANSFER



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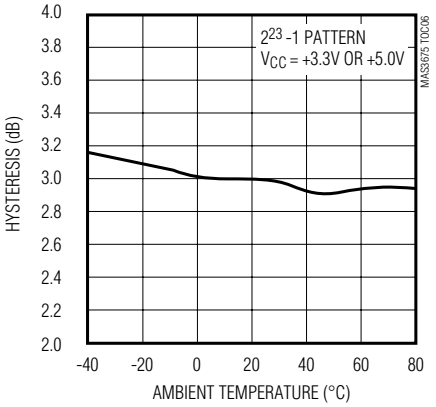
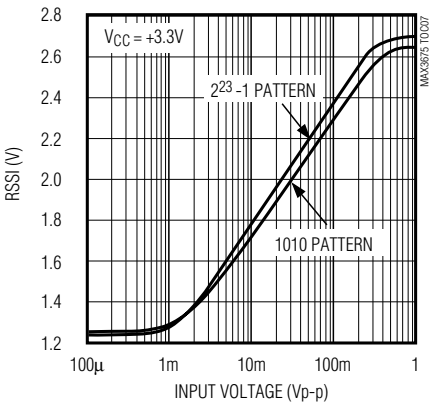
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

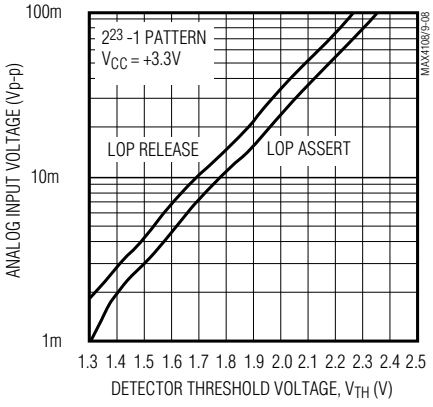
LOSS-OF-POWER HYSTERESIS vs. TEMPERATURE



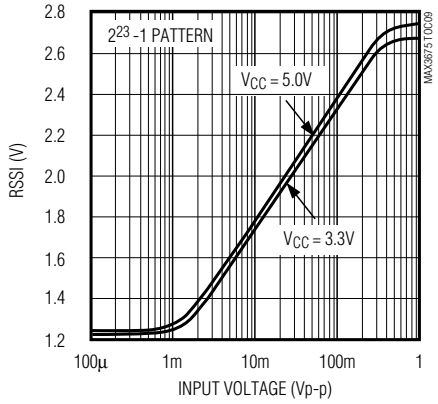
RECEIVED-SIGNAL-STRENTH INDICATOR vs. INPUT VOLTAGE



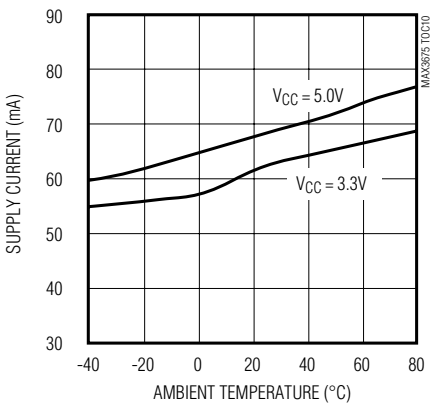
LOSS-OF-POWER ASSERT AND RELEASE LEVEL vs. THRESHOLD VOLTAGE



RECEIVED-SIGNAL-STRENGTH INDICATOR vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Pin Description

PIN	NAME	FUNCTION
1	OLC+	Positive Offset-Correction Loop Capacitor Input
2	OLC-	Negative Offset-Correction Loop Capacitor Input
3	RSSI	Received-Signal-Strength Indicator Output
4, 8, 16, 24, 25	GND	Supply Ground
5	INV	Op Amp Inverting Input. Attach to ground if op amp is not used.
6	VTH	Voltage Threshold Input. Threshold voltage for loss-of-power monitor. Attach to V_{CC} if LOP function is not used.
7	LOP	Loss-of-Power Output, TTL. Limiting amplifier loss-of-power monitor. Asserts high when input signal is below threshold set by VTH.
9, 12, 15, 18, 21, 31	V_{CC}	Positive Supply Voltage
10	SCLKO-	Negative Serial Clock Output, PECL, 622.08MHz. SDO- is clocked out on the falling edge of SCLKO-.
11	SCLKO+	Positive Serial Clock Output, PECL, 622.08MHz. SDO+ is clocked out on the rising edge of SCLKO+.
13	SDO-	Negative Serial Data Output, PECL, 622.08Mbps
14	SDO+	Positive Serial Data Output, PECL, 622.08Mbps
17	$\overline{LOL}$	Loss-of-Lock Output, TTL. PLL loss-of-lock monitor, active low (see *Design Procedure*).
19	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
20	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
22	FIL-	Negative Filter Input. PLL loop filter connection.
23	FIL+	Positive Filter Input. PLL loop filter connection.
26	DDI+	Positive Digital Data Input, PECL, 622.08Mbps serial-data stream
27	DDI-	Negative Digital Data Input, PECL, 622.08Mbps serial-data stream
28	INSEL	Input Select. Connect to GND to select digital data inputs or V_{CC} for analog data inputs.
29	ADI-	Negative Analog Data Input, 622.08Mbps serial-data stream
30	ADI+	Positive Analog Data Input, 622.08Mbps serial-data stream
32	CFILT	RSSI Filter Capacitor Input

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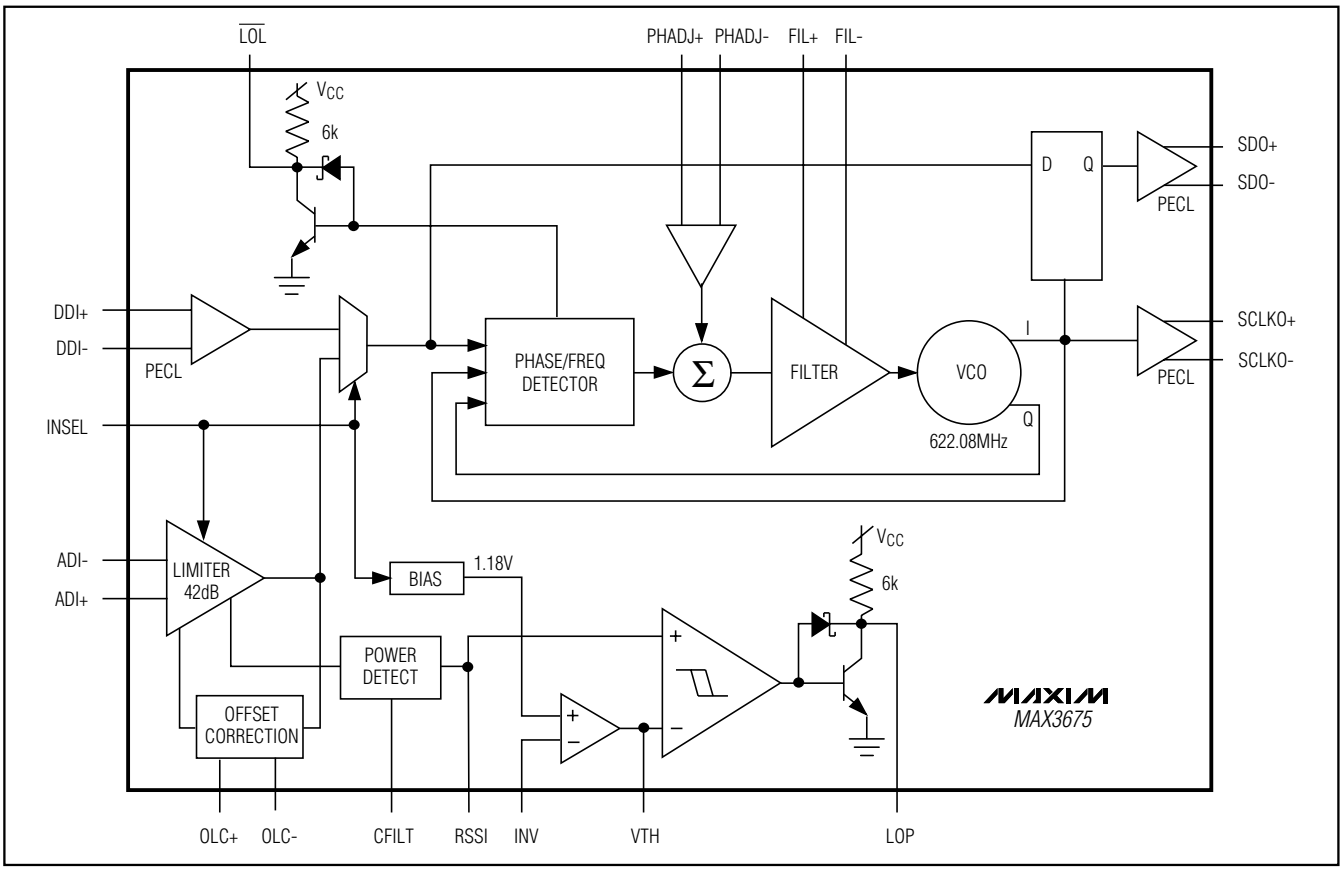

Figure 1. Functional Diagram

Detailed Description

Figure 1 shows the MAX3675's architecture. It consists of a limiting amplifier input stage followed by a fully integrated clock/data-recovery (CDR) block implemented with a PLL. The input stage is selectable between a limiting amplifier or a simple PECL input buffer. The limiting amplifier provides an LOP monitor and an RSSI. The PLL consists of a phase/frequency detector (PFD), a loop filter amplifier, and a voltage-controlled oscillator (VCO).

Limiting Amplifier

The MAX3675's on-chip limiting amplifier accepts an input signal level from 3.0mVp-p to 1.2Vp-p. The amplifier consists of a cascade of gain stages that include full-wave logarithmic detectors. The combined small-signal gain is approximately 42dB, and the -3dB bandwidth is 800MHz. Input-referred noise is less than 100μV_{RMS}, providing excellent sensitivity for small-amplitude data streams.

In addition to driving the CDR, the limiting amplifier provides both an RSSI output and an LOP monitor that allow the user to program the threshold voltage. The RSSI circuitry provides an output voltage that is linearly proportional to the input power (in decibels) detected between the ADI+ and ADI- input pins and is sensitive enough to reliably detect signals as small as 2mVp-p.

Input DC offset reduces the accuracy of the power detector; therefore, an integrated feedback loop is included that automatically nulls the input offset of the gain stage. The addition of this offset-correction loop requires that the input signal be AC-coupled when using the ADI+ and ADI- inputs.

Finally, for applications that do not require the limiting amplifier, selecting the digital inputs conserves power by turning off the postamplifier block.

Phase Detector

The phase detector produces a voltage proportional to the phase difference between the incoming data and

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the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the incoming data. The external phase adjustment pins (PHADJ+, PHADJ-) allow the user to vary the internal phase alignment.

Frequency Detector

A frequency detector incorporated into the PLL aids frequency acquisition during start-up conditions. The input data stream is sampled by quadrature components of the VCO clock, generating a difference frequency. Depending on the polarity of the difference frequency, the PFD drives the VCO so that the difference frequency is reduced to zero. Once frequency acquisition is obtained, the frequency detector returns to a neutral state.

Loop Filter and VCO

The VCO is fully integrated, while the loop filter requires an external R-C network. This filter network determines the bandwidth and peaking of the second-order PLL.

Design Procedure

Received-Signal-Strength Indicator (RSSI)

The RSSI output voltage is insensitive to temperature and supply fluctuations. The power detector functions as a broadband power meter that detects the total RMS power of all signals within the detector bandwidth (including input signal noise). The RSSI voltage varies linearly (in decibels) for inputs of 2mVp-p to 50mVp-p. The slope over this input range is approximately 29mV/dB.

The high-speed RSSI signal is filtered to an RMS level with one external capacitor tied from CFILT to V_{CC}. The impedance looking into CFILT is about 500Ω to V_{CC}. As a result, the lower -3dB cutoff frequency is set by the following simple relationship:

$$f_{FILT} = 1 / \left[2\pi(500)C_F\right]$$

For 622Mbps applications, Maxim recommends a cutoff frequency of 6.8kHz, which requires C_F = 47nF. The RSSI output is designed to drive a minimum load resistance of 10kΩ to ground and a maximum of 20pF. Loads greater than 20pF must be buffered by a series resistance of 10kΩ (i.e., voltmeter).

Input Offset Correction

The on-chip limiting amplifier provides more than 42dB of gain. A low-frequency feedback loop is integrated into the MAX3675 to remove the input offset. DC-coupling to the ADI+ and ADI- inputs is not allowed, as this would prevent the proper functioning of the DC offset-correction circuitry.

The differential input impedance (Z_{IN}) is approximately 2.5kΩ. The impedance between OLC+ and OLC- (Z_{OLC}) is approximately 120kΩ. Take care when setting the combined low-frequency cutoff (f_{CUTOFF}), due to the input DC-blocking capacitor (C_{IN}) and the offset correction loop capacitor (C_{OLC}). See Table 1 for selecting the values of C_{IN} and C_{OLC}.

These values ensure that the poles associated with C_{IN} and C_{OLC} work together to provide a flat response at the lower -3dB corner frequency (no gain peaking).

C_{IN} must be a low-TC, high-quality capacitor of type X7R or better in order to minimize f_{CUTOFF} deviations. C_{OLC} must be a capacitor of type Z5U or better.

Loss-of-Power (LOP) Monitor

A LOP monitor with a user-programmable threshold and a hysteresis comparator is also included with the limiting amplifier circuitry. Internally, one comparator input is tied to the RSSI output signal, and the other is tied to the threshold voltage (V_{TH}), which is set externally and provides a trip point for the LOP indication. A low-voltage, low-drift op amp, referenced to an internal bandgap voltage (1.18V), is supplied for programming a supply independent threshold voltage. This op amp requires two external resistors to program the LOP trip point. V_{TH} is programmable from 1.18V to 2.4V using the equation:

$$V_{TH} = 1.18\left(1 + R2 / R1\right)$$

The op amp can source only 20µA of current. Therefore, an R1 value greater than or equal to 100kΩ is recommended for proper operation. The input bias current of the op amp at the INV pin is guaranteed to be less than

Table 1. Setting the Low-Frequency Cutoff

C_{IN}	C_{OLC}	COMBINED LOW f_{CUTOFF} (kHz)
0.022µF	0.047µF	3.0
0.010µF	0.033µF	6.8
6800pF	0.022µF	10
4700pF	0.010µF	13.5
2200pF	4700pF	29
1000pF	3300pF	68
470pF	1000pF	135
330pF	680pF	190
220pF	470pF	290

±100nA. To set the threshold voltage externally (i.e., via a DAC control), completely disable the op amp by grounding the inverting terminal (INV). V_{TH} then becomes high impedance and must be driven externally.

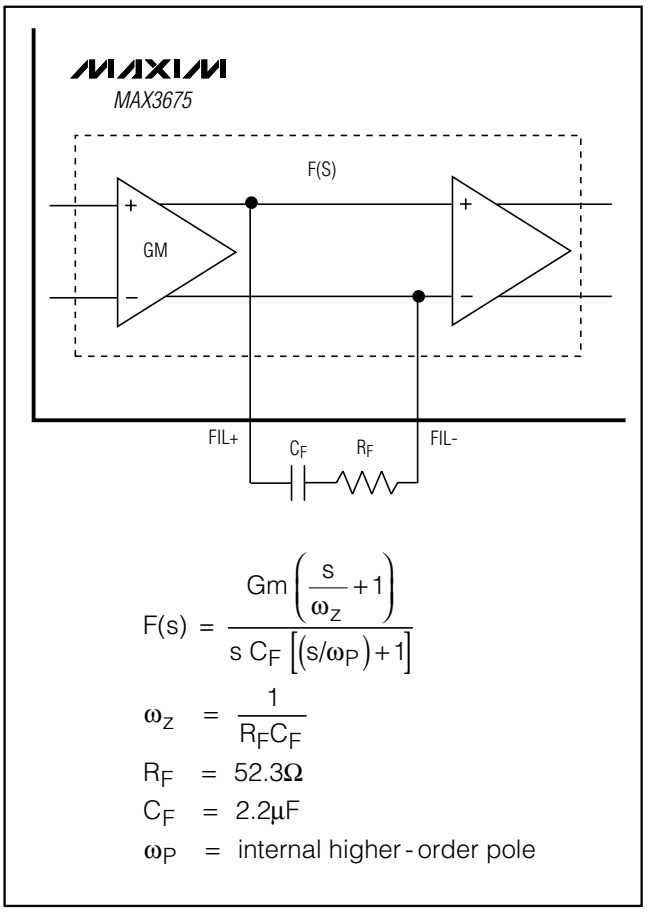
The comparator is configured with an active-high LOP output. An on-chip, 6kΩ pull-up resistor is provided to reduce external part count.

Setting the Loop Filter

The loop filter within the PLL consists of a transconductance amplifier and external filter elements R_F and C_F (Figure 2). The closed-loop bandwidth of a PLL is approximated by:

$$K_D\ K_O\ Gm\ R_F$$

where K_D is the gain of the phase detector, K_O is the gain of the VCO, and Gm is the transconductance of the filter amplifier. For the MAX3675, an estimated value of K_DK_OGm is 7k.



$$F(s) = \frac{Gm\left(\frac{s}{\omega_Z}+1\right)}{s\,C_F\left[\left(s/\omega_P\right)+1\right]}$$

$$\omega_Z = \frac{1}{R_FC_F}$$

$$R_F = 52.3\Omega$$

$$C_F = 2.2\mu F$$

$$\omega_P = \text{internal higher-order pole}$$

Figure 2. Loop Filter

Because the PLL is a second-order system, a zero in the open-loop gain is required for stability. This zero is set by the following equation:

$$\omega_Z = 1 / \left(R_FC_F\right)$$

where the recommended external value of C_F is 2.2µF.

Increasing the value of R_F increases the PLL bandwidth (f_{LOOP}). Increasing this bandwidth improves jitter tolerance and jitter-generation performance, but also reduces jitter-transfer performance. (Decreasing the bandwidth has the opposite effect.)

This type of PLL is a classical second-order system. Therefore, as f_Z (the frequency of the zero) approaches f_{LOOP}, the jitter-transfer peaking increases. For an overdamped system (f_Z/f_{LOOP}) < 0.25, the jitter peaking of a second-order system can be approximated by:

$$Mp = 1 - (f_Z / f_{LOOP})$$

where Mp is the magnitude of the peaking. For (f_Z/f_{LOOP}) < 0.1, this equation holds to within 10%.

C_F can be made smaller if meeting the jitter-transfer specifications is not a requirement. For example, setting R_F to 300Ω and C_F to 3.3nF increases the loop bandwidth to approximately 2.2MHz (Figure 3). Loop stability is ensured by maintaining a separation of 10x between f_{LOOP} and f_Z. Be careful when changing the value of R_F. Lower values of R_F are limited by the internal resistance of the IC, and upper values are limited by the internal high-frequency pole.

The MAX3675 is optimally designed to acquire lock and to provide a bit-error rate (BER) of less than 10^{-10} for long strings of consecutive zeros and ones. Using the recommended external component values of R_F = 52.3Ω ±1%

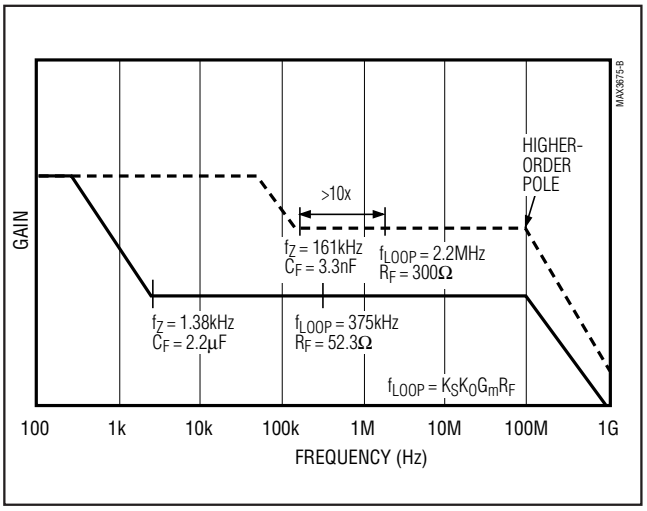


Figure 3. Loop-Filter Response

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and C_F = 2.2µF ±20%, measured results show that the MAX3675 can tolerate 1000 consecutive ones or zeros. It is important to select a type of capacitor for C_F that has a temperature stability of ±10% or better. This ensures performance over the -40°C to +85°C temperature range.

Lock Detect

The MAX3675's LOL monitor indicates when the PLL is locked. Under normal operation, the loop is locked and the $\overline{LOL}$ output signal is high. When the MAX3675 loses lock, a fast negative-edge transition occurs on $\overline{LOL}$. The output level remains at a low level (held by C_{LOL}) until the loop reacquires lock (Figure 4).

Input and Output Terminations

The MAX3675 digital data and clock I/Os (DDI+, DDI-, SDO+, SDO-, SCLK+, and SCLK-) are designed to interface with PECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to V_{CC} - 2V should be used with fixed-impedance transmission lines for proper termination. Make sure that the differential outputs have balanced loads.

The digital data input signals (DDI+ and DDI-) are differential inputs to an emitter-coupled pair. As a result, the MAX3675 can accept differential input signals as low as 250mV. These inputs can also be driven single-ended by externally biasing DDI- to the center of the voltage swing.

The MAX3675's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to V_{CC} as possible. Take care to isolate the input from the output signals to reduce feedthrough.

Applications Information

Driving the Limiting Amplifier Single-Ended

There are three important requirements for driving the limiting amplifier from a single-ended source (Figure 5):

1) There must be no DC-coupling to the ADI+ and ADI- inputs. DC levels at these inputs disrupt the offset-correction loop.
2) The terminating resistor R_T (50Ω) must be referenced to the ADI- input to minimize common-mode coupling problems.
3) The low-frequency cutoff for the limiting amplifier is determined by either C_{IN} and the 2.5kΩ input impedance or $C_b/2$ together with R_T. With C_b = 0.22µF and R_T = 50Ω, the low-frequency cutoff is 29kHz.

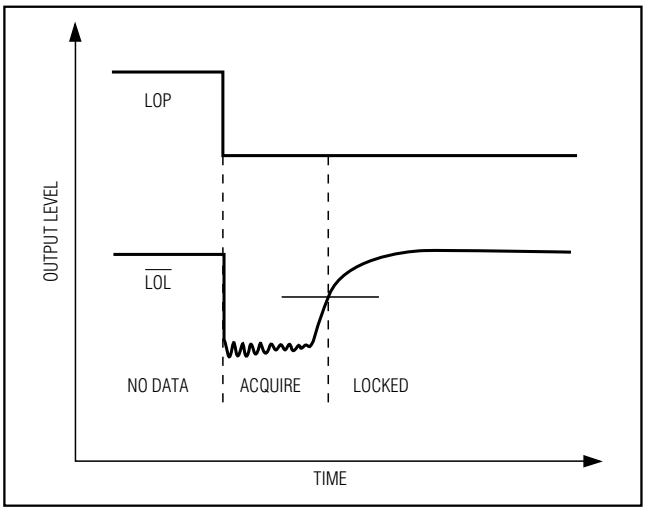

Figure 4. Loss-of-Lock Output

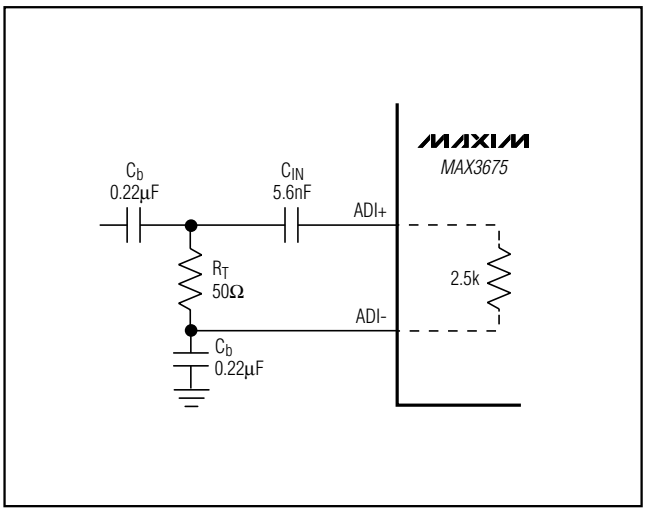

Figure 5. Single-Ended Input Termination

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Reduced Power Consumption Without the Limiting Amplifier

The limiting amplifier is biased independently from the clock recovery circuitry. Grounding INSEL turns off the limiting amplifier and selects the PECL DDI inputs.

Converting Average Optical Power to Signal Amplitude

Many of the MAX3675's specifications relate to input-signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 2 and Figure 6 are helpful for converting optical power to input signal when designing with the MAX3675.

In an optical receiver, the input voltage to the limiting amplifier can be found by multiplying the relationship in Table 2 by the photodiode responsivity and transimpedance amplifier gain.

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (power). At the inputs to the MAX3675 limiting amplifier, the power is V_{IN}^2/R. If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage at the input to the MAX3675 also increases by a factor of two.

The optical power increase is 10log(2x/x) = 10log(2) = +3dB.

At the MAX3675, the voltage increase is:

$$10\log\frac{(2V_{IN})^2/R}{V_{IN}^2/R} = 10\log(2^2) = 20\log(2) = +6dB$$

Table 2. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1)/2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\frac{r_e}{r_e+1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVE}/(r_e+1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVE}\frac{(r_e-1)}{r_e+1}$

Assuming a 50% average input data duty cycle.

In an optical receiver, the dB change at the MAX3675 always equals 2x the optical dB change.

The MAX3675's typical voltage hysteresis is 3.0dB. This provides an optical hysteresis of 1.5dB.

Jitter in Optical Receivers

Timing jitter, edge speeds, aberrations, optical dispersion, and attenuation all impact the performance of high-speed clock recovery for SDH/SONET receivers (Figure 7). These effects decrease the time available for error-free data recovery by reducing the received "eye opening" of nonreturn-to-zero (NRZ) transmitted signals.

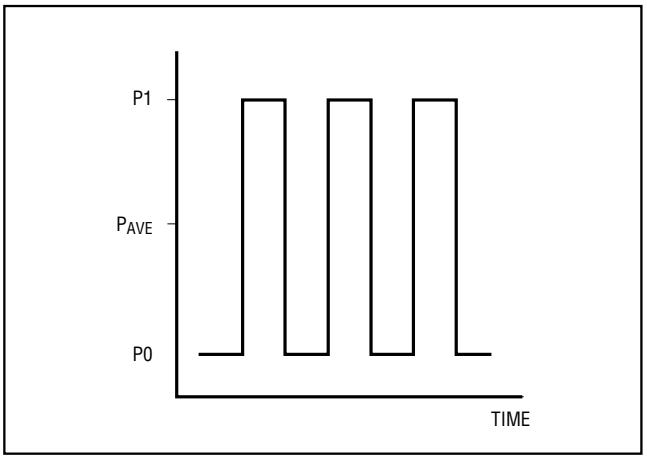

Figure 6. Optical Power Relations

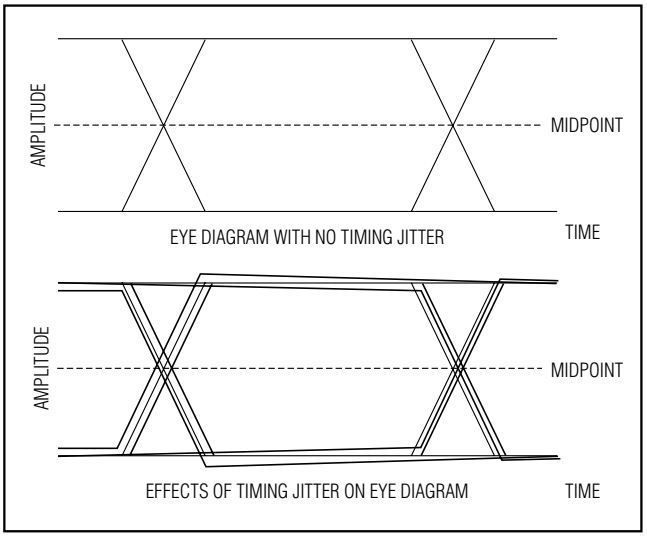

Figure 7. Eye Diagram With and Without Timing Jitter

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Optical receivers, incorporating transimpedance preamplifiers and limiting postamplifiers, can significantly clean up the effects of dispersion and attenuation. In addition, these amplifiers can provide fast transitions with minimal aberrations to the subsequent CDR blocks. However, these stages also add distortions to the midpoint crossing, contributing to timing jitter. Timing jitter is one of the most critical technical issues to consider when developing optical receivers and CDR circuits.

A better understanding of the different sources of jitter helps in the design and application of optical receiver modules and integrated CDR solutions. SDH/SONET specifications are well defined regarding the amount of jitter tolerance allowed at the inputs of optical receivers, as well as jitter peaking requirements, but they do little to define the different sources of jitter. The jitter that must be tolerated at an optical receiver input involves three significant sources, all of which are present in varying degrees in typical receiver systems:

1) Random jitter (RJ)
2) Pattern-dependent jitter (PDJ)
3) Pulse-width distortion (PWD)

Random Jitter (RJ)

RJ is caused by random noise present during edge transitions (Figure 8). This random noise results in random midpoint crossings. All electrical systems generate some random noise; however, the faster the speed of the transitions, the lower the effect of noise on random jitter. The following equation is a simple worst-case estimation of random jitter:

RJ (rms) = (rms noise) / (slew rate)

Pattern-Dependent Jitter (PDJ)

PDJ results from wide variations in the number of consecutive bits contained in NRZ data streams working against the bandwidth requirements of the receiver (Figure 9). The location of the lower -3dB cutoff frequency is important, and must be set to pass the low frequencies associated with long consecutive bit streams. AC-coupling is common in optical receiver design.

When using a limiting preamplifier with a highpass frequency response, select the input AC-coupling capacitor, C_{IN}, to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. As a result, the PDJ is dominated by the low-frequency cutoff of the preamplifier.

When using a preamplifier without a highpass response with the MAX3675, the following equation provides a good starting point for choosing C_{IN}:

$$C_{IN} \geq \frac{-t_L}{(1.25k\Omega)\ln\left[1-\frac{(PDJ)(BW)}{0.5}\right]}$$

where t_L = duration of the longest run of consecutive bits of the same value (seconds); PDJ = maximum

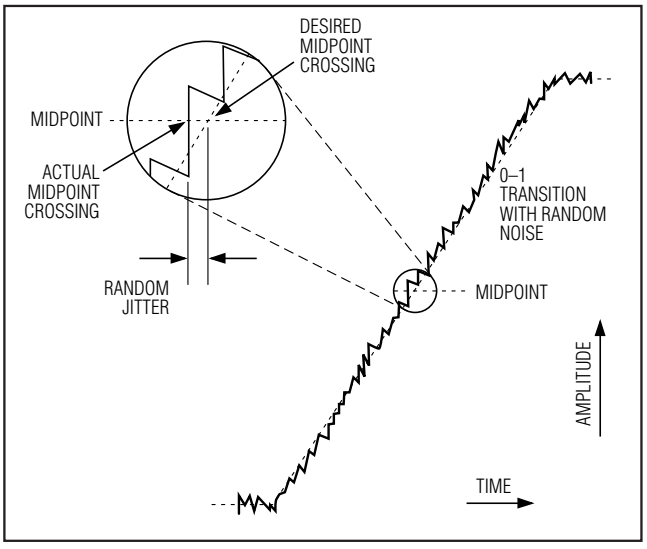

Figure 8. Random Jitter on Edge Transition

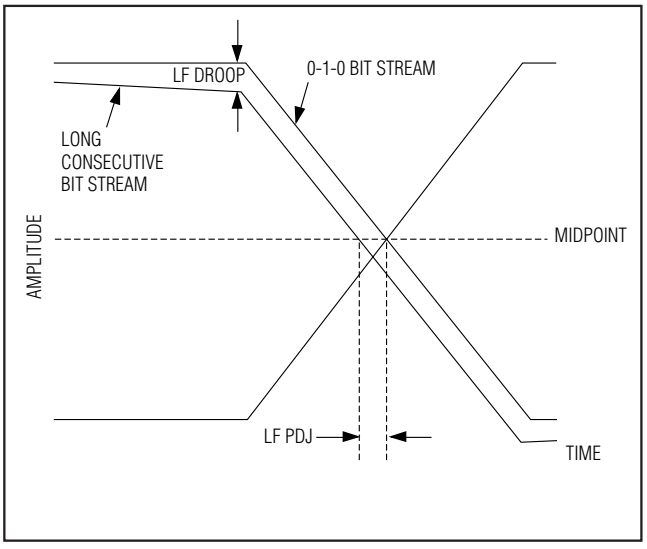

Figure 9. Pattern-Dependent Jitter Due to Low-Frequency Cutoff

allowable pattern-dependent jitter, peak-to-peak (seconds); and BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (Hertz). If the PDJ is still larger than desired, continue increasing the value of C_{IN}. Note that to maintain stability when using the MAX3675 analog inputs (ADI+, ADI-), it is important to keep the low-frequency cutoff associated with C_{OLC} below the corner frequency associated with C_{IN} (f_C) (Table 1).

PDJ can also be present due to insufficient high-frequency bandwidth (Figure 10). If the amplifiers are not fast enough to allow for complete transitions during single-bit patterns, or if the amplifier does not allow adequate settling time, high-frequency PDJ can result.

Pulse-Width Distortion (PWD)

Finally, PWD occurs when the midpoint crossing of a 0–1 transition and a 1–0 transition do not occur at the same level (Figure 11). DC offsets and nonsymmetrical rising and falling edge speeds both contribute to PWD. For a 1–0 bit stream, calculate PWD as follows:

PWD = [(width of wider pulse) -
(width of narrower pulse)] / 2

Phase Adjust

The internal clock and data alignment in the MAX3675 is well maintained close to the center of the data eye. Although not required, this sampling point can be shifted using the PHADJ inputs to optimize BER performance. The PHADJ inputs operate with differential input signals to approximately ±1V. A simple resistor-divider with a bypass capacitor is sufficient to set up these levels. When the PHADJ inputs are not used, they should be tied directly to V_{CC}.

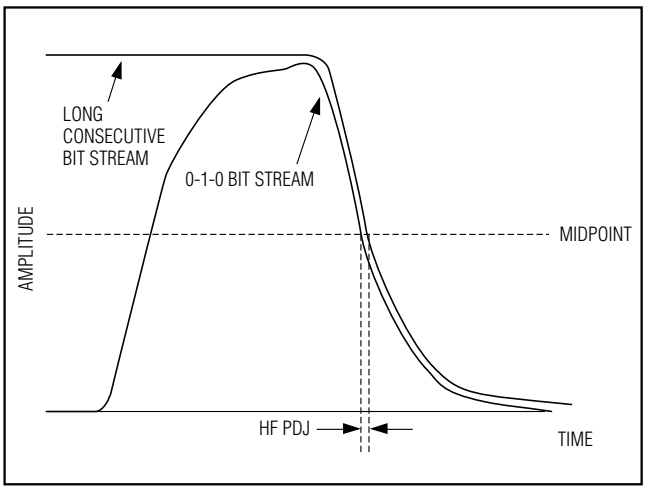

Figure 10. Pattern-Dependent Jitter Due to High-Frequency Rolloff

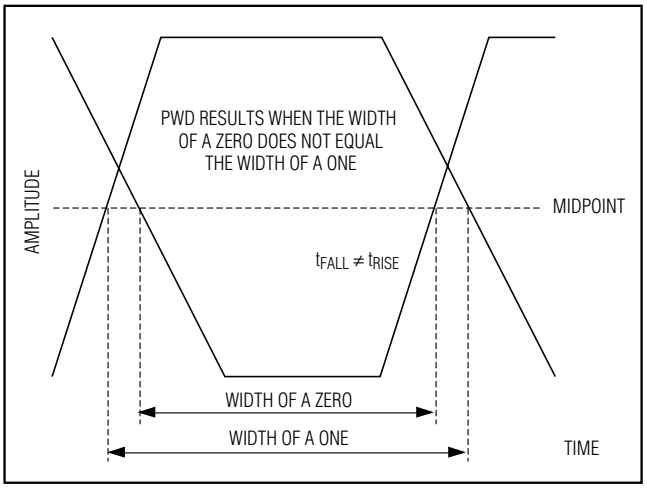

Figure 11. Pulse-Width Distortion

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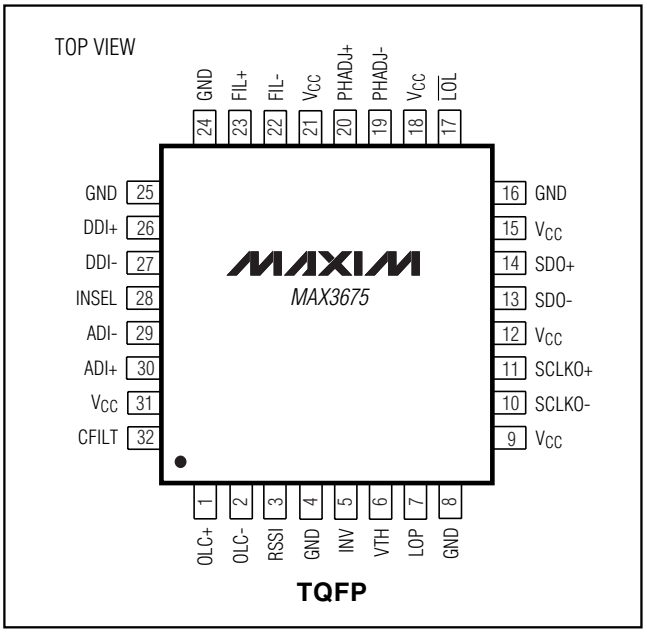
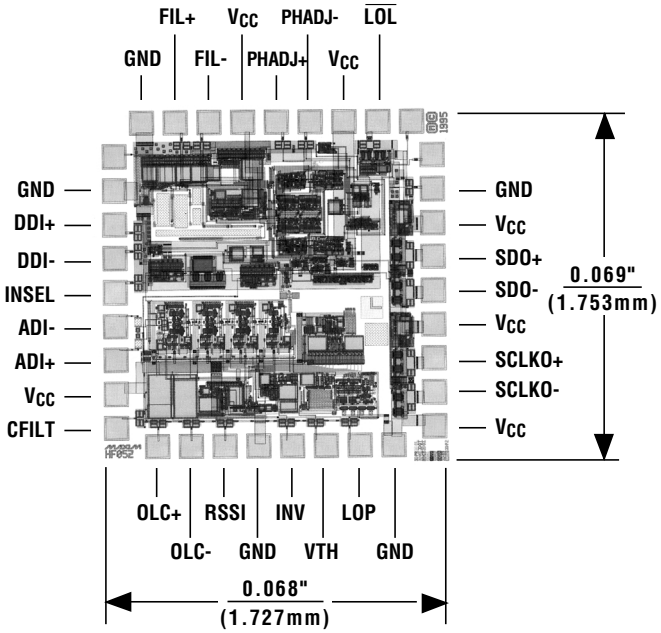
Pin Configuration



Chip Topography



Chip Information

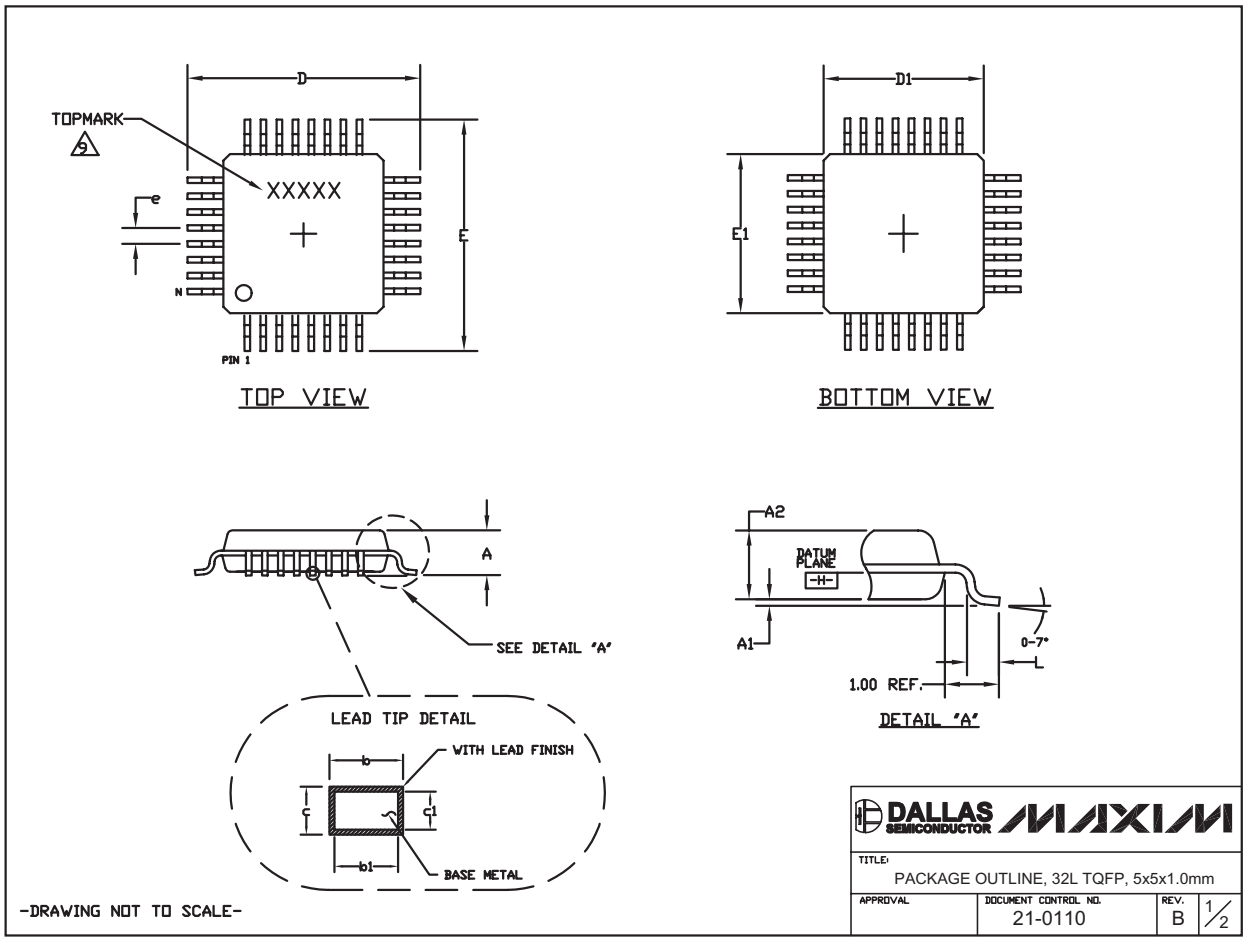
TRANSISTOR COUNT: 1380

PROCESS: BiPolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L TQFP, 5x5x01.0.EPS



622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. TOPMARK SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AAA	
	5x5x1.0 MM	
	MIN.	MAX.
A	—	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	6.80	7.20
D_1	4.80	5.20
E	6.80	7.20
E_1	4.80	5.20
L	0.45	0.75
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0110	B	2/2

Revision History

Pages changed at Rev 4: 1, 2, 15, 16