

## FEATURES

### ■ High Performance PCI Audio Accelerator

- Powerful RAM-based SLIMD™ DSP core provides high task concurrency and maximum flexibility
- Efficient bus mastering PCI interface minimizes host loading
- DMA engine with hardware scatter-gather manages up to 96 simultaneous audio/data streams

### ■ Flexible Digital Audio Interface Design

- Direct Connection to CS423x Codec
- Simple expansion to 6 audio output channels
- Direct Connection to CS4297 AC'97 Codec

### ■ Complete Solution including DSP Software and Windows 95® drivers

- Acceleration of DirectSound®, DirectSound3D®, Direct-Input™, and DirectShow™ APIs
- High Quality HRTF-Based 3D Positional Sound
- General MIDI Wavetable Synthesis with Reverb and Chorus
- Dolby® AC-3® (5.1 channel) and MPEG-2 Audio Decoding (CS4610 only) with speaker virtualization

## DESCRIPTION

The CS4610/11 is a high performance audio accelerator for the PCI bus. This device, combined with application and driver software, provides a complete system solution for hardware acceleration of Windows 95 DirectSound, DirectSound3D, Direct-Input, DirectShow, and Wavetable Synthesis.

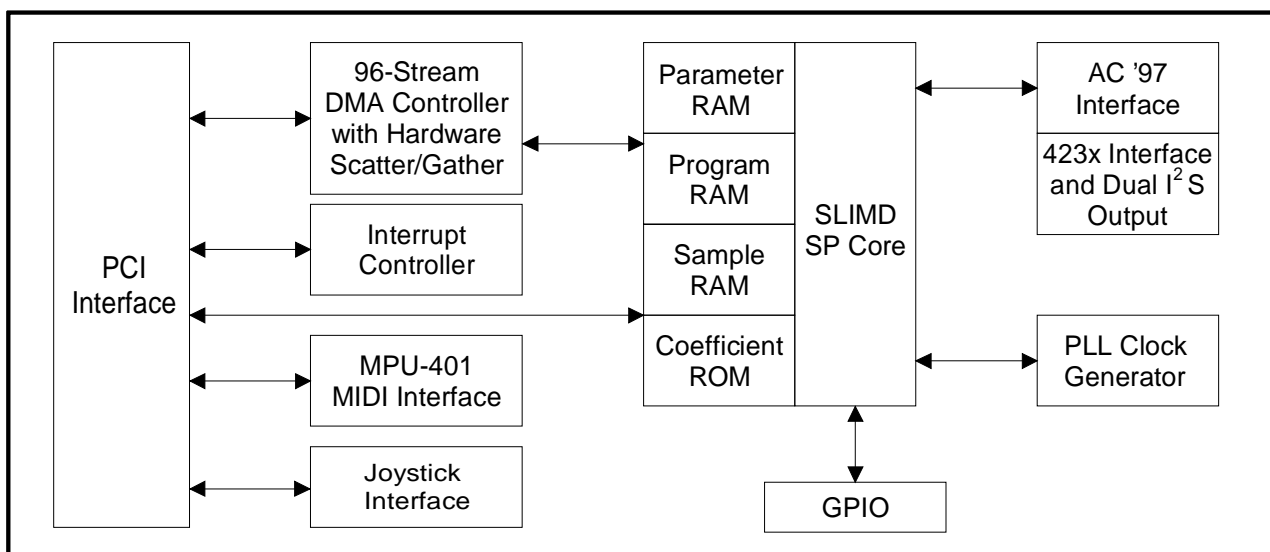
## CrystalClear™ SoundFusion™ PCI Audio Accelerator

The CS4610/11 is based on the Cirrus Logic, CrystalClear Stream Processor (SP) DSP core. The SP core is optimized for digital audio processing, and is powerful enough to handle complex signal processing tasks such as Dolby AC-3 decoding (CS4610 only) with ease. The SP core is supported by a bus mastering PCI interface and a built-in dedicated DMA engine with hardware scatter-gather support. These support functions ensure extremely efficient transfer of audio data streams to and from host-based memory buffers, providing a system solution with maximum performance and minimal host CPU loading.

The all-digital CS4610/11 supports a variety of audio I/O configurations, including direct connection to the CrystalClear CS423x Codecs via a bi-directional serial data link, or direct connection to an AC'97 Codec such as the CrystalClear CS4297.

### ORDERING INFORMATION

CS4610-CM	100-pin MQFP	20x14x3.07 mm
CS4610C-CQ	128-pin TQFP	20x14x1.60 mm
CS4611-CM	100-pin MQFP	20x14x3.07 mm



## ABSOLUTE MAXIMUM RATINGS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	PCIVDD	-	-	4.6	V
	CVDD	-	-	4.6	V
	CRYVDD	-	-	4.6	V
	VDD5REF	-	-	5.5	V
Total Power Dissipation (Note 1)		-	-	1.5	W
Input Current per Pin, DC (Except supply pins)		-	-	10	mA
Output current per pin, DC		-	-	10	mA
Input voltage (Note 2)		-0.3	-	5.75	V
Ambient temperature (power applied) (Note 3)		-45	-	85	°C
Storage temperature		-55	-	150	°C

- Notes:
1. Includes all power generated by AC and/or DC output loading.
  2. The power supply pins are at recommended maximum values. XTALI & XTALO are at 3.6 V maximum.
  3. At ambient temperatures above 70° C, total power dissipation must be limited to less than 0.4 Watts.

**WARNING:** Operation beyond these limits may result in permanent damage to the device.  
 Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
		CS4610			CS4611			
Power Supplies	PCIVDD	3	3.3	3.6	3	3.3	3.6	V
	CVDD	3	3.3	3.6	3	3.3	3.6	V
	CRYVDD	3	3.3	3.6	3	3.3	3.6	V
	VDD5REF	4.75	5	5.25	4.75	5	5.25	V
Internal DSP Frequency		-	-	100	-	-	85	MHz
Operating Ambient Temperature	T <sub>A</sub>	0	25	70	0	25	70	°C

Specifications are subject to change without notice.

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Dolby's AC3 Technology is implemented on the CS4610 Stream Processor Only. Supply of this Implementation of Dolby Technology does not convey a license nor imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

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**AC CHARACTERISTICS (PCI SIGNAL PINS ONLY)** ( $T_A = 70^\circ \text{C}$ ;

PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V;

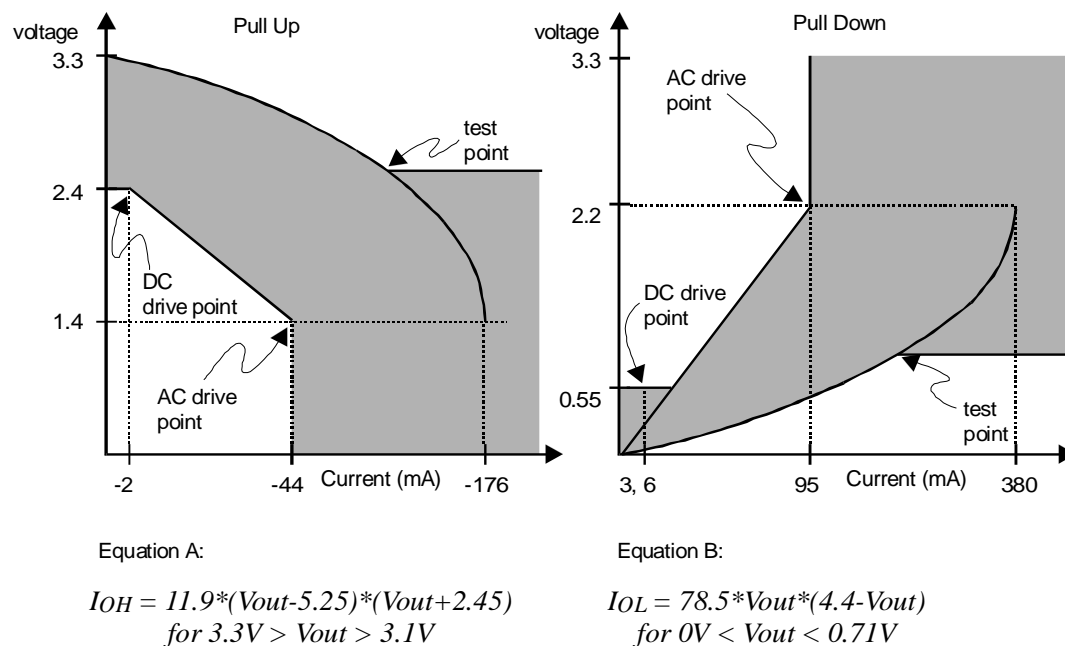
Logic 0 = 0 V, Logic 1 = 3.3 V; Reference levels = 1.4 V; unless otherwise noted; (Note 4))

Parameter	Symbol	Min	Max	Unit
Switching Current High (Note 5) $0 < V_{out} < 1.4$ $1.4 < V_{out} < 2.4$ $3.1 < V_{out} < 3.3$	$I_{OH}$	-44 $-44 + \frac{V_{out} - 1.4}{0.024}$ -	- - Note 7	mA mA
Switching Current Low (Note 5) $V_{out} > 2.2$ $2.2 > V_{out} > 0.55$ $0.71 > V_{out} > 0$	$I_{OL}$	95 $V_{out}/0.023$ -	- - Note 8	mA mA
Low Clamp Current $-5 < V_{in} < -1$	$I_{CL}$	$-25 + \frac{V_{in} + 1}{0.015}$	-	mA
Output rise slew rate 0.4 V - 2.4 V load (Note 6)	slewr	1	5	V/ns
Output fall slew rate 2.4 V - 0.4 V load (Note 6)	slewf	1	5	V/ns

Notes: 4. Specifications guaranteed by characterization and not production testing.

5. Refer to V/I curves in Figure 1. Specification does not apply to CLK and RST# signals. Switching Current High specification does not apply to SERR# and INTA# which are open drain outputs.

6. Cumulative edge rate across specified range. Rise slew rates do not apply to open drain outputs.

7. Equation A:  $I_{OH} = 11.9 * (V_{out} - 5.25) * (V_{out} + 2.45)$  for  $3.3 \text{ V} > V_{out} > 3.1 \text{ V}$ 8. Equation B:  $I_{OL} = 78.5 * V_{out} * (4.4 - V_{out})$  for  $0 \text{ V} < V_{out} < 0.71 \text{ V}$ **Figure 1. AC Characteristics**

**DC CHARACTERISTICS** ( $T_A = 70^\circ \text{C}$ ; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V;  
PCIGND = CGND = CRYGND = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
<b>PCI Interface Signal Pins</b>					
High level input voltage	$V_{IH}$	2	-	5.75	V
Low level input voltage	$V_{IL}$	-0.5	-	0.8	V
High level output voltage $I_{out} = -2 \text{ mA}$	$V_{OH}$	2.4	-	-	V
Low level output voltage $I_{out} = 3 \text{ mA}, 6 \text{ mA}$ (Note 9)	$V_{OL}$	-	-	0.55	V
High level leakage current $V_{in} = 2.7 \text{ V}$ (Note 10)	$I_{IH}$	-	-	70	$\mu\text{A}$
Low level leakage current $V_{in} = 0.5 \text{ V}$ (Note 10)	$I_{IL}$	-	-	-70	$\mu\text{A}$
<b>Non-PCI Interface Signal Pins (Except XTALO)</b>					
High level input voltage	XTALI	2.3	3.3	4.0	V
	Other Pins	2	-	5.75	V
Low level input voltage	XTALI	-0.5	0	0.8	V
	Other Pins	-0.5	-	0.8	V
High level output voltage $I_{out} = -4 \text{ mA}$ (Note 11)	$V_{OH}$	2.4	-	-	V
Low level output voltage $I_{out} = 4 \text{ mA}$	$V_{OL}$	-	-	0.4	V
High level leakage current $V_{in} = 5.25 \text{ V}$	$I_{IH}$	-	-	10	$\mu\text{A}$
Low level leakage current $V_{in} = 0$	$I_{IL}$	-	-	-10	$\mu\text{A}$

Parameter	Min	Typ	Max	Min	Typ	Max	Unit
	CS4610			CS4611			
<b>Power Supply Pins (Outputs Unloaded)</b>							
Power Supply Current: VDD5REF	-	0.6	-	-	0.6	-	mA
PCIVDD/CVDD/CRYVDD Total (Notes 4,12)	-	200	370	-	164	240	mA
Low Power Mode Supply Current	-	10	-	-	10	-	mA

- Notes: 9. The following signals are tested to 6 mA: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, and INTA#. All other PCI interface signals are tested to 3 mA.
10. Input leakage currents include hi-Z output leakage for all bi-directional buffers with three-state outputs. At supply voltages of 3.6 V or higher and ambient temperatures of  $70^\circ \text{C}$ , the high level leakage current may exceed 70  $\mu\text{A}$ . For normal operating ranges of  $25^\circ \text{C}$  and a supply voltage of 3.3 V, the high level leakage current is within specification.
11. For open drain pins, high level output voltage is dependent on external pull-up used and number of attached gates.
12. Typical values are given as average current with typical SP task execution and data streaming. Current values vary dramatically based on the software running on the SP.

**PCI INTERFACE PINS** ( $T_A = 0$  to  $70^\circ\text{C}$ ; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V)

Parameter	Symbol	Min	Max	Unit
PCICLK cycle time	$t_{\text{cyc}}$	30	-	ns
PCICLK high time	$t_{\text{high}}$	11	-	ns
PCICLK low time	$t_{\text{low}}$	11	-	ns
PCICLK to signal valid delay - bused signals	$t_{\text{val}}$	2	11	ns
PCICLK to signal valid delay - point to point	$t_{\text{val(p+p)}}$	2	12	ns
Float to active delay (Note 13)	$t_{\text{on}}$	2	-	ns
Active to Float delay (Note 13)	$t_{\text{off}}$	-	28	ns
Input Set up Time to PCICLK - bused signals	$t_{\text{su}}$	7	-	ns
Input Set up Time to PCICLK - point to point	$t_{\text{su(p+p)}}$	10, 12	-	ns
Input hold time for PCICLK	$t_{\text{h}}$	0	-	ns
Reset active time after PCICLK stable (Note 14)	$t_{\text{rst-clk}}$	100	-	$\mu\text{s}$
Reset active to output float delay (Notes 13, 14, 15)	$t_{\text{rst-off}}$	-	40	ns

- Notes: 13. For Active/Float measurements, the Hi-Z or "off" state is when the total current delivered is less than or equal to the leakage current. Specification is guaranteed by design, not production tested.  
 14. RST# is asserted and de-asserted asynchronously with respect to PCICLK.  
 15. All output drivers are asynchronously floated when RST# is active.

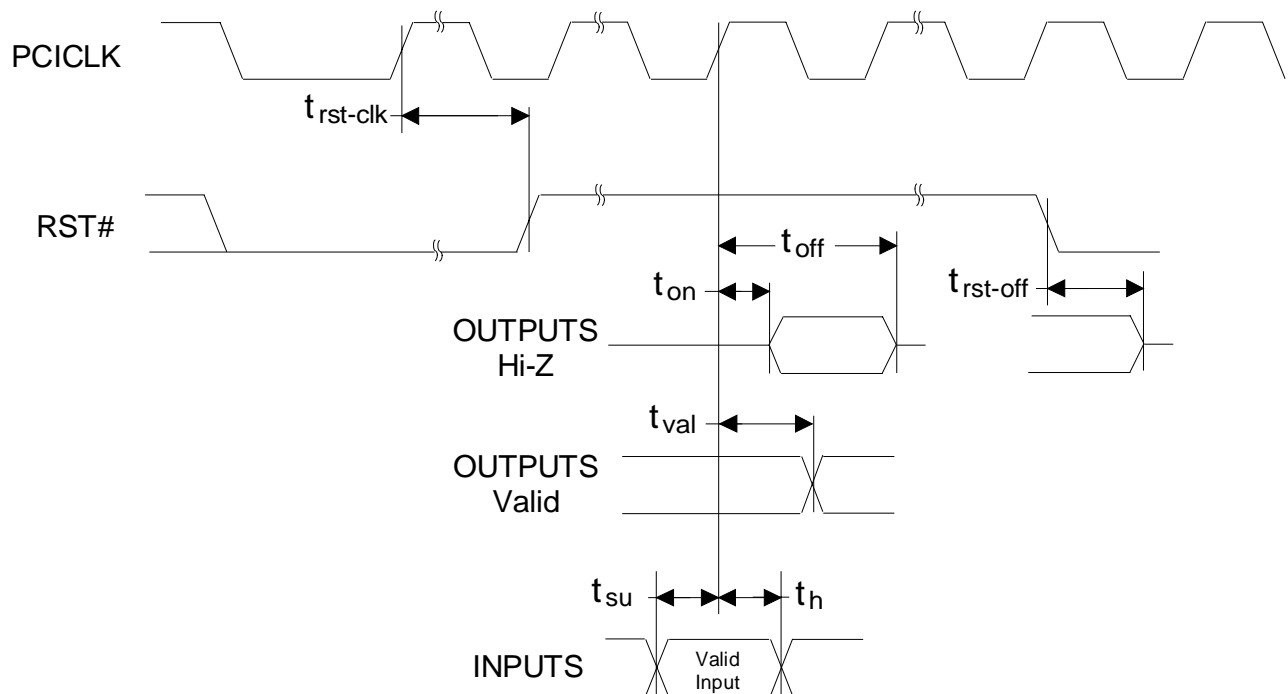


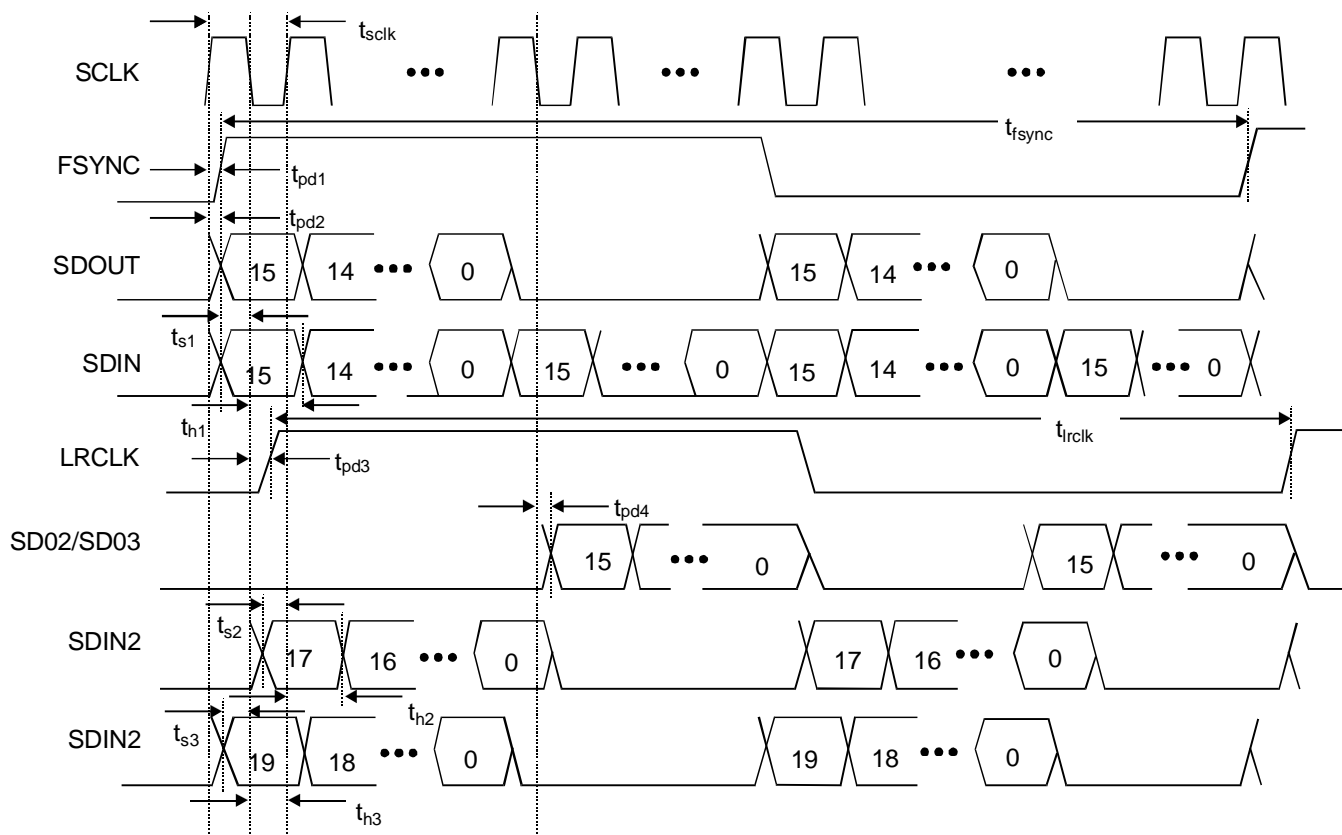
Figure 2. PCI Timing Measurement Conditions

**CS4610/11 + CS423X CONFIGURATION** ( $T_A = 0$  to  $70^\circ\text{C}$ ;

PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V;

Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK input cycle time	$t_{\text{sclk}}$	320	354	-	ns
FSYNC input cycle time	$t_{\text{fsync}}$	20480	22676	-	ns
SCLK rising to FSYNC transition	$t_{\text{pd1}}$	-20	-	20	ns
SCLK rising to SDOUT valid	$t_{\text{pd2}}$	-	25	45	ns
SDIN valid to SCLK falling	$t_{\text{s1}}$	30	-	-	ns
SDIN hold after SCLK falling	$t_{\text{h1}}$	30	-	-	ns
LRCLK output cycle time	$t_{\text{lrlclk}}$	20480	22676	-	ns
SCLK falling to LRCLK transition	$t_{\text{pd3}}$	-	25	45	ns
SCLK falling to SDO2/SDO3 valid	$t_{\text{pd4}}$	-	25	45	ns
SDIN2 valid to SCLK rising (SI2F1-0: 00)	$t_{\text{s2}}$	30	-	-	ns
SDIN2 hold after SCLK rising (SI2F1-0: 00)	$t_{\text{h2}}$	30	-	-	ns
SDIN2 valid to SCLK falling (SI2F1-0: 01)	$t_{\text{s3}}$	30	-	-	ns
SDIN2 hold after SCLK falling (SI2F1-0: 01)	$t_{\text{h3}}$	30	-	-	ns


**Figure 3. CS4610/11 and CS423x Link and 6 Channel Output Timing Diagram**

**AC'97 SERIAL INTERFACE TIMING** ( $T_A = 0$  to  $70^\circ\text{C}$ ; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK cycle time	$t_{\text{aclk}}$	78	81.4	-	ns
ABITCLK rising to ASDOUT valid	$t_{\text{pd5}}$	-	17	25	ns
ASDIN valid to ABITCLK falling	$t_{\text{s5}}$	15	-	-	ns
ASDIN hold after ABITCLK falling	$t_{\text{h5}}$	5	-	-	ns
PCICLK rising to ARST# valid	$t_{\text{pd6}}$	-	10	-	ns

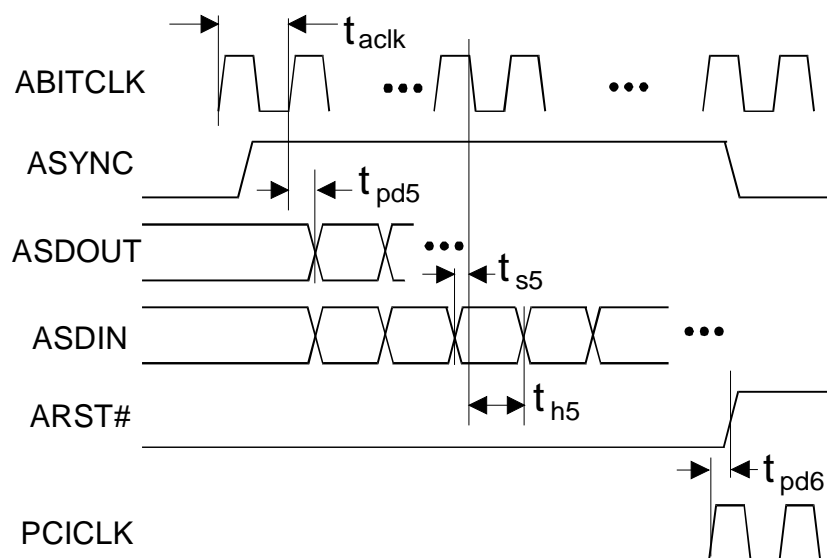
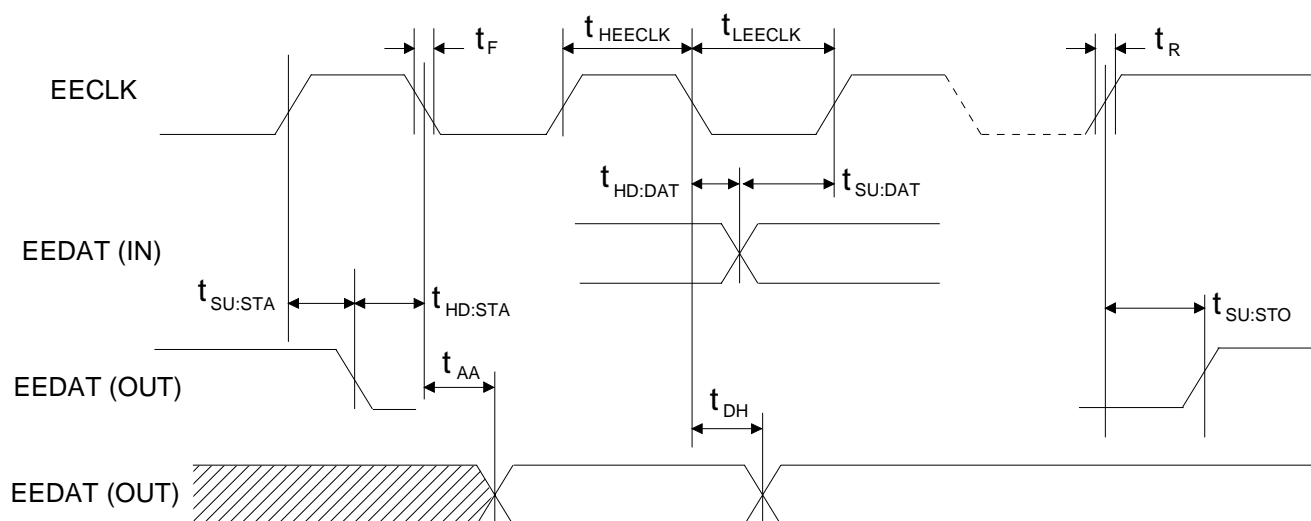


Figure 4. AC'97 Configuration Timing Diagram

**EEPROM TIMING CHARACTERISTICS** Note 4. ( $T_A = 0$  to  $70^\circ\text{C}$ ,  $\text{PCIVDD} = \text{CVDD} = \text{CRYVDD} = 3.3\text{ V}$ ;  $\text{VDD5REF} = 5\text{ V}$ ;  $\text{VDD5REF} = 5\text{ V}$ ;  $\text{PCIGND} = \text{CGND} = \text{CRYGND} = 0\text{ V}$ ; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; PCI clock frequency = 33 MHz; unless otherwise noted)

Parameter	Symbol	Min	Max	Units
EECLK Low to EEDAT Data Out Valid	$t_{AA}$	0	7.0	$\mu\text{s}$
Start Condition Hold Time	$t_{HD:STA}$	5.0	-	$\mu\text{s}$
EECLK Low	$t_{LEECLK}$	10	-	$\mu\text{s}$
EECLK High	$t_{HEECLK}$	10	-	$\mu\text{s}$
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	5.0	-	$\mu\text{s}$
EEDAT In Hold Time	$t_{HD:DAT}$	0	-	$\mu\text{s}$
EEDAT In Setup Time	$t_{SU:DAT}$	250	-	ns
EEDAT/EECLK Rise Time (Note 16)	$t_R$	-	1	$\mu\text{s}$
EEDAT/EECLK Fall Time	$t_F$	-	300	ns
Stop Condition Setup Time	$t_{SU:STO}$	5.0	-	$\mu\text{s}$
EEDAT Out Hold Time	$t_{DH}$	0	-	$\mu\text{s}$

Notes: 16. Rise time on EEDAT is determined by the capacitance on the EEDAT line with all connected gates and the required external pull-up resistor.



**Figure 5. EEPROM Timing**



## OVERVIEW

The CS4610 and CS4611 are high performance audio accelerator DSPs for the PCI bus. These devices, combined with application and driver software, provide a complete system solution for cost effective acceleration of Windows® DirectSound, DirectSound3D, DirectInput, DirectShow, MIDI playback via Wavetable Synthesis with reverberation and chorus effects processing, and more.

The CS4610 is a high-performance, full-featured version of the SoundFusion audio accelerator. The CS4611 is a reduced-cost version of the CS4610. The CS4611 has a lower max clock speed and does not support AC-3 or MPEG-2. Please refer to the *OEM Software Reference Manual* for more details.

There are three main functional blocks within the CS4610/11: the Stream Processor, the PCI Interface, and the DMA Engine. The Stream Processor (SP) is a high speed custom Digital Signal Processor (DSP) core designed by Cirrus Logic, Inc. specifically for audio signal processing. This extremely powerful DSP core is capable of running complex algorithms such as Dolby Digital AC-3 or MPEG-2 audio decoding for applications such as DVD movie playback or gaming. The SP is capable of running a number of different signal processing algorithms simultaneously. This high concurrency capability is valuable for applications such as immersive 3D games, which may play a number of DirectSound streams, a number of DirectSound3D streams, and a MIDI music sequence simultaneously.

Separate RAM memories are included on-chip for the SP program code (Program RAM), parameter data (Parameter RAM), and audio sample data (Sample RAM). A small ROM memory (Coefficient ROM) is included to store fixed coefficient data required for the sample rate conversion and audio decompression algorithms.

The RAM-based DSP architecture of the CS4610/11 ensures maximum system flexibility. The software function/feature mix can be adapted

to meet the requirements of a variety of different applications, such as DirectX™ games, DVD movie playback, or DOS applications. This RAM-based architecture also provides a means for future system upgrades, allowing the addition of new or upgraded functionality through software updates.

The CS4610/11 provides an extremely efficient bus mastering interface to the PCI bus. The PCI Interface function allows economical burst mode transfers of audio data between host system memory buffers and the CS4610/11 device. Program code and parameter data are also transferred to the CS4610/11 over the PCI Interface.

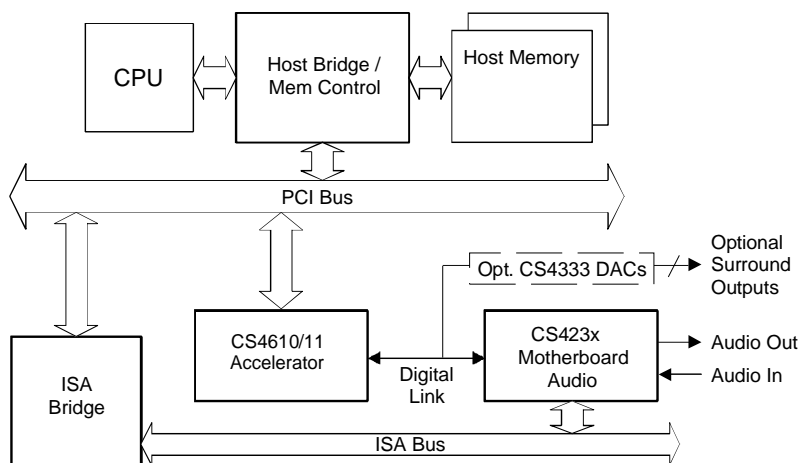
The CS4610/11 DMA Engine provides dedicated hardware to manage transfer of up to 96 concurrent audio/data streams to and from host memory buffers. The DMA Engine provides hardware scatter-gather support, allowing simple buffer allocation and management. This implementation improves system efficiency by minimizing the number of host interrupts.

The CS4610/11 supports a variety of audio I/O configurations, including direct connection to the CrystalClear CS423x Codecs or to an AC'97 Codec such as the CrystalClear CS4297. The system's flexibility is further enhanced by the inclusion of auxiliary ADC and DAC ports, a bi-directional serial MIDI port, a joystick port, a hardware volume control interface, and a serial data port which allows connection of an optional external EEPROM device.

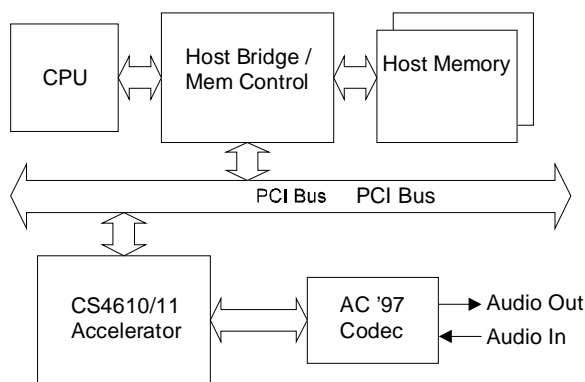
The block diagram in Figure 6 depicts a motherboard audio subsystem based on the CS4610/11 and the CS423x. This approach features the proven ISA legacy support of the CS423x Codecs (which include the CS423xB family as well as the CS4235 and CS4239 devices). The CS423x provides DOS applications with hardware compatibility for the Sound Blaster Pro™, OPL3, and MPU-401 register sets. In this configuration, the CS423x also provides the system joystick interface. The CS423x

provides all Analog-to-Digital conversion (ADC) and Digital-to-Analog conversion (DAC) functions. Digital audio is transferred between the CS423x and the CS4610/11 over a proprietary bi-directional serial data link between the two devices. MIDI data from the CS423x MPU-401 UART is also transferred serially to the CS4610. DOS applications can directly address the CS423x audio functions on the ISA bus. Windows DirectX audio applications will address the PCI-based CS4610/11 device through Windows DirectX drivers, wherein the CS423x is utilized as the external Codec for analog I/O.

A system diagram depicting connection of the CS4610/11 to the CrystalClear CS4297 AC'97 Codec is given in Figure 7. All analog audio inputs and outputs are connected to the AC'97 Codec. Audio data is passed between the AC'97 Codec and the CS4610/11 over the serial AC-Link. The CS4610/11 provides a hardware interface for connection of a joystick and MIDI devices. Legacy audio support under a Windows DOS Box is provided via virtualization of the Sound Blaster™, OPL3 FM synthesizer and MPU-401 MIDI interface registers.



**Figure 6. CS4610/11 + CS423x Motherboard Audio Configuration**



**Figure 7. CS4610/11 + AC '97 Codec Configuration**

## **Stream Processor DSP Core**

The CS4610/11 Stream Processor (SP) is a custom DSP core design optimized for processing and synthesizing digital audio data streams. The SP features a Somewhat Long Instruction Multiple Data (SLIMD) modified dual Harvard architecture. The device uses a 40-bit instruction word and operates on 32-bit data words. The SP core is conservatively rated at 300 Million Instructions per second (300 MIPS) when running at a 100 MHz internal clock speed (CS4611 runs at 85 MHz). The SP includes two Multiply-Accumulate (MAC) blocks and one 16-bit Arithmetic and Logic Unit (ALU). The MAC units perform 20-bit by 16-bit multiplies and have 40-bit accumulators, providing higher quality than typical 16-bit DSP architectures.

## **PLL and Clock Control**

The CS4610/11 includes a programmable Phase Locked Loop (PLL) circuit which generates the high frequency internal SP clock from a lower frequency input clock. The PLL input may come from the CS4610/11 crystal oscillator circuit or the serial port clock (ASCLK/SCLK). The CS4610/11 Clock Control circuitry allows gating of clocks to various internal functional blocks to conserve power during power conservation modes, as well as during normal modes of operation when no tasks are being executed.

## **Host Interface**

The CS4610/11 host interface is comprised of two separate interface blocks which are memory mapped into host address space. The CS4610/11 interface blocks can be located anywhere in the host 32-bit physical address space. The interface block locations are defined by the addresses programmed into the two Base Address Registers in the CS4610/11 PCI Configuration Space. These base addresses are normally set up by the system's Plug and Play BIOS. The first interface block (lo-

cated using Base Address 0) is a 4 kByte register block containing general purpose configuration, control, and status registers for the device. The second interface block (located using Base Address 1) is a 1 MByte block which maps all of the CS4610/11 internal RAM memories (SP Program RAM, Parameter RAM, and Sample RAM), along with the SP debug registers, into host memory space. This allows the host to directly peek and poke RAM locations on the device. The relationship between the Base Address Registers in the CS4610/11 PCI Configuration Space and the host memory map is depicted in Figure 8.

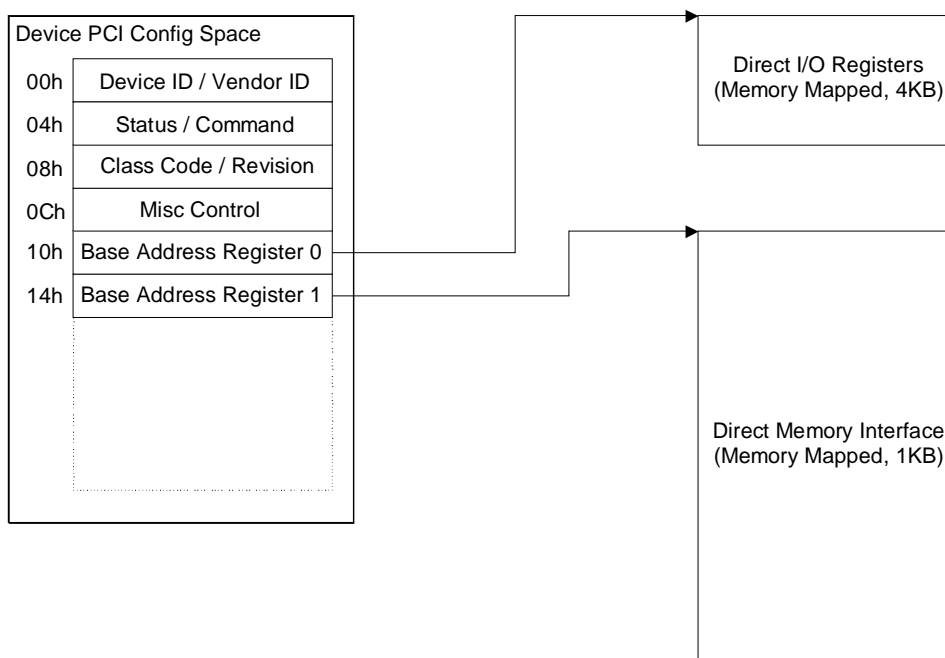
## **CS4610/11 PCI Interface**

The CS4610/11 provides a bus mastering PCI bus interface which complies with the PCI Local Bus Specification version 2.1.

## **PCI Bus Transactions**

As a target of a PCI bus transaction, the CS4610/11 supports the Memory Read (from internal registers or memory), Memory Write (to internal registers or memory), Configuration Read (from CS4610/11 configuration registers), Configuration Write (to CS4610/11 configuration registers), Memory Read Multiple (aliased to Memory Read), Memory Read Line (aliased to Memory Read), and the Memory Write and Invalidate (aliased to Memory Write) transfer cycles. The I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not supported.

As Bus Master, the CS4610/11 generates the Memory Read Multiple and Memory Write transactions. The Memory Read, Configuration Read, Configuration Write, Memory Read Line, Memory Write and Invalidate, I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not generated.



**Figure 8. CS4610/11 Host Interface Base Address Registers**

Initiator	Target	Type	PCI Dir
Host	Registers (BA0)	Mem Write	In
Host	Registers (BA0)	Mem Read	Out
Host	Memories (BA1)	Mem Write	In
Host	Memories (BA1)	Mem Read	Out
Host	Config Space 1	Config Write	In
Host	Config Space 1	Config Read	Out
DMA	Host System	Mem Write	Out
DMA	Host System	Mem Read	In

**Table 1. CS4610/11 PCI Interface Transaction Summary**

The PCI bus transactions supported by the CS4610/11 device are summarized in Table 1. Note that no Target Abort conditions are signalled by the device. Byte, Word, and Doubleword transfers are supported for Configuration Space accesses. Only Doubleword transfers are supported for Register or

Memory area accesses. Bursting is not supported for host-initiated transfers to/from the CS4610/11 internal register space, RAM memory space, or PCI configuration space (disconnect after first phase of transaction is completed).

## Configuration Space

The content and format of the primary PCI Configuration Space for the CS4610/11 device is given in Table 2.

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID: R/O, 6001h		Vendor ID: R/O, 1013h		00h
Status Register, bits 15-0: Bit 15 Detected Parity Error: Error Bit Bit 14 Signalled SERR: Error Bit Bit 13 Received Master Abort: Error Bit Bit 12 Received Target Abort: Error Bit Bit 11 Signalled Target Abort: Error Bit Bit 10-9 DEVSEL Timing: R/O, 01b (medium) Bit 8 Data Parity Error Detected: Error Bit Bit 7 Fast Back to Back Capable: R/O 0 Bit 6-0UDF, 66MHz, Reserved: R/O 0000000 Reset Status State: 0200h Write of 1 to any error bit position clears it.		Command Register, bits 15-0: Bit 15-10: Reserved, R/O 0 Bit 9 Fast B2B Enable: R/O 0 Bit 8 SERR Enable: R/W, default 0 Bit 7 Wait Control: R/O 0 Bit 6 Parity Error Response: R/W, default 0 Bit 5 VGA Palette Snoop: R/O 0 Bit 4 MWI Enable: R/O 0 Bit 3 Special Cycles: R/O 0 Bit 2 Bus Master Enable: R/W, default 0 Bit 1 Memory Space Enable: R/W, default 0 Bit 0 IO Space Enable: R/O 0		04h
Class Code: R/O 040100h Class 04h (multimedia device), Sub-class 01h (audio), Interface 00h			Revision ID: R/O 01h	08h
BIST: R/O 0	Header Type: Bit 7: R/O 0 Bit 6-0: R/O 0 (type 0)	Latency Timer: Bit 7-3: R/W,default 0 Bit 2-0: R/O 0	Cache Line Size: R/O 0	0Ch
Base Address Register 0 Device Control Register space, memory mapped. 4 kByte size Bit 31-12: R/W, default 0. Compare address for register space accesses Bit 11 - 4: R/O 0, specifies 4 kByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				10h
Base Address Register 1 Device Memory Array mapped into host system memory space, 1 MByte size Bit 31-20: R/W, default 0. Compare address for memory array accesses Bit 19 - 4: R/O 0, specifies 1 MByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				14h
Base Address Register 2: R/O 00000000h, Unused				18h
Base Address Register 3: R/O 00000000h, Unused				1Ch
Base Address Register 4: R/O 00000000h, Unused				20h
Base Address Register 5: R/O 00000000h, Unused				24h

**Table 2. CS4610/11 PCI Configuration Space 1**

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Cardbus CIS Pointer: R/O 00000000h, Unused				28h
Subsystem ID R/O 0000h see <i>Subsystem Vendor ID Fields</i> section		Subsystem Vendor ID R/O 0000h see <i>Subsystem Vendor ID Fields</i> section		2Ch
Expansion ROM Base Address: R/O 00000000h, Unused				30h
Reserved: R/O 00000000h				34h
Reserved: R/O 00000000h				38h
Max_Lat: R/O 18h 24 x 0.25uS = 6 uS	Min_Gnt: R/O 04h 4 x 0.25uS = 1uS	Interrupt Pin: R/O 01h, INTA used	Interrupt Line: R/W, default 0	3Ch

**Table 2. CS4610/11 PCI Configuration Space 1 (Continued)**

### ***Subsystem Vendor ID Fields***

The Subsystem ID and Subsystem Vendor ID fields in the CS4610/11 PCI Configuration Space default to value 0000h unless an external EEPROM device is detected or unless the host has written to the appropriate internal register to program the values. When programmed through the EEPROM all four bytes can be written. However, when programming through the host interface (BIOS code), only the Subsystem Vendor ID (bytes 1 and 0) can be programmed. The Subsystem ID (bytes 3 and 2) is forced to the most significant byte (byte 1) of the Subsystem Vendor ID. Therefore, when loaded through host code, bytes one, two and three will all have the same value.

### ***CS4610/11 Interrupt Signal***

The CS4610/11 PCI Interface includes an interrupt controller function which receives interrupt requests from multiple sources within the CS4610/11 device, and presents a single interrupt line (INTA#) to the host system. Interrupt control registers in the CS4610/11 provide the host interrupt service routine with the ability to identify the source of the interrupt and to clear the interrupt sources. In the CS4610/11, the single external interrupt is expand-

ed by the use of “virtual channels”. Each data stream which is read from or written to a modulo buffer is assigned a virtual channel number. This virtual channel number is signalled by the DMA subsystem anytime the associated modulo buffer pointer passes the mid-point or wraps around. Virtual channels are also used for message passing between the CS4610/11 and the host.

### ***Serial Port Configurations***

The CS4610/11 provides a flexible Serial Audio Interface which allows connection to external Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs) or Codecs (combined ADC and DAC functions) in several different configurations. The CS4610/11 serial audio interface includes a primary input/output port with dedicated serial data pins (SDIN, SDO2), two auxiliary audio output ports (SDO2, SDO3) which share pins with the joystick interface button input functions, and one auxiliary audio input port (SDIN2). Each of these digital audio input and output pins carry two channels of audio data. These two channels may comprise the left and right channels of a stereo audio signal, or they may be two independent monaural audio signals.



Each digital audio channel is internally buffered through a 16 sample x 20-bit FIFO. The data format for the serial digital audio ports varies depending on the configuration. The primary configurations supported include a CS4610/11 plus CS423x configuration for motherboard audio, a CS4610/11 plus CS423x configuration with full 5.1 channel output capability, and an AC'97 controller configuration (CS4610/11 plus an AC'97 Codec).

### ***CS4610/11 + CS423x Motherboard Audio Accelerator***

A system block diagram for the CS4610/11 plus CS423x configuration is given in Figure 6. This configuration utilizes a proprietary bi-directional digital audio link between the CS4610/11 and the CS423x. The connection between these devices is depicted in Figure 9.

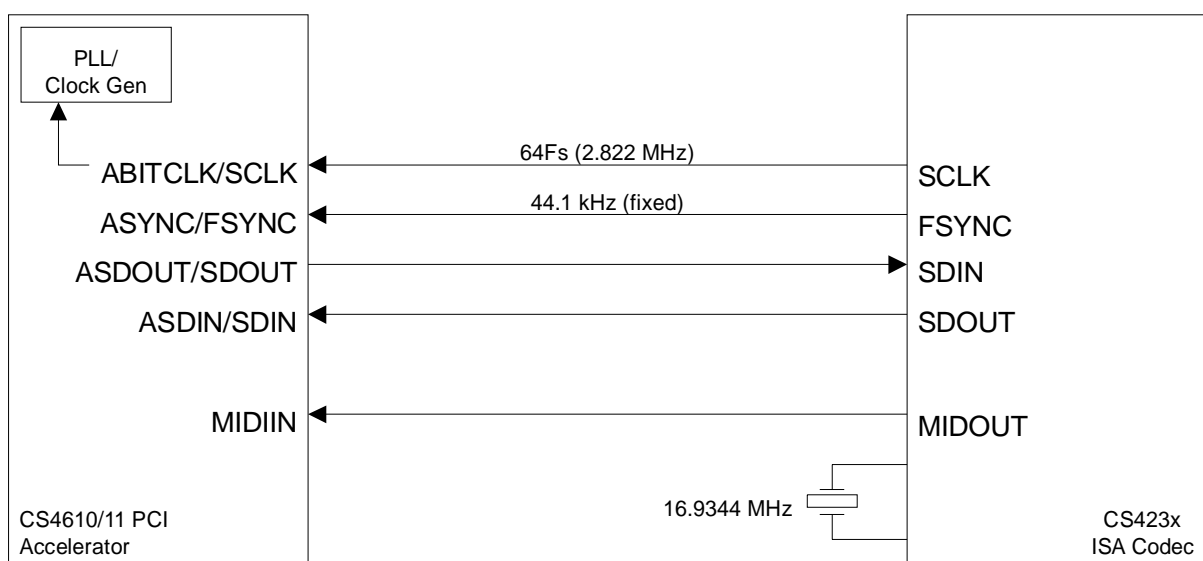
In the CS4610/11 plus CS423x configuration, the CS423x is the serial port timing master. The serial port runs at a fixed 44.1 kHz sampling rate, and the 2.822 MHz SCLK output from the CS423x is selected as the CS4610/11 PLL clock generator input.

Note that in this configuration the SDIN signal carries two stereo streams from the CS423x to the

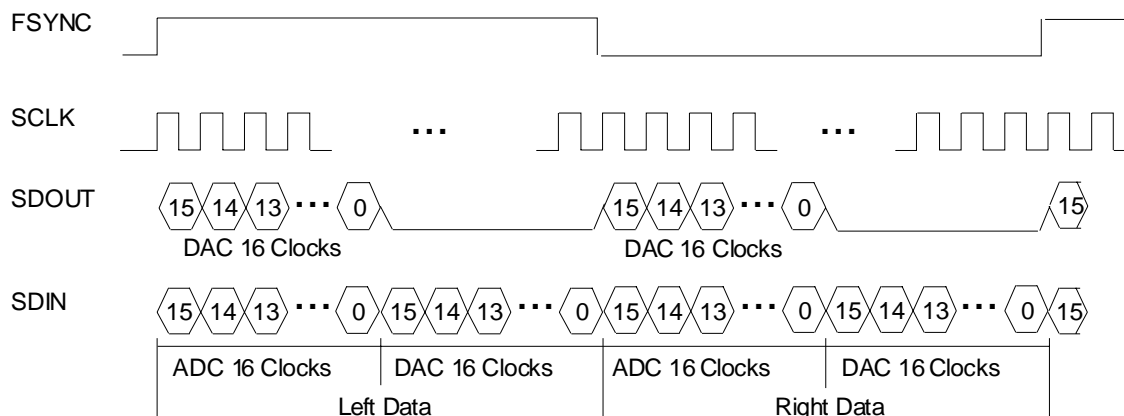
CS4610/11: the CS423x ADC data and the CS423x output data. The SDOUT signal carries the CS4610/11 final output to the CS423x DACs. SDIN and SDOUT transitions occur on rising edges of SCLK (SDIN is sampled on falling edges of SCLK). The data is transmitted in left-justified format, MSB first, 16-bit data, with 32 clock cycles for each phase of the FSYNC signal. FSYNC transitions occur on rising edges of SCLK, the FSYNC high phase indicates left channel data on SDIN and SDOUT while the FSYNC low phase indicates right channel data. The SDOUT signal carries 16 bits of data followed by 16 bits of zero pad for each channel (left and right). The SDIN signal carries 16 bits of ADC data followed by 16 bits of playback data for each channel (left and right). The serial port clock and data timing relationship for this configuration is indicated in Figure 10. The clock and data signal functions for this configuration are summarized in Table 3.

### ***Motherboard Configuration with 5.1 channel output capability (CS4610 only)***

This configuration is the same as the CS4610 plus CS423x motherboard accelerator configuration with the addition of two Crystal™ CS4333 Stereo



**Figure 9. CS4610/11 + CS423x Connection Diagram**



**Figure 10. Serial Audio Port Format for CS4610/11 + CS423x Configuration**

Pin Name	Direction	Functional Description
SCLK	Input	Main timing driver for digital audio link, both edges used internally for timing. Also functions as the source to the PLL for internal clock generation.
FSYNC	Input	Framing signal for digital audio link, high time indicates left channel data and low time indicates right channel data. Frame is sampled on the falling edge of the SCLK input.
SDOUT	Output	Primary output port serial data pin. This data is the CS4610/11 output stream going to the CS423x device. The serial data on this pin transitions on the rising edge of the SCLK input.
SDIN	Input	Primary input port serial data pin. This data contains both CS423x ADC data and the CS423x output data. The serial data on this pin is sampled on the falling edge of the SCLK input.

**Table 3. Serial Audio Port Signal Summary for CS4610/11 + CS423x Configuration**

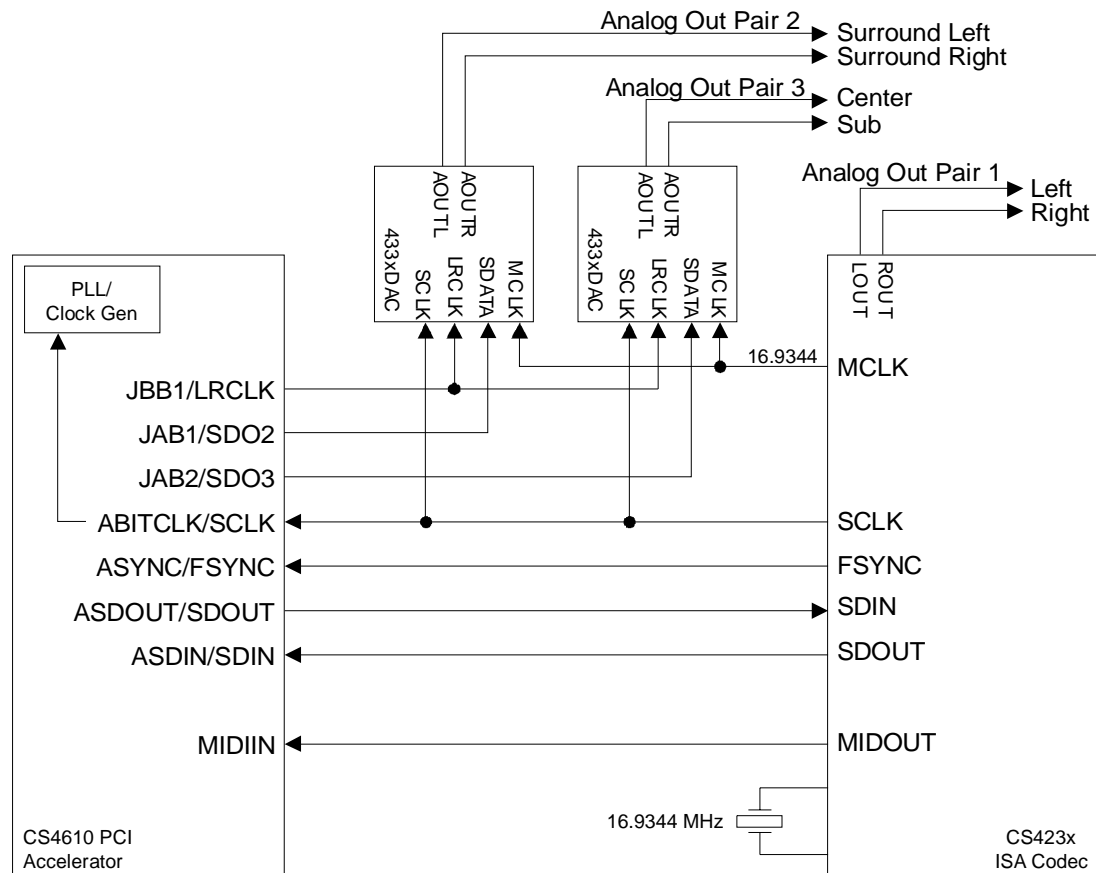
DACs to expand the audio output capability to six channels. This expanded output capability is useful for applications where discrete 5.1 channel output is desired for Dolby AC-3 audio programs. The connection diagram for the additional CS4333 DACs is given in Figure 11. The CS4333 DACs share the SCLK output from the CS423x with the CS4610. The CS4333 DACs also receive a 16.9344 MHz MCLK signal from the CS423x. Note that the CS423x MCLK output has limited drive strength and should be buffered in this application. The LRCLK framing clock and the SDO2/SDO3 digital audio outputs are provided from the CS4610. The SDO2 and SDO3 transitions occur on falling edges of SCLK (the primary output SDOUT transitions on rising edges of SCLK). LRCLK transitions occur on falling edges of SCLK, with the LRCLK high phase indicating left channel data present on SDO2/SDO3. SDO2/SDO3 data is right justified, with 16 bits of zero pad followed by 16-bits of data,

transmitted MSB first. There are 64 SCLKs per LRCLK, and MCLK runs at 384× the frame rate. The serial port clock and data timing relationship for this configuration is indicated Figure 12. The clock and data signal functions for this configuration are summarized in Table 4.

### **AC'97 Controller Configuration**

In this configuration the CS4610/11 functions as an AC'97 controller. The CS4610/11 communicates with an AC'97 Codec, such as the CrystalClear CS4297, over the AC-link as specified in the Intel® Audio Codec '97 Specification version 1.03. A block diagram for the AC'97 Controller Configuration is given in Figure 7. The signal connections between the CS4610/11 and the AC'97 Codec are indicated in Figure 13. In this configuration, the AC'97 Codec is the timing master for the digital audio link. The CS4610/11 ASDOUT output supports data transmission on all 10 possible sample

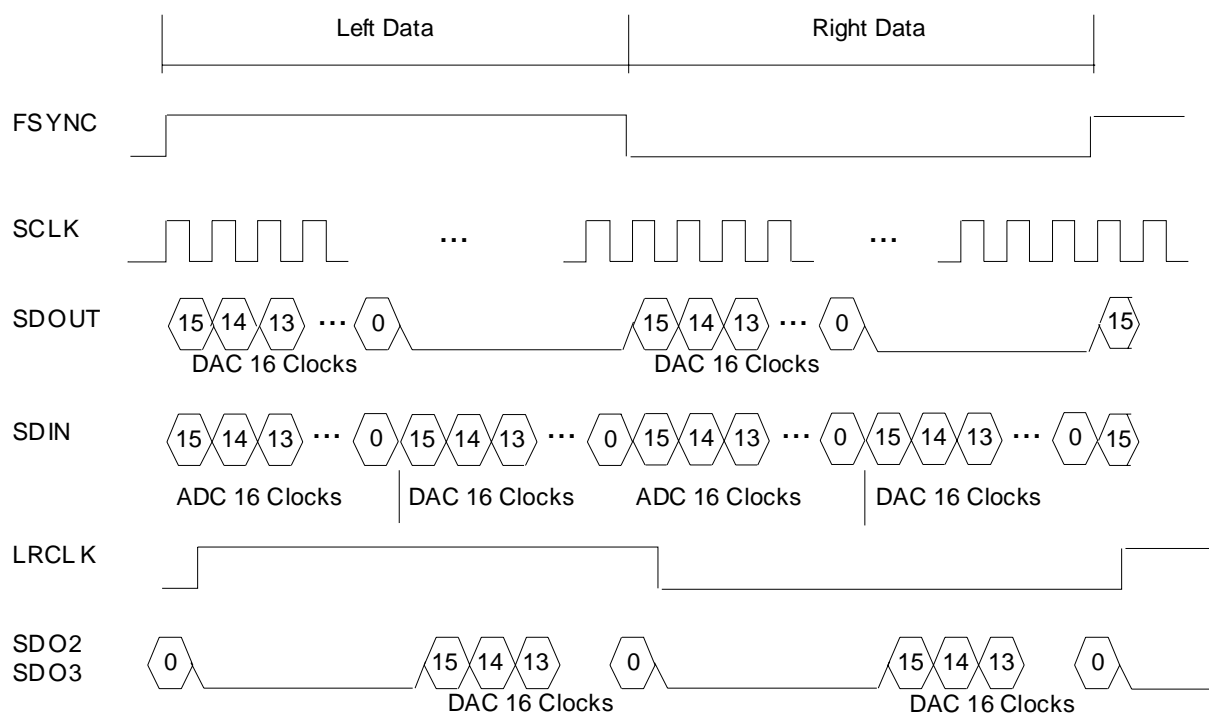




**Figure 11. CS4610 + CS423x Expanded 6-Channel Output Configuration**

Pin Name	Direction	Functional Description
SCLK	Input	Main timing driver for digital audio link, both edges used internally for timing. Also functions as the source to the PLL for internal clock generation.
FSYNC	Input	Framing signal for digital audio link, high time indicates left channel data and low time indicates right channel data. FSYNC is sampled on the falling edge of the SCLK input.
SDOUT	Output	Primary output port serial data pin. This data is the CS4610 output stream going to the CS423x DACs. SDOUT transitions on the rising edge of the SCLK input.
SDIN	Input	Primary input port serial data pin. This data contains both CS423x ADC data and the CS423x output data. SDIN is sampled on the falling edge of the SCLK input.
LRCLK	Output	Framing signal for external 4333 DACs, high time indicates left channel data and low time indicates right channel data. LRCLK transitions on the falling edge of the SCLK input.
SDO2, SDO3	Output	Second and third output port serial data pins. These output streams are the expanded output channels beyond the CS423x left / right pair. The serial data on these pins transition on the falling edge of the SCLK input. Note that this is a DIFFERENT SCLK edge than the one for the SDOUT pin.

**Table 4. Serial Audio Port Signal Summary for CS4610 + CS423x Expanded Output Configuration**



**Figure 12. Serial Audio Port Format for CS4610 + CS423x Expanded Output Configuration.**

slots (output slots 3 - 12). The CS4610/11 ASDIN input supports receiving of audio sample data on 6 input sample slots (input slots 3 - 8). The SDO2, SDO3 serial outputs and the SDIN2 serial input are not supported in this configuration.

### MIDI Port

In the AC'97 controller configuration, the CS4610/11 provides a bi-directional MIDI interface to allow connection of external MIDI devices. The CS4610/11 MIDI interface includes 16-byte FIFOs for the MIDI transmit and receive paths.

### Joystick Port

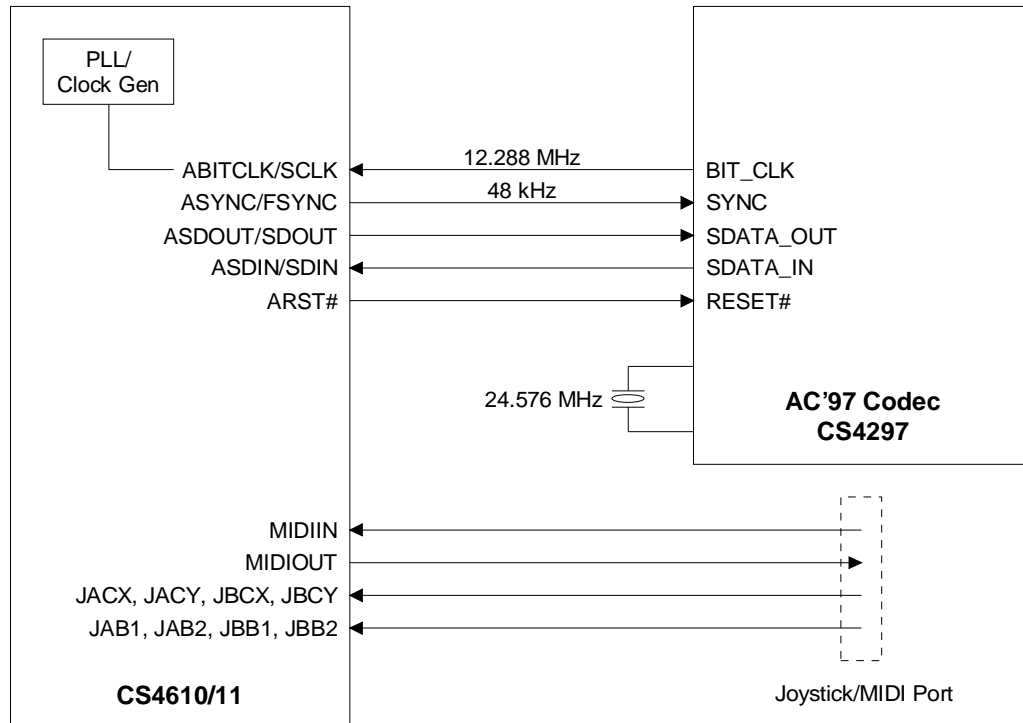
In the AC'97 controller configuration, the CS4610/11 provides a joystick port. The CS4610/11 joystick port provides four "coordinate" channels and four "button" channels of input capability. The coordinate channels provide joystick positional information to the host, and the button channels provide user button event information. The joystick interface is capable of

operating in the traditional "polled" mode, but also provides a "hardware accelerated" mode of operation wherein internal counters assist the host with coordinate position determination. The joystick schematic is illustrated in Figure 14.

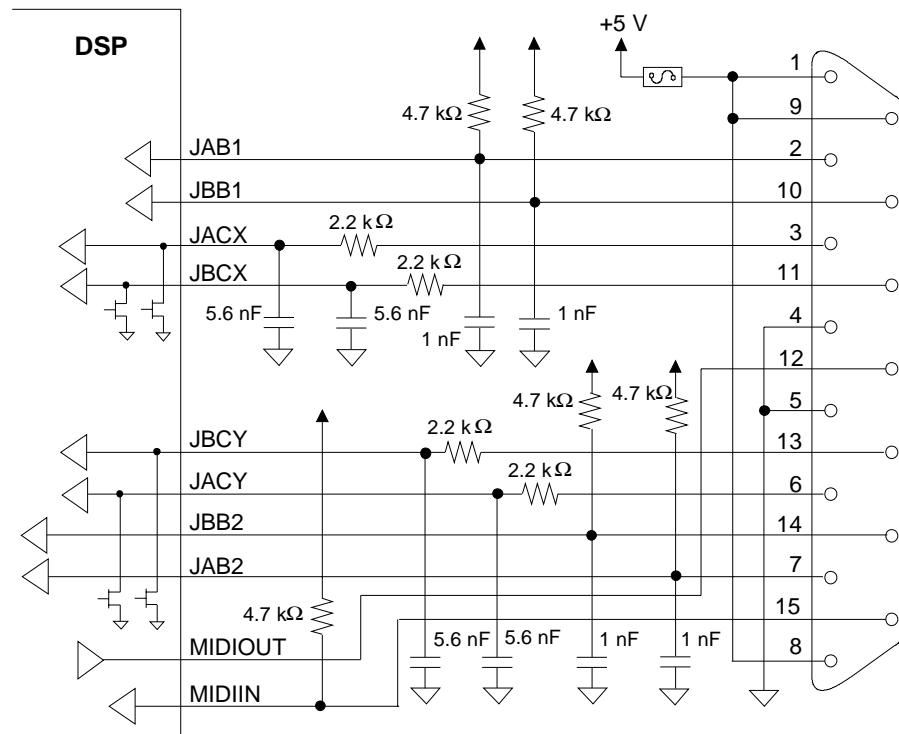
### EEPROM Configuration Interface

The CS4610/11 EEPROM configuration interface allows the connection of an optional external EEPROM device to provide power-up configuration information. The external EEPROM is not required for proper operation of the CS4610. However, in some applications power-up configuration settings other than the CS4610/11 device default values may be required to support specific operating system compatibility requirements (the CS4610/11 default is the CS4610/11 + CS423x configuration). These default values can be programmed through BIOS code or by using the external EEPROM.

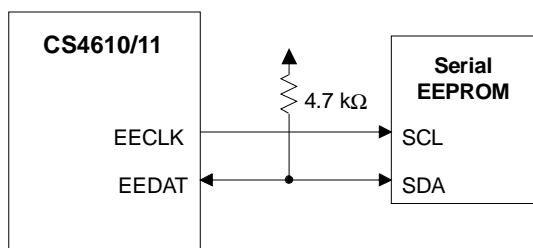
After a hardware reset, an internal state machine in the CS4610/11 will automatically detect the pres-



**Figure 13. CS4610/11 - AC '97 Codec Connection Diagram**



**Figure 14. Joystick Logic**



**Figure 15. External EEPROM Connection**

ence of an external EEPROM device and load the Subsystem ID and Subsystem Vendor ID fields, along with two bytes of general configuration information, into internal registers. At power-up, the CS4610/11 will attempt to read from the external device, and will check the data received from the device for a valid signature header. If the header data is invalid, the data transfer is aborted. After power-up, the host can read or write from/to the EEPROM device by accessing specific registers in the CS4610/11. Cirrus Logic provides software to program the EEPROM.

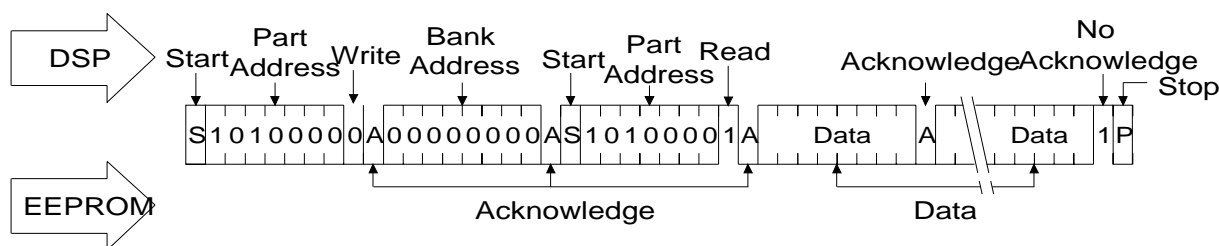
The two wire interface for the optional external EEPROM device is depicted in Figure 15. During data transfers, the data line (EEDAT) can change state only while the clock signal (EECLK) is low. A

state change of the data line while the clock signal is high indicates a start or stop condition to the EEPROM device.

The EEPROM device read access sequence is shown in the Figure 16. The timing follows that of a random read sequence. The CS4610/11 first performs a “dummy” write operation, generating a start condition followed by the slave device address and the byte address of zero. The slave address is made up of a device identifier (0xA) and a bank select (bits A2-A0). The CS4610/11 always begins access at byte address zero and continues access a byte at a time. The byte address automatically increments by one until a stop condition is detected. The CS4610/11 will read a total of seven bytes from the EEPROM.

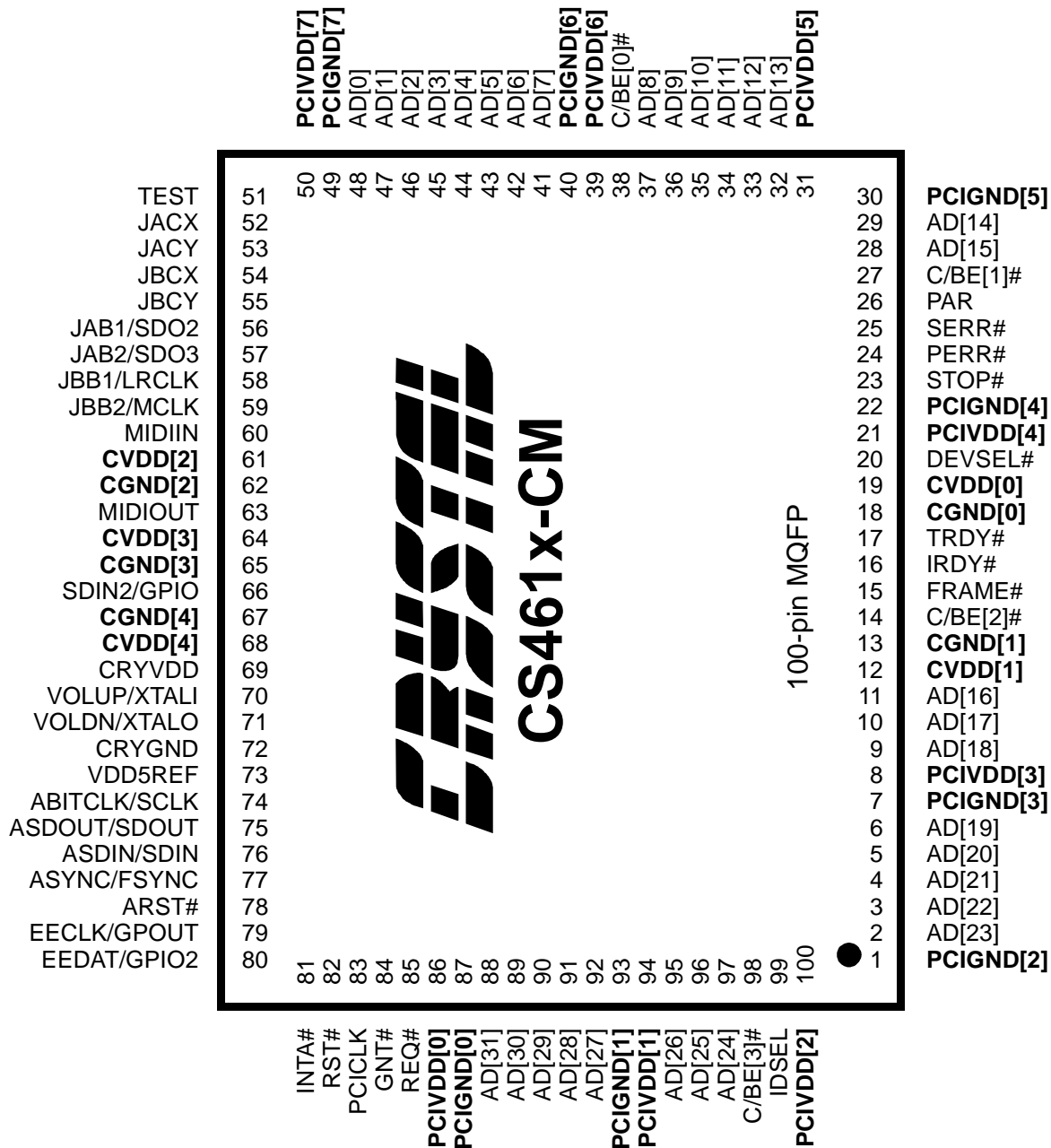
### General Purpose I/O Pins

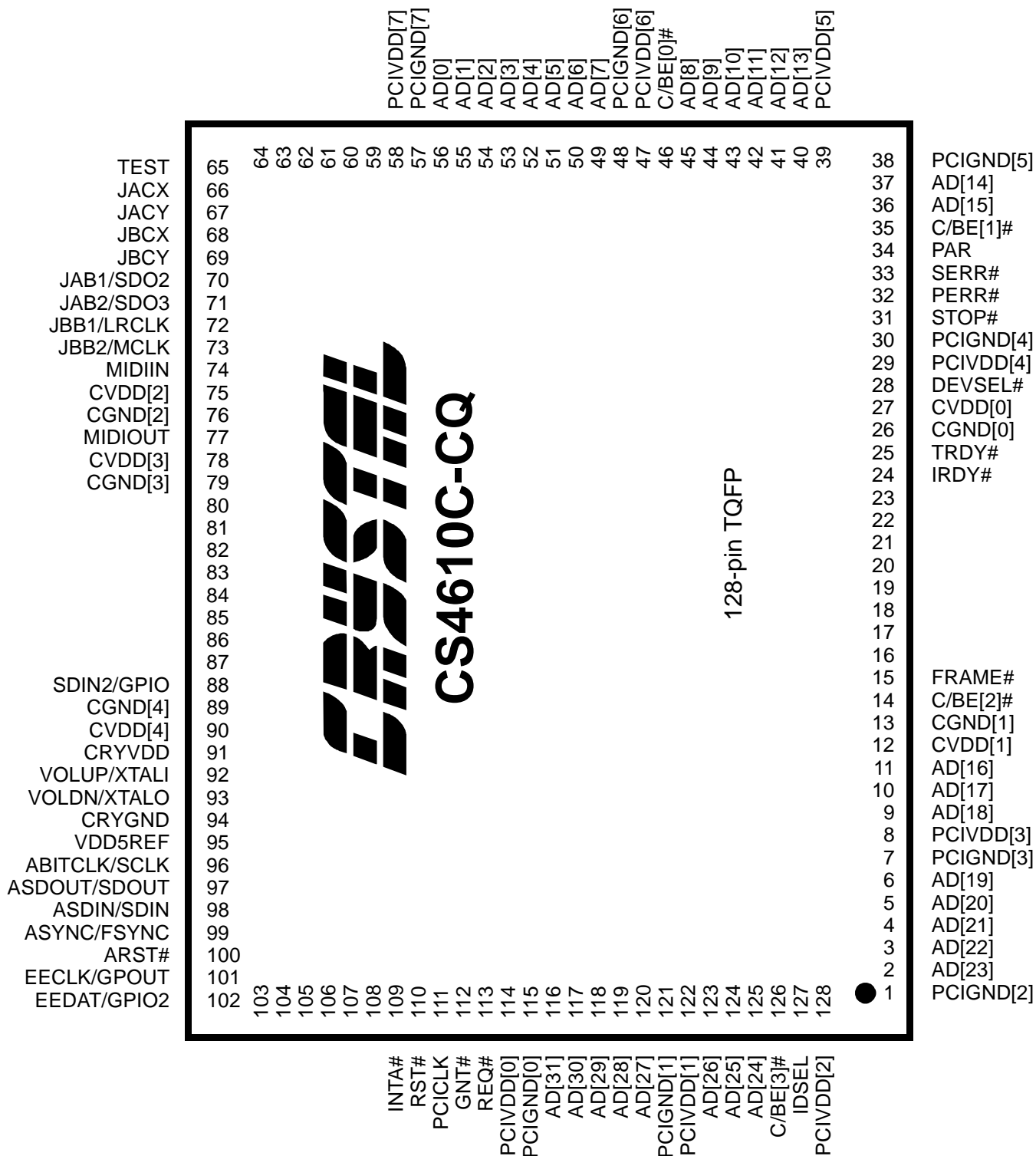
Many of the CS4610/11 signal pins are internally multiplexed to serve different functions depending on the environment in which the device is being used. Several of the CS4610/11 signal pins may be used as general purpose I/O pins when not required for other specific functions in a given application.



**Figure 16. External EEPROM Read Access Sequence**

## PIN DESCRIPTIONS





Note: A '#' sign suffix on a pin names indicates an active-low signal.

### **PCI Interface**

#### **AD[31:0] - Address/Data Bus, I/O**

**(M) pins 88-92, 95-97, 2-6, 9-11, 28-29, 32-37, 41-48**

**(Q) pins 116-120, 123-125, 2-6, 9-11, 36-37, 40-45, 49-56**

These pins form the multiplexed address / data bus for the PCI interface.

#### **C/BE[3:0]# - Command Type / Byte Enables, I/O**

**(M) pins 98, 14, 27, 38; (Q) pins 126, 14, 35, 46**

These four pins are the multiplexed command / byte enables for the PCI interface. During the address phase of a transaction, these pins indicate cycle type. During the data phases of a transaction, active low byte enable information for the current data phase is indicated. These pins are inputs during slave operation and they are outputs during bus mastering operation.

#### **PAR - Parity, I/O**

**(M) pin 26; (Q) pin 34**

The Parity pin indicates even parity across AD[31:0] and C\_BE[3:0] for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.

#### **FRAME# - Cycle Frame, I/O - Active Low**

**(M) pin 15; (Q) pin 15**

FRAME# is driven by the current PCI bus master to indicate the beginning and duration of a transaction.

#### **IRDY# - Initiator Ready, I/O**

**(M) pin 16; (Q) pin 24**

IRDY# is driven by the current PCI bus master to indicate that as the initiator it is ready to transmit or receive data (complete the current data phase).

#### **TRDY# - Target Ready, I/O**

**(M) pin 17; (Q) pin 25**

TRDY# is driven by the current PCI bus target to indicate that as the target device it is ready to transmit or receive data (complete the current data phase).

#### **STOP# - Transition Stop, I/O**

**(M) pin 23; (Q) pin 31**

STOP# is driven active by the current PCI bus target to indicate a request to the master to stop the current transaction.

#### **IDSEL - Initialize Device Select, Input**

**(M) pin 99; (Q) pin 127**

IDSEL is used as a chip select during PCI configuration read and write cycles.

**DEVSEL# - Device Select, I/O****(M) pin 20; (Q) pin 28**

DEVSEL# is driven by the PCI bus target device to indicate that it has decoded the address of the current transaction as its own chip select range.

**REQ# - Master Request, Three-State Output****(M) pin 85; (Q) pin 113**

REQ# indicates to the system arbiter that this device is requesting access to the PCI bus. This pin is high-impedance when RST# is active.

**GNT# - Master Grant, Input****(M) pin 84; (Q) pin 112**

GNT# is driven by the system arbiter to indicate to the device that the PCI bus has been granted.

**PERR# - Parity Error, I/O****(M) pin 24; (Q) pin 32**

PERR# is used for reporting data parity errors on the PCI bus.

**SERR# - System Error, Open Drain Output****(M) pin 25; (Q) pin 33**

SERR# is used for reporting address parity errors and other catastrophic system errors.

**INTA# - Host Interrupt A (for SP), Open Drain Output****(M) pin 81; (Q) pin 109**

INTA# is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.

**PCICLK - PCI Bus Clock, Input****(M) pin 83; (Q) pin 111**

PCICLK is the PCI bus clock for timing all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.

**RST# - PCI Device Reset****(M) pin 82; (Q) pin 110**

RST# is the PCI bus master reset.

**VDD5REF: Clean 5 V Power Supply****(M) pin 73; (Q) pin 95**

VDD5REF is the power connection pin for the 5 V PCI pseudo supply for the PCI bus drivers.



**PCIVDD[7:0] - PCI Bus Driver Power Supply**

**(M) pins 50, 39, 31, 21, 8, 100, 94, 86;**  
**(Q) pins 58, 47, 39, 29, 8, 128, 122, 114**

PCIVDD pins are the PCI driver power supply pins.

**PCIGND[7:0] - PCI Bus Driver Ground Pins**

**(M) pins 49, 40, 30, 22, 7, 1, 93, 87;**  
**(Q) pins 57, 48, 38, 30, 7, 1, 121, 115**

PCIGND pins are the PCI driver ground reference pins.

**External Interface Pins**

**TEST - Test Mode Strap, Input**

**(M) pin 51; (Q) pin 65**

This pin is sampled at reset for test mode entry. If it is high at reset, test mode is enabled. This pin should normally be pulled to ground in a production design.

**EEDAT/GPIO2 - External EEPROM Data / General Purpose I/O Pin 2, I/O Drain**

**(M) pin 80; (Q) pin 102**

Data line for external serial EEPROM containing device configuration data. When used with an external EEPROM, a 4.7 kΩ pullup resistor is required. In designs without EEPROM requirements, this pin can be used as a general purpose input or open drain output.

**EECLK/GPOUT - External EEPROM Clock / General Purpose Output Pin, Output**

**(M) pin 79; (Q) pin 101**

Clock line for external serial EEPROM containing device configuration data. In designs without EEPROM requirements, this pin can be used as a general purpose output pin.

**SDIN2/GPIO - Serial Data Input 2 / General Purpose I/O Pin, I/O**

**(M) pin 66; (Q) pin 88**

This dual function pin defaults as a general purpose I/O pin. In non-AC'97 system configurations, this pin can function as a second stereo digital data input pin if enabled.

**VOLUP/XTALI - Volume Up Button / Crystal Input, Input**

**(M) pin 70; (Q) pin 92**

This dual function pin is either the volume up button control input or the crystal oscillator input pin, depending on system configuration. When a crystal is used, it must be designed for fundamental mode, parallel resonant. This pin may also be used as a general purpose input if its primary function is not needed.

**VOLDN/XTALO - Volume Down Button / Crystal Output, I/O**

**(M) pin 71; (Q) pin 93**

This dual function pin is either the volume down button control input or the crystal oscillator output pin, depending on system configuration. This pin may also be used as a general purpose input if its primary function is not needed.

***Clock / Miscellaneous*****CRYVDD - Crystal & PLL Power Supply****(M) pin 69; (Q) pin 91**

Power pin for crystal oscillator and internal phase locked loop.

**CRYGND - Crystal & PLL Ground Supply****(M) pin 72; (Q) pin 94**

Ground pin for crystal oscillator and internal phase locked loop.

**JACX, JACY, JBCX, JBCY - Joystick A and B X/Y Coordinates, I/O****(M) pins 52, 53, 54, 55; (Q) pins 66, 67, 68, 69**

These pins are the 4 axis coordinates for the joystick port. These pins may also be used as a general purpose inputs or open drain outputs if their primary function is not needed.

**JAB1/SDO2 - Joystick A Button 1 / Serial Data Output 2, I/O****(M) pin 56; (Q) pin 70**

This dual function pin defaults as JAB1 (button 1 input for joystick A). In non-AC'97 system configurations, this pin can function as a second stereo digital data output pin if enabled. This pin can also be a general purpose polled input if a second data output stream is not required.

**JAB2/SDO3 - Joystick A Button 2 / Serial Data Output 3, I/O****(M) pin 57; (Q) pin 71**

This dual function pin defaults as JAB2 (button 2 input for joystick A). In non-AC'97 system configurations, this pin can function as a third stereo digital data output pin if enabled. This pin can also be a general purpose polled input if a third data output stream is not required.

**JBB1/LRCLK - Joystick B Button 1 / L/R Framing Clock, I/O****(M) pin 58; (Q) pin 72**

This dual function pin defaults as JBB1 (button 1 input pin for joystick B). In non-AC'97 system configurations, this pin can function as an alternate framing clock output pin for SDO2 and SDO3. This pin can also be used as a general purpose polled input if alternate data output streams are not required.

**JBB2/MCLK - Joystick B Button 2 / Master Clock, I/O****(M) pin 59; (Q) pin 73**

This dual function pin defaults as JBB2 (button 2 input pin for joystick B). In non-AC'97 system configurations, this pin can function as a master (256x sample rate) output clock if enabled. This pin can also be used as a general purpose polled input if alternate data output streams are not required.

**MIDIIN - MIDI Data Input****(M) pin 60; (Q) pin 74**

This is the serial input pin for the internal MIDI port.

**MIDIOUT - MIDI Data Output**

**(M) pin 63; (Q) pin 77**

This is the serial output pin for the internal MIDI port.

**CVDD[4:0] - Core Power Supply**

**(M) pins 68, 64, 61, 12, 19;**

**(Q) pins 90, 78, 75, 12, 27**

Core / Stream Processor power pins.

**CGND[4:0] - Core Ground Supply**

**(M) pins 67, 65, 62, 13, 18;**

**(Q) pins 89, 79, 76, 13, 26**

Core / Stream Processor ground reference pins.

***Serial Codec Interface***

**ABITCLK/SCLK - AC '97 Bit Rate Clock / Serial Audio Data Clock, I/O**

**(M) pin 74; (Q) pin 96**

Master timing clock for serial audio data. In AC'97 configurations, this pin is an input which drives the timing for the AC'97 interface, along with providing the source clock for the PLL. In CS423x (ISA Codecs) digital link configurations, this pin is an input for the SCLK from the CS423x DSP port.

**ASYNC/FSYNC - AC '97 Frame Sync / Serial Audio Frame Sync, O/I**

**(M) pin 77; (Q) pin 99**

Framing clock for serial audio data. In AC'97 configurations, this pin is an output which indicates the framing for the AC'97 link. In CS423x digital link configurations, this pin is an input for the FSYNC from the CS423x's DSP port.

**ASDOUT/SDOUT - AC '97 Data Out / Serial Audio Data Out, Output**

**(M) pin 75; (Q) pin 97**

Serial audio output data.

**ASDIN/SDIN - AC '97 Data In / Serial Audio Data In, Input**

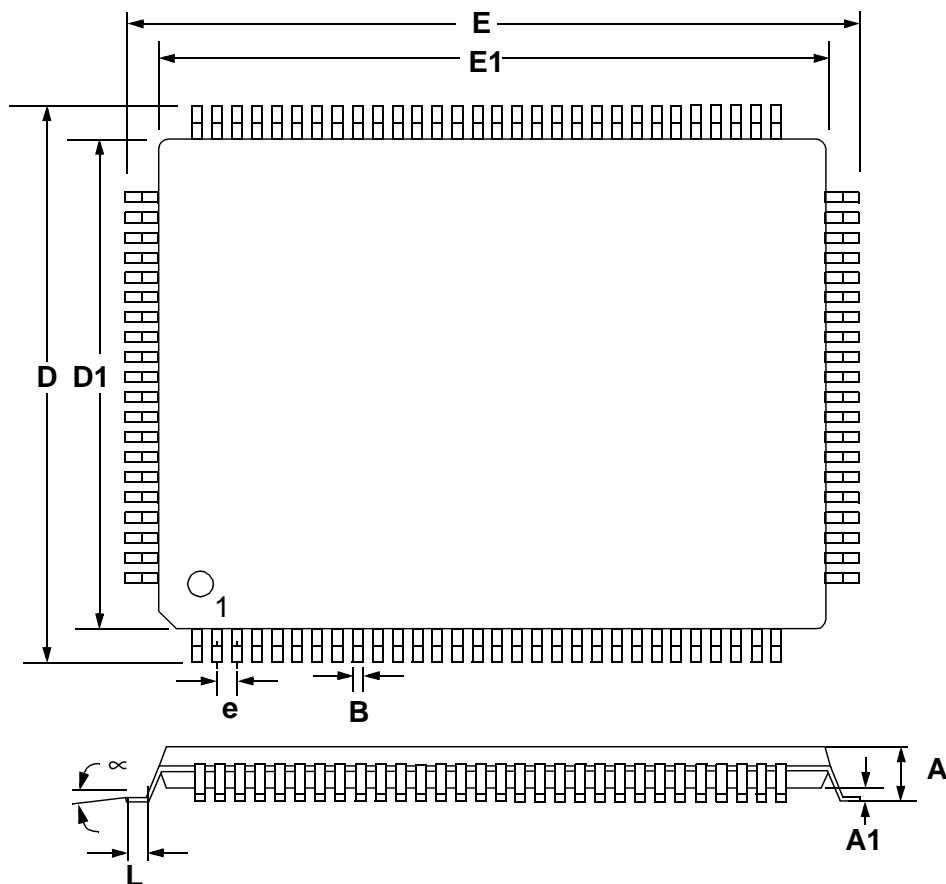
**(M) pin 76; (Q) pin 98**

Serial audio input data.

**ARST# - AC '97 Reset, Output**

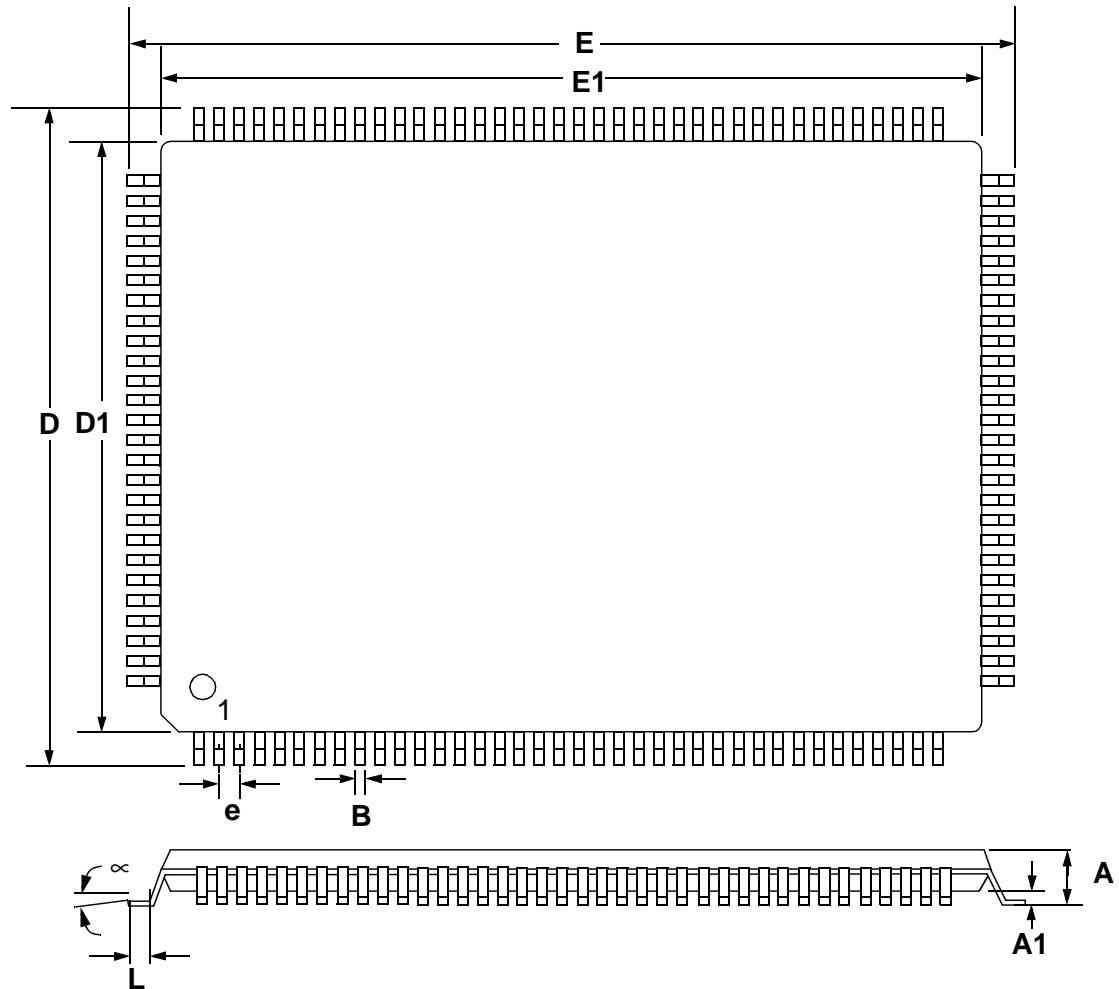
**(M) pin 78; (Q) pin 100**

AC'97 link reset pin. This pin also functions as a general purpose reset output in non-AC'97 configurations and will follow RST# pin 82 to ground, but must be forced high by software.

**MECHANICAL DRAWINGS**
**‘M’ Package 100-pin MQFP**


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.000	0.134	0.000	3.400
A1	0.010	0.014	0.250	0.350
B	0.009	0.015	0.220	0.380
D	0.667	0.687	16.950	17.450
D1	0.547	0.555	13.900	14.100
E	0.904	0.923	22.950	23.450
E1	0.783	0.791	19.900	20.100
e	0.022	0.030	0.550	0.750
∞	0.000	7.000	0.000	7.00
L	0.018	0.030	0.450	0.750

**‘Q’ Package 128-pin TQFP**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.000	0.063	0.000	1.600
A1	0.002	0.006	0.050	0.150
B	0.007	0.011	0.170	0.270
D	0.626	0.634	15.900	16.100
D1	0.547	0.555	13.900	14.100
E	0.862	0.870	21.900	22.100
E1	0.783	0.791	19.900	20.100
e	0.016	0.024	0.400	0.600
∞	0.000	7.000	0.000	7.000
L	0.018	0.030	0.450	0.750