19-0298; Rev 4; 5/96

EVALUATION KIT AVAILABLE

MAXIM

6-Bit Quadrature Digitizer

MAX2101

General Description

The MAX2101 6-bit quadrature digitizer combines quadrature demodulation with analog-to-digital conversion on a single bipolar silicon die. This unique RF-to-Bits™ function bridges the gap between existing RF downconverters and CMOS digital signal processors (DSPs).

The MAX2101's simple receiver subsystem is designed for digital communications systems such as those used in DBS, TVRO, WLAN, and other applications.

The MAX2101 accepts input signals from 400MHz to 700MHz and applies adjustable gain, providing at least 40dB of dynamic range.

Each baseband is filtered by an on-chip, 5th-order Butterworth lowpass filter, or the user can select an external filter path. Baseband sample rate is 60Msps. The MAX2101 is available in a commercial temperature range, 100-pin MQFP package.

Applications

Recovery of PSK and QAM Modulated RF Carriers

Direct-Broadcast Satellite (DBS) Systems

Television Receive-Only (TVRO) Systems

Cable Television (CATV) Systems

Wireless Local Area Networks (WLANs)

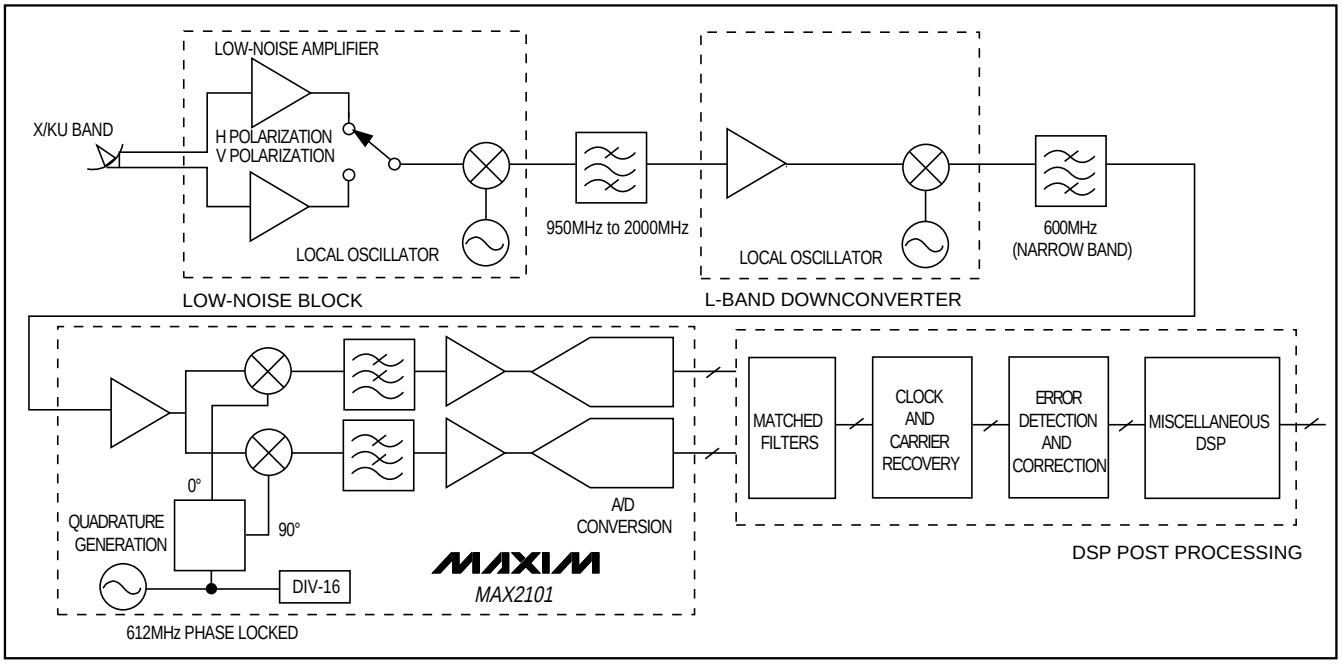
Features

- **ADCs Provide Greater than 5.5 Effective Bits at f_S = 60Msps, f_{IN} = 15MHz**
- **Fully Integrated Lowpass Filters with Externally Variable Bandwidth (10MHz to 30MHz)**
- **40dB Dynamic Range**
- **Integrated VCO and Quadrature Generation Network for I/Q Demodulation**
- **Divide-by-16 Prescaler for Oscillator PLL**
- **Programmable Counter for Variable Sample Rates**
- **Signal-Detection Function**
- **Selectable Offset Binary or Twos-Complement Output Data Format**
- **Automatic Baseband Offset Cancellation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2101CMQ	0°C to +70°C	100 MQFP

Typical Application Circuit



™*RF-to-Bits is a registered trademark of Tektronix, Inc.*

6-Bit Quadrature Digitizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Ranges (Note 1)
- V_{CC}.....(-0.3V to +6.5V)
- V_{INA}.....(V_{CCA} + 0.3V)
- V_{IND}.....(V_{CCD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C) 1.6W
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, <10sec).....+300°C

Note 1: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in conductive foam or shunt the terminals together. Discharge the conductive foam to the destination socket before insertion.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS (V_{GND} = System Ground, V_{CCA} = V_{CCD} = 5.0V ±5%)						
Digital Supply Current	I_{CCD}	V_{CCA}, V_{CCO}, V_{CCD}, V_{CCC}			102	mA
ADC Supply Current	I_{CCAD}	V_{CCAD}			80	mA
RF Blocks Supply Current	I_{CCRF}	V_{CCIF}, V_{CC2}, V_{CC1}, V_{CCQ}			170	mA
IF Port DC Dynamic Range	V_{IF}		0.5		100	mV
IF Port Input Resistance	R_{IF}		40		75	Ω
AGC Input Voltage	V_{AGMIN}	V_{IF} = 100mV	1.0		1.5	V
	V_{AGMAX}	V_{IF} = 0.5mV	2.3		2.9	
AGC Input Resistance	R_{AGC}		50		100	kΩ
AGC Input Capacitance	C_{AGC}	(Note 2)			2	pF
AGC Range	AGCR		40			dB
AGC Control Slope Variation	SV_{AGC}	Variation dB/V			4:1	
AGC Control Input Bias Current	I_{AGC}	Voltage range = 1V to 4V		±20		µA
Lowpass Filter Tune Input Resistance	R_{ILPF}		10			kΩ
Lowpass Filter Tune Input Capacitance	C_{ILPF}	(Note 2)			2	pF
TNKA, TNKB Resonant Port Bias Voltage	V_{LO}	4.1V on complementary input	1		3	V
LO Resonant Port Input Resistance	R_{ILO}	(Note 2)	10			kΩ
LO Resonant Port Input Capacitance	C_{ILO}	(Note 2)			2	pF
LO Prescaler Output High (Note 3)	V_{OH}	R_L = 1MΩ, C_L = 15pF	2.4			V
LO Prescaler Output Low	V_{OL}	R_L = 1MΩ, C_L = 15pF			0.5	V
LO Prescaler Output Source Current	I_{OH}	R_L = 1MΩ, C_L = 15pF, V_O = 2.4V	400			µA
LO Prescaler Output Sink Current	I_{OL}	R_L = 1MΩ, C_L = 15pF, V_O = 0.5V	50			µA
Baseband Amplifier DC Gain	A_{VBB}		27	29	31	dB
Baseband Input—Input Capacitance	C_{IBB}	(Note 2)			2	pF
Baseband Amplifier I/Q Offset Match (Note 4)	V_{OFFBB}	LSB = 24mV, ENOPB = 0V, V_{FTUNE} = V_{FTMIN} to V_{FTMAX}			1.0	LSB
Baseband Amplifier Offset Adjust Input Resistance	R_{OFFBB}	Voltage Range = 1V to 4V	10			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Detect Output Minimum	V_{PWR}	V_{OBB} = 0V_{p-p}				1.5	V
Power Detect Output Maximum	V_{PWR}	V_{OBB} > 2V DC		3.75			V
ADC LSB Size	LSB			21		25	mV
ADC Amplitude Response Match	A_{VM}	Channel to channel				0.4	dB
ADC Input Offset	V_{OFFAD}	LSB = 24mV, either channel				0.5	LSB
ADC Differential Nonlinearity	DNL					1.0	LSB
ADC Integral Nonlinearity	INL					1.0	LSB
RF Signal Path DC Gain	A_{VRF}	AGC set to maximum gain		63			dB
Composite I/Q Gain Mismatch	$\Delta M_{(IQ)}$	Entire signal path, DC, V_{FTUNEI} = V_{FTUNEQ} = V_{2R5}				0.5	dB
Buffered Reference Voltage (Zero Temperature Coefficient)	V_{REF}	R_L = 1kΩ, C_L = 0.1µF		1.18		1.25	V
Buffered Reference Voltage (Proportional to Absolute Temperature)	V_{PTAT}	R_L = 40kΩ, C_L = 0.01µF	T_A = +25°C	1.0		1.3	V
			T_A = 0°C to +70°C (Note 2)	0.9		1.5	
V_{PTAT} Temperature Coefficient		T_A = 0°C to +70°C			4.5		mV/°C
Buffered Reference Voltage (2 x VREF)	V_{2R5}	Ratio of V_{2R5} to V_{REF}		1.9		2.1	V
Data Output High (Note 3)	V_{OH}	R_L = 1MΩ, C_L = 15pF		2.2			V
Data Output Low	V_{OL}	R_L = 1MΩ, C_L = 15pF				0.5	V
Data Output Source Current (Note 3)	I_{OH}	R_L = 1MΩ, C_L = 15pF, V_O = 2.4V		400			µA
Data Output Sink Current	I_{OL}	R_L = 1MΩ, C_L = 15pF, V_O = 0.5V		50			µA
Data Clock Output High (Note 3)	V_{OH}	R_L = 1MΩ, C_L = 15pF		2.2			V
Data Clock Output Low	V_{OL}	R_L = 1MΩ, C_L = 15pF				0.5	V
Data Clock Output Source Current (Note 3)	I_{OH}	R_L = 1MΩ, C_L = 15pF, V_O = 2.4V		400			µA
Data Clock Output Sink Current	I_{OL}	R_L = 1MΩ, C_L = 15pF, V_O = 0.5V		50			µA
Master Clock Input Dynamic Range	P_{MCLK}	R_L = 50Ω external, f = 5MHz		0		10	dBm
Master Clock Input Resistance	R_{IMCLK}			2			kΩ
Master Clock Input Capacitance	C_{IMCLK}					5	pF
Reference Clock Output High (Note 3)	V_{OH}	R_L = 10MΩ, C_L = 15pF		2.2			V
Reference Clock Output Low	V_{OL}	R_L = 10MΩ, C_L = 15pF				0.5	V
Reference Clock Output Source Current (Note 3)	I_{OH}	R_L = 1MΩ, C_L = 15pF, V_O = 2.4V		400			µA
Reference Clock Output Sink Current	I_{OL}	R_L = 1MΩ, C_L = 15pF, V_O = 0.5V		50			µA
Digital Input High Threshold (Note 5)	V_{IH}					2.0	V
Digital Input Low Threshold (Note 5)	V_{IL}			0.8			V
Digital Input Current High (Note 5)	I_{IH}	V_{IH} = 2.0V		-150		-500	µA
Digital Input Current Low (Note 5)	I_{IL}	V_{IL} = 0.8V		-400		-790	µA
FLTRSEL Input Current High	I_{IH}	V_{IH} = 2.0V					µA
FLTRSEL Input Current Low	I_{IL}	V_{IL} = 0.8V					µA

6-Bit Quadrature Digitizer

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC SPECIFICATIONS (GND = System Ground, V_{CC} = V_{CCD} = 5.0V ±5%)						
IF Port Dynamic Range (Notes 2, 6)	P_{IF}	R_S = 50Ω, f_{IF} = 400MHz to 700MHz	-50		-10	dBm
IF Port VSWR (Note 6)	VSWR	R_S = 50Ω, R_{TERM} = 25Ω, no matching network, f_{IF} = 400MHz to 700MHz		1.7		
IF Input Frequency Range	f_{IF}	(Note 2)	400		700	MHz
Noise Figure (Note 6)	NF	R_{TERM} = 50Ω, gain configured for P_{IF} = -50dBm		20		dB
Noise Figure Variation	Δ_{NF}	Maximum gain to minimum gain		1		dB/dB
Input 3rd-Order Intercept Point	IIP3	Gain configured for P_{IF} = -10dBm, f_{BB1} = 5MHz, f_{BB2} = 6MHz		6		dBm
		Gain configured for P_{IF} = -50dBm, f_{BB1} = 5MHz, f_{BB2} = 6MHz		-34		
LO Frequency Coverage	f_{LO}	External resonator, guaranteed	400		700	MHz
LO Device Phase Noise Floor	Φ_N	10MHz off f_C, 1Hz bandwidth		-140		dBc/Hz
LO Device Phase Noise	Φ_N	10kHz off f_C, 1Hz bandwidth (limited by external tank Q)		-88		dBc/Hz
MIXER Output Baseband Gain Flatness	Δ_{AV}	5Hz to 20MHz		0.4		dB
Lowpass Filter Stop-Band Attenuation	A_{SB}	f = 2 x f_C (with respect to signal level at f = 0.5 x f_C)		28		dB
Lowpass Filter Tune Voltage	V_{FTMIN}	f_C = 10MHz	1.5		2.1	V
	V_{FTMAX}	f_C = 30MHz	2.3		2.9	
Composite I/Q Amplitude Balance	$\Delta M_{(IQ)}$	f_{LO} = 650MHz		0.3		dB
Composite I/Q Phase Balance	$\Delta\Phi_{(IQ)}$	f_{LO} = 650MHz		1.5		degree
Composite Group Delay Variation	ΔT	100Hz to 15MHz, each channel excluding filter		0.5		ns
ADC 0.1dB Bandwidth	$BW_{0.1dB}$			20		MHz
ADC Maximum Sample Rate, Each Section	SR_{MAX}	(Note 2)	60			Msps
ADC Aperture Uncertainty	t_{AU}	f_S = 60Msps		80		ps
ADC Transient Response	t_{TRAN}	Full-scale transition, settle to within 1%		10		ns
Baseband Overdrive Recovery	Recover	$V_{BASEBAND}$ = $3V_{p-p}$		10		ns
ADC Effective Number of Bits	ENB	f_{IN} = 15MHz, f_S = 60Msps, V_{IN} = 95% FS		5.5		Bits
ADC Input IP3 Rejection	$IIP3_{AD}$	f_1 = 10MHz, FS - 7dB; f_2 = 12MHz, FS - 7dB		-38		dBc

Note 2: Guaranteed by design.
Note 3: A warm-up of 10 seconds is required at T_A = 0°C.
Note 4: Sample characterization at T_A = 0°C to +70°C.
Note 5: Digital inputs include Programmable Sample Rate Control (S0–S2), Binary Enable (BINEN).
Note 6: R_S = Source Resistance of signal source driving IF input (IFIN, pin 90).
R_{TERM} = Termination Resistance for inverting IF input (IFINB, pin 91).

TIMING CHARACTERISTICS

(V_{GND} = system ground, V_{CCA} = V_{CCD} = 5.0V ±5%, T_A = +25°C, unless otherwise noted.) (Note 4)

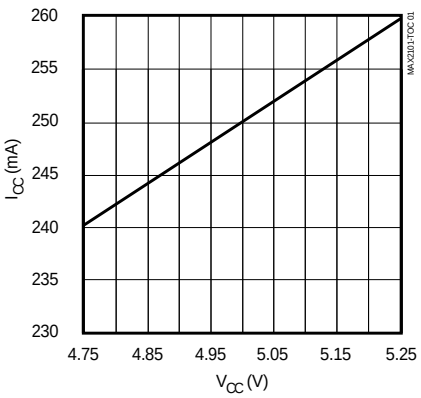
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Data Clock Period (Figure 2)	t_{PC}		16		ns
Propagation Delay, Clock to Data (Figure 2)	t_{PCQ}		4		ns
Data Output Skew (all 12 outputs) Settled within 20% (Figure 2)	t_{SKEW}		1		ns
Aperture Delay Relative to Data Clock (Figure 2)	$t_{APERTURE}$		1		ns
Aperture Delay Match, Channel to Channel	$t_{AP-MATCH}$		20		ps
Data Output Rise, Fall Time (20% to 80%) (Note 7)	t_r, t_f		4		ns
Data Clock Output Rise, Fall Time (20% to 80%) (Note 7)	t_r, t_f		3		ns
Reference (Div 6) Clock Output Rise, Fall Time (20% to 80%) (Note 7)	t_r, t_f		5		ns
Reference Clock Output Jitter, RMS	t_j		30		ps
VCO Prescaler Output Rise, Fall Time (20% to 80%) (Note 7)	t_r, t_f		3		ns

Note 7: R_L = 1MΩ, C_L = 15pF

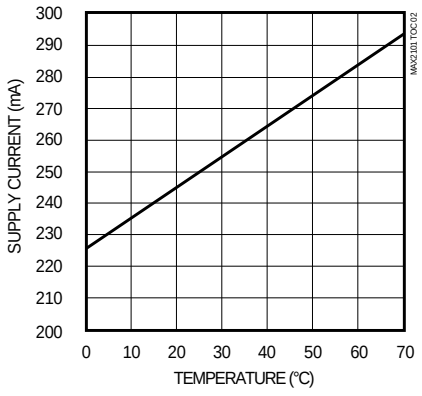
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

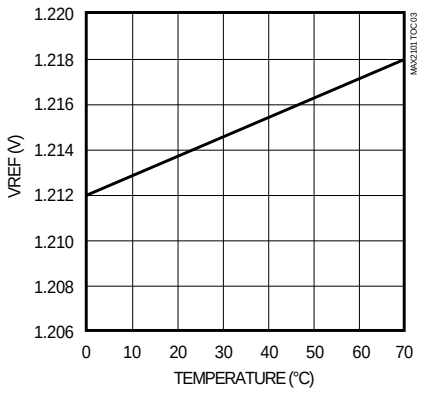
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



VREF (PIN 88) VOLTAGE vs. TEMPERATURE

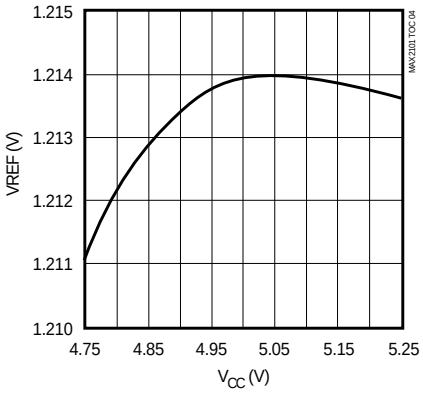


6-Bit Quadrature Digitizer

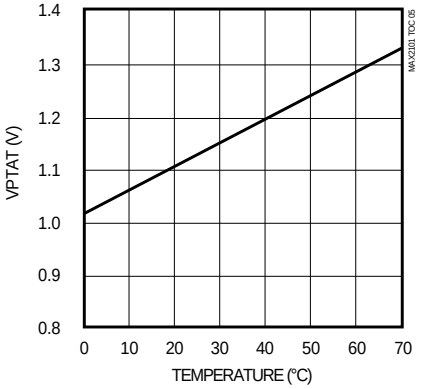
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

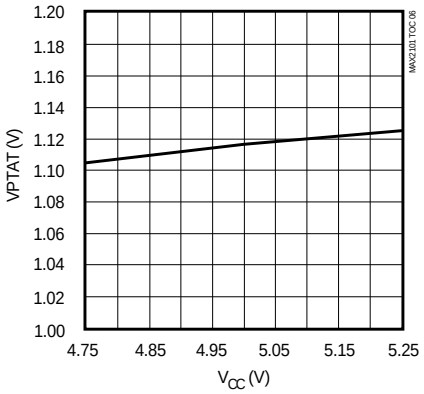
VREF (PIN 88) VOLTAGE vs. SUPPLY VOLTAGE



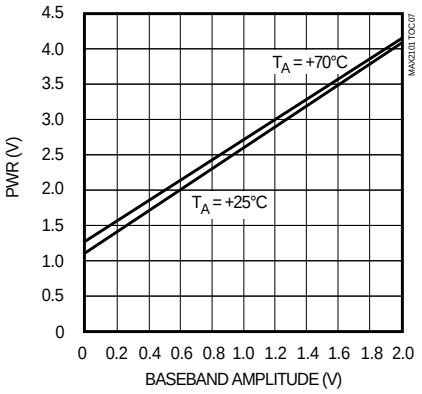
VPTAT (PIN 97) vs. TEMPERATURE



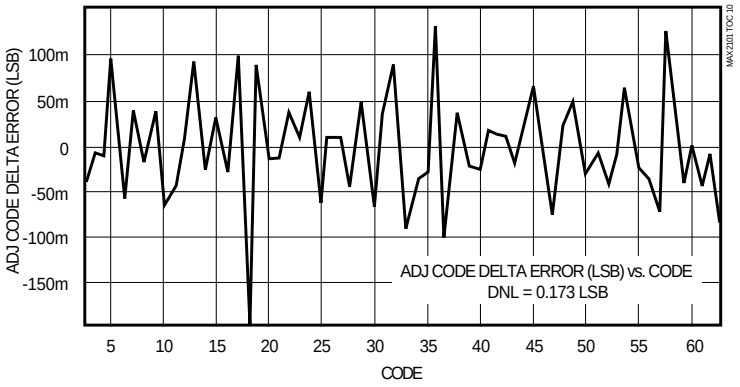
VPTAT (PIN 97) VOLTAGE vs. SUPPLY VOLTAGE



PWR (PINS 85, 96) VOLTAGE vs. BASEBAND AMPLITUDE



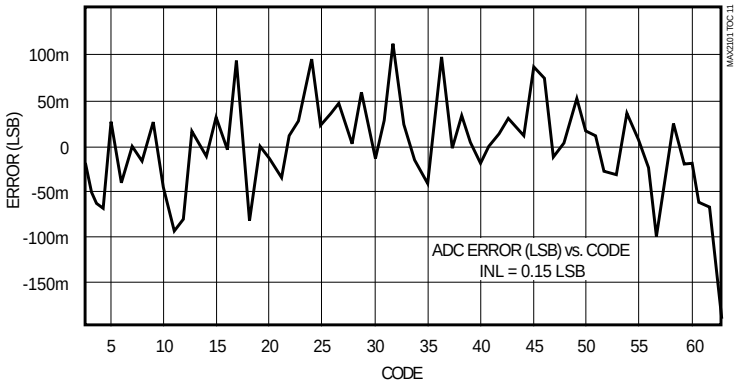
DIFFERENTIAL LINEARITY vs. ADC CODE



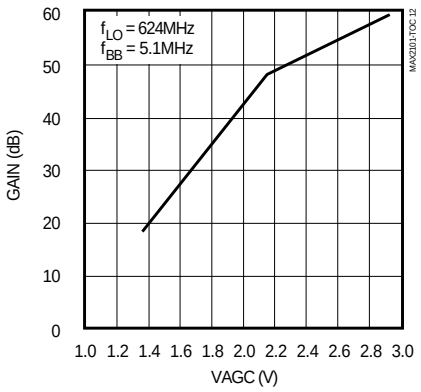
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

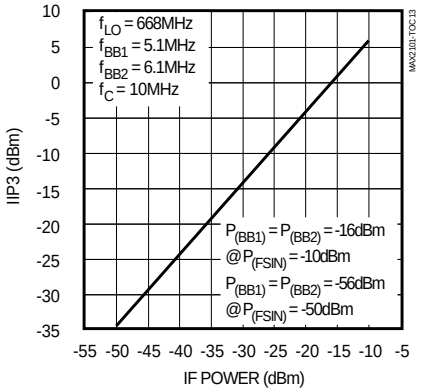
INTEGRAL NONLINEARITY vs. ADC CODE



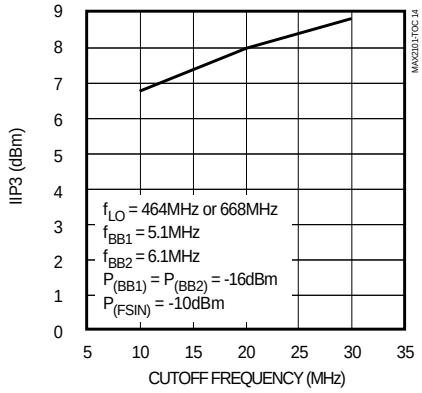
RF SIGNAL PATH GAIN vs. AGC (PIN 93) VOLTAGE



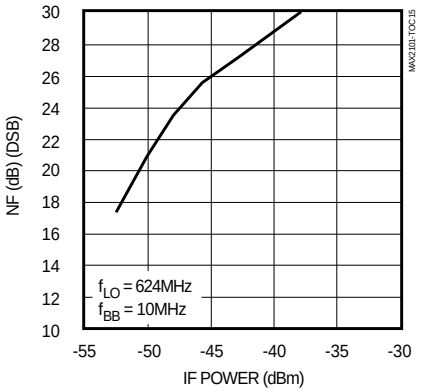
INPUT IP3 vs. IF POWER



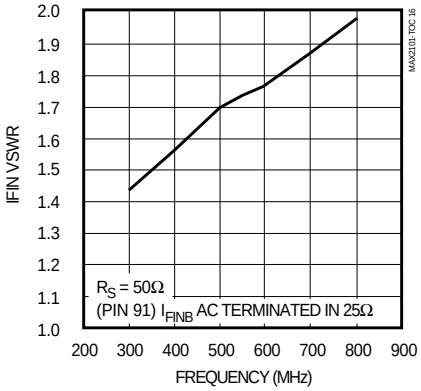
INPUT IP3 vs. FILTER CUTOFF FREQUENCY



NOISE FIGURE vs. IF INPUT POWER



IFIN (PIN 90) VSWR vs. FREQUENCY



6-Bit Quadrature Digitizer

Pin Description

PIN	NAME	FUNCTION
1, 9, 12, 13, 18, 19, 63, 67, 82, 83, 89, 92, 98, 99	GND	Ground
2	VGNDQ	Q Channel Baseband Ground
3	BBINQ	Q Channel Baseband Amplifier, External Input
4	FTUNEQ	Q Channel Filter Cutoff Frequency Control
5	OFFQ	Q Channel Baseband Amplifier Offset Adjust
6	BBOUTQ	Q Channel Baseband Amplifier Output
7	BBOUTQB	Q Channel Baseband Amplifier Inverted Output
8	VCCQ	Q Channel Baseband +5V Supply
10	VGNDP	Prescaler Ground
11	VCCP	Prescaler +5V Supply
14	TNKB	Oscillator Resonator Port
15	VCC2	Oscillator +5V Supply
16	VGND2	Oscillator Ground
17	TNKA	Oscillator Resonator Port
20, 21	VGNDAD	A/D Converter Ground
22, 59	VSUBAD	A/D Converter Substrate
23	VCOPRE	Divide-by-16 Prescaler Output
24	VCOPREB	Divide-by-16 Prescaler Complementary Output
25, 29, 38, 40, 44, 52	VCCO	Digital Output +5V Supply
26	VGNDO	Digital Output Ground
27	D5Q	Q Channel Data Output, bit 5 (MSB)
28	D4Q	Q Channel Data Output, bit 4
30, 37, 43, 51, 55	VGNDO	Digital Output Ground
31	D3Q	Q Channel Data Output, bit 3
32	D2Q	Q Channel Data Output, bit 2
33, 48	VCCD	Digital Logic +5V Supply
34, 47	VGNDD	Digital Logic Ground

PIN	NAME	FUNCTION
35	D1Q	Q Channel Data Output, bit 1
36	D0Q	Q Channel Data Output, bit 0 (LSB)
39	RCLK	Reference Clock, divide by six from master clock (MCLK)
41	DCLKB	Data Clock Complementary Output
42	DCLK	Data Clock Output
45	D0I	I Channel Data Output, bit 0 (LSB)
46	D1I	I Channel Data Output, bit 1
49	D2I	I Channel Data Output, bit 2
50	D3I	I Channel Data Output, bit 3
53	D4I	I Channel Data Output, bit 4
54	D5I	I Channel Data Output, bit 5 (MSB)
56	BINEN	Binary Enable
57	S2	Programmable Sample Rate Control Input, bit 2 (MSB)
58	S1	Programmable Sample Rate Control Input, bit 1
60, 61	VCCAD	A/D Converter +5V Supply
62	S0	Programmable Sample Rate Control Input, bit 0 (LSB)
64	VCCC	Clock Buffer +5V Supply
65	MCLK	Master Clock
66	VGNDC	Clock Buffer Ground
68	ENOPB	Offset Correction/Enable Correction
69	CQB	Inverting Input Q Channel Offset Correction
70	CQ	Noninverting Input Q Channel Offset Correction
71	CI	Noninverting Input I Channel Offset Correction
72	CIB	Noninverting Input I Channel Offset Correction
73	VCCI	I Channel Baseband +5V Supply
74	BBOUTIB	I Channel Baseband Amplifier Inverted Output
75	BBOUTI	I Channel Baseband Amplifier Output
76	OFFI	I Channel Baseband Amplifier Offset Adjust
77	FTUNEI	I Channel Filter Cutoff Frequency Control

Pin Description (continued)

PIN	NAME	FUNCTION
78	BBINI	I Channel Baseband Amplifier, External Input
79	VGNDI	I Channel Baseband Ground
80	VREFIN	High Impedance, connect to VREF (pin 88)
81	MIXOUTI	I Channel Mixer Output
84	VSUBRF	RF Demodulator Substrate
85	PWRI	I Channel Power Indicator
86	2R5	2x VREF Output
87	VCCIF	IF Signal Processing +5V Supply
88	VREF	Bandgap Reference Voltage Output
90	IFIN	IF Amplifier Noninverting Input
91	IFINB	IF Amplifier Inverting Input
93	AGC	Automatic Gain Control Input
94	VGNDIF	IF Signal-Processing Ground
95	FLTRSEL	Baseband Signal Path Select
96	PWRQ	Q Channel Power Indicator
97	VPTAT	PTAT Reference Voltage Output
100	MIXOUTQ	Q Channel Mixer Output

Detailed Description

The MAX2101 6-bit quadrature digitizer solves one of the most challenging problems of high dynamic range digital-receiver design by combining quadrature demodulation and analog-to-digital (A/D) conversion in a single device. The MAX2101's unique RF-to-Bits function bridges the gap between RF downconverters and CMOS digital signal processors (DSPs). Figure 1 is a simplified connection diagram.

The MAX2101 accepts input signals from 400MHz to 700MHz and applies gain depending on the input amplitude. The signal is then split and downconverted to baseband by two mixers, which are driven by two local oscillator (LO) signals in quadrature. An internal voltage-controlled oscillator (VCO) feeds the two LOs.

Each baseband is filtered by an internal 5th-order Butterworth lowpass filter. The on-board lowpass filters have an externally variable bandwidth of 10MHz to 30MHz. Each baseband is then converted by a 6-bit analog-to-digital converter (ADC). The conversion result is stored in a register and is output using the data clock. See Figure 2 for the relation between baseband signal, sample and data clock, and digitized data. The external master clock is internally divided by six and is available at RCLK for external system functions, frequency synthesizers, etc. See Figures 3 and 4 for functional diagrams.

IF Input Port (IFIN, $\overline{IFINB}$)

The MAX2101 provides a balanced IF input. The inputs are self-biasing, so the input signals should be AC terminated, depending on system requirements. To minimize noise, the unused input should be AC terminated with 25Ω. To minimize distortion, AC terminate the unused input with a 50Ω resistor.

VCO Resonator Tank Ports (TNKA, TNKB) and Prescaler

The MAX2101 integrates a negative impedance oscillator with balanced inputs. Use a parallel tank network, as shown in Figure 5. The phase-noise performance of the oscillator near the carrier is dominated by the resonant network. The resonant inductor must have a sufficiently high Q and a self-resonant frequency (SRF) that is more than twice the intended LO frequency. Be sure to minimize parasitic elements surrounding the tank network by using proper layout techniques. See the *Applications Information* section.

The VCO prescaler output provides phase-lock loop capability for controlling the VCO frequency. The prescaler generates the VCO frequency divided by 16. As a result, the prescaler delivers a 25MHz to 43.75MHz signal over the VCO operating frequency range of 400MHz to 700MHz. The differential outputs should have equivalent termination.

6-Bit Quadrature Digitizer

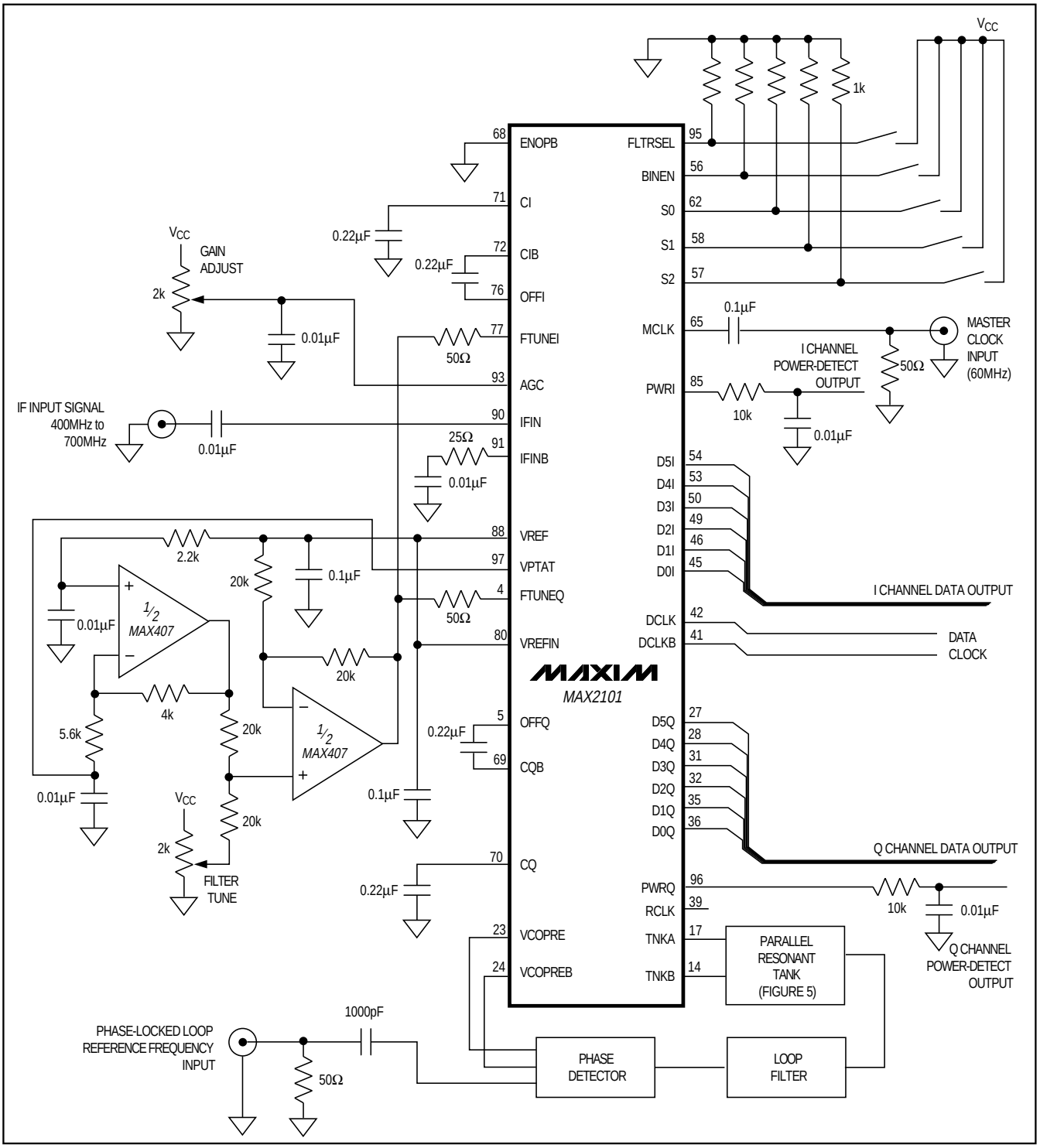


Figure 1. Typical Connection Diagram

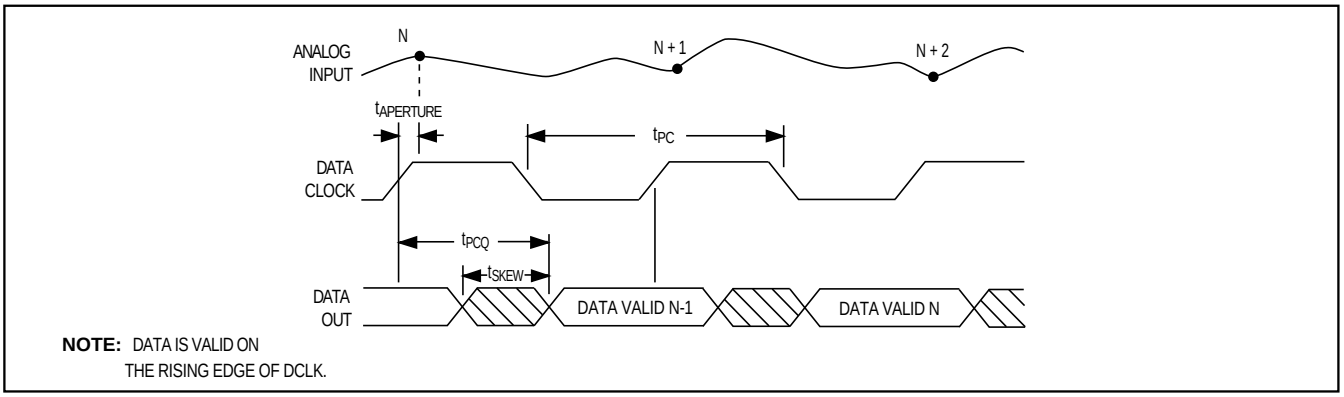


Figure 2. Baseband Signal, Sample/Data Clock, and Digitized Data Timing

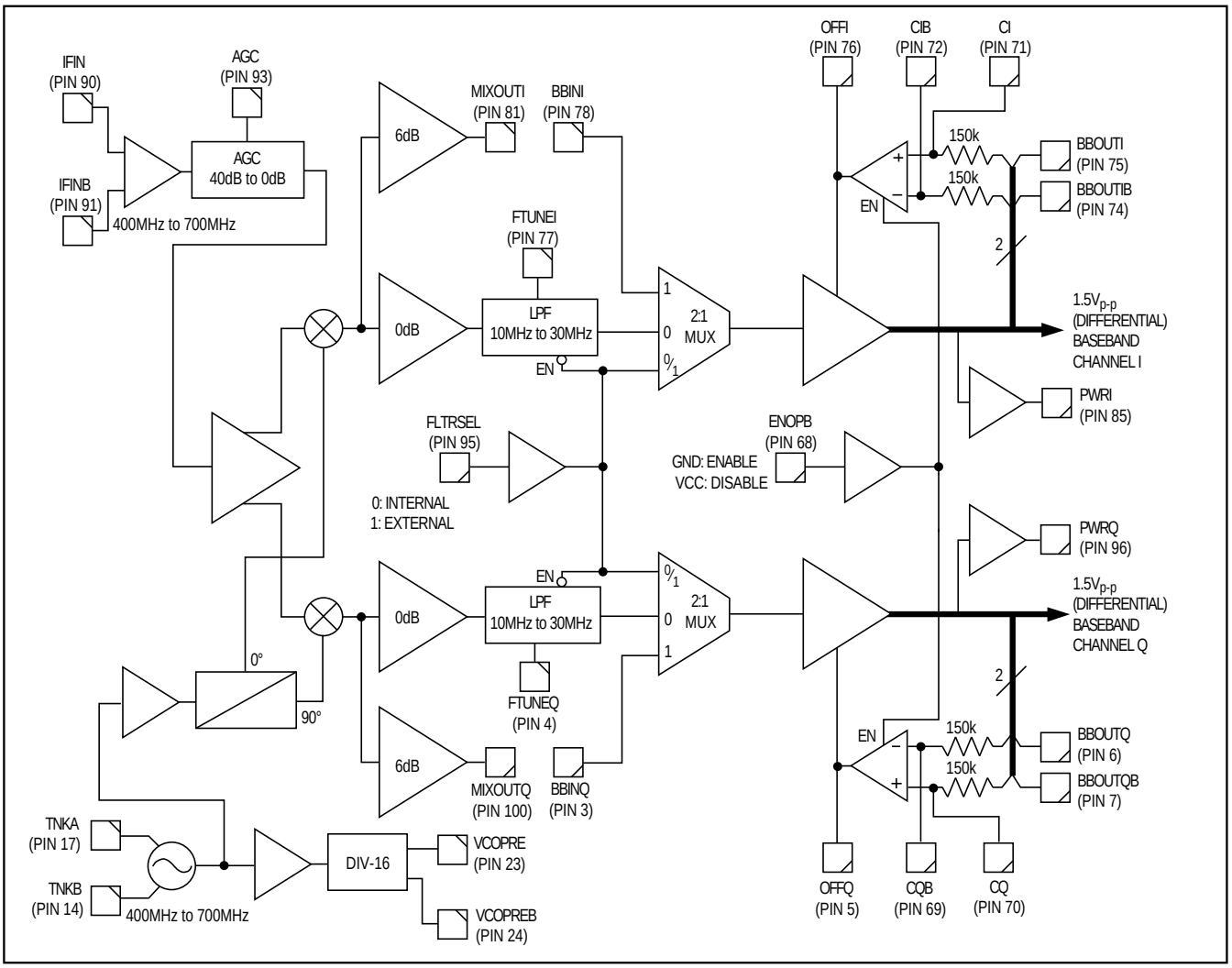


Figure 3. Functional Diagram—MAX2101 RF Front-End Section

6-Bit Quadrature Digitizer

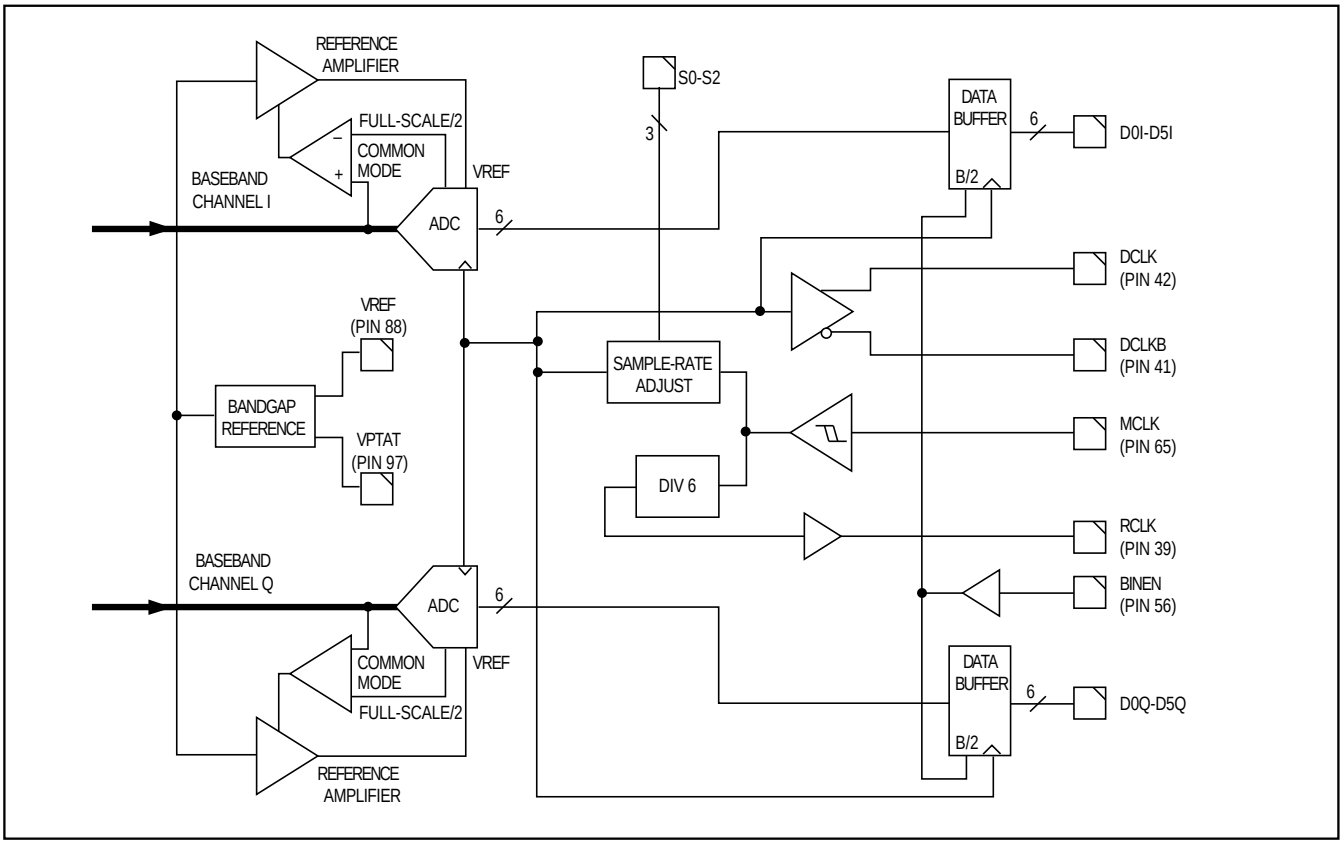


Figure 4. Functional Diagram—MAX2101 ADCs and Supporting Sections

Filter Tuning

The MAX2101 integrates two 5th-order Butterworth low-pass filters for anti-alias filtering of the baseband signal. One filter exists for each of the I and Q channels. The filters' cutoff frequency is set by driving the FTUNE pins, pin 77 (I channel) and pin 4 (Q channel). The user sets the I/Q channel filters independently. Figure 6 shows a typical transfer curve of a filter's cutoff frequency versus FTUNE voltage.

The MAX2101's anti-aliasing filtering function provides superior channel-to-channel matching compared to a discrete implementation. The filters are realized using a gyrator topology, which inherently has a strong temperature dependency. The temperature dependency of the filters must be compensated to achieve a consistent filter response over ambient temperature. This compensation is easily summed with the user-supplied filter tune signal, with the techniques discussed for both current-drive and voltage-drive implementations later in this section. Figure 7 shows a typical characteristic of the FTUNE signal required to provide a constant filter cutoff frequency over temperature.

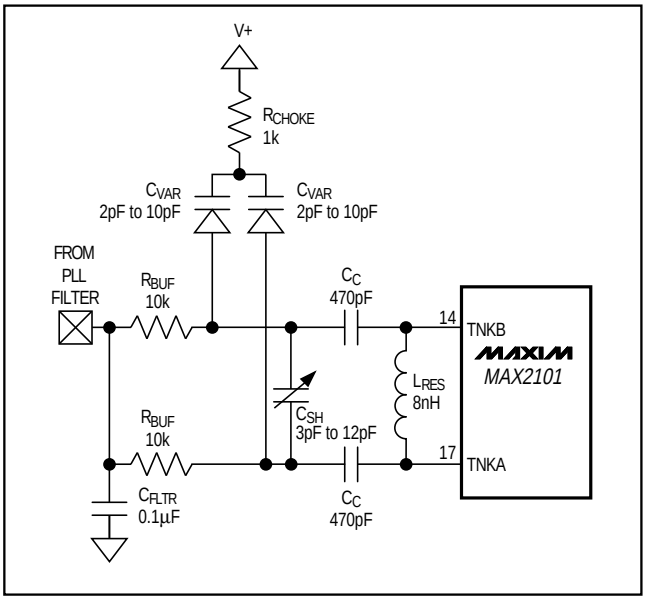


Figure 5. Typical Parallel Resonant Network

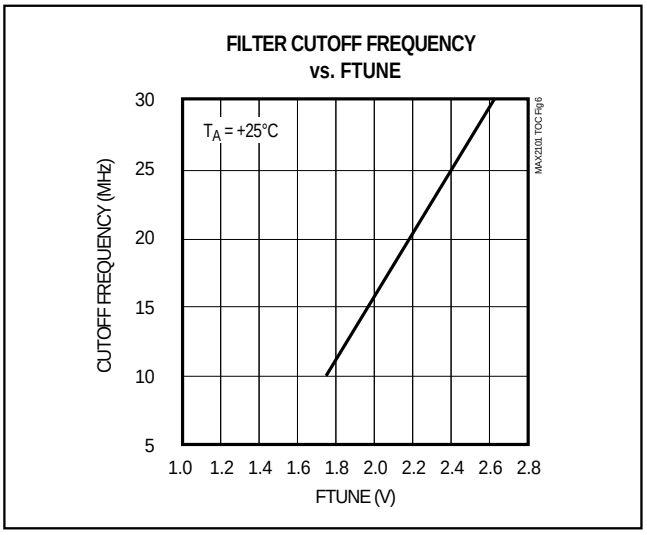


Figure 6. Typical Filter Cutoff Frequency vs. FTUNE Input Voltage

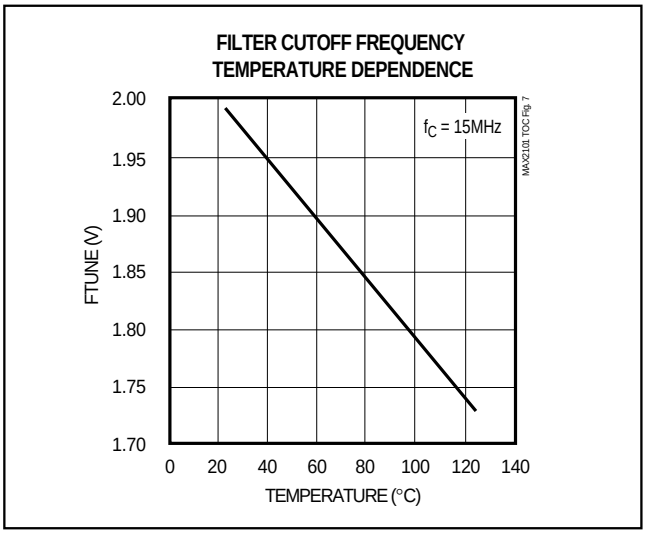


Figure 7. Typical Filter Cutoff Frequency Temperature Dependence

The MAX2101 provides temperature-compensated bias voltages that, when scaled and summed with the user-supplied filter-control signal, provide the necessary compensation for the filters. The filter-control signal can originate in one of two forms: an analog current, or an analog voltage. The temperature compensation signal will be added to the control signal as discussed below.

Voltage Drive

A suggested technique of filter drive uses a voltage source, such as a voltage output DAC. The temperature compensation signals, VPTAT and VREF, are shifted and scaled, then summed with the control voltage, and the sum is applied to the FTUNE inputs. See Figure 8 for a possible implementation.

The transfer function for Figure 8's voltage drive configuration can be evaluated as follows:

$$V_{TC} = V_{REF} + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

$$V_{FTUNE} = V_{SET} + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

Thus, the user-supplied signal V_{SET}, which is characterized by a very small (ideally 0) temperature coefficient, will be summed with a small signal ($|V_{REF} - V_{PTAT}| \leq$ 200mV) whose temperature dependence compensates for the filter's TC.

Current Drive

An alternate form of filter drive uses a current source, such as a current-output DAC. The current is transformed to the appropriate voltage via a transresistance network, which will drive the FTUNE input(s). The temperature compensation signals, VPTAT and VREF, are shifted and scaled, transformed to current, added to the user-supplied current, and the sum is transformed back into the temperature compensated control voltage (Figure 9).

Amplifier U1A generates a shifted reference signal, V_{TC}. V_{TC} is transformed into a current through the resistor R_{TC}. R_{TC} also scales this signal such that, when compared to the feedback resistor R_F, the proper temperature dependence is added to the user-supplied filter control current I_{SET} to compensate for the TC of the filter.

The expression for the final filter tune signal is expressed as:

$$V_{FTUNE} = I_{SET}(R_F) + \frac{R_F}{R_{TC}}(V_{REF} - V_{PTAT})$$

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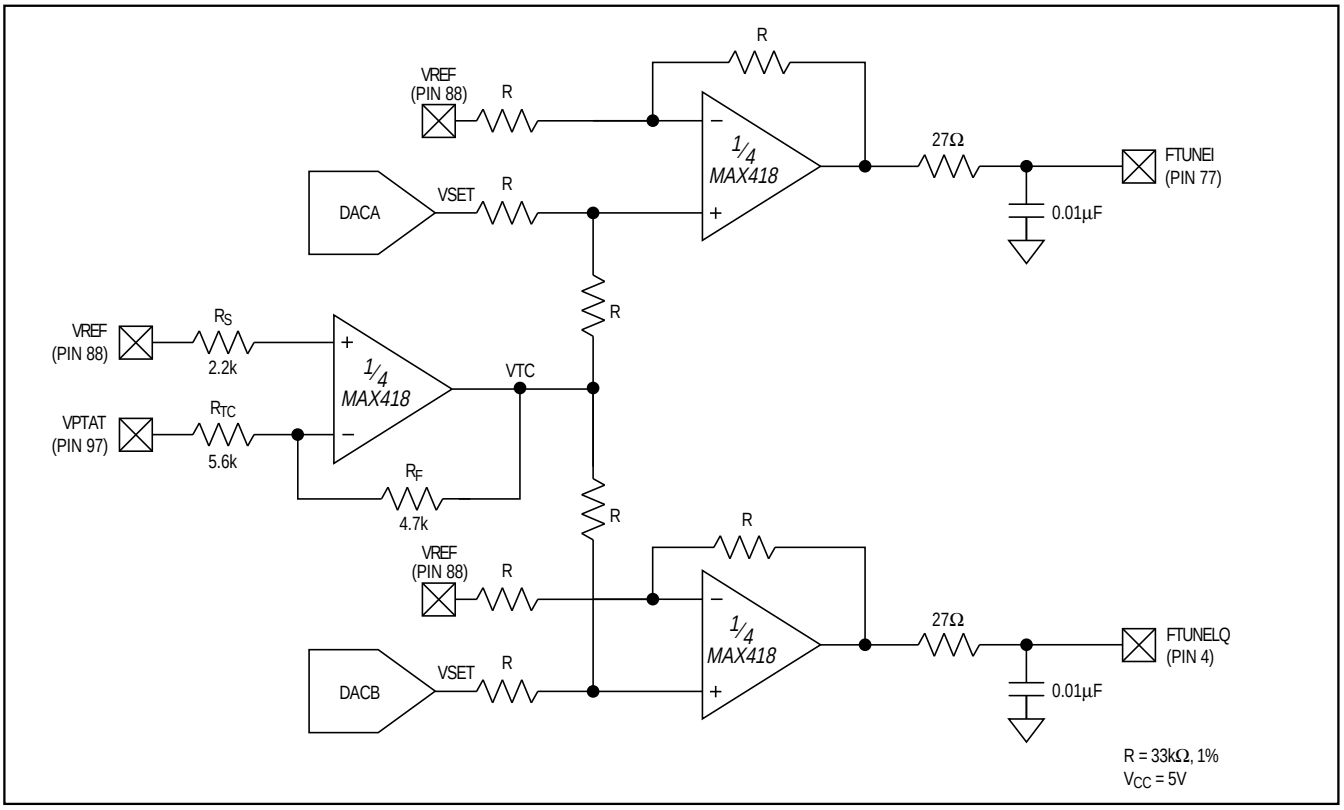

Figure 8. Independent Filter Tune Control Using Two Voltage-Output DACs

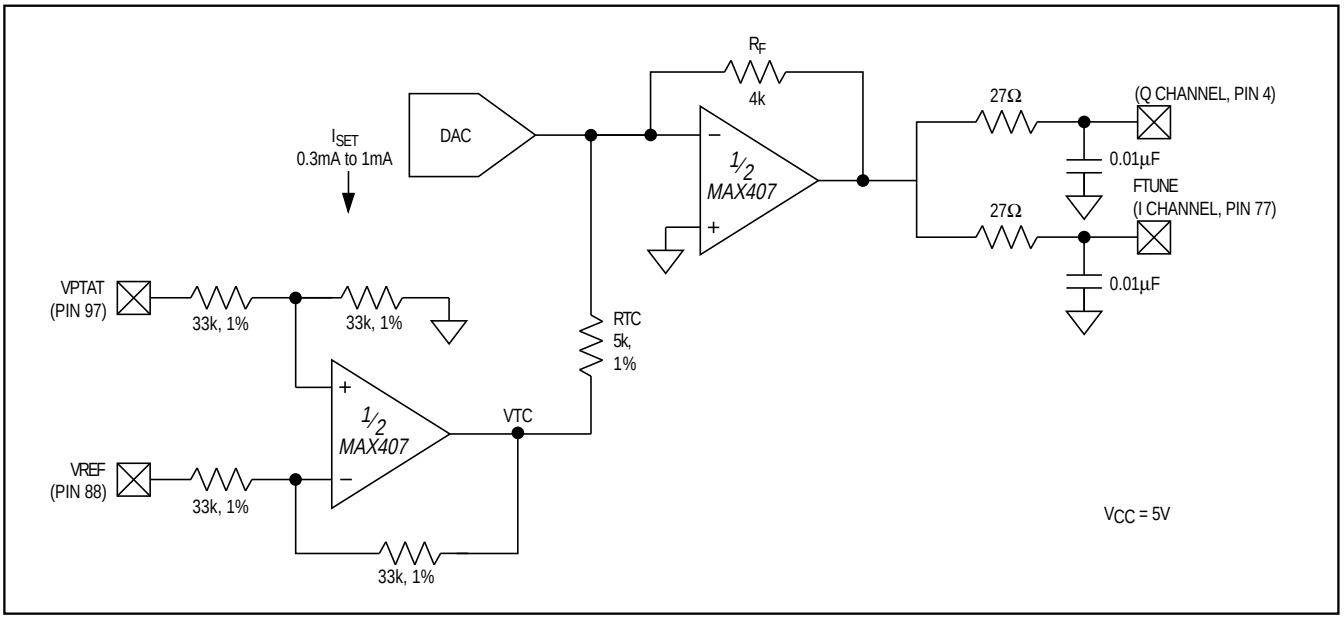

Figure 9. Filter Tune Control Using a Single Current-Output DAC

Filter Temperature Compensation

In both techniques discussed above, the ratio R_F/R_{TC} determines the compensation required to produce a filter response with 0TC. As noted in the VPTAT vs. Temperature graph in the *Typical Operating Characteristics*, this ratio should be set at 0.8.

Baseband Offset Correction

The MAX2101 integrates a high level of RF signal processing, and applies substantial gain from the IF inputs to the baseband signals applied to the ADC. Offset in the signal path can seriously decrease the component's dynamic range, and variation in offset between I and Q channels can seriously degrade overall receiver performance. Several circuit design techniques are used to minimize offset within the chip. However, two characteristics of the component contribute to offset in the signal path.

The off-chip tank network for the VCO resonates the LO frequency with a relatively large amplitude. If the LO couples into the IF input, the coupled LO will mix down to a DC value, which depends on the AGC setting. This DC signal manifests itself as an offset in the baseband signal. The second source of offset is the active lowpass anti-aliasing filters. This offset depends on the cutoff frequency. These two elements represent the major contributors to DC offset in the signal path.

Offset Adjust Pins OFFI, OFFQ

The MAX2101 offers an offset adjust pin for each of the I and Q channels, labeled OFFI and OFFQ, respectively. The offset adjust input exhibits an adjustment range that is sufficient to correct for the errors mentioned above. The polarity of the OFF_ input is such that a positive change of the OFF_ voltage results in a negative transition in the baseband signal, BBOUT_. The offset adjust range compensates for up to 5LSBs of offset.

A feedback-controlled, offset-correction network can be realized that will null any offset detected in the baseband signal applied to the ADCs. The differential baseband signal is sampled at the input to the ADC and integrated over a sufficiently large period of time (determined by the minimum frequency of the baseband signal), extracting the offset signal. This error signal is internally applied to the OFF_ input, completing the feedback loop. The MAX2101 integrates the op amps and 150kΩ pickoff resistors of the offset correction network. Figure 10 shows a simplified schematic diagram of the network. Simply connect the appropriate capacitors as shown in Figure 11.

The network in Figure 11 is a lowpass filter with a 5Hz cutoff frequency. The user can tailor the cutoff frequency by choosing the appropriate value of capacitance, according to the following relation:

$$C = \frac{1}{2\pi f_O (150k\Omega)}$$

where:

C = integrator capacitance

for cutoff frequency

Frequency components of the baseband signal near or below the cutoff frequency will interfere with the operation of this network. Fortunately, the compressed and encoded nature of baseband signals at this stage of the signal chain in typical applications will insure minimal low-frequency components. Hence, this technique will eliminate all offsets, independent of AGC setting, filter cutoff frequency, or changes in ambient temperature.

Pin 68, ENOPB, is normally connected to ground. Pulling ENOPB to V_{CC} disables the op amps, thus opening the servo loop, and disabling offset correction. The baseband pins (6, 7, 74, 75) should be left unconnected, or buffered with a high-impedance load (resistive load greater than 10kΩ and capacitive load less than 3pF).

Sample Clock Generation

The master sample clock (MCLK) input for the MAX2101 is typically driven by a low-noise, low-drift crystal oscillator. The signal should be between 0dBm and +10dBm, and must be AC coupled to the MCLK input. This signal is buffered and divided according to the programmable sample-rate prescaler (PSRP). The actual sample rates are binary weighted divisors of the MCLK frequency. Program the sample rates with pins S0, S1, and S2, as shown in Table 1.

Table 1. Sample-Rate Control

S2 S1 S0	Sample Rate	Description
0 0 0	$f_C/1$	Full Sample Rate
0 0 1	$f_C/2$	Div–2 Sample Rate
0 1 0	$f_C/4$	Div–4 Sample Rate
0 1 1	$f_C/8$	Div–8 Sample Rate
1 0 0	$f_C/8$	Div–8 Sample Rate
1 0 1	$f_C/16$	Div–16 Sample Rate
1 1 0	$f_C/32$	Div–32 Sample Rate
1 1 1	$f_C/64$	Div–64 Sample Rate

*Note: The inputs S0, S1, and S2 are **not** latched.*

6-Bit Quadrature Digitizer

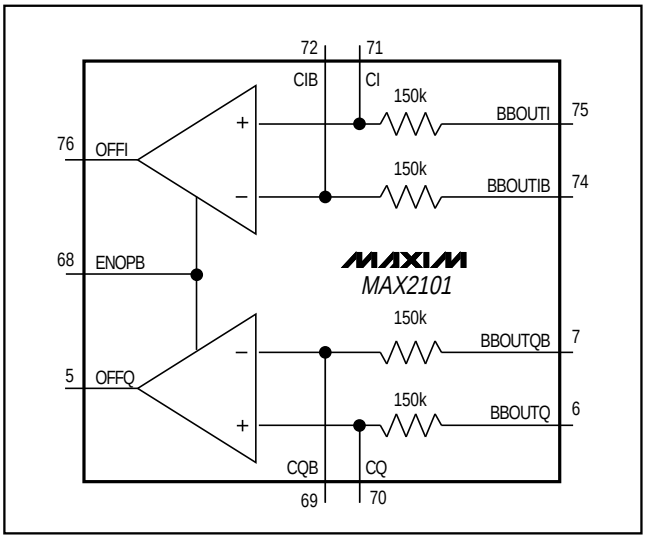

Figure 10. Offset Correction Network

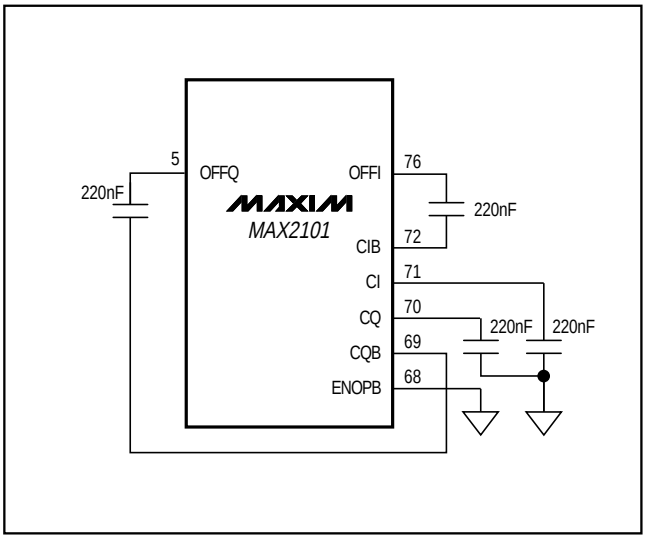

Figure 11. Offset Correction

Digital Signal Interfacing

The single-ended, LS-TTL compatible data outputs from the ADCs are clocked out with respect to the rising edge of the data clock (DCLK). The output drivers provide sufficient logic levels at speeds up to 60Mbps into a fanout of 1 with a total load capacitance of 15pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold timing.

The data clock outputs are also LS-TTL compatible and provide a signal to latch the data at rates up to 60Mbps. The outputs are differential to minimize the harmonic energy that might feed back into the LO or IF inputs. The balanced outputs should have equivalent termination to minimize unwanted EMI.

Select either binary or twos-complement output with the binary enable (BINEN) pin. A logic high will select offset binary, and a logic low will select a twos-complement format.

Input Termination Network

The MAX2101 accepts as an input a narrow band IF whose center frequency is located somewhere in the UHF range, between 400MHz and 700MHz. The MAX2101 comprises a significant part of a receiver chain characterized by extremely high dynamic range coupled with demanding intermodulation requirements. As such, it is imperative to provide proper input termination to the MAX2101, to minimize effective VSWR and noise figure at this stage of the system RF signal processing chain.

The input of the MAX2101 is designed to deliver a VSWR less than 2:1 over the 400MHz to 700MHz range. The equivalent input network of the input pins IFIN and IFINB is discussed and illustrated below. However, standard narrow-band impedance matching techniques can be used to improve on this VSWR for the intended IF of the system.

Equivalent Input Circuitry

The MAX2101's input amplifier is designed to provide a controlled input impedance, provide gain for the signal path, and provide for the component's minimum noise figure. The amplifier uses a feedback topology to provide gain that is insensitive to input frequency, in addition to delivering constant input impedance. Figure 12 illustrates the amplifier's input portion.

Ideally, the input amplifier will be designed to match to an anticipated source impedance of 50Ω. The resistive portion of the input impedance at pin IFIN can be approximated as follows:

$$R_{IN} = \frac{R_F + r_E}{(1 + A_V)}$$

where r_E is the dynamic resistance at Q3's emitter, and A_V is the open-loop gain of the differential-pair amplifier stage.

The amplifier can be designed so the frequency response does not appreciably affect the input impedance. Details of the amplifier are left out for simplicity.

Figure 12 shows how several parasitic elements contribute to the input impedance over the frequencies of interest. C_{PAD} represents the parasitic capacitance associated with the bond pad and input metallization.

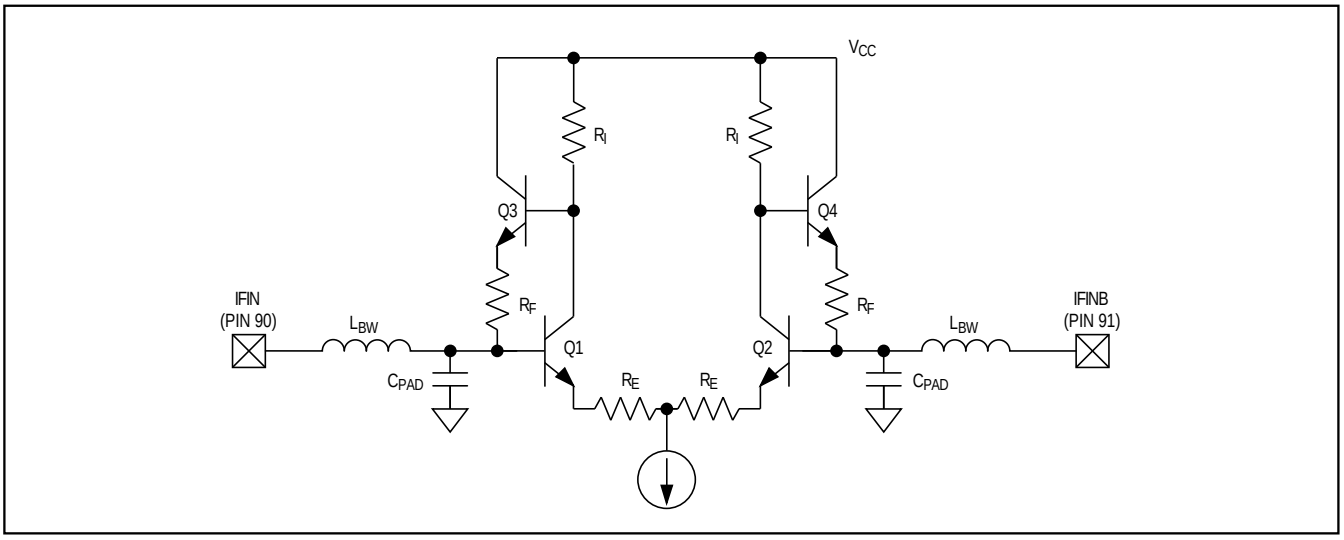

Figure 12. Equivalent Input Network

At frequencies of interest, C_{PAD} will add a small phase error to the impedance term. The inductance L_{BW} models the bond wire and lead frame in series with the input amplifier. This inductor represents a significant portion of the input impedance, and will contribute the majority of the variation in input impedance as the input frequency is swept from 400MHz to 700MHz. These variables combine to produce an actual input impedance versus frequency (Figure 13).

As a result, it is challenging to achieve an extremely low VSWR for the input of a monolithic amplifier, especially over a wide range of frequencies. The MAX2101 provides a VSWR less than 2:1, and delivers this performance over the wide range of anticipated IFs currently considered. Fortunately, for DBS, TVRO, and related applications, the UHF IF is relatively narrow band, allowing the use of standard techniques for narrow-band impedance matching.

Narrow-Band Match

Many references cover narrow-band matching techniques. The match network synthesis is simplified by assuming the impedance of the source driving the MAX2101's IFIN port is positive, real, and equal to 50Ω. For a given IF, you can simply use a Smith chart to "map" an impedance to the intended source resistance. Using a two-element matching network, you can choose the element next to the input (C_{SH} in Figure 14) to translate the real portion of the impedance to match the source resistance. The second element (L_{SER} in Figure 14) cancels the reactive component of the network (including the effect of C_{SH}), resulting in a real, matched input impedance that provides maximum power transfer. The transformation uses only reactive elements so that no additional resistive thermal noise is added, which would degrade the noise figure.

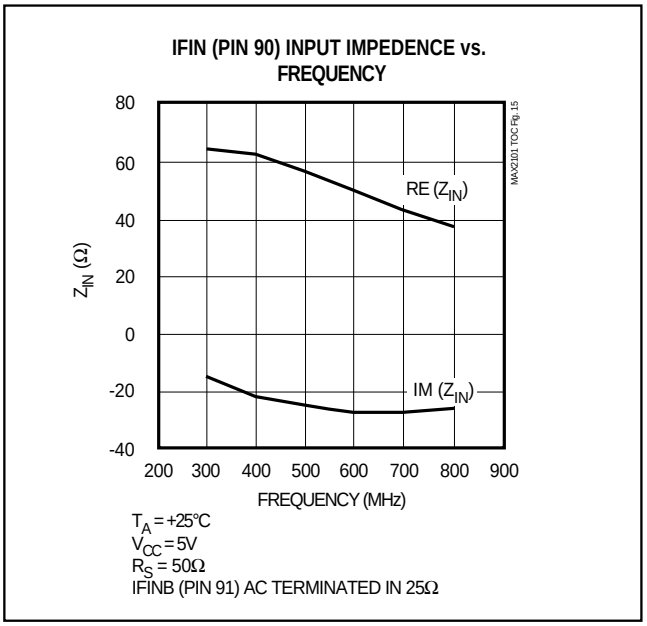

Figure 13. Typical MAX2101 IFIN Z_{IN} vs. Frequency (Zs = 50)

Figure 14 shows the resulting impedance matching network. The incident signal is AC coupled by C_C. L_{SER} and C_{SH} are the matching elements. C_{SH} includes board layout capacitance. The values of these ele-

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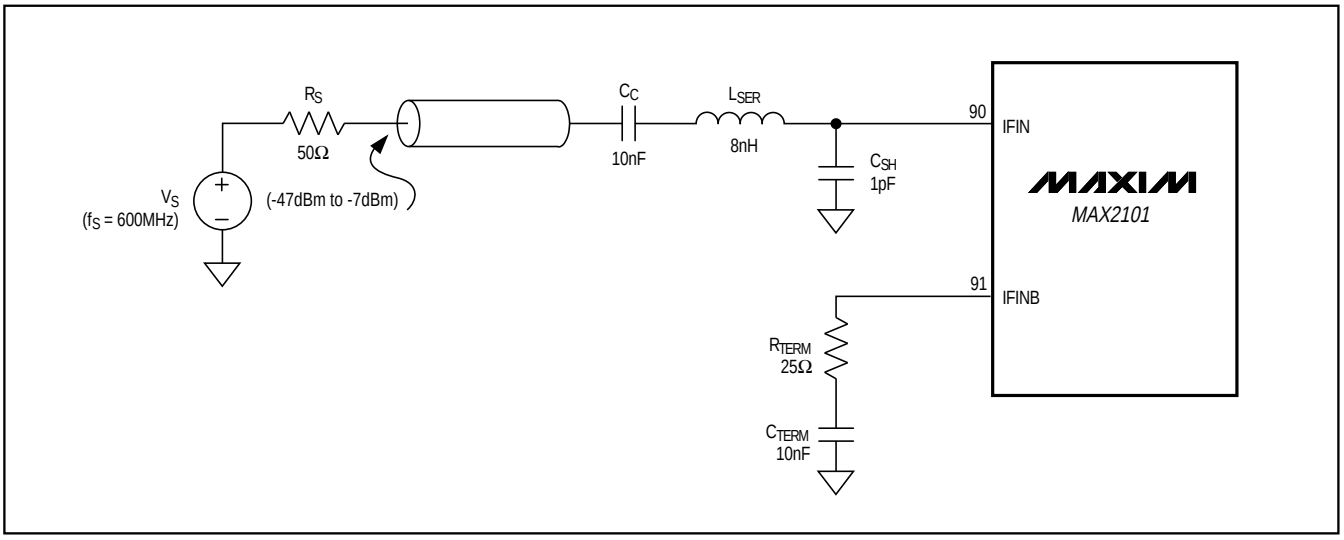


Figure 14. Example of Input Network to Minimize VSWR and Noise Figure

ments were calculated assuming a 600MHz source frequency. Capacitor C_{TERM} provides an AC termination for the complementary input IFINB. Resistor R_{TERM} provides superior noise figure performance by optimizing the tradeoff between thermal induced noise and the gain of the input amplifier. This network also provides ancillary rejection of out-of-band energy, improving the receiver noise figure and resulting SNR. The topology shown above produces a VSWR less than 1.7:1 over the intended UHF band. Do not DC couple the inputs to ground, as this would result in saturation of the input stage.

More elaborate matching networks can be designed depending on the need of the receiver system.

Applications Information

Voltage-Controlled Oscillator Equivalent Input Network and Resonator Issues

The MAX2101 performs the quadrature demodulation and digitizing functions within a digital receiver system. A vital component of the quadrature detection function is the generation of a local oscillator (LO) frequency. This signal is typically generated by a VCO controlled by a phase-locked loop. The VCO topology normally used for high dynamic range receivers is the negative resistance amplifier and resonator, due to superior phase-noise performance. The MAX2101 provides the negative resistance amplifier on-chip, and can be easily interfaced with an off-chip resonant network.

The MAX2101's VCO amplifier uses a differential topology for several reasons. The differential interface with the resonator network provides superior rejection of spurious signals that might otherwise add to or distort the resulting LO. The differential interface minimizes the effect of parasitic package-related elements that affect the resonant frequency and the loaded Q of the network. The differential-drive network minimizes second-harmonic distortion that might create undesirable mixing products within the signal chain.

Figure 15 shows the simplified input network of the negative impedance amplifier, configured as a Wilson oscillator. The amplifier is a simple differential emitter coupled pair with emitter degeneration for controlled open-loop gain. The positive feedback necessary to create the negative input impedance is performed with the feedback capacitors, C_F, and the coupling capacitors, C_C. The capacitors ensure operation over the intended 400MHz to 700MHz spectrum, and add minimal noise to the system. R_{B1} provides a proper bias voltage for the capacitors (partially constructed with voltage-dependent pn junctions) and provides for DC interface with a shunting resonant inductor. Note that biasing networks are simplified for brevity.

The MAX2101's negative impedance amplifier expects a parallel resonant network. Figure 5 shows an example of a tunable resonant network. The resonator is driven from the phase-locked loop filter output, as noted. The loaded Q of the resonant network, and to a lesser extent the absolute values of the resonant elements, determine the VCO's phase-noise performance. As a result, take care during the design of the resonator to maximize the loaded Q. To achieve the phase-noise

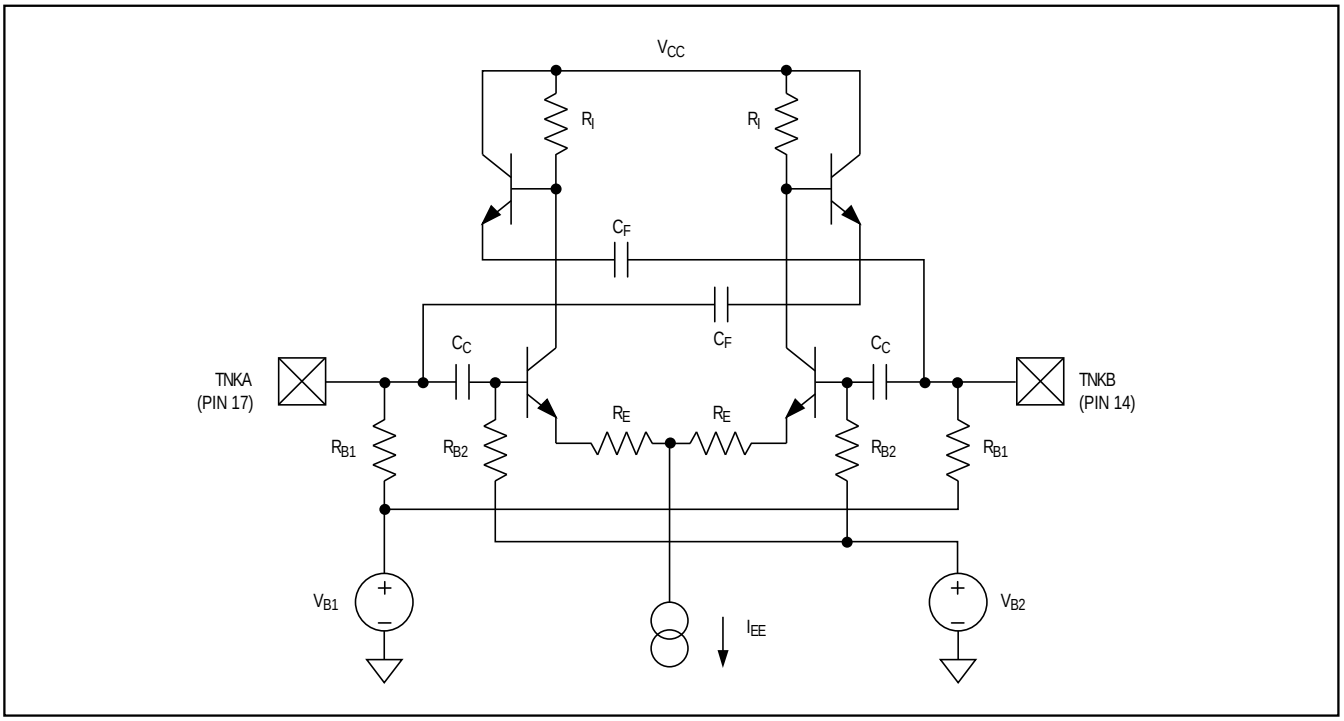


Figure 15. Simplified Input Network for VCO Resonator Ports

performance in the specification, the resonant network should exhibit a loaded Q greater than 20.

The resonating inductor L_{RES} should exhibit as high a Q factor as is reasonably possible. The inductor's self-resonant frequency (SRF) should be well in excess of the intended frequencies of operation. An air-wound design is a simple example of an inductor that would fit these criteria.

A dual varactor topology is recommended for C_{VAR} to compensate for the large-signal amplitude incident across the resonator ports. The dual varactor in the arrangement shown in Figure 5 (to first order) allows cancellation of capacitance modulation due to the large signals, as the two diodes are driven in a complementary fashion by the LO signal. The dual varactor design also allows use of devices with larger C_O values, simplifying device selection. The varactor should be driven with a large reverse bias to increase the MAX2101's effective Q.

The resonant frequency is primarily determined by C_{SH}, which shunts the varactor diodes. C_{SH} is trimmed (selected) to determine the approximate tuning range of the phase-locked loop. For applications relevant to the MAX2101, this frequency range can cover the UHF spectrum from 400MHz to 700MHz. The varactor within the loop will then determine the actual LO frequency within a much narrower tuning range. Depending on the expected tuning range variation, C_{SH} could be made of a combination of fixed capacitance and trimmed capacitance. This shunt capacitance will increase the loaded Q of the resonator and lower the V to F gain constant, improving the oscillator's phase-noise performance.

The coupling capacitors C_C couple the variable capacitor network to the tank ports and resonating inductor. These elements should be selected to present low impedance (less than 1Ω) at the lowest expected operating frequency. These capacitors should also exhibit low effective series resistance (ESR) to maintain a high resonator-loaded Q. R_{CHOKE} provides a DC bias for the varactors, while ensuring a high impedance at the intended operating frequency. The magnitude of the choke network's series impedance should be approximately 10 times the resonant inductor's impedance at the operating frequency. Resistors R_{BUF} provide drive for the varactor while ensuring adequate isolation between the two differential resonator ports. C_{FLTR}, in combination with R_{BUF}, provides additional filtering of the drive signal from the loop.

6-Bit Quadrature Digitizer

DBS System Application

A direct-broadcast satellite (DBS) receiver consists of an antenna to receive the X/Ku band carrier from the satellite, a low-noise block (LNB), an L-band downconverter, and a quadrature demodulator. The system stages include a dual ADC, a matched filter, clock and carrier recovery, error detection and correction, and additional system-dependent DSP. See the *Typical Application Circuit* on the first page of the data sheet.

The LNB provides polar demodulation (vertical and horizontal) and downconversion of the X/Ku band signals to a first intermediate frequency (IF_1) in the 950MHz to 2000MHz range. The L-band downconverter converts IF_1 to a second IF (IF_2) in the 400MHz to 700MHz range. The MAX2101 performs the next stages as follows: 1) the quadrature demodulator converts IF_2 to two baseband signals, I and Q; and 2) the dual ADCs digitize the baseband signals, which are then processed by the various digital blocks to compensate for transmission distortion and to extract the digital baseband data.

One interface that causes system designers trouble is the quadrature demodulator to ADC interface. Power is needed to drive the low-impedance interconnect between these two functions. Additionally, this portion of the signal path can introduce phase and amplitude errors that complicate back-end error correction. The integrated MAX2101 solves all of these design problems associated with DBS systems.

The MAX2101 combines bipolar technology with excellent RF and data-converter design to integrate the quadrature demodulation and ADC functions. The MAX2101 also includes an IF gain block, a VCO and prescaler necessary to generate an accurate LO frequency, and fully integrated baseband anti-aliasing filters for both I and Q channels. By integrating several functions supporting the quadrature demodulation and A/D block, the MAX2101 replaces several components and eliminates many board-level design and manufacturing problems.

Layout, Grounding, Bypassing

The MAX2101's supply pins are separated to isolate high-current digital noise spikes from sensitive RF and analog sections. All ground potentials must be DC coupled, and resistive drops should contribute no more than 50mV difference between the ground pins. A single-point analog ground ("star" ground point) should be established at the ground supply connection to the PC board, separate from the active circuitry. Three ground planes should be established, connected at the star ground point. The three ground planes should be dedicated as follows: analog and RF ground plane, digital ground plane, and output ground plane. The various ground pins should be connected to this star ground network according to Table 2. The ground current return path for all supplies should be low impedance at frequencies of interest for each supply.

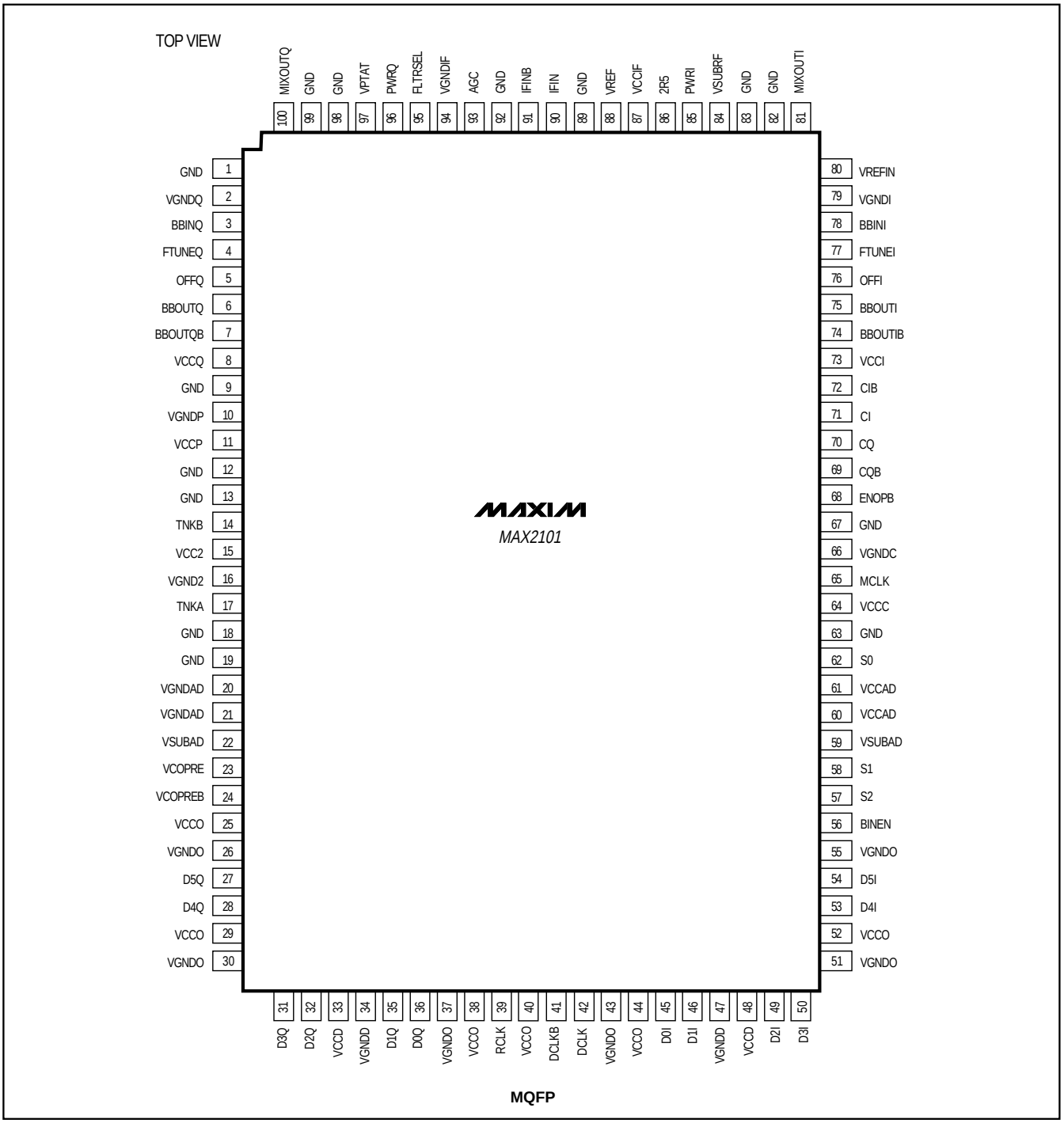
Table 2. Ground Plane Assignments

Ground Pin	Pin Number	Ground Plane
VGNDIF	94	analog
VGNDI	79	analog
VGNDQ	2	analog
VGND2	16	analog
VGNDAD	20, 21	analog
VGNDP	10	digital
VGNDC	66	digital
VGNDD	34, 47	digital
VGNDO	26, 30, 37, 43, 51, 55	output

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the MAX2101 package.

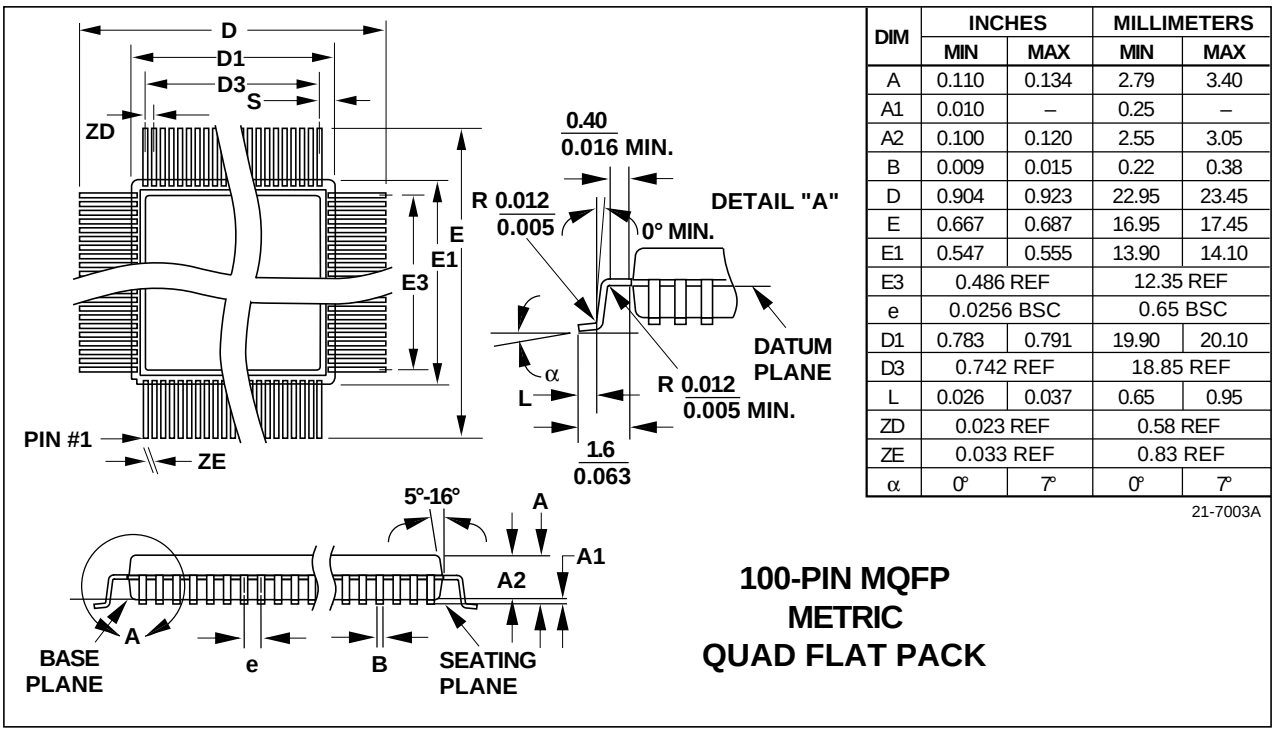
The MAX2101 requires +5V ±5% for all supply pins. Bypass the supply pins with high-quality 0.1µF and 0.001µF ceramic capacitors located as close to the package as possible. The high-frequency supplies, VCCIF and VCC2, both require an additional ceramic surface-mount bypass capacitor nominally valued at 47pF. The baseband supplies (VCCI and VCCQ) need additional filtering to ensure sufficient channel-to-channel isolation. Place a small-value resistor, such as 5Ω, between the supply and the pins to create a single-pole filter with the bypass capacitor. The DC IR drop across the resistor should not exceed 150mV. Alternatively, place an RF choke between the supply and the pins. The SRF of the selected choke must be high enough to block energy from the other baseband channel.

Pin Configuration



6-Bit Quadrature Digitizer

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.110	0.134	2.79	3.40
A1	0.010	–	0.25	–
A2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.904	0.923	22.95	23.45
E	0.667	0.687	16.95	17.45
E1	0.547	0.555	13.90	14.10
E3	0.486 REF		12.35 REF	
e	0.0256 BSC		0.65 BSC	
D1	0.783	0.791	19.90	20.10
D3	0.742 REF		18.85 REF	
L	0.026	0.037	0.65	0.95
ZD	0.023 REF		0.58 REF	
ZE	0.033 REF		0.83 REF	
α	0°	7°	0°	7°

21-7003A

100-PIN MQFP
METRIC
QUAD FLAT PACK

6-Bit Quadrature Digitizer

MAX2101