

**Document Title**

**8M DDR SYNCHRONOUS SRAM**

**Revision History**

<u>Rev No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev. 0.0	-Initial document.	July. 2000	Advance
Rev. 0.1	-ZQ tolerance changed from 10% to 15%	Aug. 2000	Advance
Rev. 0.2	-Stop Clock Standby Current condition changed from $V_{IN}=V_{DD}-0.2V$ or $0.2V$ fixed to $V_{IN}=V_{IH}$ or $V_{IH}$	Oct. 2000	Advance
Rev. 0.3	- $V_{DDQ}$ Max. changed to 2.0V SA0, SA1 defined for Boundary Scan Order	Nov. 2000	Advance
Rev. 0.5	-Deleted -HC16 part(Part Number, Idd, AC Characteristics)	Jan. 2001	Preliminary
Rev. 0.6	- Absolute Maximum ratings $V_{DDQ}$ changed from 3.13V to 2.825V	Feb. 2001	Preliminary
Rev. 0.7	- $\overline{LB0}$ input level changed from High/Low to $V_{DDQ}/V_{SS}$ - Stop Clock Standby Current condition changed from $K=Low, \overline{K}=High$ to $K=Low, \overline{K}=Low$ - $t_{CHQV}/t_{CLQV}$ changed from 0.1ns to 0.2ns for -33 part from 0.1ns to 0.2ns for -30 part from 0.1ns to 0.25ns for -25part - $t_{CHQX}/t_{CLQX}$ changed from -0.3ns to -0.2ns for -33 part from -0.3ns to -0.2ns for -30 part from -0.4ns to -0.25ns for -25part - $t_{CHQZ}/t_{CLQZ}$ changed from 0.1ns to 0.2ns for -33 part from 0.1ns to 0.2ns for -30 part from 0.1ns to 0.25ns for -25part - $t_{KXCH}$ changed from 1.8ns to 1.7ns for -33 part - $t_{KXCL}$ changed from 1.8ns to 1.7ns for -33 part	Mar. 2001	Preliminary
Rev. 1.0	- Clarification on the features and the timing waveforms regarding the burst controllability. - Recommended DC operating conditions for Clock added. - AC test conditions for $V_{DDQ}=1.8V$ and Single ended clock added. (AC Test Conditions 2) - Package thermal characteristics added.	May. 2001	Final
Rev. 2.0	- Add-HC35 part(Part Number, Idd, AC Characteristics)	Sep. 2001	Final
Rev. 3.0	- Absolute Maximum Rating $V_{DDQ}$ changed from 2.825V to 2.4V - $V_{CM-CLK}$ Min changed from 0.6V to 0.68V	Jan. 2002	Final
Rev. 4.0	- Add-HC37 part(Part Number, Idd, AC Characteristics)	Jan. 2002	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



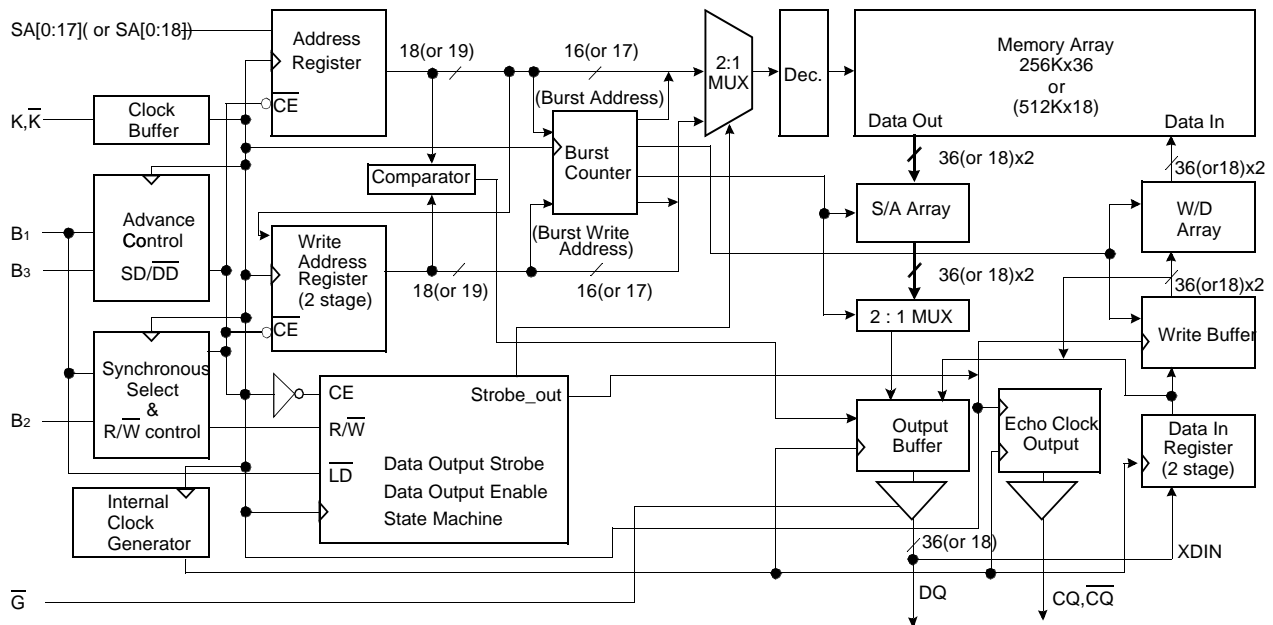
**FEATURES**

- 256Kx36 or 512Kx18 Organizations.
- Maximum Frequency : 370MHz (Data Rate : 740Mbps)
- 2.5V V<sub>DD</sub>/1.5V V<sub>DDQ</sub> (2.0V max V<sub>DDQ</sub>).
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write
- Free Running Active High and Active Low Echo Clock Output Pin.
- Asynchronous Output Enable.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Single and Double Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleaved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Maximum Frequency	Access Time
256Kx36	K7D803671B-HC37	370MHz	1.7*
	K7D803671B-HC35	357MHz	1.7*
	K7D803671B-HC33	333MHz	1.7*
	K7D803671B-HC30	300MHz	1.9*
	K7D803671B-HC25	250MHz	2.0*
512Kx18	K7D801871B-HC37	370MHz	1.7*
	K7D801871B-HC35	357MHz	1.7*
	K7D801871B-HC33	333MHz	1.7*
	K7D801871B-HC30	300MHz	1.9*
	K7D801871B-HC25	250MHz	2.0*

**NOTE** : \*Access time equals t<sub>KXCH</sub>/t<sub>KXCL</sub>

**FUNCTIONAL BLOCK DIAGRAM**



**PIN DESCRIPTION**

Pin Name	Pin Description	Pin Name	Pin Description
K, K̄	Differential Clocks	ZQ	Output Driver Impedance Control Input
SA	Synchronous Address Input	TCK	JTAG Test Clock
SA0, SA1	Synchronous Burst Address Input (SA0 = LSB)	TMS	JTAG Test Mode Select
DQ	Synchronous Data I/O	TDI	JTAG Test Data Input
CQ, CQ̄	Differential Output Echo Clocks	TDO	JTAG Test Data Output
B1	Load External Address	VREF	HSTL Input Reference Voltage
B2	Burst R/W Enable	VDD	Power Supply
B3	Single/Double Data Selection	VDDQ	Output Power Supply
Ḡ	Asynchronous Output Enable	VSS	GND
LBO	Linear Burst Order	NC	No Connection

**PACKAGE PIN CONFIGURATIONS(TOP VIEW)**

**K7D803671B(256Kx36)**

	1	2	3	4	5	6	7	8	9
<b>A</b>	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
<b>B</b>	DQ	DQ	SA	Vss	B1	Vss	SA	DQ	DQ
<b>C</b>	Vss	VDDQ	SA	SA	$\overline{G}$	SA	SA	VDDQ	Vss
<b>D</b>	DQ	DQ	NC	Vss	VDD	Vss	SA	DQ	DQ
<b>E</b>	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
<b>F</b>	DQ	CQ1	DQ	VDD	VDD	VDD	DQ	CQ2	DQ
<b>G</b>	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
<b>H</b>	DQ	DQ	DQ	VDD	$\overline{K}$	VDD	DQ	DQ	DQ
<b>J</b>	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
<b>K</b>	DQ	DQ	DQ	Vss	B2	Vss	DQ	DQ	DQ
<b>L</b>	Vss	VDDQ	Vss	$\overline{LBO}$	B3	MODE	Vss	VDDQ	Vss
<b>M</b>	DQ	$\overline{CQ1}$	DQ	VDD	VDD	VDD	DQ	$\overline{CQ2}$	DQ
<b>N</b>	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
<b>P</b>	DQ	DQ	NC	Vss	VDD	Vss	SA	DQ	DQ
<b>R</b>	Vss	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	Vss
<b>T</b>	DQ	DQ	SA	Vss	SA0	Vss	SA	DQ	DQ
<b>U</b>	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

\* Mode Pin(6L) is a internally NC.

**K7D801871B(512Kx18)**

	1	2	3	4	5	6	7	8	9
<b>A</b>	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
<b>B</b>	NC	DQ	SA	Vss	B1	Vss	SA	NC	DQ
<b>C</b>	Vss	VDDQ	SA	SA	$\overline{G}$	SA	SA	VDDQ	Vss
<b>D</b>	DQ	NC	NC	Vss	VDD	Vss	SA	DQ	NC
<b>E</b>	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
<b>F</b>	NC	CQ1	NC	VDD	VDD	VDD	DQ	NC	DQ
<b>G</b>	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
<b>H</b>	DQ	NC	DQ	VDD	$\overline{K}$	VDD	NC	DQ	NC
<b>J</b>	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
<b>K</b>	NC	DQ	NC	Vss	B2	Vss	DQ	NC	DQ
<b>L</b>	Vss	VDDQ	Vss	$\overline{LBO}$	B3	MODE	Vss	VDDQ	Vss
<b>M</b>	DQ	NC	DQ	VDD	VDD	VDD	NC	$\overline{CQ1}$	NC
<b>N</b>	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
<b>P</b>	NC	DQ	SA	Vss	VDD	Vss	SA	NC	DQ
<b>R</b>	Vss	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	Vss
<b>T</b>	DQ	NC	SA	Vss	SA0	Vss	SA	DQ	NC
<b>U</b>	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

\* Mode Pin(6L) is a internally NC.

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## FUNCTION DESCRIPTION

The K7D803671B and K7D801871B are 9,437,184 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 262,144 words by 36 bits for K7D803671B and 524,288 words by 18 bits for K7D801871B, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and  $\bar{K}$  are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted (Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

Data outputs are updated from output registers off the rising edges of K clock for SDR read operations, and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representative of data output access time for all SDR and DDR operations.

The chip is operated with a single +2.5V power supply and is compatible with Extended HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

### Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.

Interleave and linear burst operation is controlled by LBO pin and the burst count is controllable with the maximum burst length of 4. To avoid data contention, at least one NOP operations are required between the last read and the first write operation.

### Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array.

### Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.

Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

### Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

### Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and Vss, and are equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with  $\bar{G}$  high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time  $\bar{G}$  are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

**TRUTH TABLE**

K	$\overline{G}$	B1	B2	B3	DQ	Operation
L	X	X	X	X	Hi-Z	Clock Stop
↑	X	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	L	H	H	DOUT	Load Address, Single Read
↑	L	L	H	L	DOUT	Load Address, Double Read
↑	X	L	L	H	DIN	Load Address, Single Write
↑	X	L	L	L	DIN	Load Address, Double Write
↑	X	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".  
- K &  $\overline{K}$  are complementary.

**BURST SEQUENCE TABLE**

**4 Burst Operation for Interleaved Burst ( $\overline{LBO} = V_{DDQ}$ )**

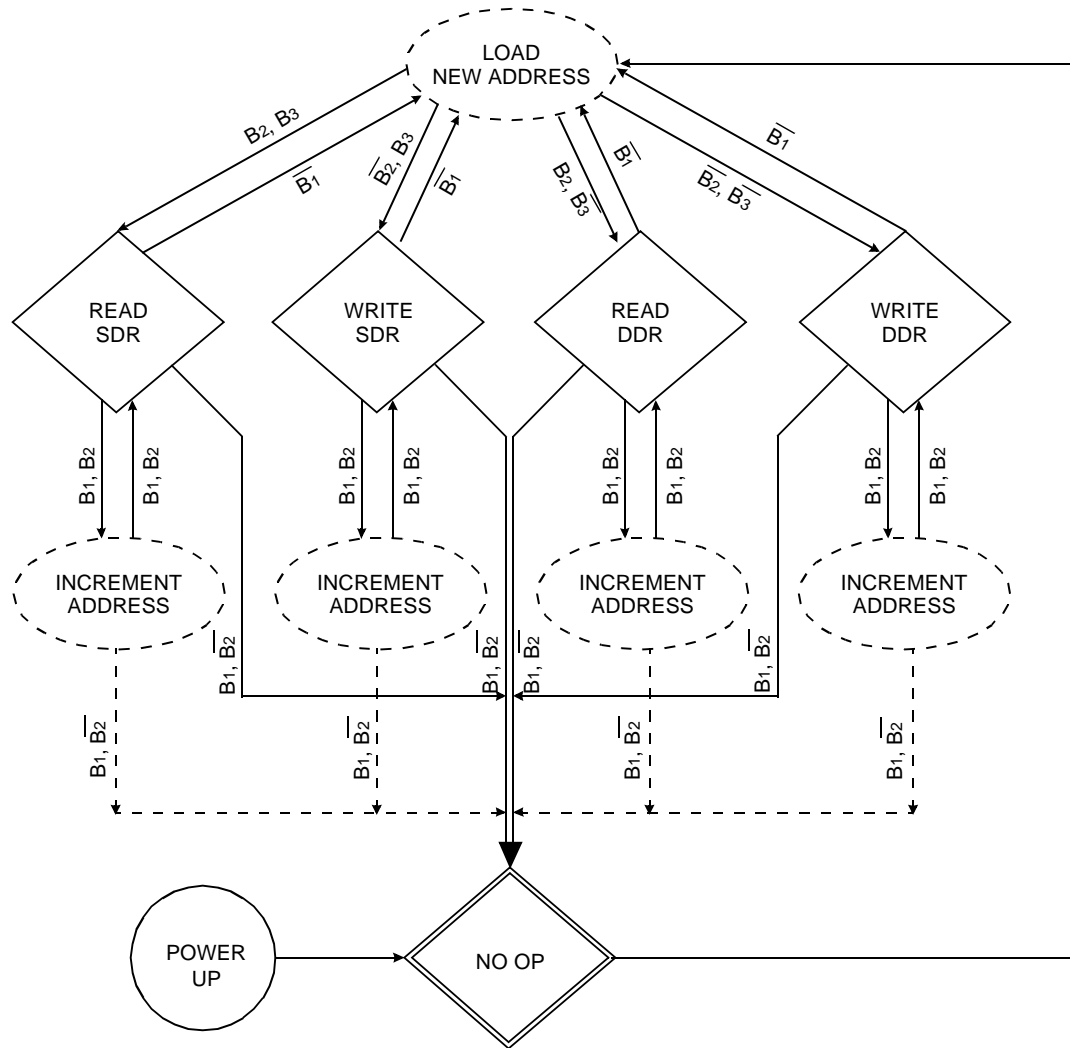
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst  $\overline{LBO} = V_{DDQ}$  is recommended. If  $\overline{LBO} = V_{DD}$ , it must not exceed 2.63V.

**4 Burst Operation for Linear Burst ( $\overline{LBO} = V_{SS}$ )**

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

- State transitions ;  $\overline{B_1}$  =(Load Address),  $B_1$ =(Increment Address, Continue)  
 $B_2$  =(Read),  $\overline{B_2}$  =(Write)  
 $B_3$  =(Single Data Rate),  $\overline{B_3}$  =(Double Data Rate)

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.13	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 2.4	V
Voltage on any pin Relative to Vss	VIN	-0.5 to VDDQ+0.5 (2.4V MAX)	V
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C

**NOTE :** Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	2.37	2.5	2.63	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	2.0	V	
Input High Level Voltage	VIH	VREF+0.1	-	VDDQ+0.3	V	1, 2
Input Low Level Voltage	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.68	0.75	1.0	V	
Clock Input Signal Voltage	VIN-CLK	-0.3	-	VDDQ+0.3	V	1, 4
Clock Input Differential Voltage	VDIF-CLK	0.1	-	VDDQ+0.6	V	1, 5
Clock Input Common Mode Voltage	VCM-CLK	0.68	0.75	0.9	V	1, 6

- NOTE :** 1. These are DC test criteria. DC design criteria is  $V_{REF} \pm 50mV$ . The AC  $V_{IH}/V_{IL}$  levels are defined separately for measuring timing parameters.
2.  $V_{IH} (Max)DC = V_{DDQ} + 0.3$ ,  $V_{IH} (Max)AC = 2.6V$  (2.1V for DQs) (pulse width  $\leq 20\%$  of cycle time).
  3.  $V_{IL} (Min)DC = -0.3V$ ,  $V_{IL} (Min)AC = -1.0V$  (-0.5V for DQs) (pulse width  $\leq 20\%$  of cycle time).
  4.  $V_{IN-CLK}$  specifies the maximum allowable DC level for the differential clock. i.e  $V_{IL-CLK}$  and  $V_{IH-CLK}$ .
  5.  $V_{DIF-CLK}$  specifies the minimum Clock differential voltage required for switching. i.e DC voltage difference between  $V_{IL-CLK}$  and  $V_{IH-CLK}$ .
  6.  $V_{CM-CLK}$  specifies the Clock crossing point for the differential clock or the allowable common clock level for a single ended clock.

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = t <sub>KHKH</sub> min)	IDD37		880		
	IDD35		850		
	IDD33	-	750	mA	1,2
	IDD30		670		
	IDD25		600		
Average Power Supply Operating Current(x18) (Cycle time = t <sub>KHKH</sub> min)	IDD37		830		
	IDD35		800		
	IDD33	-	700	mA	1,2
	IDD30		620		
	IDD25		550		
Stop Clock Standby Current (V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , K=Low, $\bar{K}$ =Low)	ISB1	-	150	mA	1
Input Leakage Current (V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DDQ</sub> )	I <sub>LI</sub>	-1	1	μA	
Output Leakage Current (V <sub>OUT</sub> =V <sub>SS</sub> or V <sub>DDQ</sub> )	I <sub>LO</sub>	-1	1	μA	
Output High Voltage(Programmable Impedance Mode)	V <sub>OH1</sub>	V <sub>DDQ</sub> /2	V <sub>DDQ</sub>	V	3
Output Low Voltage(Programmable Impedance Mode)	V <sub>OL1</sub>	V <sub>SS</sub>	V <sub>DDQ</sub> /2	V	4
Output High Voltage(I <sub>OH</sub> =-0.1mA)	V <sub>OH2</sub>	V <sub>DDQ</sub> -0.2	V <sub>DDQ</sub>	V	5
Output Low Voltage(I <sub>OL</sub> =0.1mA)	V <sub>OL2</sub>	V <sub>SS</sub>	0.2	V	5

- NOTE** :1. Minimum cycle. I<sub>OUT</sub>=0mA.  
2. 50% read cycles.  
3. |I<sub>OH</sub>|=(V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5)±15% @ V<sub>OH</sub>=V<sub>DDQ</sub>/2 for 175Ω ≤ R<sub>Q</sub> ≤ 350Ω.  
4. |I<sub>OL</sub>|=(V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5)±15% @ V<sub>OL</sub>=V<sub>DDQ</sub>/2 for 175Ω ≤ R<sub>Q</sub> ≤ 350Ω.  
5. Minimum Impedance Mode when Z<sub>Q</sub> pin is connected to V<sub>SS</sub>.

**PIN CAPACITANCE**

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	4	pF
Data Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	5	pF

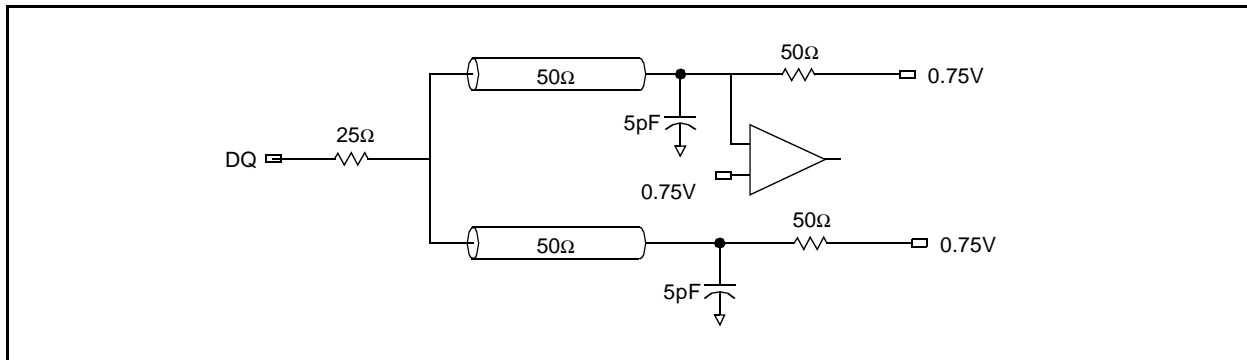
**NOTE** : Periodically sampled and not 100% tested.(T<sub>A</sub>=25°C, f=1MHz)



**AC TEST CONDITIONS 1** ( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{DD}=2.37$  -  $2.63\text{V}$ ,  $V_{DDQ}=1.5\text{V}$ )

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	$V_{IH}/V_{IL}$	1.25/0.25	V	-
Input Reference Level	$V_{REF}$	0.75	V	-
Input Rise/Fall Time	$T_R/T_F$	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

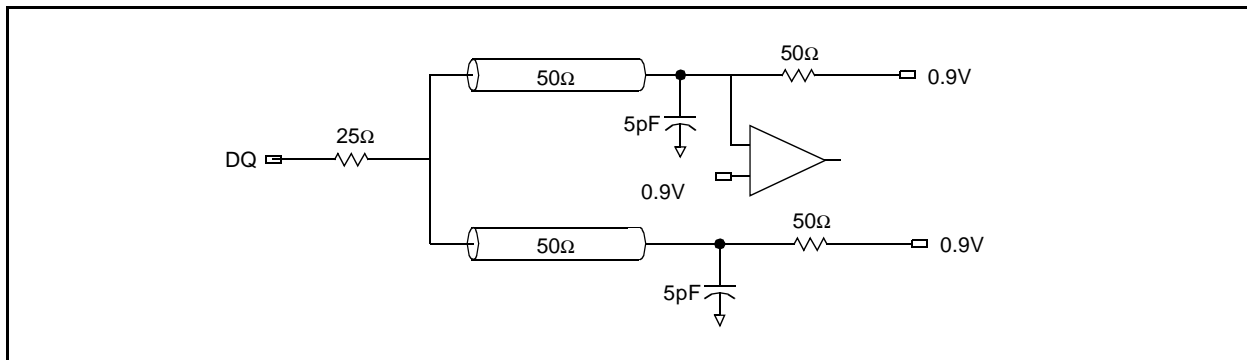
**AC TEST OUTPUT LOAD 1**



**AC TEST CONDITIONS 2** ( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{DD}=2.37$  -  $2.63\text{V}$ ,  $V_{DDQ}=1.8\text{V}$ )

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	$V_{IH}/V_{IL}$	1.64/0.18	V	-
Input Reference Level	$V_{REF}$	0.9	V	-
Input Rise/Fall Time	$T_R/T_F$	0.5/0.5	ns	-
Output Timing Reference Level		0.9	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

**AC TEST OUTPUT LOAD 2**



**AC CHARACTERISTICS**(For both AC test condition 1 and 2)

Parameter	Symbol	-33		-30		-25		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tkHKKH	3.0	-	3.3	-	4.0	-	ns	
Clock High Pulse Width	tkHKKL	1.3	-	1.5	-	1.7	-	ns	
Clock Low Pulse Width	tkLKKH	1.3	-	1.5	-	1.7	-	ns	
CQ High Pulse Width	tCHCL	tkHKKL-0.1	tkHKKL+0.1	tkHKKL-0.2	tkHKKL+0.2	tkHKKL-0.3	tkHKKL+0.3	ns	
CQ Low Pulse Width	tCLCH	tkLKKH-0.1	tkLKKH+0.1	tkLKKH-0.2	tkLKKH+0.2	tkLKKH-0.3	tkLKKH+0.3	ns	
Clock to Echo Clock(CQ) High	tkXCH	0.5	1.7	0.5	1.9	0.5	2.0	ns	1
Clock to Echo Clock(CQ) Low	tkXCL	0.5	1.7	0.5	1.9	0.5	2.0	ns	
Echo Clock to Output Valid	tCHQV/tCLQV	-	0.2	-	0.2	-	0.25	ns	1,2
Echo Clock to Output Hold	tCHQX/tCLQX	-0.2	-	-0.2	-	-0.25	-	ns	1
Echo Clock to Output High-Z	tCHQZ/tCLQZ		0.2		0.2		0.25	ns	1
$\bar{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	ns	1
$\bar{G}$ High to Output High-Z	tGHQZ	-	2.1	-	2.3	-	2.5	ns	1
$\bar{G}$ Low to Output Valid	tGLQV	-	2.1	-	2.3	-	2.5	ns	1
Address Setup Time	tAVKH	0.4	-	0.4	-	0.5	-	ns	
Address Hold Time	tkHAX	0.4	-	0.4	-	0.5	-	ns	
Burst Control Setup Time	tBVKH	0.4	-	0.4	-	0.5	-	ns	
Burst Control Hold Time	tkHBX	0.4	-	0.4	-	0.5	-	ns	
Data Setup Time	tDVKH	0.4	-	0.4	-	0.5	-	ns	
Data Hold Time	tkHDX	0.4	-	0.4	-	0.5	-	ns	

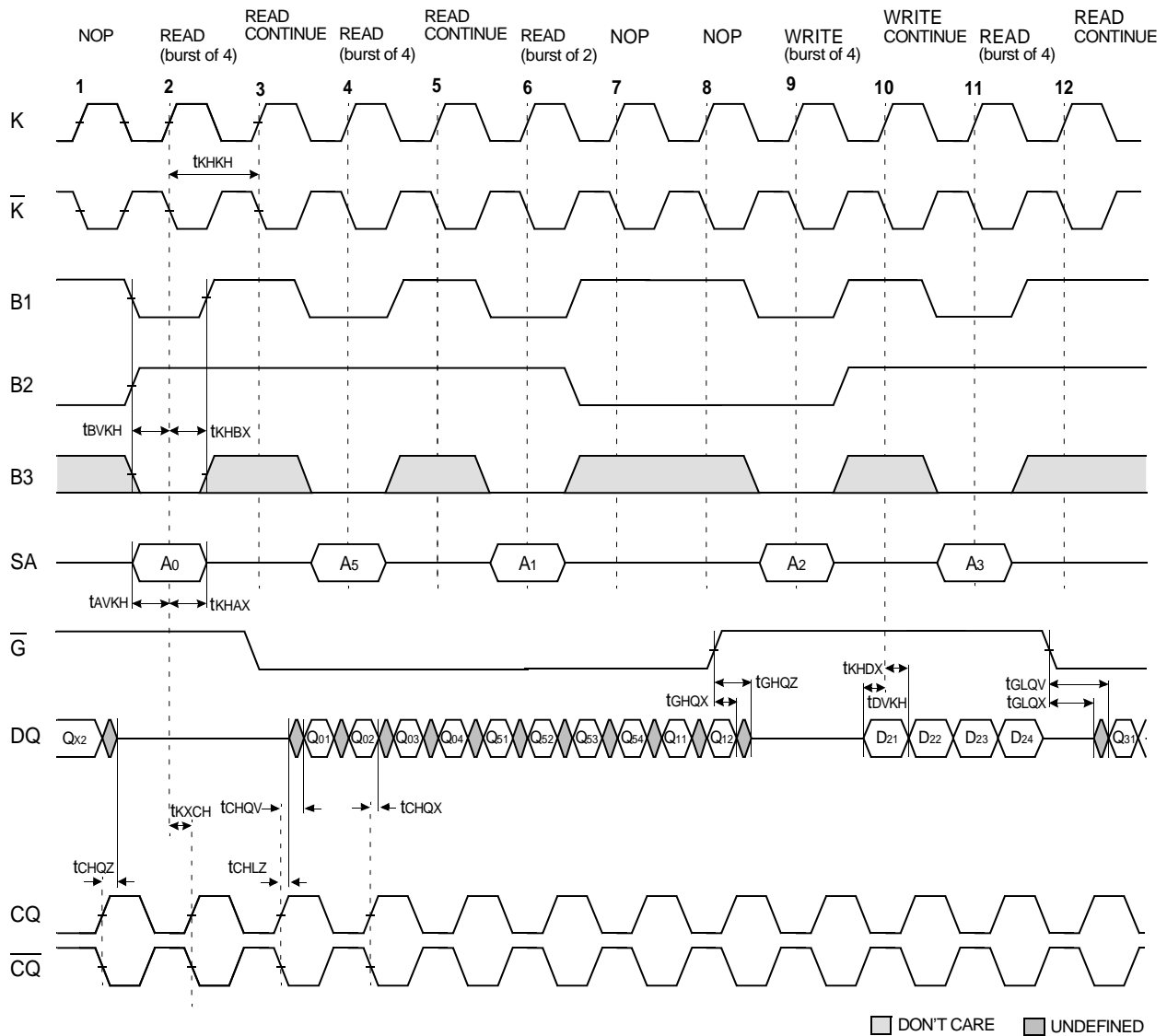
NOTE : 1. See AC Test Output Load figure  
2. Design target is 0ns

**AC CHARACTERISTICS**(For AC test condition 1)

Parameter	Symbol	-37		-35		Unit	Note
		Min	Max	Min	Max		
Clock Cycle Time	tkHKKH	2.7	-	2.8	-	ns	
Clock High Pulse Width	tkHKKL	1.3	-	1.3	-	ns	
Clock Low Pulse Width	tkLKKH	1.3	-	1.3	-	ns	
CQ High Pulse Width	tCHCL	tkHKKL-0.1	tkHKKL+0.1	tkHKKL-0.1	tkHKKL+0.1	ns	
CQ Low Pulse Width	tCLCH	tkLKKH-0.1	tkLKKH+0.1	tkLKKH-0.1	tkLKKH+0.1	ns	
Clock to Echo Clock(CQ) High	tkXCH	0.5	1.7	0.5	1.7	ns	1
Clock to Echo Clock(CQ) Low	tkXCL	0.5	1.7	0.5	1.7	ns	
Echo Clock to Output Valid	tCHQV/tCLQV	-	0.2	-	0.2	ns	1,2
Echo Clock to Output Hold	tCHQX/tCLQX	-0.2	-	-0.2	-	ns	1
Echo Clock to Output High-Z	tCHQZ/tCLQZ		0.2		0.2	ns	1
$\bar{G}$ Low to Output Low-Z	tGLQX	0.5	-	0.5	-	ns	1
$\bar{G}$ High to Output High-Z	tGHQZ	-	2.1	-	2.1	ns	1
$\bar{G}$ Low to Output Valid	tGLQV	-	2.1	-	2.1	ns	1
Address Setup Time	tAVKH	0.4	-	0.4	-	ns	
Address Hold Time	tkHAX	0.4	-	0.4	-	ns	
Burst Control Setup Time	tBVKH	0.4	-	0.4	-	ns	
Burst Control Hold Time	tkHBX	0.4	-	0.4	-	ns	
Data Setup Time	tDVKH	0.4	-	0.4	-	ns	
Data Hold Time	tkHDX	0.4	-	0.4	-	ns	

NOTE : 1. See AC Test Output Load figure  
2. Design target is 0ns

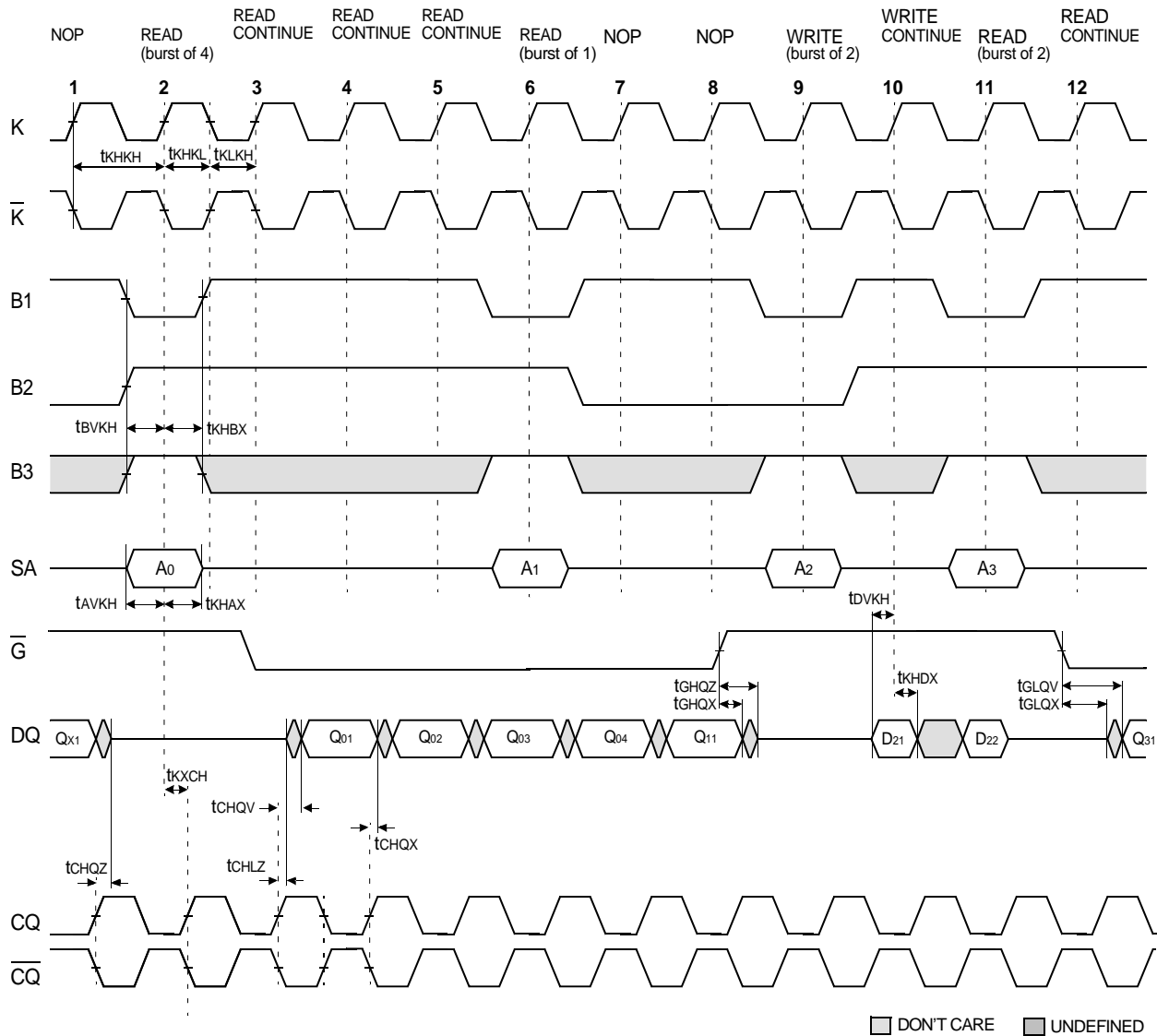
**TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES  
(Burst Length=4, 2)**



**NOTE**

1.  $Q_{01}$  refers to output from address A.  $Q_{02}$  refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

**TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES  
(Burst Length=4, 2, 1)**



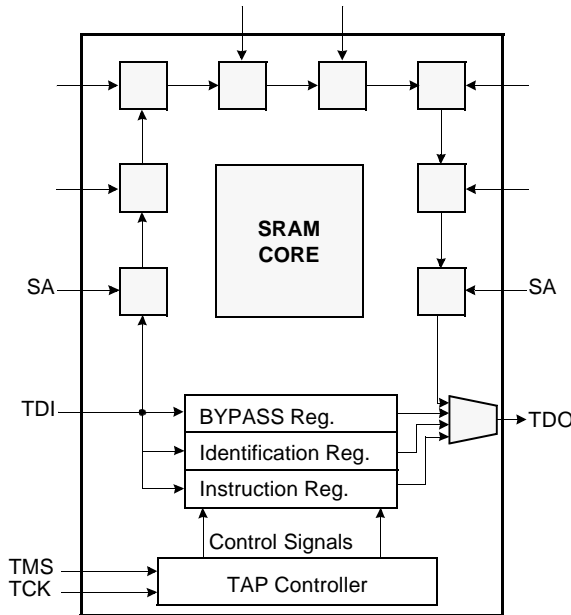
**NOTE :**

1. Q<sub>01</sub> refers to output from address A<sub>0</sub>. Q<sub>02</sub> refers to output from the next internal burst address following A<sub>0</sub>, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This device supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

**IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG**

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

**JTAG Block Diagram**



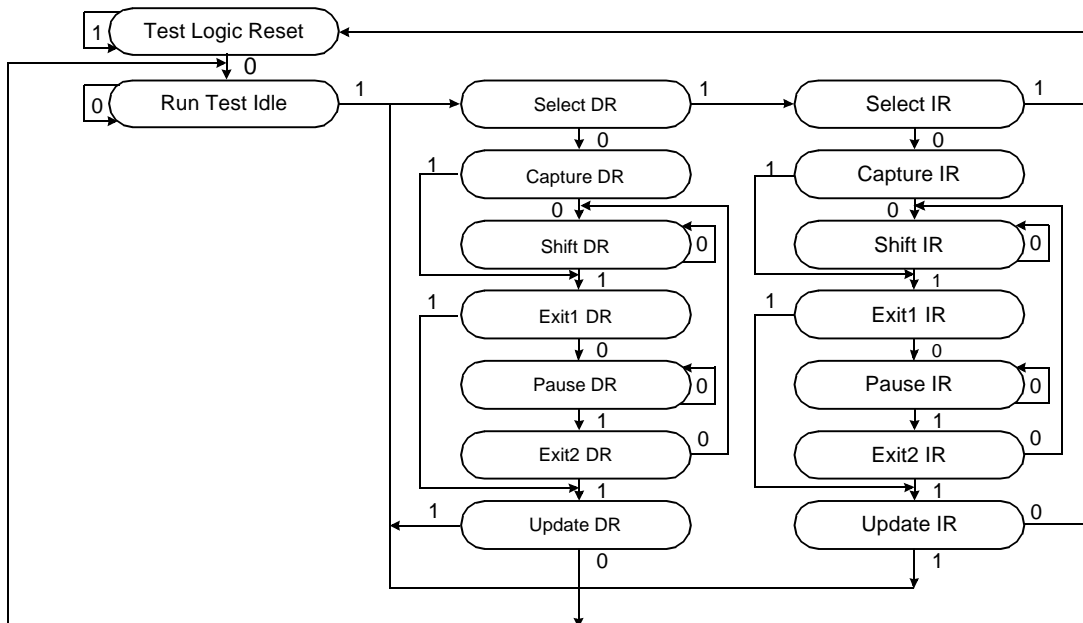
**JTAG Instruction Coding**

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

**NOTE :**

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

**TAP Controller State Diagram**



**SCAN REGISTER DEFINITION**

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	68 bits
512Kx18	3 bits	1 bits	32 bits	49 bits

**ID REGISTER DEFINITION**

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

**BOUNDARY SCAN EXIT ORDER(x36)**

36	4A	SA		SA	6A	35
37	4C	SA		SA	6C	34
38	3A	SA		SA	7A	33
39	3B	SA		SA	7B	32
40	3C	SA		SA	7C	31
41	3D	NC		SA	7D	30
42	2B	DQ		DQ	8B	29
43	1B	DQ		DQ	9B	28
44	2D	DQ		DQ	8D	27
45	3F	DQ		DQ	7F	26
46	1D	DQ		DQ	9D	25
47	2F	CQ		CQ	8F	24
48	1F	DQ		DQ	9F	23
49	3H	DQ		DQ	7H	22
50	2H	DQ		DQ	8H	21
51	1H	DQ		DQ	9H	20
52	5A	ZQ		$\overline{G}$	5C	19
53	5B	B <sub>1</sub>		K	5G	18
54	5K	B <sub>2</sub>		$\overline{K}$	5H	17
55	5L	B <sub>3</sub>		NC	6L	16
56	4L	$\overline{LBO}$		DQ	9K	15
57	1K	DQ		DQ	8K	14
58	2K	DQ		DQ	7K	13
59	3K	DQ		DQ	9M	12
60	1M	DQ		$\overline{CQ}$	8M	11
61	2M	$\overline{CQ}$		DQ	9P	10
62	1P	DQ		DQ	7M	9
63	3M	DQ		DQ	8P	8
64	2P	DQ		DQ	9T	7
65	1T	DQ		DQ	8T	6
66	2T	DQ		SA	7P	5
67	3T	SA		SA	7T	4
68	4R	SA		SA	6R	3
				SA <sub>0</sub>	5T	2
				SA <sub>1</sub>	5R	1

1.Pin 6L is reserved for Mode Pin and the scanned data is fixed to "0"  
2.Pin 3D is reserved for Address bit for 16Mb density and the scanned data is fixed to "0"

**BOUNDARY SCAN EXIT ORDER(x18)**

26	4A	SA		SA	6A	25
27	4C	SA		SA	6C	24
28	3A	SA		SA	7A	23
29	3B	SA		SA	7B	22
30	3C	SA		SA	7C	21
31	3D	NC		SA	7D	20
32	2B	DQ				
				DQ	9B	19
				DQ	8D	18
				DQ	7F	17
33	1D	DQ				
34	2F	CQ				
				DQ	9F	16
35	3H	DQ				
				DQ	8H	15
36	1H	DQ				
37	5A	ZQ		$\overline{G}$	5C	14
38	5B	B <sub>1</sub>		K	5G	13
39	5K	B <sub>2</sub>		$\overline{K}$	5H	12
40	5L	B <sub>3</sub>		NC	6L	11
41	4L	$\overline{LBO}$		DQ	9K	10
42	2K	DQ		DQ	7K	9
43	1M	DQ		$\overline{CQ}$	8M	8
				DQ	9P	7
44	3M	DQ				
45	2P	DQ				
46	1T	DQ		DQ	8T	6
				SA	7P	5
47	3P	SA		SA	7T	4
48	3T	SA		SA	6R	3
49	4R	SA		SA <sub>0</sub>	5T	2
				SA <sub>1</sub>	5R	1

1.Pin 6L is reserved for Mode Pin and the scanned data is fixed to "0"  
2.Pin 3D is reserved for Address bit for 16Mb density and the scanned data is fixed to "0"



**JTAG DC OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	2.37	2.5	2.63	V	
Input High Level	V <sub>IH</sub>	1.7	-	V <sub>DD</sub> +0.3	V	
Input Low Level	V <sub>IL</sub>	-0.3	-	0.7	V	
Output High Voltage(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.1	-	V <sub>DD</sub>	V	
Output Low Voltage(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	V <sub>SS</sub>	-	0.2	V	

**NOTE** : 1. The input level of SRAM pin is to follow the SRAM DC specification.

**JTAG AC TEST CONDITIONS**

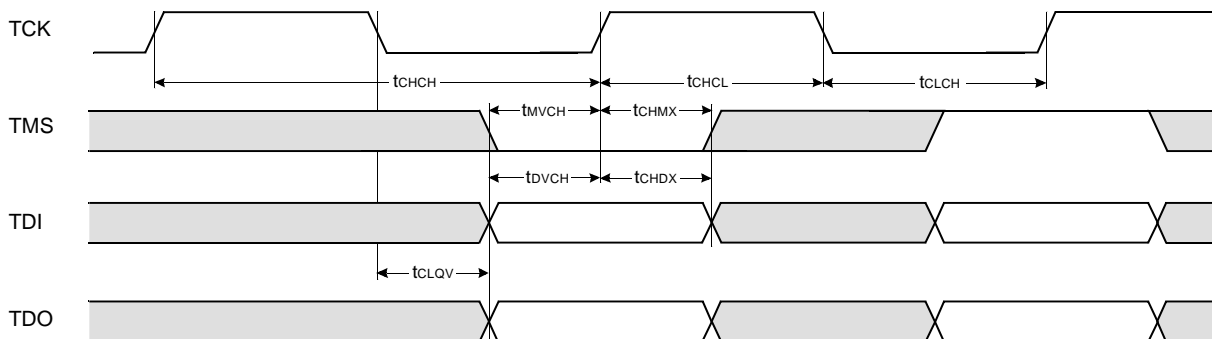
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V <sub>IH</sub> /V <sub>IL</sub>	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

**NOTE** : 1. See SRAM AC test output load on page 5.

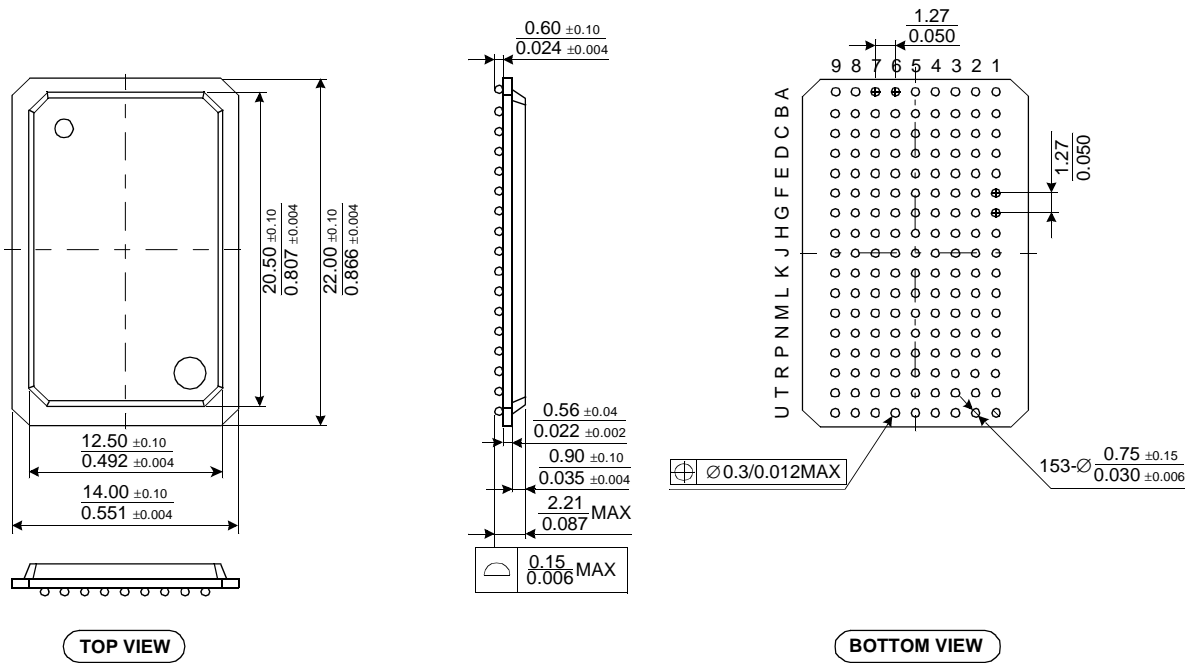
**JTAG AC Characteristics**

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t <sub>CHCH</sub>	50	-	ns	
TCK High Pulse Width	t <sub>CHCL</sub>	20	-	ns	
TCK Low Pulse Width	t <sub>CLCH</sub>	20	-	ns	
TMS Input Setup Time	t <sub>MVCH</sub>	5	-	ns	
TMS Input Hold Time	t <sub>CHMX</sub>	5	-	ns	
TDI Input Setup Time	t <sub>DVCH</sub>	5	-	ns	
TDI Input Hold Time	t <sub>CHDX</sub>	5	-	ns	
Clock Low to Output Valid	t <sub>CLQV</sub>	0	10	ns	

**JTAG TIMING DIAGRAM**



**153 BGA PACKAGE DIMENSIONS**



- NOTE :**
1. All Dimensions are in Millimeters.
  2. Solder Ball to PCS Offset : 0.10 MAX.
  3. PCB to Cavity Offset : 0.10 MAX.

**153 BGA PACKAGE THERMAL CHARACTERISTICS**

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	30.0	°C/W	1W Heating
Junction to Case	Theta_JC	5.9	°C/W	
Junction to Board	Theta_JB	4.8	°C/W	2W Heating

**NOTE :** 1. Junction temperature can be calculated by :  $T_J = T_A + P_D \times \text{Theta}_{JA}$ .