TMC2242C

Digital Half-Band Interpolating/Decimating Filter

12-bit In/16-bit Out, 60 MHz

Features

- Pin-compatible upgrade of TMC2242B
- User-selectable interpolate d.c. gain, 0 dB or -6 dB
- True unity d.c. gain in all “0 db” modes
- 40 MSPS performance in equal-rate filter modes
- 40 and 60 MSPS speed grades in all other modes
- User-selectable 2:1 decimation, 1:2 interpolation, and equal-rate filter modes, plus unfiltered bypass/delay mode
- Defeatable $\pi x/\sin(\pi x)$ compensation filter
- Passband ripple <0.014 dB
- Stopband rejection >56 dB
- Dedicated 12-bit two’s complement or unsigned input bus
- 16-bit two’s complement or unsigned output bus with user-selectable rounding to 8 to 16 effective bits
- Programmable limiter prevents overflow or clips to CCIR601 levels
- New double-latency modes match Y channel data flow to slower-sampled C_B and C_R data flows
- New dual-channel interpolation and decimation for YUV422

Applications

- Digital-to-Analog Converter Prefiltering with optional x/sinx correction
- 1:2 interpolation
- Analog-to-Digital Converter Postfiltering
- 2:1 decimation
- Low-ripple low-pass (0 to 0.2 f_S) filter

Description

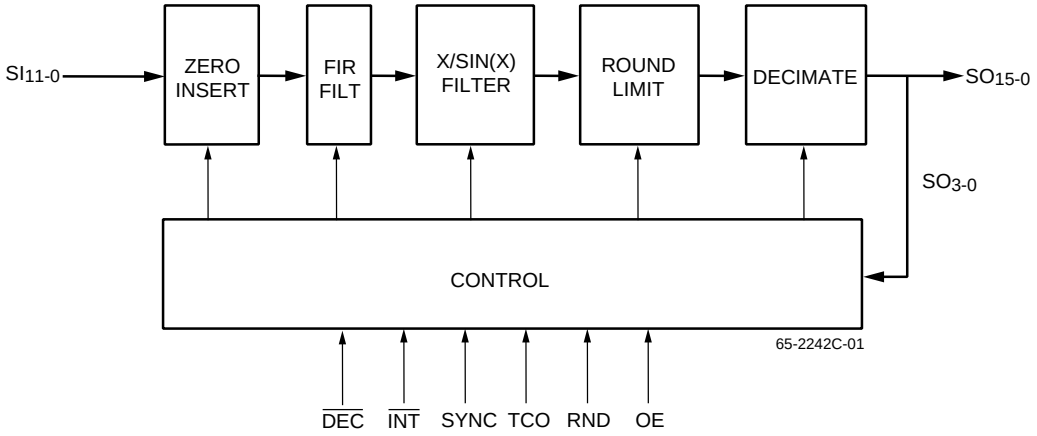
The TMC2242C, a linear-phase low-pass half-band digital filter with fixed coefficients, can be used to halve or double the sampling rate of a digital signal. When used as a decimating post-filter with a double-speed oversampling A/D converter, it greatly reduces the cost and complexity of the required analog antialiasing pre-filters. When used as an interpolating pre-filter with a double-speed oversampling D/A converter, it greatly reduces the complexity and cost of the necessary analog post-filter, particularly when its x/sin(x) correction filter is engaged.

The TMC2242C user selects the mode of operation (decimate, interpolate, equal-rate, bypass, x/sin(x))and rounding. The part can accept 12-bit two’s complement or unsigned data at up to 60 MHz and can output saturated two’s complement or offset binary data rounded to from 8 to 16 bits. Within the speed grade I/O limit, the output sample rate may be 1/2, 1, or 2 times the input sample rate. Two-channel modes permit it to interpolate or to decimate two multiplexed data streams (such as video C_B and C_R) jointly.

The filter response is flat to within ±0.014 dB up to $0.21f_S$ (e.g. 5.75MHz at a 27MHz clock rate), with stopband attenuation greater than 56dB above $0.29f_S$. Symmetric-coefficient filters such as the TMC2242C always have linear phase response. Half-band response is -6 dB.

Fabricated on an advanced submicron CMOS process, the TMC2242C is available in a 44-lead PLCC package. Performance is guaranteed from 0 to 70°C and over a power supply range of 4.75 to 5.25V.

Block Diagram



Functional Description

The TMC2242C implements a fixed-coefficient linear-phase Finite Impulse Response (FIR) filter, with special rate-matching input and output structures for decimation and interpolation. For parts of each speed grade, the faster of either the input or the output bus will operate at the respective guaranteed maximum clock rate. The total internal pipeline latency from the input of an impulse to the corresponding output peak (digital group delay) is 34 clock cycles; the 39-value output response begins after 15 clock cycles and ends after 53 cycles. (The double-latency interpolation and decimation modes feature group delays of 68 clock cycles.)

To interpolate, the chip accepts incoming data on alternate clock cycles, inserting zeroes on the remaining clock cycles. In decimation mode, the chip's output register is strobed at half the clock rate. In bypass and equal-rate filter modes, these input zero insertion and output register hold functions are disabled.

When interpolating, the user should normally bring SYNC HIGH for at least one clock cycle, returning it LOW with the first desired input data value. The chip will then continue to accept data on alternate rising edges of CLK. The user may leave SYNC LOW or change its value once per clock cycle, with equivalent results. The chip can be powered up and operated with SYNC grounded, but the input-to-output latency may vary by 1/2 input sample period and the host system won't know which (even- or odd-numbered) CLK rising edges strobe the input register. The setup and hold timing requirements for SYNC, with respect to the rising edges of CLK, are the same as those for all other data and control inputs except OE, which is asynchronous. In two-channel mode, it must remain low after the first incoming data value.

When decimating, the user should likewise bring SYNC HIGH for at least one clock cycle, returning it LOW when a fresh output is desired. The chip will continue to update the output register on alternate rising edges of CLK. The user may leave SYNC LOW or change its value once per clock cycle, with equivalent results. The chip can be powered up and operated with SYNC grounded, but the host system won't know whether the data outputs are updated on even- or odd-numbered system clock cycles. In any half-band decimating filter, a given single-cycle impulse's arrival time (on an odd versus an even clock cycle) determines whether it generates a half-amplitude two-cycle impulse or a half-speed, 40-clock, filtered output shaped by the nonzero, non-center coefficients. The SYNC control permits the host system to obtain consistent results. In two-channel mode, it must remain low after the first incoming data value.

When the result is rounded to fewer than 16 bits, the unneeded lowest positions of the output bus are tristated and become supplementary control bits, which enable the x/sin(x) filter, bypass/delay, double-latency, dual-channel, and other special modes. Unless more than 12 output bits are enabled, the TMC2242C offers x/sin(x) correction filtering, with or without the main low-pass filter, and without impacting the 34-cycle group delay. Bidirectional pins SO_{3-2} enable these modes, per Table 1. If 14 or more output bits are used, the low pass filter remains enabled, the x/sin(x), disabled.

Table 1. Operating Modes

$\overline{INT}$	$\overline{DEC}$	RND_2	SO_{3-2}	Function
0	0	0	Output	Interpolate (0 dB)
0	1	0	Output	Interpolate[1] (-6 dB)
1	0	0	Output	Decimate
1	1	0	Output	Equal Rate Lowpass
0	0	1	00	Interpolate (0 dB)
0	1	1	00	Interpolate[1] (-6 dB)
1	0	1	00	Decimate
1	1	1	00	Equal Rate Lowpass
0	0	1	01	Interpolate (0 dB) * x/sinx
0	1	1	01	Interpolate[1] (-6 dB) * x/sinx
1	0	1	01	Decimate * x/sinx
1	1	1	01	Equal Rate LPF * x/sinx
0	0	1	10	Delay + Interpolate[2] (0 dB)
0	1	1	10	Delay + Interpolate[2] (0 dB) * x/sinx
1	0	1	10	Delay + Decimate[2]
1	1	1	10	Bypass (Delay Only)
0	0	1	11	2-Channel Interpolate[3] (0 db)
0	1	1	11	2-Channel Interpolate[3] * x/sinx
1	0	1	11	2-Channel Decimate[3]
1	1	1	11	Delay * x/sinx

Note:

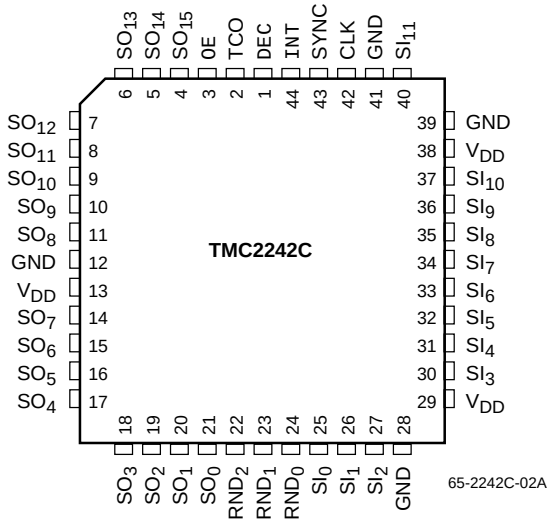
1. These modes limit to 15 bits (SO_{14-0}) instead of 16 (SO_{15-0}) and are provided for backward compatibility to earlier parts.
2. These modes, which double the chip's overall group delay from 34 to 68 CLK cycles, can be used to equalize inter-component delays where Y is sampled at twice the rate of C_B or C_R (e.g. 4:2:2 and 8:4:4 formats).
3. These modes accommodate multiplexed two-channel data, e.g. C_B/C_R.

Table 2. Package Interconnections

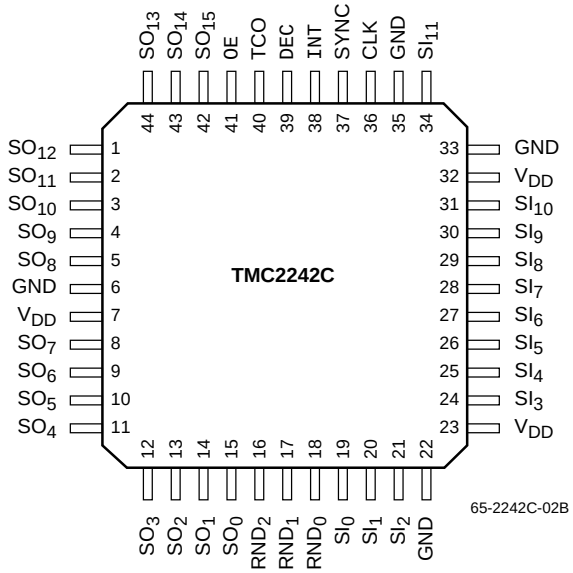
Signal Type	Name	Function	PLCC Pin	MQFP Pin
Timing	CLK	Clock	42	36
	SYNC	Synchronization	43	37
Data In	SI_{11-0}	Input Data Port	40, 37-30, 27-25	34, 31-24, 21-19
Data Out	SO_{15-4}	Output Data Port	4-11, 14-17	42-44, 1-5, 8-11
Dual-Function Controls	SO_{3-0}	Output Data; Controls	18-21	12-15
	$\overline{INT}$	Interpolate	44	38
	$\overline{DEC}$	Decimate	1	39
	RND_{2-0}	Rounding Position	22-24	16-18
	TCO	Output Format	2	40
	OE	Output Enable	3	41

The output data format is two's complement if TCO is HIGH, inverted or offset binary if LOW. Unless all 16 output bits are used, the user can also select either signed or unsigned input data, via pin SO_0 (see pin description note 2, below). As shown in pin description note 1, the output is half-LSB rounded to the resolution selected by the value of RND_{2-0}. The asynchronous three-state output enable control simplifies connection to a data bus with other drivers.

Pin Assignments



44 Lead PLCC



44 Lead MQFP

Pin Descriptions

Pin Name	Pin Number PLCC	Pin Number MQFP	Pin Function Description
Dedicated Timing Controls			
CLK	42	36	**Clock**. The chip operates from a single-phase master clock, to whose rising edges all timing parameters are referenced. All internal registers are strobed on every rising edge of CLK, although the output register is strobed on alternate rising edges during decimation. In all modes, the frequency applied to CLK is the higher of the input and output data sampling rates. During interpolation, the chip reads its input bus on alternate rising edges of CLK.
SYNC	43	37	**Synchronization**. During interpolation, the chip accepts input data on alternate rising edges of CLK and inserts zeroes on the remaining cycles. If SYNC is HIGH during CLK rising edge 0 and LOW during CLK rising edge 1, the chip will accept data on CLK 1 and insert a zero on CLK 2. Thereafter, if SYNC is either held LOW or fed a square wave of half the CLK frequency, the part will continue to accept data on odd-numbered CLK edges and to stuff zeroes on even-numbered edges. Similarly, during decimation, the output data change only on alternate clock cycles. If the user operates SYNC as above, each even-numbered rising edge of CLK will trigger a change in the output. In all other modes, the state of SYNC doesn't affect operation of the chip.
Dedicated Data Input Port			
SI_{11-0}	40, 37-30, 27-25	34, 31-24, 21-19	**Input Data**. A 12-bit two's complement or unsigned input word is registered by the rising edges of CLK. SI_0 is the LSB.
Dedicated Data Output Port			
SO_{15-0}	4-11, 14-21	42-44, 1-5, 8-15	**Output Data MSBs**. When $\overline{OE}$ is LOW, the 12 most significant bits of the filter's output emerge here, following each rising edge of CLK. The format may be two's complement, unsigned, or inverted offset binary. Bits SO_{15-4} correspond to input bits SI_{11-0}, respectively. An on-chip limiter prevents overflows and underflows in the output data.
Dual Function Data Output/Control Input Pins			
SO_{3-2}			**Output Data**. These pins serve as data outputs when RND_2 is LOW. When RND_2 is HIGH, they become additional filter mode controls (Table 1).
SO_1			**Output Data 2nd LSB.** This pin is a data output when RND_{2-1} are LOW. When either RND_2 or RND_1 is HIGH, it becomes an additional rounding control.[1]
SO_0			**Output Data LSB**. This pin is a data output if and only if all RND bits are LOW. Otherwise, it augments the data I/O format controls.[2]
Dedicated Static Controls (Set state before first desired data input.)			
$\overline{INT}$, $\overline{DEC}$	44, 1	38, 39	**Interpolate and Decimate.** Jointly with SO_{3-2}, these bits select the chip's overall operating mode, as discussed earlier in Table 1
TCO	2	40	**Output format control.** When TCO is HIGH, the output data are in two's complement format. When TCO is LOW, they are inverted offset binary, unless SO_0 is HIGH and RND is nonzero, in which case they are unsigned.
RND_{2-0}	22-24	16-18	**Round and output tristate.** Selects output rounding position and active bus width 8-16 bits. All outputs at and below the rounding bit position are tristated, allowing the 4 LSBs to become control inputs.
Active, Asynchronous Control			
$\overline{OE}$	3	41	**Output enable.** LOW activates output bus from SO_{15} down to the effective LSB, as chosen by RND_{2-0}. All drivers at and below the rounding point are disabled, as are all drivers when $\overline{OE}$ is HIGH.

Notes:

1. Rounding Operation Detail

RND_{2-0}	SO_1	Output Rounding
000	Output[A]	SO_{15-0} (16 bits)
001	Output[A]	SO_{15-1} (15 bits)
010	X	SO_{15-2} (14 bits)
011	X	SO_{15-3} (13)
100	0	SO_{15-4} (12)
100	1	SO_{15-8} (8)
101	0	SO_{15-5} (11)
110	1	SO_{15-6} (10)
111	X	SO_{15-7} (9)

A. If RND_{2-0} = 00X, do not drive SO_1, externally.

2. I/O Format Operation Detail

RND	SO_0	TCO	In Format	Out Format
0	Output	0	2's Comp	Inverted Offset
0	Output	1	2's Comp	2's Comp
>0	0	0	2's Comp	Inverted Offset
>0	0	1	2's Comp	2's Comp
>0	1	0	Unsigned	Unsigned
>0	1	1	Unsigned	2's Comp

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Max	Units
Supply Voltage		-0.5	7.0	V
Input Voltage		-0.5	V_{DD} + 0.5	V
Output Applied Voltage[2]		-0.5	V_{DD} + 0.5	V
Externally Forced Current[3,4]		-3.0	+6.0	mA
Short Circuit Duration	Single output in HIGH state to ground		1	sec
Operating Temperature (Case)		-20	110	°C
Junction Temperature			140	°C
Lead Soldering Temperature	10 seconds		300	°C
Storage Temperature		-65	150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

		Conditions	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2242C			40	MHz
		TMC2242C-1			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		6			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		0			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

P arameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD}=25pF, f_{CLK}=Max				
		TMC2242C			150	mA
		TMC2242C-1			220	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK}=Max				
		TMC2242C			135	mA
		TMC2242C-1			200	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IH} (PD)	Input Current, HIGH (Pulldown SO0–SO3)	V_{DD} = Max, V_{IN} = V_{DD}			-10 +150	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Leakage Current, HIGH	$\overline{OE}$ = HIGH, V_{OUT} = V_{DD}			±10	µA
I_{OZH} (PD)	Leakage Current, HIGH (Pulldown SO0–SO3)	$\overline{OE}$ = HIGH, V_{OUT} = V_{DD}			-10 +150	µA
I_{OZL}	Leakage Current, LOW	$\overline{OE}$ = HIGH, V_{OUT} = 0 V			±10	µA
I_{OS}	Short-Circuit Current	V_{DD} = Max, Output = HIGH, one pin to ground, one second duration max.	-90		-150	mA
V_{OH}	Output Voltage, HIGH	SO15-0, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	SO15-0, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	2.5			ns
t_{ENA}	Output Enable Time	C_{LOAD} = 0 pF			15	ns
t_{DIS}	Output Disable Time	C_{LOAD} = 0 pF			30	ns

Table 3a. Input Data Formats and Bit Weighting

Format	SI_{11}	SI_{10}	S_9	. . .	SI_1	S_0
Two's Comp.	-2^0	2^{-1}	2^{-2}	. . .	2^{-10}	2^{-11}
Unsigned	2^0	2^{-1}	2^{-2}	. . .	2^{-10}	2^{-11}

Table 3b. Output Data Formats and Bit Weighting

Format	SO_{15}	SO_{14}	SO_{13}	. . .	SO_5	SO_4
Two's Comp.	-2^0	2^{-1}	2^{-2}	. . .	2^{-10}	2^{-11}
Unsigned[1]	2^0	2^{-1}	2^{-2}	. . .	2^{-10}	2^{-11}
-6 dB t.c.[2]	-2^0	-2^0	2^{-1}	. . .	2^{-9}	2^{-10}
-6 dB Unsgn[3]	0	2^0	2^{-1}	. . .	2^{-9}	2^{-10}

Notes:
1. Inverted offset binary is the same as unsigned, except that all bits are complemented.
2. In -6 dB interpolation modes, the two's complement sign bit is replicated in SI_{15} and SI_{14}.
3. In -6 dB interpolation mode, the unsigned MSB is preceded by a 0 in SO_{15}.
4. A leading minus sign denotes the two's complement sign bit.
5. In all operating modes except "interpolate -6 dB," dc gain is exactly unity.

Table 4. Rounded LSBs as a function of RND_{2-0}

												RND_{2-0}
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_{0r}	000
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_{1r}	z	001
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_{2r}	z	z	010
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_5	SO_4	SO_{3r}	z	z	z	011
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_5	SO_{4r}	z	z	z	z	100[2]
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_6	SO_{5r}	z	z	z	z	z	101
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_7	SO_{6r}	z	z	z	z	z	z	110
SO_{15}	SO_{14}	SO_{13} …	SO_8	SO_{7r}	z	z	z	z	z	z	z	111

Note:
1. The "r" indicates that the trailing significant output bit has been rounded to the nearest 1/2 LSB. All output drivers at and below the rounding bit are disabled, allowing the lower output bits to be used as control inputs.
2. If $SO_1 = 1$, format is 8 bits, viz: SO_{15}…SO8r z…z.

Table 5. Steady-State Output Values and Limit Triggers

Input		Interpolate -6 dB		All Other Modes		Interpretation	
Unsigned	2's Comp.	Unsigned	2's Comp.	Unsigned	2's Comp.	Unsigned	2's Comp.
FFF	7FF	7FF8[1]	3FF8[1]	FFF0[1]	7FF0[1]	full-scale	full-scale +
C00	400	6000	2000	C000	4000	3/4-scale	1/2 scale +
801	001	4008	0008	8010	0010		1 LSB +
800	000	4000	0000	8000	0000	1/2-scale	Zero
7FF	FFF	3FF8	FFF8	7FF0	FFF0		1 LSB –
400	C00	2000	E000	4000	C000	1/4-scale	1/2-scale –
000	800	0000[1]	C000[1]	0000[1]	8000[1]	zero	full-scale –

Notes:
1. Full-scale values are minima and maxima permitted by on-chip limiter. Transient overshoots arising from large input signal transitions will be clipped to these limits.

Performance Curves

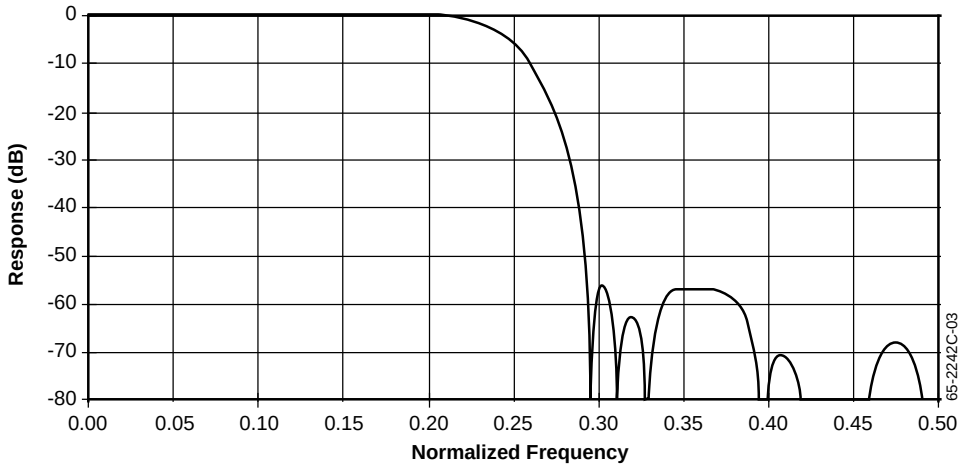


Figure 1. Frequency Response

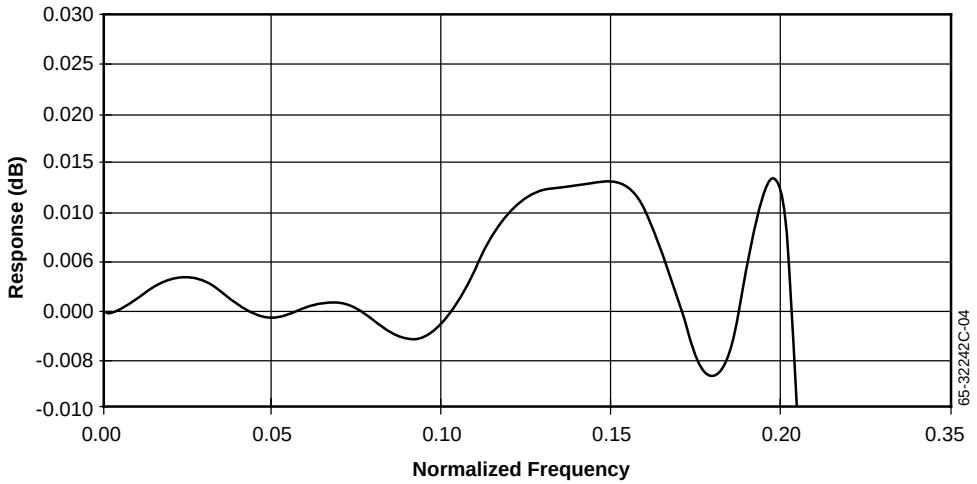


Figure 2. Passband Ripple Response

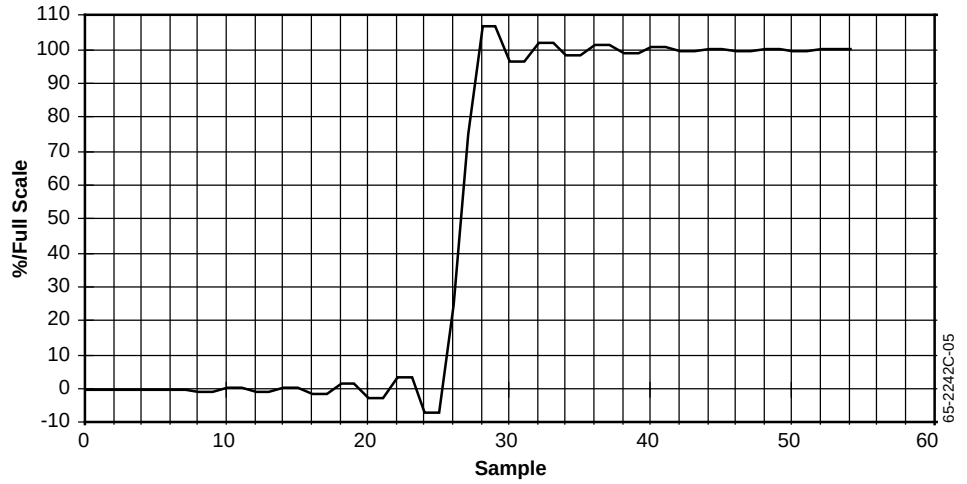


Figure 3. Step Response

Equivalent Circuits

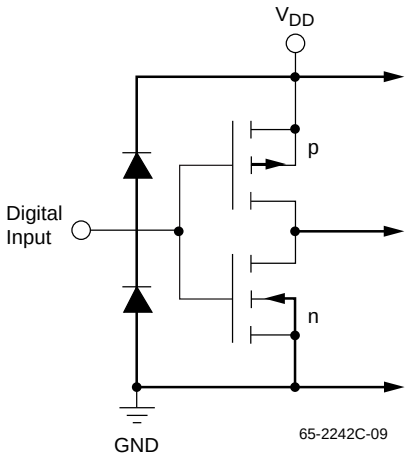


Figure 4. Equivalent Digital Input Circuit

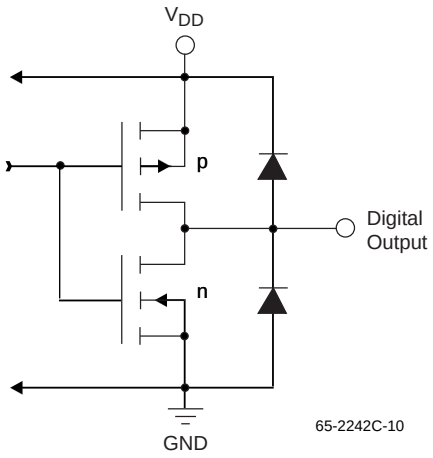
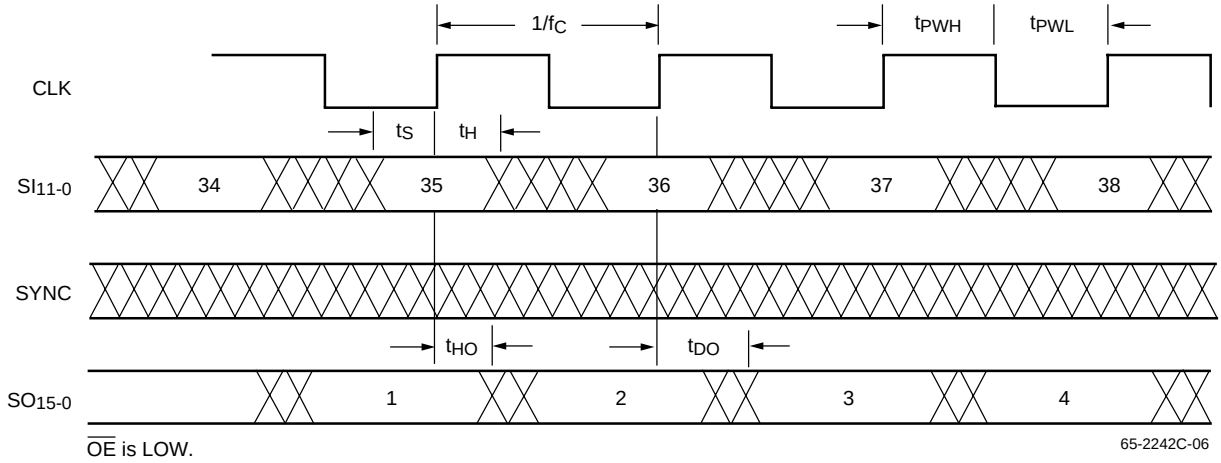


Figure 5. Equivalent Digital Output Circuit

Timing Diagrams



Note: Values at SO_{15-0} are impulse response centers (peaks) corresponding to same-numbered inputs.

Figure 6. Equal Rate Mode

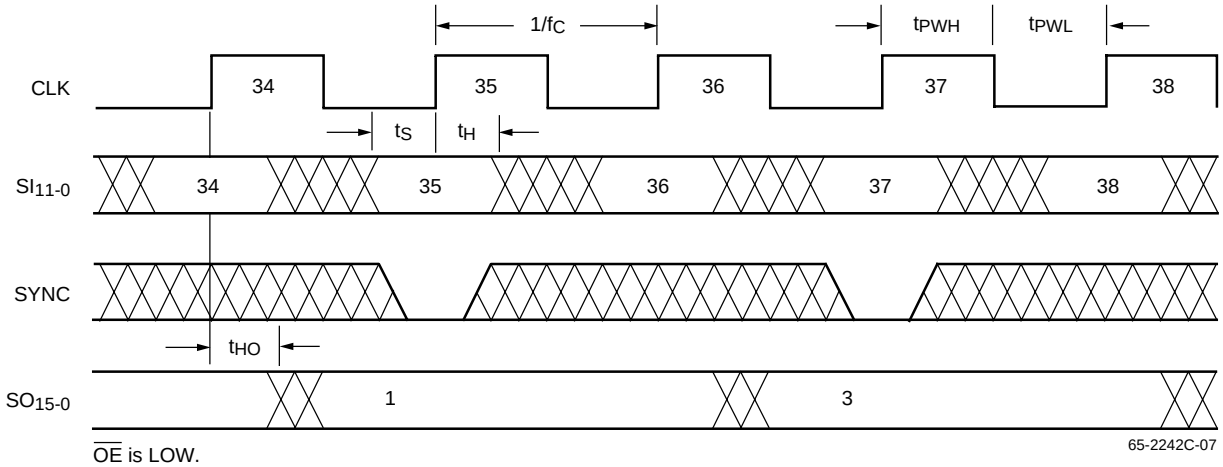


Figure 7. Decimate Mode

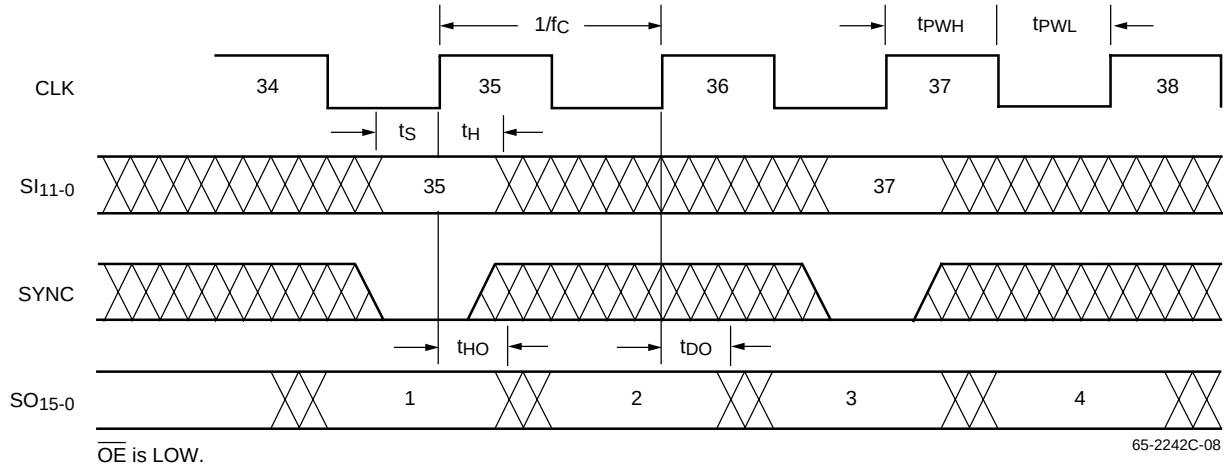


Figure 8. Interpolate Mode

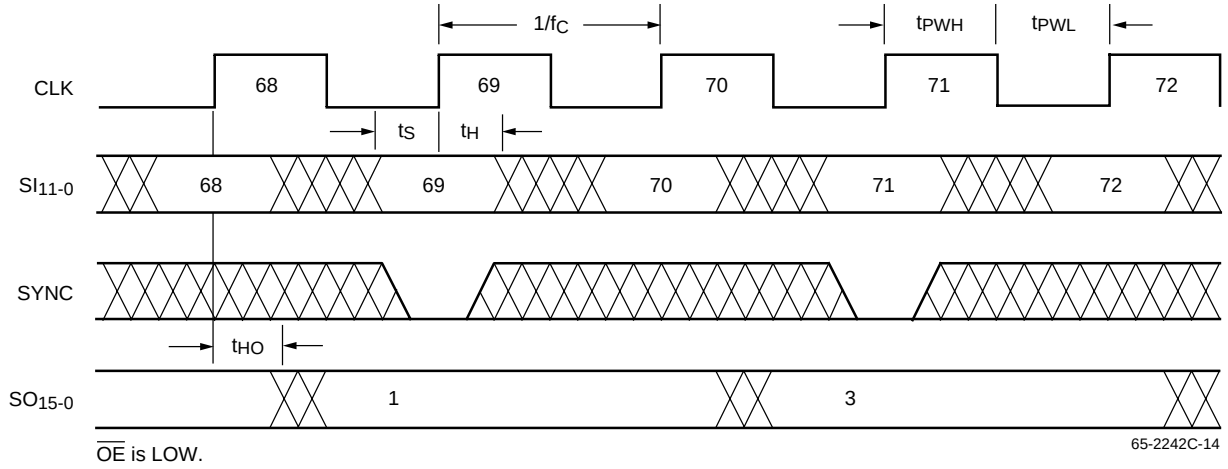


Figure 9. Decimate Mode – Double Latency

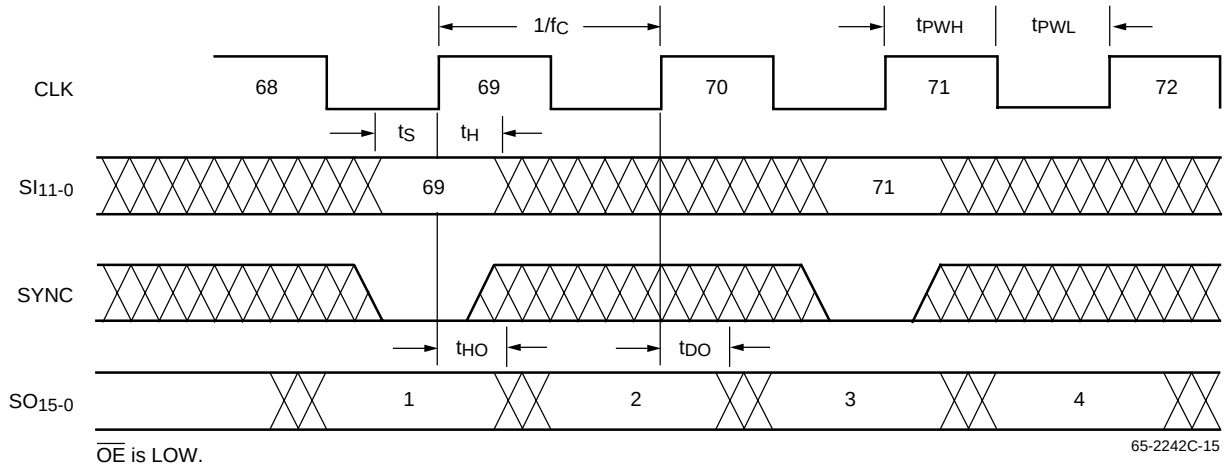
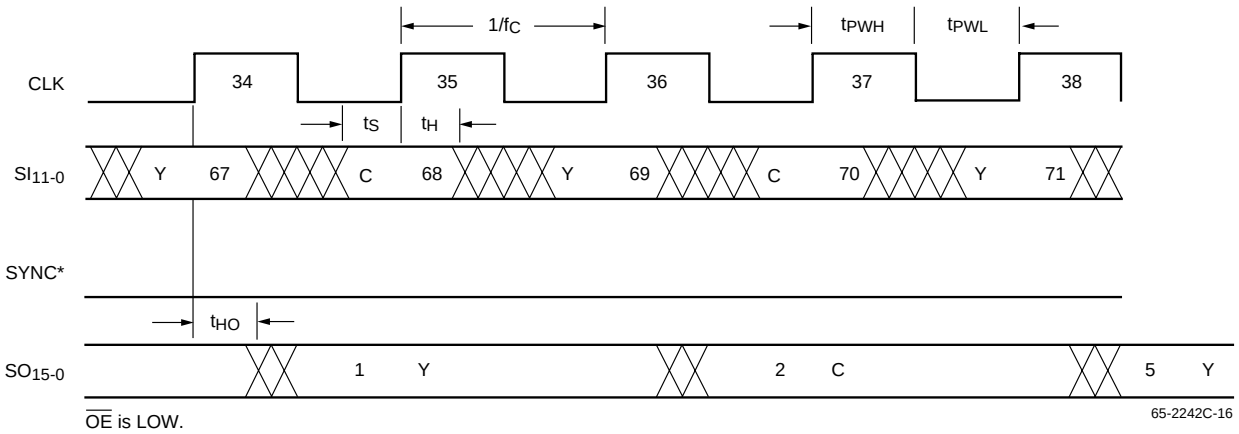


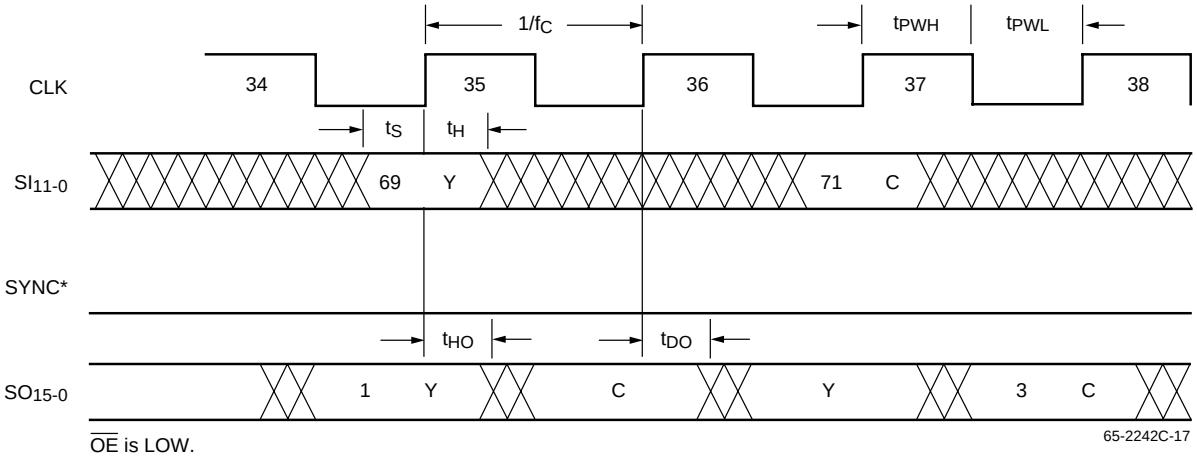
Figure 10. Interpolate Mode – Double Latency



$\overline{OE}$ is LOW.

*In two-channel modes, sync must be left low after the first data input.

Figure 11. Decimate Mode – Two-Channel



$\overline{OE}$ is LOW.

*In two-channel modes, sync must be left low after the first data input.

Figure 12. Interpolate Mode – Two-Channel

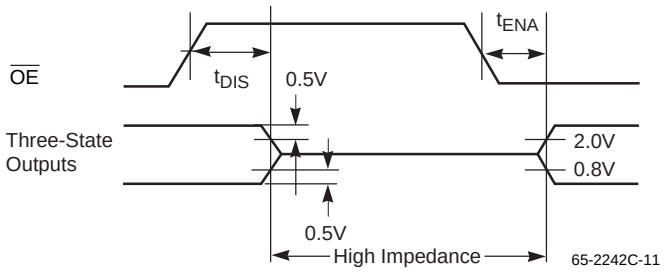


Figure 13. Threshold Levels for Three State Measurements

Applications Discussion

The TMC2242C is well-suited to filtering digitized composite or component NTSC or PAL video. In Figure 14, the TMC1175A 8-bit video A/D converter outputs, D_{7-0}, are connected to the TMC2242C inputs, SI_{11-4}, respectively. To minimize noise and any chance of electrostatic damage, inputs SI_{3-0} should be grounded. Controls RND_{2-0} are set to 100 and SO_1 is forced high to effect 8-bit rounding. SO_{3-2}, TCO, and $\overline{DEC}$ are forced low, whereas $\overline{INT}$ and SO_0 are forced high. (Setting SO_0 high and TCO low selects unsigned binary format at the input and output data ports, eliminating the need for external MSB inverters.)

In Figure 15, the TMC2242C drives a fast D/A converter to reconstruct analog composite video. The TMC3003 10-bit digital-to-analog converter inputs, D_{9-0} are connected to the TMC2242C outputs SO_{15-6}, respectively. The TMC2242C RND_{2-0} controls are set to 110 for rounded 10-bit interpolation operation.

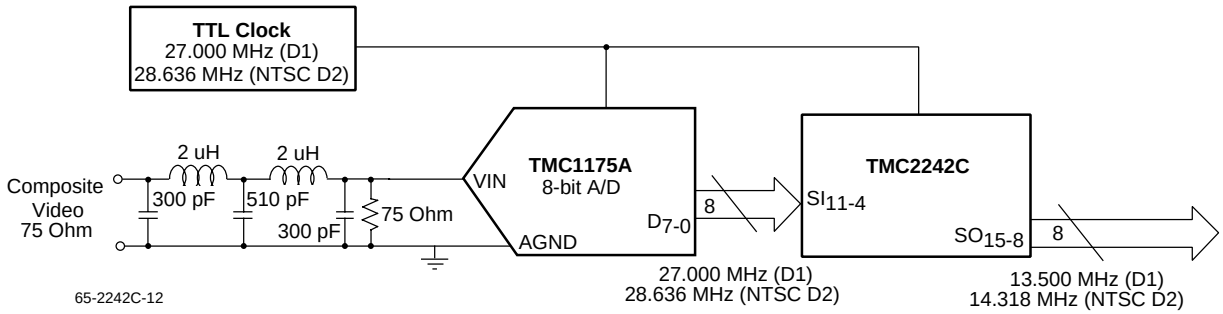
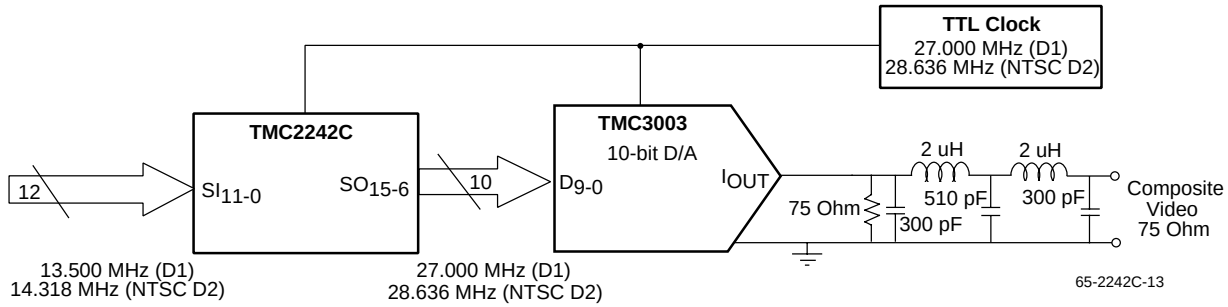


Figure 12. Decimating Oversampled Video With a Low Cost 8-bit A/D

TCO = 0 RND = 100 SO(3:0) = 0011 DEC = 0 INT = 1



Note: Data buses are unsigned binary.

Figure 13. Interpolating Digital Video Signals before Reconstruction

TCO = 0 RND = 110 SO(3:0) = 0011 DEC = 0 INT = 0

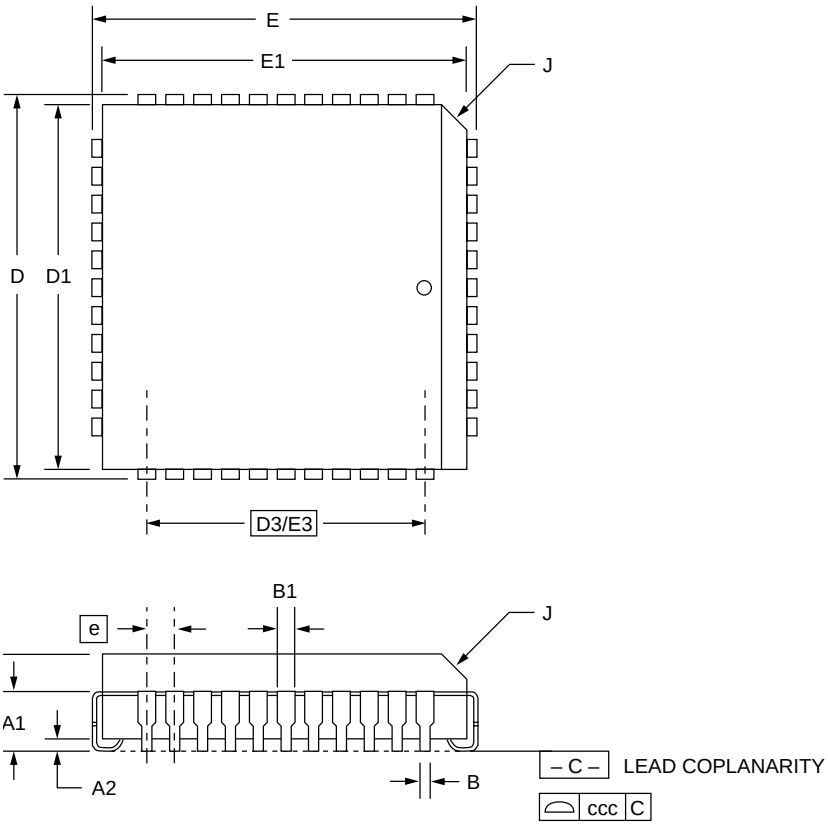
Notes:

Mechanical Dimensions – 44-Pin PLCC Package

nbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
	.165	.180	4.19	4.57	
	.090	.120	2.29	3.05	
	.020	—	.51	—	
	.013	.021	.33	.53	
	.026	.032	.66	.81	
	.685	.695	17.40	17.65	
E1	.650	.656	16.51	16.66	3
E3	.500 BSC		12.7 BSC		
	.050 BSC		1.27 BSC		
	.042	.056	1.07	1.42	2
'NE	11		11		
	44		44		
	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)

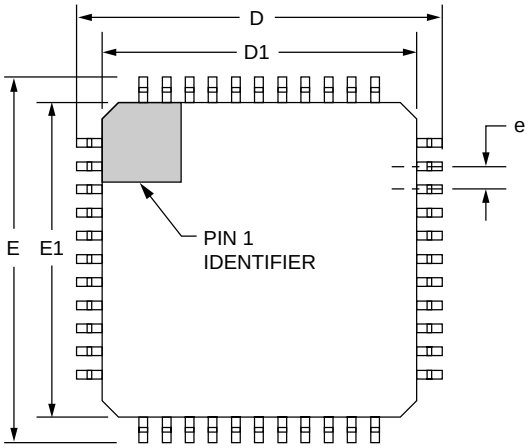


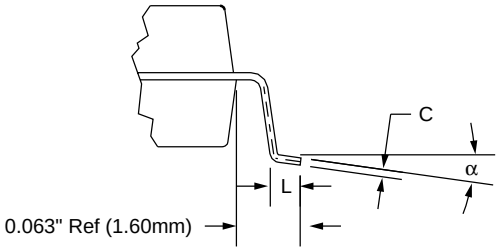
Mechanical Dimensions – 44-Lead MQFP Package

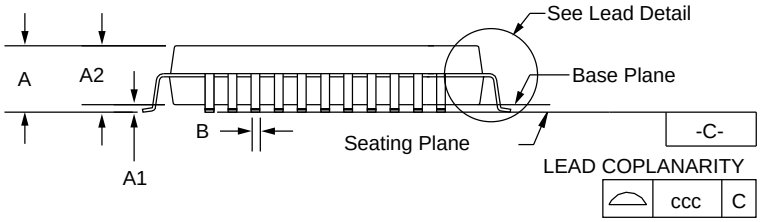
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.077	.093	1.95	2.35	
A1	.000	.010	.00	.25	
A2	.077	.083	1.95	2.11	
B	.012	.018	.30	.46	7
C	.005	.009	.13	.23	
D/E	.510	.530	12.95	13.45	
D1/E1	.390	.398	9.90	10.10	2
e	.032 BSC		.81 BSC		
L	.026	.037	.66	.94	6
N	44		44		4
ND	11		11		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.







Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2242CR2C	0°C to 70°C	40 MHz	Commercial	44-Lead PLCC	2242CR2C
TMC2242CR2C1	0°C to 70°C	60 MHz	Commercial	44-Lead PLCC	2242CR2C1
TMC2242CKTC	0°C to 70°C	40 MHz	Commercial	44-Lead MQFP	2242CKTC
TMC2242CKTC1	0°C to 70°C	60 MHz	Commercial	44-Lead MQFP	2242CKTC1